SSI 32P3000
Pulse Detector with Programmable Filter

Advance Information

July, 1990

2

DESCRIPTION

The SSI 32P3000 is a bipolar integrated circuit that provides all data processing necessary for detection and qualification of encoded read signals. The circuit will handle a data rate of 48 Mbit/s.

In read mode the SSI 32P3000 provides amplification and qualification of head preamplifier outputs. Pulse qualification is accomplished using level qualification of differentiated input zero crossings. An AGC amplifier is used to compensate for variations in head preamp output levels, presenting a constant input level to the pulse qualification circuitry. The AGC loop can be disabled so that a constant gain can be used for embedded servo decoding or other processing needs.

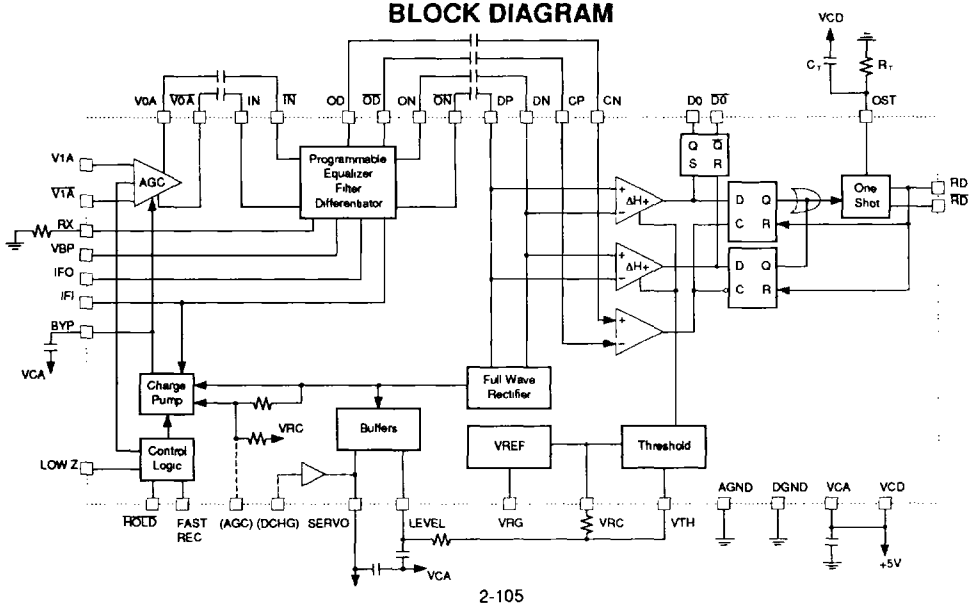
Write to read transient recovery is enhanced by providing AGC input impedance switching and a selectable Fast Recovery mode that provides a higher decay current.

Additionally, the SSI 32P3000 contains an integrated programmable electronic filter with cutoff frequencies between 9 and 27 MHz. High frequency boost (for pulse slimming) of up to +12db is also provided. The SSI 32P3000 requires only a +5V power supply and is available in a 36-pin SOM package.

FEATURES

- **Compatible with 48 Mbit/s data rate operation**
- **Fast attack/decay modes for rapid AGC recovery**
- **Low Drift AGC hold, fast AGC recovery, and low AGC input impedance control signals**
- **Includes programmable pulse slimming equalization and programmable channel filter and differentiator with no external filter components**
- **±0.5 ns filter group delay variation from 0.3 *fc* to *fc* = 26 MHz**
- **Independent positive and negative threshold qualification to supress error propagation**
- **0.5 ns max pulse pairing**
- **+5V only operation**
- **36-pin SOM package**

BLOCK DIAGRAM



SSI 32P3000
Pulse Detector with Programmable Filter

DESCRIPTION

The SSI 32P3000 Pulse Detector is designed to support a 48 Mbit/s data rate. The signal processing circuits include a wide band variable gain amplifier, a programmable electronic filter, differentiator and pulse slimming equalizer, a precision wide bandwidth fullwave rectifier, and a dual rate charge pump. A fully differential filter, differentiator, equalizer, and fullwave rectifier are provided to minimize external noise pickup. To optimize recovery for constant density recording, the AGC charge pump current tracks the programmable filter current IFI. The differentiator zero tracks the programmable filter cutoff frequency. Thus in constant density recording applications, an approximately constant differentiated signal amplitude is maintained. The desired filter response and equalization are easily programmed with the SSI 32D4661, Time Base Generator DACs. A dual rate attack charge pump and a Fast Decay mode are included for fast transient recovery. At maximum IFI current, the normal AGC attack current is .18 mA. When the signal exceeds 125% of the nominal signal level, the attack current is increased by a factor of 7. The nominal decay current is 4 μA. The decay current is increased 20 times when the FAST REC input is high. In this mode, transients that produce low gain will recover more rapidly with the Fast Decay current, while transients that produce high gain will put the circuit in the fast attack recovery mode. When LOW Z is high, the AGC amplifier input impedance is reduced to allow quick recovery of the AGC amplifier input ac coupling capacitors. When the HOLD input is low, the AGC action is stopped and the AGC amplifier gain is set by the voltage at the BYP pin. In most applications, the BYP pin voltage is stored on an external capacitor when HOLD goes low. In applications where AGC action is not desired, the BYP voltage can be set by a resistor divider network connected from VCC to VRC. If a programmable gain is desired, the resistor network could be driven by a current DAC. The precision fullwave rectifier produces an accurate Level and Servo output signal. These outputs are referenced to the reference voltage VRC. SERVO and LEVEL are buffered open emitter outputs with 100 ohm series current limiting resistors. These outputs could be further filtered with external capacitors.

Independent positive and negative threshold qualification comparators are used to suppress the error propagation of a positive and negative threshold hysterisis comparator. However, a slight amount of hysterisis is included to increase the comparator output time when a signal that just exceeds the threshold level is detected. This eases the timing with respect to the zero crossing clock comparator. A differential comparator with floating hysterisis threshold allows differential signal qualification for noise rejection. An accurate feed forward qualification level is generated by comparing the difference between Level and VRC. VRC is referenced to VCA. Thus with the VTH resistor network connected from VCA to VRC, an accurate fixed threshold can be established. A qualified signal zero crossing triggers the output one shot. The one shot period is set by an external resistor. Low level differential outputs are provided for high speed operation and to minimize noise generation.

PIN DESCRIPTION

INPUT PINS

NAME	TYPE	DESCRIPTION
VIA, $\overline{VIA}$		AGC Amplifier input pins.
IN, $\overline{IN}$		Equalizer/filter input pins.
DP, DN		Data inputs to data comparators and fullwave rectifier.
CP, CN		Differentiated data inputs to the clock comparator.
VTH		Threshold level setting input for the data comparators.
FACT REC		TTL compatible input when high puts the charge pump in the fast decay mode.
LOW Z		TTL compatible input when high reduces the AGC amplifier input resistance.
HOLD		TTL compatible input when low disables the AGC action by turning off the charge pump.
OUTPUT PINS		
VOA, $\overline{VOA}$		AGC amplifier output pins.
ON, $\overline{ON}$		Equalizer/filter normal output pins.
OD, $\overline{OD}$		Equalizer/filter differentiated output pins.
DO, $\overline{DO}$		ECL compatible data comparator latch output pins.
RD, $\overline{RD}$		ECL compatible read data output pins.
LEVEL		Open NPN emitter output that provides a fullwave rectified signal for the VTH input. The signal is referenced to VRC.
SERVO		Open NPN emitter output that provides a fullwave rectified servo signal. The signal is referenced to VRC.
ANALOG PINS		
OST		Pin for R_T C_T network to set RD output pulse width. An external C_T capacitor will not be required if an extra 15% pulse width tolerance error is acceptable.
VRC		Reference voltage pin for SERVO and LEVEL. VRC is referenced to VCA.
VRG		Reference voltage pin for the programmable filter. VRG is referenced to ground.
VBP		The equalizer high frequency boost is set by an external voltage applied to this pin. VBP must be proportional to VRG. Programmable boost is implemented by using a DAC that uses VRG as its reference. A fixed amount of boost can be set by an external resistor divide network connected from VBP to VRG and GND.
RX		Pin to set filter reference current. External resistor Rx from this pin to ground sets the filter reference current IFO.

PIN DESCRIPTION (Continued)

ANALOG PINS (Continued)

NAME	TYPE	DESCRIPTION
IFO		Reference current output pin. The reference current is normally supplied as the reference current to a current DAC which generates the programmable input current for the IFI pin.
IFI		Programmable filter input current pin. The filter cutoff frequency is proportional to the current into this pin. The current must be proportional to the reference current out of IFO. A fixed filter cutoff frequency is generated by connecting IFO to IFI and selecting Rx to set the desired frequency.
BYP		The AGC integrating capacitor C_A is connected between BYP and VCA.
VCA, VCD		Analog and Digital +5 volts.
AGND, DGND		Analog and Digital grounds.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, FAX (714) 731-5457