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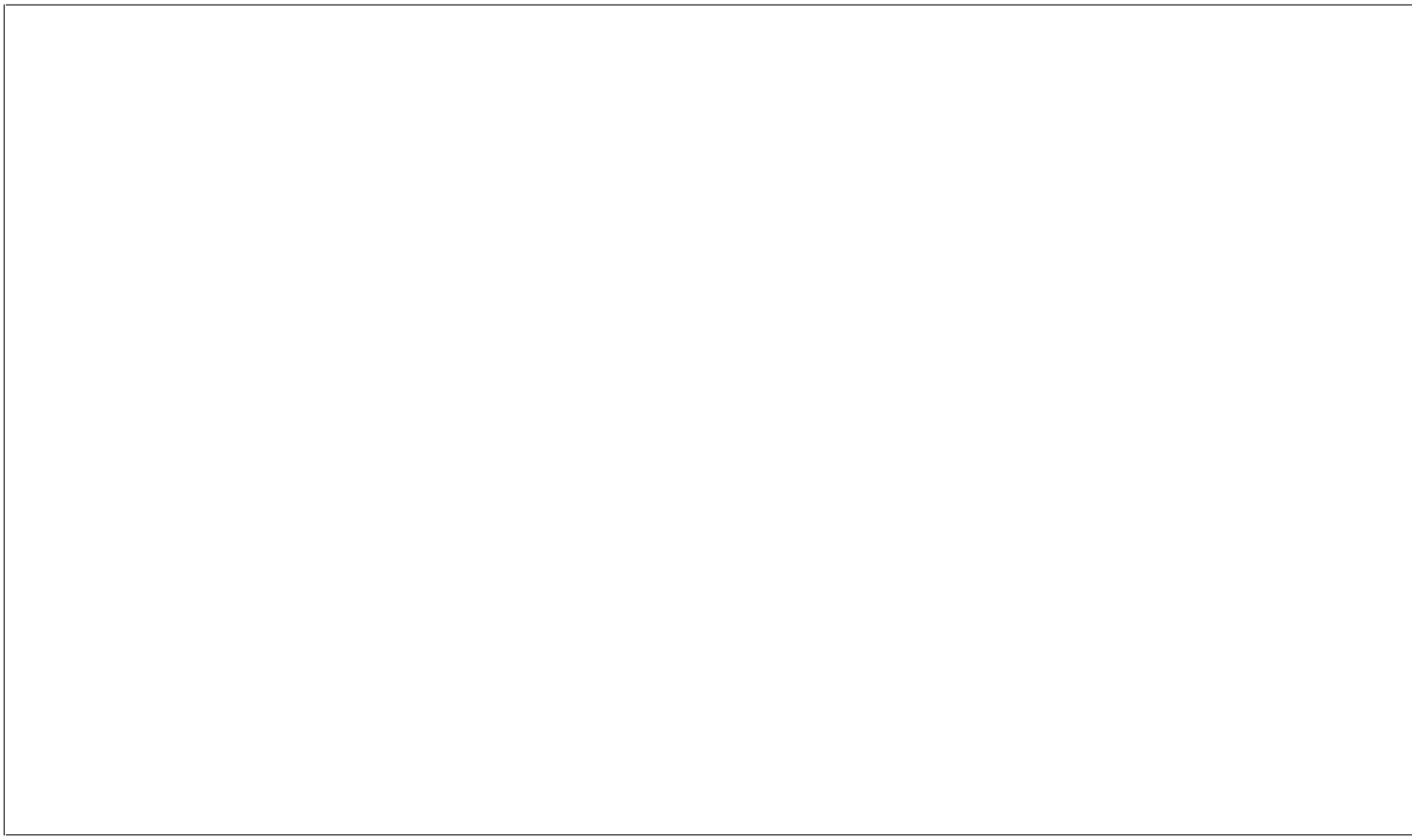

Components
for Entertainment Electronics

2 Band TV Tuner

TUA6022, TUA6024

Mixer-Oscillator-PLL
with balanced IF-Amplifier

Preliminary Data Sheet 03.99

Edition 03.99
Published by Siemens AG, Bereich Halbleiter, Marketing-Kommunikation, Balanstraße 73, 81541 München

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TUA6022, TUA6024 **Revision History:Current Version: 03.99**		
Previous Version:		
old Page	new Page	Subjects (major changes since last revision)

Data Classification

Maximum Ratings
Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Characteristics
The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25 °C and the given supply voltage.

Operating Range
In the operating range the functions given in the circuit description are fulfilled.
For detailed technical information about **"Processing Guidelines"** and
"Quality Assurance" for ICs, see our **"Product Overview"**.

SIEMENS

2 Band TV Tuner Mixer-Oscillator-PLL with balanced IF-Amplifier

TUA6022, TUA6024

Preliminary Data Sheet

BIPOLAR

1 Features

General

- Suitable for PAL tuners
- Full ESD protection

Mixer/Oscillator

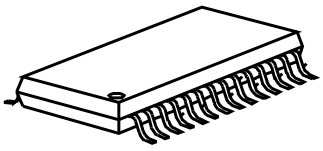
- High impedance mixer input for VHF
- Low impedance mixer input for UHF
- 4 pin oscillator for VHF
- 4 pin oscillator for UHF

IF-Amplifier

- balanced SAW preamplifier
- Low output impedance

PLL

- PLL with short lock-in time; no asynchronous divider stage
- High voltage VCO tuning output
- Fast I^2C bus
- 3 NPN bandswitch buffers
- Internal VHF/UHF switch
- Lock-in flag
- Power-down reset
- Programmable reference divider ratio (64, 80, 128)
- Programmable charge pump current



P-TSSOP-28-1

Package

2 Ordering Information

Type	Package	Ordering Code
TUA6022XS	P-TSSOP-28-1	Q67037-A1079
TUA6022-K	P-TSSOP-28-1	Q67037-A1080
TUA6022-S	P-TSSOP-28-1	Q67037-A1081
TUA6024XS	P-TSSOP-28-1	Q67037-A1082
TUA 6024-K	P-TSSOP-28-1	Q67037-A1055
TUA 6024-S	P-TSSOP-28-1	Q67037-A1056

3 Functional Description

The **TUA6022, TUA6024** device combines a digitally programmable phase locked loop (PLL), with a mixer-oscillator block including two balanced mixers and oscillators for use in TV tuners.

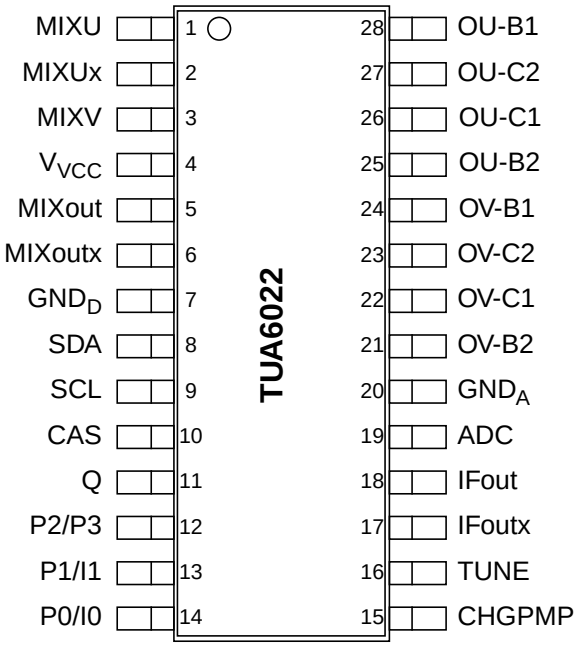
The PLL block with four hard-switched chip addresses forms a digitally programmable phase locked loop. With a 4 MHz quartz crystal, the PLL permits precise setting of the frequency of the tuner oscillator up to 900 MHz in increments of 62.5 kHz. The tuning process is controlled by a microprocessor via an I^2C bus. The device has three output ports, two of them (P0 and P1) can also be used as TTL input ports. A flag is set when the loop is locked. The input ports and lock flag can be read by the processor via the I^2C bus.

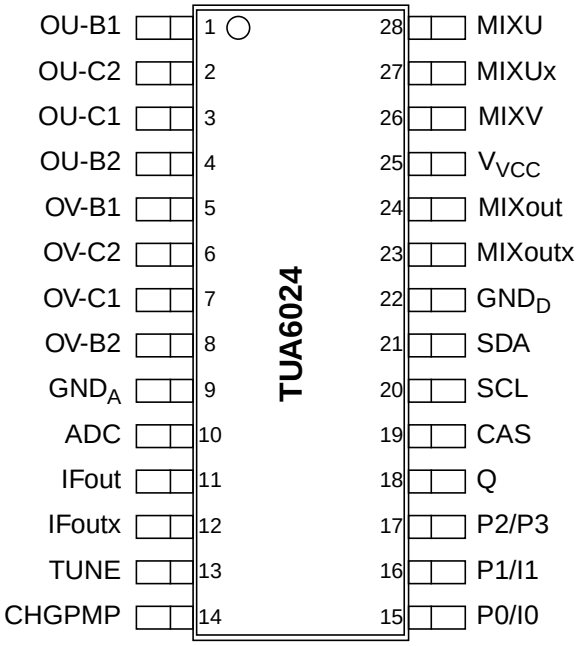
The mixer-oscillator block includes two balanced mixers (one mixer with high-impedance input and one mixer with a balanced low-impedance input), two frequency and amplitude-stable balanced oscillators for VHF, HYPER and UHF, a low-noise reference voltage source and a band switch.

4 Application

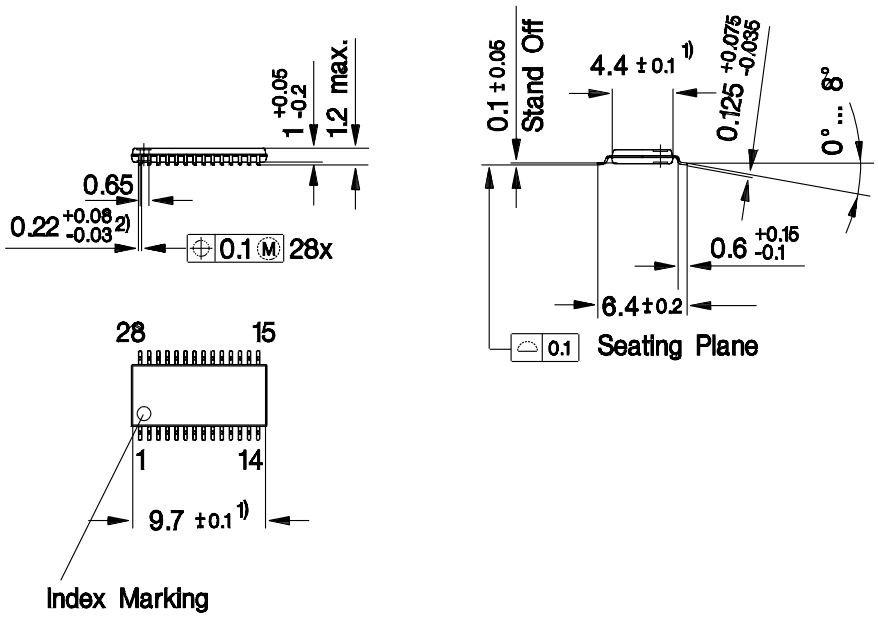
The IC is suitable for PAL tuners in TV- and VCR-sets or cable set-top receivers for analog TV and Digital Video Broadcasting.

5 Pin Configuration





6 Package Outlines



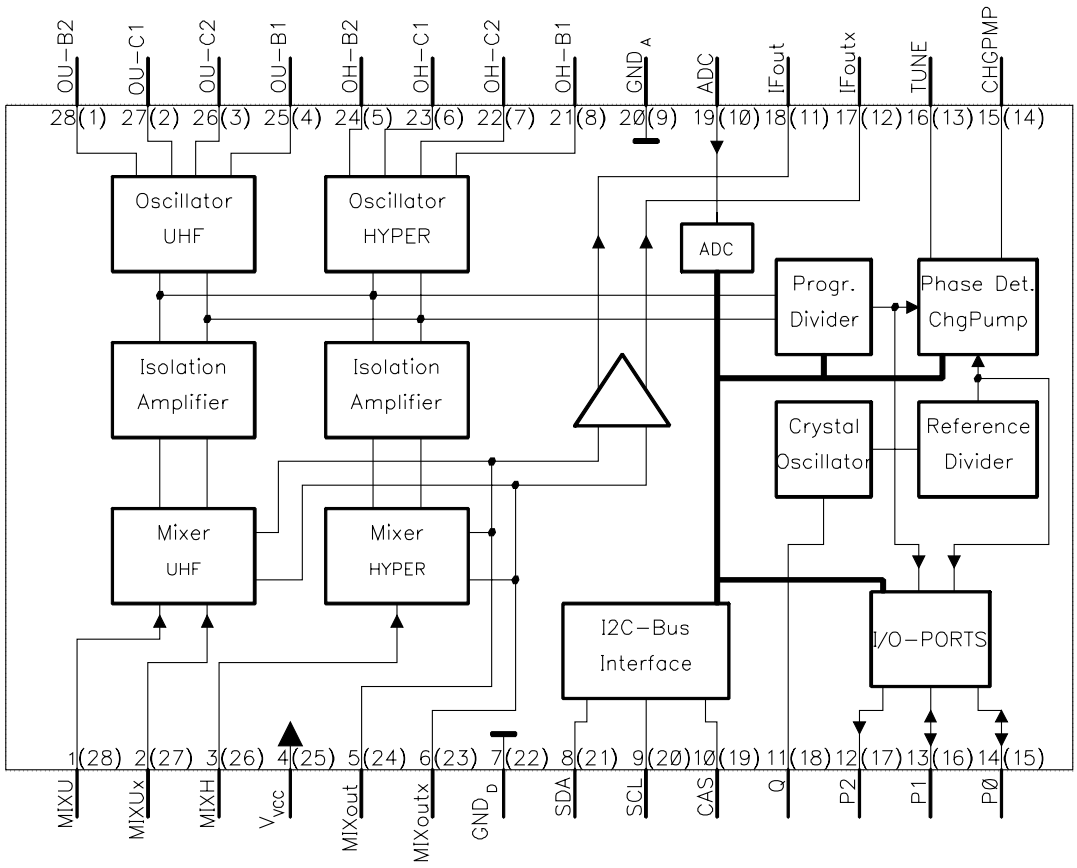
1) Does not include plastic or metal protrusion of 0.15 max. per side

2) Does not include dambar protrusion of 0.08 max. per side

7 Pin Definitions and Functions

Pin No.		Symbol	Function
TUA6024	TUA6022		
1	28	OU-B2	UHF oscillator amplifier, high-impedance base input, symmetrical to OU-B1
2	27	OU-C1	UHF oscillator amplifier, high-impedance collector output, symmetrical to OU-C2
3	26	OU-C2	UHF oscillator amplifier, high-impedance collector output, symmetrical to OU-C1
4	25	OU-B1	UHF oscillator amplifier, high-impedance base input, symmetrical to OU-B2
5	24	OV-B2	HYPER oscillator amplifier, high-impedance base input, symmetrical to OV-B1
6	23	OV-C1	HYPER oscillator amplifier, high-impedance collector output, symmetrical to OV-C2
7	22	OV-C2	HYPER oscillator amplifier, high-impedance collector output, symmetrical to OV-C1
8	21	OV-B1	HYPER oscillator amplifier, high-impedance base input, symmetrical to OV-B2
9	20	GND_A	Analog Ground
10	19	ADC	ADC input
11	18	IFout	IF output, symmetrical to IFoutx
12	17	IFoutx	Inverse IF output, symmetrical to IFout
13	16	TUNE	VCO tuning voltage output
14	15	CHGPMP	Charge pump output / loop filter
15	15	P0/I0	Port output / TTL input
16	13	P1/I1	Port output / TTL input
17	12	P2/P3	Port output (P2 = TUA6022-K, P3 = TUA6024-S)
18	11	Q	4 MHz low-impedance crystal oscillator input
19	10	CAS	Chip address select
20	9	SCL	Clock input for the I^2C bus
21	8	SDA	Data input/output for the I^2C bus
22	7	GND_D	Digital Ground
23	6	MIXoutx	Inverse Mixer output, symmetrical to MIXout
24	5	MIXout	Mixer output, symmetrical to MIXoutx
25	4	V_{VCC}	Analog supply voltage
26	3	MIXV	VHF mixer input, high-impedance
27	2	MIXUx	UHF mixer input, low-impedance, symmetrical to MIXU
28	1	MIXU	UHF mixer input, low-impedance, symmetrical to MIXUx

8 Block Diagram



The pin numbers given in parenthesis refer to the TUA 6022

9 Circuit Description

9.1 Mixer-Oscillator block

The mixer oscillator section includes two balanced mixers (double balanced mixer), two balanced oscillators for VHF and / or HYPER band and UHF, a reference voltage source and a band switch.
Filters between tuner input and IC separate the TV frequency signals into two bands. The band switching in the tuner front-end is done by using two or three port outputs. In the selected band the signal passes a tuner input stage with MOSFET amplifier, a double-tuned bandpass filter and is then fed to the balanced mixer input of the IC which has in case of VHF / Hyperband a high-impedance input and in case of UHF a low-impedance input. The input signal is mixed there with the signal from the activated on chip oscillator to the IF frequency which is filtered out at the balanced high-impedance output pair by means of a parallel tuned circuit. The following SAW preamplifier has a low output impedance to drive the SAW filter directly.

9.2 PLL block

The mixer-oscillator signal VCO/VCOx is internally DC-coupled as a differential signal at the programmable divider inputs. The signal subsequently passes through a programmable divider with ratio N = 256 through 32767 and is then compared in a digital frequency / phase detector to a reference frequency f_{ref} = 62.5 kHz. This frequency is derived from a unbalanced, low-impedance 4 MHz crystal oscillator (pin Q) divided by Q = 64.

The phase detector has two outputs UP and DOWN that drive two current sources I+ and I- of a charge pump. If the negative edge of the divided VCO signal appears prior to the negative edge of the reference signal, the I+ current source pulses for the duration of the phase difference. In the reverse case the I- current source pulses. If the two signals are in phase, the charge pump output (CHGPMP) goes into the high-impedance state (PLL is locked). An active low-pass filter integrates the current pulses to generate the tuning voltage for the VCO (internal amplifier, external pullup resistor at TUNE and external RC circuitry). The charge pump output is also switched into the high-impedance state when the control bit T0 = 1. Here it should be noted, however, that the tuning voltage can alter over a long period in the high-impedance state as a result of self-discharge in the peripheral circuity. TUNE may be switched off by the control bit OS to allow external adjustments.

If the VCO is not working the PLL locks to a tuning voltage of 33V.

By means of control bit 5I the pump current can be switched between two values by software. This programmability permits alteration of the control response of the PLL in the locked-in state. In this way different VCO gains can be compensated, for example.

The software-switched ports P0, P1 and P2 are general-purpose open-collector outputs. The test bit T1 = 1, switches the test signals f_{ref} (4 MHz / 64) and C_y (divided input signal) to P0 and P1 respectively. P0, P1 are bidirectional.

The lock detector resets the lock flag FL when the width of the charge pump current pulses is greater than the period of the crystal oscillator (i.e. 250 ns). Hence, when FL = 1, the maximum deviation of the input frequency from the programmed frequency is given by

$$\Delta f = \pm I_P (K_{VCO} / f_Q) (C_1+C_2) / (C_1C_2)$$

where I_P is the charge pump current, K_{VCO} the VCO gain, f_Q the crystal oscillator frequency and C_1, C_2 the capacitances in the loop filter (see application circuit). As the charge pump pulses at 62.5 kHz (= f_{ref}), it takes a maximum of 16 µs for FL to be reset after the loop has lost lock state.

Once FL has been reset, it is set only if the charge pump pulse width is less than 250 ns for eight consecutive f_{ref} periods. Therefore it takes between 128 and 144 µs for FL to be set after the loop regains lock.

9.3 I²C-Bus Interface

Data is exchanged between the processor and the PLL via the I²C bus. The clock is generated by the processor (input SCL), while pin SDA functions as an input or output depending on the direction of the data (open collector, external pull-up resistor). Both inputs have hysteresis and a low-pass characteristic, which enhance the noise immunity of the I²C bus.

The data from the processor pass through an I²C bus controller. Depending on their function the data are subsequently stored in registers. If the bus is free, both lines will be in the marking state (SDA, SCL are HIGH). Each telegram begins with the start condition and ends with the stop condition. Start condition: SDA goes LOW, while SCL remains HIGH. Stop condition: SDA goes HIGH while SCL remains HIGH. All further information transfer takes place during SCL = LOW, and the data is forwarded to the control logic on the positive clock edge.

The table ”Bit Allocation” (see 9.3.1 Bit Allocation Read / Write on page 8) should be referred to the following description. All telegrams are transmitted byte-by-byte, followed by a ninth clock pulse, during which the control logic returns the SDA line to LOW (acknowledge condition). The first byte is comprised of seven address bits. These are used by the processor to select the PLL from several peripheral components (chip select). The LSB bit (R/W) determines whether data are written into (R/W = 0) or read from (R/W = 1) the PLL.

In the data portion of the telegram during a WRITE operation, the MSB bit of the first or third data byte determines whether a divider ratio or control information is to follow. In each case the second byte of the same data type has to follow the first byte.
If the address byte indicates a READ operation, the PLL generates an acknowledge and then shifts out the status byte onto the SDA line. If the processor generates an acknowledge, a further status byte is output; otherwise the data line is released to allow the processor to generate a stop condition. The status word consists of two bits from the TTL input ports, three bits from the A/D converter, the lock flag and the power-on flag.

Four different chip addresses can be set by appropriate DC level at pin CAS (see 9.3.4 Address selection on page 9).

When the supply voltage is applied, a power-on reset circuit prevents the PLL from setting the SDA line to LOW, which would block the bus. The power-on reset flag POR is set at power-on and if V_{VCC} falls below 3.2 V. It will be reset at the end of a READ operation.

9.3.1 Bit Allocation Read / Write

Byte	MSB	bit6	bit5	bit4	bit3	bit2	bit1	LSB	Ack	Remarks
Write Data										
Address Byte	1	1	0	0	0	MA1	MA0	0	A	
Progr. Divider Byte 1	0	n14	n13	n12	n11	n10	n9	n8	A	
Progr. Divider Byte 2	n7	n6	n5	n4	n3	n2	n1	n0	A	
Control Byte 1	1	5I	T1	T0	1	RSA	RSB	OS	A	
Control Byte 2	x	x	x	x	P3	P2	P1	P0	A	
Read Data										
Address Byte	1	1	0	0	0	MA1	MA0	1	A	
Status Byte	POR	FL	x	I1	I0	A2	A1	A0	A	

9.3.2 Description of symbols

Symbol	Description
MA0, MA1	Address selection bits (see 9.3.4 Address selection on page 9)
n14 to n0	programmable divider bits: $N = 2^{14} \times n14 + 2^{13} \times n13 + ... + 2^3 \times n3 + 2^2 \times n2 + 2^1 \times n1 + n0$
5I	charge pump current: bit = 0 : charge pump current = 50 µA bit = 1 : charge pump current = 220µA
T1, T0	test bits (see 9.3.5 Test modes on page 9)
RSA, RSB	reference divider bits (see 9.3.6 Reference divider ratio on page 9)
OS	tuning amplifier control bit: bit = 0 : enable V_{TUNE} bit = 1 : disable V_{TUNE}
PO, P1, P2/P3	NPN ports control bits bit = 0 : NPN open-collector output is inactive, TTL inputs at P0, P1 bit = 1 : NPN open-collector output is active UHF / VHF bandswitch (see 9.3.3 UHF/VHF Bandswitch on page 9)
A0, A1, A2	ADC bits (see 9.3.7 A/D Converter levels on page 9)
I0, I1	input data from P0/I0, P1/I1
FL	PLL lock flag bit = 1 : loop is locked
POR	Power-on reset flag flag is set at power-on and reset at the end of READ operation
x	don‘t care

9.3.3 UHF/VHF Bandswitch

IC is in UHF mode	Ports Pn			
	P0	P1	P2	P3
TUA6022XS, TUA6024XS	x	1	x	n.a.
TUA6022-K, TUA6024-K	x	x	1	n.a.
TUA6022-S, TUA6024-S	x	x	n.a.	1

9.3.4 Address selection

Voltage at CAS	MA1	MA0
(0...0.1) * V_{VCC}	0	0
open circuit	0	1
(0.4...0.6) * V_{VCC}	1	0
(0.9...1) * V_{VCC}	1	1

9.3.5 Test modes

Test mode	T1	T0
Normal operation	0	0
Charge pump output, CHGPMP is in high-impedance state	0	1
P1 = Cy output, P0 = f_{ref} output	1	0
TTL-inputs I1/I0 are Cy/f_{ref} inputs of phase detector	1	1

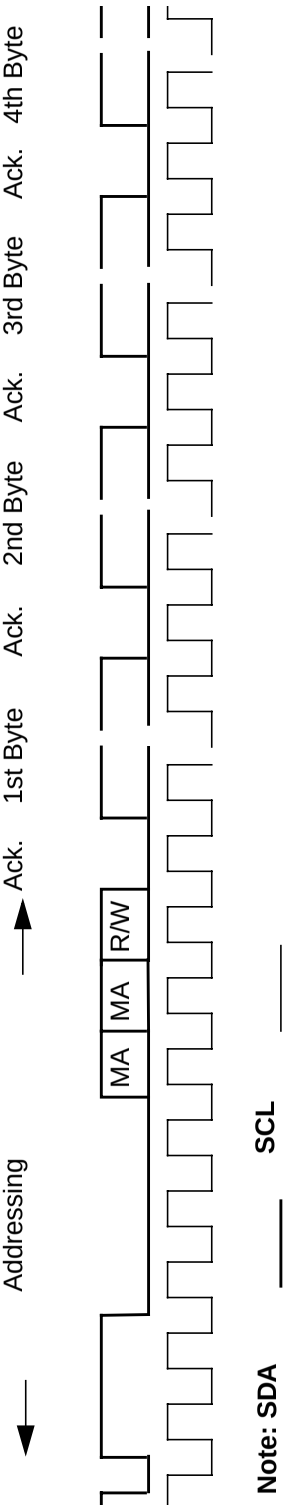
9.3.6 Reference divider ratio

Reference divider ratio	RSA	RSB
80	x	0
128	0	1
64	1	1

9.3.7 A/D Converter levels

Voltage at ADC	A2	A1	A0
(0...0.15) * V_{VCC}	0	0	0
(0.15...0.3) * V_{VCC}	0	0	1
(0.3...0.45) * V_{VCC}	0	1	0
(0.45...0.6) * V_{VCC}	0	1	1
(0.6...1) * V_{VCC}	1	0	0

9.3.8 I²C Bus Timing Diagram



Telegram examples:

Start-Addr-DR1-DR2-CW1-CW2-Stop
Start-Addr-CW1-CW2-DR1-DR2-Stop
Start-Addr-DR1-DR2-Stop
Start-Addr-CW1-CW2-Stop

Abbreviations:

Start	= start condition
Addr	= address byte
DR1	= prog. divider byte 1
DR2	= prog. divider byte 2
CW1	= control byte 1
CW2	= control byte 2
Stop	= stop condition

10 Electrical Characteristics

10.1 Absolute Maximum Ratings

The maximal ratings may not be exceeded under any circumstances, not even momentary and individual, as permanent damage to the IC will result.

Ambient Temperature under bias: T_A= -20 to +85° C

Parameter[1]	Symbol	Limit Values		Unit	Test Conditions
		min	max		
Supply voltage	V_{VCC}	-0.3	6	V	
Junction temperature	T_J		+150	°C	
Storage temperature	T_{Stg}	-40	+125	°C	
Thermal resistance (junction to ambient)	R_{thSA}		120	K/W	
PLL					
CHGPMP	V_{CHGPMP}	-0.3	3	V	
	I_{CHGPMP}		1	mA	
Crystal oscillator pins Q	V_Q		V_{VCC}	V	
	I_Q	-5		mA	
Bus input/output SDA	V_{SDA}	-0.3	V_{VCC}	V	
Bus output current SDA	$I_{SDA(L)}$		5	mA	open collector
Bus input SCL	V_{SCL}	-0.3	V_{VCC}	V	
Chip address switch CAS	V_{CAS}	-0.3	V_{VCC}	V	
VCO tuning output (loop filter)	V_{TUNE}	-0.3	35	V	
Port outputs P0...P2/P3	V_P	-0.3	V_{VCC}	V	
	$I_{P(L)}$	-1	15	mA	t_{max} = 0.1 sec. at 5.5 V
Total port output current	$\Sigma I_{P(L)}$		40	mA	t_{max} = 0.1 sec. at 5.5 V
Mixer-Oscillator					
Mix inputs VHF / Hyper	$V_{MIX\ V}$	-0.3	3	V	
Mix inputs UHF	$V_{MIX\ U}$		2	V	
	$I_{MIX\ U}$	-5	6	mA	
VCO base voltage	V_B	-0.3	3	V	
VCO collector voltage	V_C		V_{VCC}	V	
ESD-Protection[2]					
all pins	V_{ESD}		1	kV	

1. All values are referred to ground (pin), unless stated otherwise.
Currents with a positive sign flows into the pin and currents with a negative sign flows out of pin.

2. according to MIL STD 883D, method 3015.7 and EOS/ESD assn. standard S5.1 - 1993

10.2 Operating Range

Within the operational range the IC operates as described in the circuit description.
The AC / DC characteristic limits are not guaranteed.

Parameter	Symbol	Limit Values		Unit	Test Conditions
		min	max		
Supply voltage	V_{VCC}	+4.5	+5.5	V	
Programmable divider factor	N	256	32767		
VHF Mixer input frequency range	f_{MIXV}	40	500	MHz	
UHF Mixer input frequency range	f_{MIXU}	350	900	MHz	
VHF Oscillator frequency range	f_{OH}	75	560	MHz	
UHF Oscillator frequency range	f_{OU}	380	950	MHz	
Ambient temperature	T_{amb}	-20	+85	°C	

10.3 AC/DC Characteristics

AC / DC characteristics involve the spread of values guaranteed in the specified supply voltage and ambient temperature range. Typical characteristics are the median of the production.

Parameter T_A = 25 °C, V_{VCC}	Symbol	Limit Values			Unit	Test conditions
		min	typ	max		
Supply						
Supply voltage	V_{VCC}	4.5	5	5.5	V	
Current consumption	I_{VCC}	56	70	84	mA	
Digital Unit						
PLL						
Crystal oscillator connections Q						
Crystal frequency	f_Q	3.2	4.0	4.8	MHz	series resonance
Crystal resistance	R_Q	10		100	Ω	series resonance
Oscillation frequency	f_Q	3,99975	4,000	4,00025	MHz	f_Q = 4 MHz
Input impedance	Z_Q	-700	-900	-1100	Ω	f_Q = 4 MHz
Charge pump output CHGPMP						
HIGH output current	I_{CPH}	±90	±220	±300	µA	5I = 1, V_{CP} = 2 V
LOW output current	I_{CPL}	±22	±50	±75	µA	5I = 0, V_{CP} = 2 V
Tristate current	I_{CPZ}		+1		nA	T0 = 1, V_{CP} = 2 V
Output voltage	V_{CP}	1.0		2.5	V	locked
Drive output TUNE (open collector)						
HIGH output current	I_{TH}			10	µA	V_{TH} = 33 V, T0 = 1
LOW output voltage	V_{TL}			0.4	V	I_{TL} = 1.0 mA
I^2C-Bus						
Bus inputs SCL, SDA						
HIGH input voltage	V_{IH}	3		5.5	V	
LOW input voltage	V_{IL}	0		1.5	V	
HIGH input current	I_{IH}			10	µA	V_{IH} = V_S
LOW input current	I_{IL}	-10			µA	V_{IL} = 0 V
Bus output SDA (open collector)						
HIGH output current	I_{OH}			10	µA	V_{OH} = 5.5 V
LOW output voltage	V_{OL}			0.4	V	I_{OL} = 3 mA
Edge speed SCL,SDA						
Rise time	t_r			300	ns	
Fall time	t_f			300	ns	

Parameter T_A = 25 °C,V_{VCC}	Symbol	Limit Values			Unit	Test conditions
		min	typ	max		
Clock timing SCL						
Frequency	f_{SCL}	0		400	kHz	
HIGH pulse width	t_H	0.6			µs	
LOW pulse width	t_L	1.3			µs	
Start condition						
Set-up time	t_{susta}	0.6			µs	
Hold time	t_{hsta}	0.6			µs	
Stop condition						
Set up time	t_{susto}	0.6			µs	
Bus free	t_{buf}	1.3			µs	
Data transfer						
Set-up time	t_{sudat}	0.1			µs	
Hold time	t_{hdat}	0			µs	
Input hysteresis SCL, SDA	V_{hys}		200		mV	
Pulse width of spikes which are suppressed	t_{sp}	0		50	ns	
Capacitive load for each bus line	C_L			400	pF	
Port outputs P0, P1, P2/P3 (open collector)						
HIGH output current	I_{POH}			1	µA	V_{POH} = 5 V
LOW output voltage	V_{POL}			0.5	V	I_{POL} = 15 mA
TTL port inputs P0, P1						
HIGH input voltage	V_{PIH}	2.7			V	
LOW input voltage	V_{PIL}			0.8	V	
HIGH input current	I_{PIH}			10	µA	V_{PIH} = 5.5 V
LOW input current	I_{PIL}	-10			µA	V_{PIL} = 0 V
ADC port input						
HIGH input current	I_{ADCH}			10	µA	
LOW input current	I_{ADCL}	-10			µA	
Address selection input CAS						
HIGH input current	I_{CASH}			50	µA	V_{CASH} = 5 V
LOW input current	I_{CASL}	-50			µA	V_{CASL} = 0 V

Parameter T_A = 25 °C,V_{VCC}	Symbol	Limit Values			Unit	Test conditions
		min	typ	max		
Analog Unit						
VHF low and VHF high Band Section (including IF amplifier)						
Voltage gain	G_{MixV}	20	23	26	dB	f_{RF} = 43.25 to 463.25 MHz, f_{IF} = 33.4 to 58.75 MHz
Mixer noise figure	F_{MixV}		9	11	dB	f_{RF} = 43.25 to 463.25 MHz
Mixer input impedance	R_{MixV}	1	2	3	kΩ	serial equivalent circuit, f_{MixV} = 100 MHz
	C_{MixV}		2	3	pF	serial equivalent circuit, f_{MixV} = 100 MHz
Oscillator drift, PLL unlocked	Δf_{OscV}			400	kHz	V_S = 5 V±10%
				500	kHz	ΔT = 25 °C
				100	kHz	t = 5 s up to 15 min after switching on
Oscillator pulling, PLL unlocked	V_{MIXV}	100	108		dBµV	Δf = 10 kHz f_{RF} = 48.25 MHz
		80	88		dBµV	Δf = 10 kHz f_{RF} = 399.25 MHz
N + 5 pulling, PLL unlocked	V_{MIXV}	-50			dBc	f_{RF} = 48.25 MHz, f_{RF1} = 82.25 MHz, P_{RF}=P_{RF1} = 80dBµV
	V_{MIXV}	-50			dBc	f_{RF} = 399.25 MHz, f_{RF1} = 437.25 MHz, P_{RF}=P_{RF1} = 80dBµV
Oscillator phase noise	$L(fm)_{VHF}$	-80	-86		dBc/ Hz	fm = 10kHz, application circuit
IF suppression	a_{IF}	15	20		dB	V_{MixB} = 80 dBµV
UHF Band Section (including IF amplifier)						
Voltage gain	G_{MixU}	31	34	37	dB	f_{RF} = 367.25 MHz to 863.25 MHz, f_{IF} = 33.4MHz to 58.75 MHz
Mixer noise figure	F_{MixU}		6	9	dB	f_{RF} = 367.25 to 615.25 MHz
			7	10	dB	f_{RF} = 623.25 to 863.25 MHz
Mixer input impedance	R_{MixU}	14	20	26	Ω	serial equivalent circuit, f_{MixU} = 600 MHz
	L_{MixU}	6	10	14	nH	serial equivalent circuit, f_{MixU} = 600 MHz

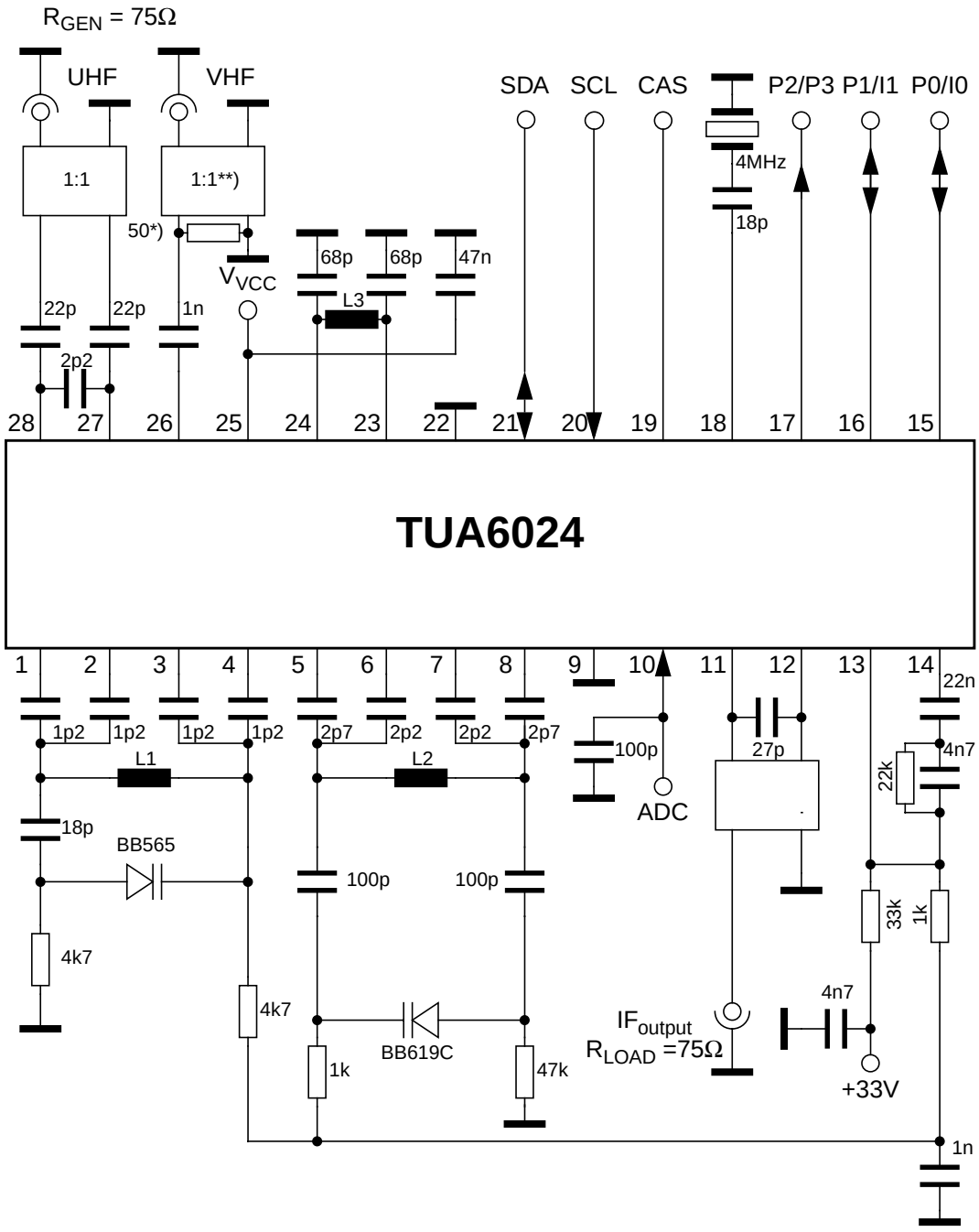
Parameter T_A = 25 °C, V_{VCC}	Symbol	Limit Values			Unit	Test conditions
		min	typ	max		
Oscillator drift, PLL unlocked	Δf_{OscU}			400	kHz	V_S = 5 V±10%
				800	kHz	ΔT = 25 °C
				100	kHz	t = 5 s up to 15 min after switching on
Oscillator pulling, PLL unlocked	V_{MIXU}	100	108		dBµV	Δf = 10 kHz f_{RF} = 375.25 MHz
		100	108		dBµV	Δf = 10 kHz f_{RF} = 847.25 MHz
N + 5 pulling, PLL unlocked	V_{MIXU}	-50			dBc	f_{RF} = 471.25 MHz, f_{RF1} = 510.25 MHz, P_{RF} = P_{RF1} = 80dBµV
	V_{MIXU}	-50			dBc	f_{RF} = 847.25 MHz, f_{RF1} = 886.25 MHz, P_{RF}= P_{RF1} = 80 dBµV
Oscillator phase noise	$L(fm)_{UHF}$	-80	-86		dBc/ Hz	fm = 10kHz, application circuit
IF suppression	a_{IF}	15	20		dB	V_{MixB} = 80 dBµV
SAW preamplifier						
IF output impedance	R_{IFout}, R_{IFoutx}			80	Ω	serial equivalent circuit, f_{IF} = 38.9 MHz
	L_{IFout} L_{IFoutx}		tbf		nH	
Rejection at the IFoutput						
Channel 6 beat	INT_{CH6}	tbf	tbf		dBc	V_{RFpix} = V_{RFsnd} = 80 dBµV; note 1
Channel A-5 beat	INT_{CHA-5}	tbf	tbf		dBc	V_{RFpix} = 80 dBµV; note 2

Notes:

1. Channel 6 beat is the interfering product of f_{RFpix}, f_{RFsnd} - f_{OSC} of channel 6 at 42 MHz.
2. Channel A-5 beat is the interfering product of f_{RFpix} + f_{RFsnd} - f_{OSC} of channel A-5,f_{BEAT} = 45.5 MHz. The possible mechanisms are: f_{OSC} - 2 x f_{IF} or 2 x f_{RFpix} - f_{OSC}. For the measurement V_{RF} = 80 dBµV.

11 Test Circuit

11.1 DC and RF Parameter Measurement

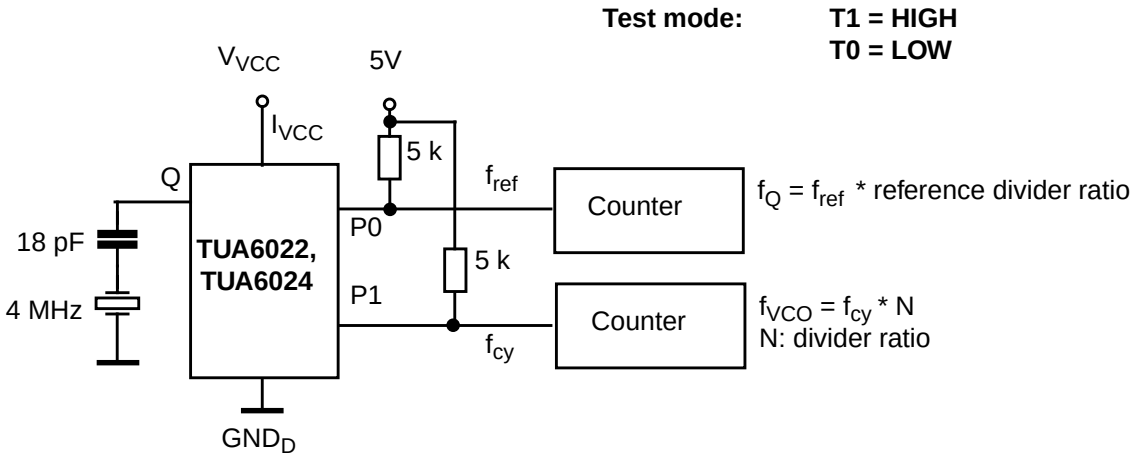


*) not for noise measurement
**) 1:2 transformer for noise measurement

Coils:

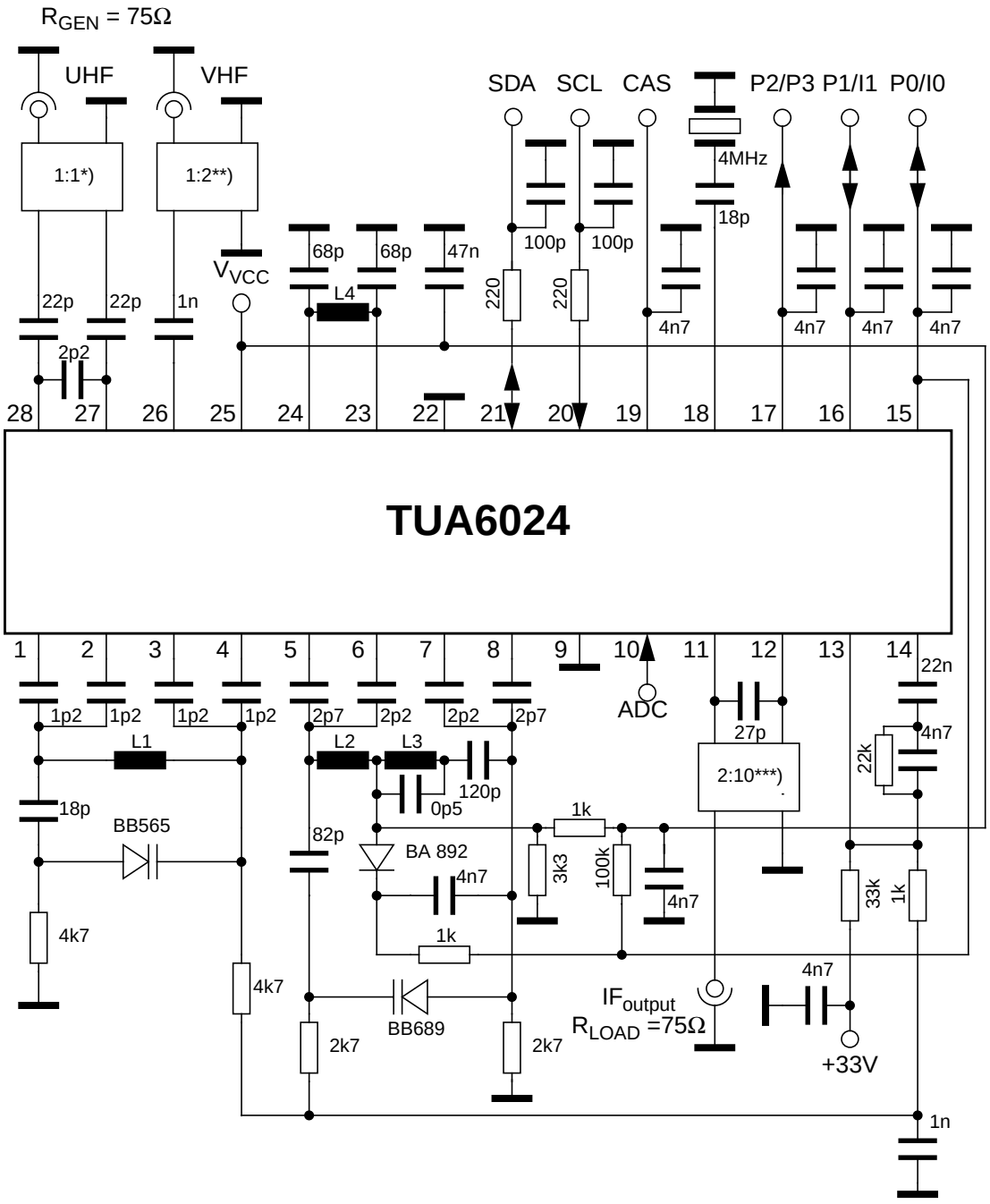
coil	turns	wire size [mm]	coil diameter [mm]
L1	2	0.4	3
L2	4	0.4	3
L3	Neosid Part-No. 00503600 0.58µH		

11.2 Measurement of Crystal Oscillator Frequency



12 Application Circuit

12.1 Application Circuit (Evaluation Board)



Transformers:

*)	TOKO B4F Type 617DB-1023
**)	TOKO B4FType 617PT-1026
***)	TOKO 7KL 291GCS-1499F

RF-Bands:

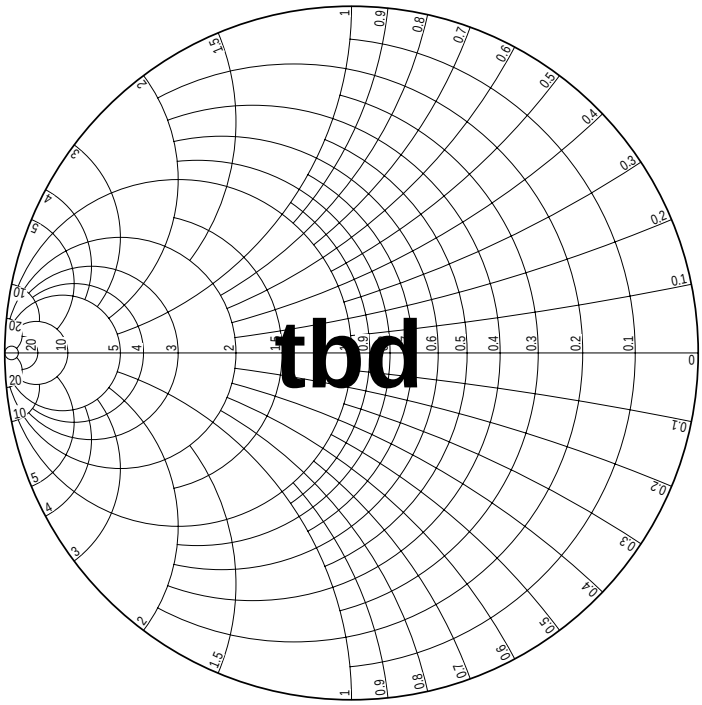
48.25 MHz	to	147.25 MHz
154.25 MHz	to	423.25 MHz
431.25 MHz	to	855.25 MHz

Coils:

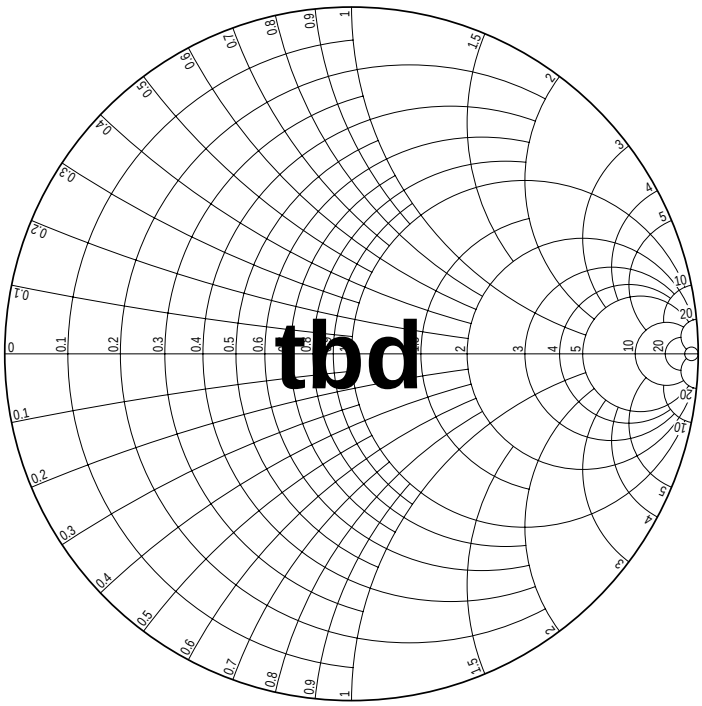
coil	turns	wire size [mm]	coil diameter [mm]
L1	1.5	0.4	2
L2	2.5	0.5	2.5
L3	8.5	0.5	3
L4	14.5	0.3	4

13 Electrical Diagrams

13.1 Input admittance VHF mixer input Y_0 = 20mS (single ended)



13.2 Input impedance UHF mixer input Z_0 = 50 Ω (symmetrical)



13.3 Output impedance IF output Y_0 = 20mS (symmetrical)