

BIPOLAR HIGH-SPEED 6-BIT FLASH A/D CONVERTER

DESCRIPTION

The TS 83016 is a monolithic bipolar 6-bit parallel flash analog-to-digital converter, which is an alternate source for the AD9016 circuit.

The TS 83016 uses 64 parallel comparators to digitize fast moving analog input signals without external sample-and-hold circuits or input buffers. The analog input is designed for -1 V to $+1\text{ V}$ operation.

In this TS 83016, the performance and features of the TS 83006 are combined with on-board demultiplexing circuits. Output data of the TS 83016 are demultiplexed to two 6-bit data banks, each of which includes a Data Ready signal and overflow bit.

Controls pins allow to invert the MSB and/or LSBs of each data bank.

With encode rates up to 600 MHz, the TS 83016 is specified to operate from commercial to military temperature range with an analog input frequency up to 200 MHz, making it ideal for a variety of applications and environments. The TS 83016 is packaged in a hermetic 68-pin LCCC configuration and is also available in die form.

MAIN FEATURES

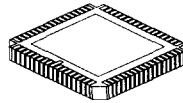
- 6-bit resolution.
- 600 MHz sampling rate.
- 32 dB SNR at 200 MHz analog input.
- Demultiplexed outputs, each with data ready signal and overflow bit.
- Power consumption : 1.70 W.
- 550 MHz large signal input bandwidth.
- $-55^{\circ}\text{C} / +125^{\circ}\text{C}$ specified.
- ECL 10 K compatible.
- Overflow bit & bit invert functions.
- Very low input capacitance : 8 pF.
- No sample & hold required.
- Pin to pin compatible with AD 9016.

SCREENING

- Standard.
- MIL-STD-883, class B.

APPLICATIONS

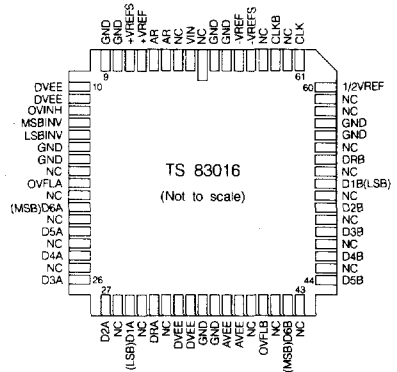
- Military systems.
- Radar pulse analysis.
- Electronic countermeasures.
- Transient recorders.
- Communication/signal intelligence.



E
LCCC 68
(Leadless Ceramic Chip Carrier)

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PIN CONNECTIONS
(Top view)
LCCC CERAMIC - 68 PINS



Note : For details see «Pin Description»

ABSOLUTE MAXIMUM RATINGS (see Note)

Parameter	Symbol	Value	Unit
Positive supply voltage	A_R	0.7 to 5.5	V
Negative supply voltage	AV_{EE}, DV_{EE}	-6 to +0.3	V
Upper reference voltage	$+V_{REF}, +V_{REFS}$	-1.5 to 1.5	V
Lower reference voltage	$-V_{REF}, -V_{REFS}$		
Midscale reference voltage	$1/2 V_{REF}$		
Analog input voltage	V_{IN}		
Reference voltage range	$+V_{REF}$ to $-V_{REF}$	2.2	V
Clock input voltages	CLK, CLKB	V_{EE} to 0	V
Maximum difference between negative supplies	DV_{EE} to AV_{EE}	± 0.5	V
Digital output current	I_D	20	mA
Midscale reference, upper reference sense, low reference sense current	$I(-V_{REFS}, 1/2 V_{REFS}, +V_{REFS})$	4	mA
Junction temperature	T_j	+175	$^{\circ}C$
Storage temperature	T_{stg}	-65 to +150	$^{\circ}C$
Operating temperature range	T_{case}	-55 to +125	$^{\circ}C$
Lead temperature (soldering 10 s)	T_{leads}	+260	$^{\circ}C$
Digital input voltages	LSB _{INV} , MSB _{INV} , OV _{INH}	V_{EE} to 0	V
Note : Absolute maximum ratings are limiting values applied individually while other parameters are within specified operating conditions. Long exposure to maximum rating may affect device reliability.			

USER WARNING

The power supplies must be applied before all the other signals to prevent damage from occurring on the device.

To prevent reliability problem and dynamic performance damage, high speed transition on power supply must be avoided.

SPECIFICATIONS

Electrical operating characteristics

 $V_{EE} = DV_{EE} = -5.2\text{ V}$; $AR = 3\text{ V}$; $R_L = 100\ \Omega$ to -2 V ; $T_C = 25^\circ\text{C}$ (unless otherwise specified)

Parameter	T _{case}	Test level	Min.	Typ.	Max.	Unit
RESOLUTION			6			Bits
DIGITAL INPUTS AND OUTPUTS				ECL 10 K		
Logic compatibility						
Clock inputs						
• Logic «0» voltage	full	IV			-1.5	V
• Logic «1» voltage	full	IV	-1.1			V
Output data						
• Logic «0» voltage (Note 1)	full	II, D			-1.5	V
• Logic «1» voltage (Note 2)	full	II, D	-1.1			V
MAXIMUM CLOCK FREQUENCY		III	500	600		MHz
ANALOG INPUT						
Voltage range	full	V		±1		V
Input capacitance		IV		8		pF
Input resistance		V		350		k Ω
Analog bandwidth (Note 3)		V		550		MHz
REFERENCE INPUT						
Differential reference voltage	full	II, D		2	2.1	V
Reference ladder resistance	full	II, D	90	150	210	Ω
POWER REQUIREMENTS						
Positive supply voltage	full	I, D II	2 2	3 3	5.25 5.25	V V
Positive supply current (AR = 3 V)	full	I, D II		40 45	62 65	mA mA
Negative supply voltage	full	I, D II	-5.7 -5.7	-5.2 -5.2	-4.7 -4.7	V V
Negative supply current (V _{EE} = -5.2 V)	full	I, D II		290 320	365 400	mA mA
Nominal power dissipation (Note 4)		V				W
Reference ladder dissipation		V		30		mW
THERMAL RESISTANCE						
Junction-to-ambient (Note 5)		V		33		$^\circ\text{C/W}$
Junction-to-case		V		1.2		$^\circ\text{C/W}$
ACCURACY						
Integral nonlinearity (Note 6)	full	I, D II		0.1 0.15	0.25 0.5	LSB LSB
Differential nonlinearity (Note 6)	full	I, D II		0.15 0.2	0.25 0.5	LSB LSB
Monotonicity and no missing codes	full	IV	Guaranteed over specified temperature range			

SPECIFICATIONS (Continued)

Electrical operating characteristics

$AV_{EE} = DV_{EE} = -5.2\text{ V}$; $AR = 3\text{ V}$; $R_L = 100\ \Omega$ to -2 V ; $T_C = 25^\circ\text{C}$ (unless otherwise specified)

Parameter	Test level	Min.	Typ.	Max.	Unit
DYNAMIC CHARACTERISTICS					
Signal to noise ratio (SNR)					
$F_S = 500\text{ MHz}$ $F_{in} = 1\text{ MHz}$	III	34.9	36.1		dB
$F_S = 400\text{ MHz}$ $F_{in} = 10\text{ MHz}$	III	34.9	36.1		dB
$F_S = 400\text{ MHz}$ $F_{in} = 100\text{ MHz}$	III	31.8	34		dB
$F_S = 400\text{ MHz}$ $F_{in} = 196\text{ MHz}$	III	28.2	32		dB
$F_S = 10\text{ MHz}$ $F_{in} = 1.5\text{ MHz}$	D	35.5	37		dB
Total harmonic distortion (THD)					
$F_S = 500\text{ MHz}$ $F_{in} = 1\text{ MHz}$	III	42	48		dB
$F_S = 400\text{ MHz}$ $F_{in} = 10\text{ MHz}$	III	42	44		dB
$F_S = 400\text{ MHz}$ $F_{in} = 100\text{ MHz}$	III	33	36		dB
$F_S = 400\text{ MHz}$ $F_{in} = 196\text{ MHz}$	III	31	36		dB
$F_S = 10\text{ MHz}$ $F_{in} = 1.5\text{ MHz}$	D	35.5	37		dB
Effective number of bits					
$F_S = 500\text{ MHz}$ $F_{in} = 1\text{ MHz}$	III	5.5	5.7		Bits
$F_S = 400\text{ MHz}$ $F_{in} = 10\text{ MHz}$	III	5.5	5.7		Bits
$F_S = 400\text{ MHz}$ $F_{in} = 100\text{ MHz}$	III	5.0	5.4		Bits
$F_S = 400\text{ MHz}$ $F_{in} = 196\text{ MHz}$	III	4.4	5.1		Bits
$F_S = 10\text{ MHz}$ $F_{in} = 1.5\text{ MHz}$	D	5.6	5.9		Bits
Note 1 : With $I_{OUT} = 2\text{ mA}$.					
Note 2 : With $I_{OUT} = 12\text{ mA}$.					
Note 3 : See definition of terms.					
Note 4 : With $AR = 3\text{ V}$. $AV_{EE} = DV_{EE} = -5.2\text{ V}$.					
Note 5 : 33°C/W on glass epoxy board. 18°C/W on ceramic board.					
Note 6 : Histogram based on sampling of 1.5 MHz sinusoidal analog signal with and encode rate of 10 MHz .					

EXPLANATION OF TEST LEVELS	
Test level	
I	100 % production tested.
II	100 % production tested at $+25^\circ\text{C}$, and sample tested at specified temperatures.
III	Sample tested only.
IV	Parameter is guaranteed by design and characterization testing.
V	Parameter is a typical value only.
D	100 % probe tested on wafer at $T_{amb} = +25^\circ\text{C}$.



TIMING DIAGRAM

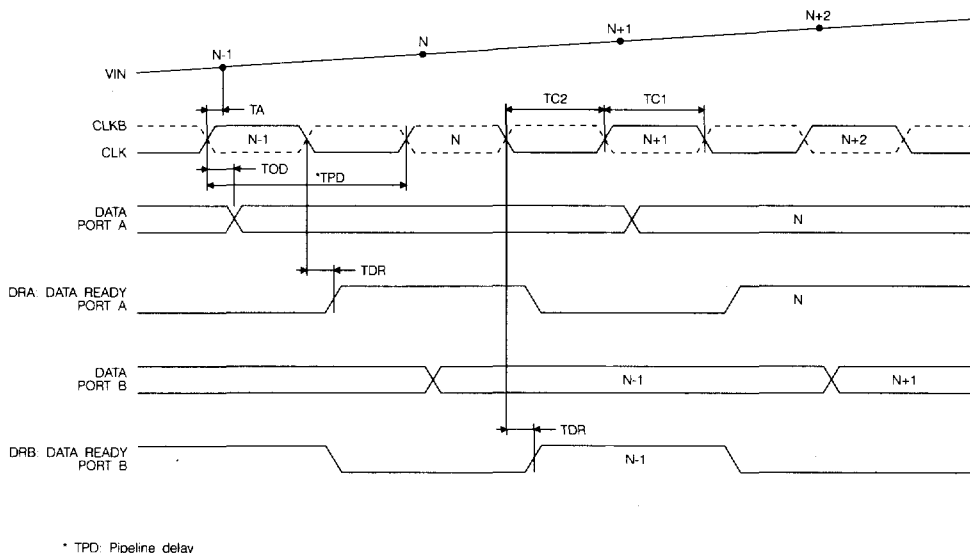


Figure 1

SWITCHING PERFORMANCES (Notes 1 and 2)

Parameter	Symbol	Typ.	Unit
Minimum Clock pulse width (high)	TC1	0.8	ns
Minimum Clock pulse width (low)	TC2	1	ns
Aperture delay	TA	0.3	ns
Aperture uncertainty (Note 1)		3	ps
Output delay	TOD	2.9	ns
Data ready output delay	TDR	3.7	ns
Output rise time (Note 3)		1.1	ns
Output fall time (Note 3)		1.3	ns

Note 1 : See definitions of terms.
Note 2 : $AV_{EE} = DV_{EE} = -5.2V$; $AR = 3V$; $+V_{REF} = +1V$; $-V_{REF} = -1V$.
Note 3 : Outputs terminated through $100\ \Omega$ to $-2V$. $C_{load} < 6\ pF$. Clock command rise/fall time should be less than 1.5 ns in normal operating mode.

FUNCTIONAL BLOCK DIAGRAM

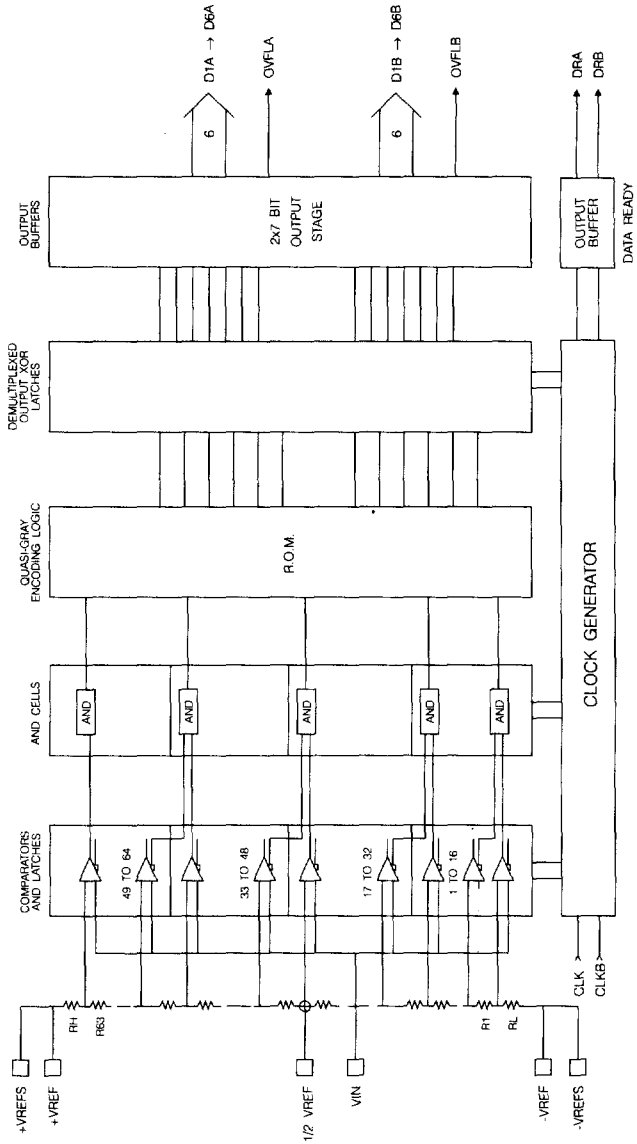


Figure 2

PIN DESCRIPTION

Pin	Name	Function
4, 5	AR	Positive supply voltage, (analog return)
37, 38	AV _{EE}	Negative supply voltage, analog section
61	CLK	Non inverted input of clock command (ECL)
63	CLKB	Inverted input of clock command (ECL)
29, 27, 26, 24, 22, 20	D1A-D6A	Digital data output (ECL), port A
10, 11, 33, 34	DV _{EE}	Negative supply voltage, digital section
31	DRA	Data ready output signal (ECL), port A
52, 50, 48, 46, 44, 42	D1B-D6B	Digital data output (ECL), port B
54	DRB	Data ready output signal (ECL), port B
8, 9, 15, 16, 35, 36, 56, 57, 67, 68	GND	Ground connections. Pins 8, 9, 15, 16, 35, 36, 56 and 57 are digital ground Pins 67 and 68 are analog ground
14	LSB _{INV}	LSBs invert, (D1 - D5) (see note 1)
13	MSB _{INV}	MSBs invert, (D6) (see note 2)
18	OVFLA	Overflow data output (ECL), port A
40	OVFLB	Overflow data output (ECL), port B
12	OVINH	Overflow inhibit (see note 3)
2	V _{IN}	Analog input, nominally between -1 V and +1 V
66	-V _{REF}	Negative reference voltage
65	-V _{REFS}	Negative reference voltage sense
60	1/2 V _{REF}	Midpoint of reference resistor ladder
6	+V _{REF}	Positive voltage reference
7	+V _{REFS}	Positive reference voltage sense
1, 3, 17, 19, 21, 23, 25, 28, 30, 32, 39, 41, 43, 45, 47, 49, 51, 53, 55, 58, 59, 62, 64	NC	Not connected

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Seal ring of LCCC 68 package is internally connected to ground. Heat spreader of LCCC 68 is internally connected to V_{EE} (device substrate).

Note 1 : When tied at V_{EE} (or floating), lower order (D1-D5) output bits are inverted. No inversion when grounded.

Note 2 : When tied at V_{EE} (or floating), MSB is inverted. No inversion when grounded.

Note 3 : When connected to ground, the overflow bit is inhibited and the nonreturn-to-zero feature is activated.

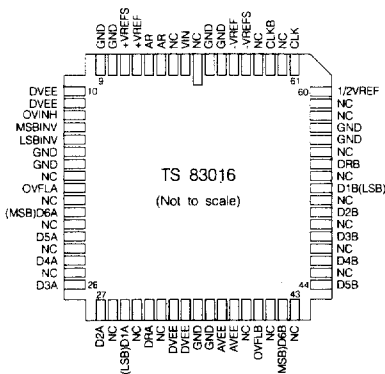


Figure 3

THEORY OF OPERATION

The block diagram (see page 6) shows a conventional flash converter structure having one comparator per state. This architecture enables very high speed operation, without external sample and hold.

The analog input signal is fed to all comparators, and is compared to a set of 64 reference levels (6 bits + overflow), derived from a resistor ladder network.

Midpoint tap (1/2 V_{REF}) of the reference ladder is provided for linearity adjustment or transfer function modification.

When not used, a decoupling capacitor of 100 nF connected to AGND is recommended to minimize high frequency noise injection.

A set of 64 AND latches following the comparator array indicates the appropriate quantization level of the analog input signal. An encoder stage and master-slave latches provide synchronized output data in binary code.

High speed output ECL buffers using active pulldown current sources, makes it possible to drive capacitive loads (up to 6 pF) at maximum sampling rate without the need of external buffers.

A Data Ready circuit delivers differential output strobe signals, (DRA, DRB) which track internal propagation delay, and facilitate in output data acquisition.

The output data words alternate between demultiplexed Data Port A and Data Port B, at half the converter's sample rate.

APPLICATIONS

User warning

The power supplies must be applied before all the other signals to prevent damage from occurring on the device.

Functional description

The TS 83016 operates with input analog signals varying between $\pm V_{REF}$ reference voltages, (Nominally $+V_{REF} = +1\text{ V}$, $-V_{REF} = -1\text{ V}$), applied across an internal resistor ladder.

Maximum differential Reference voltage is 2.1 V, so external reference generator circuit must limit the voltage to this value, to avoid permanent damage caused to the TS 83016 by excessive current densities.

The offset errors caused by input $\pm V_{REF}$ access resistances, can be cancelled using voltage sense lines ($\pm V_{REFS}$ pins). (Maximum sense current : 500 μA).

The typical input capacitance of the TS 83016 is 8 pF, which can be driven directly by most 50 Ω signal sources.

Differential input ECL clock signals are recommended for the TS 83016, to reduce jitter and thus to improve output noise floor. Fast clock transition times (< 500 ps, 300 ps recommended), are required when digitizing high-frequency input waveforms.

Clock generator with very low clock period jitter should also be used.

The differential Data Ready (DRA, DRB) signals track the internal propagation delay of output data (typically $TDR = 3.7\text{ ns}$). This enables easy external clock generation for output data acquisition over full temperature range.

Internal output ECL buffers were designed for driving heavy capacitive loads (up to 6 pF) at maximum Data rates.

Output Data format can be determined by two control pins :

LSB_{INV}, which allows the user to invert the five least significant bits.

MSB_{INV}, which allows the most significant bit to be inverted.

Selection among True/Inverted Binary, and True/Inverted Two's Complement output coding, is handled by proper setting of LSB_{INV}, MSB_{INV} control pins. (see TS 83016 Truth Table).

The OVINH (Overflow inhibit) control pin handles output RZ (Return to zero), or NRZ (Non Return to Zero) feature in overflow conditions.

When OVINH is connected to V_{EE} or allowed to float, and V_{IN} exceeds $+V_{REFS}$ sense voltage, overflow bit turns to ECL logic 1, and output bits to ECL logic 0.

For normal operation, (i.e. True Binary, Return to Zero), the LSB_{INV} and MSB_{INV} control pins are to be connected to Ground and OVINH tied at V_{EE} (or allowed to float).

Timing

Output Data change on rising edge of clock signal, (Comparators in latch mode), after T_{od} (typ = 2.9 ns) output propagation delay. (Pipeline delay is one clock cycle).

Output Data should be latched on rising edge of Data Ready signals (DRA, DRB), corresponding to falling edge of Clock input command (see Figure 1, Timing Diagram).

Application board layout and power supplies recommendations

Multilayer printed circuit board is recommended, because it enables compact implementation, and allows easy design of low impedance continuous Supply and Ground planes.

Digital input/output signal paths length should be matched and kept short, to avoid propagation delay mismatches, increased output bits times skew, and reflections.

So long as propagation delay along the line is shorter than digital signal rise or fall time, the reflection has little effect on the waveform.

However, if long interconnection lengths cannot be avoided, proper design of transmission line impedance with adapted ECL termination loads has to be observed.

It is important that separate supply planes be retained for Analog and Digital V_{EE} . Proper Supply decoupling by high resonant frequency chip capacitor near the device, and high quality tantalum capacitor at each power supply incoming, is especially recommended.

Packaging

The TS 83016 is packaged in a 68 LCCC chip carrier, with Tungsten-Copper heat spreader.

The top of the LCCC 68 Package (Heat spreader) is internally connected to V_{EE} (Device substrate).

A seal ring is internally connected to ground, which reduces internal coupling and thus improves output noise floor.

Sockets may be used for prototype evaluation, but should be avoided after-wards, because of possible limitations of TS 83016 dynamic performance.

TRUTH TABLE

Step	Input voltage	OVINH	Binary		Two's complement	
			True	Inverted	True	Inverted
			MSB _{INV} (GND) LSB _{INV} (GND)	MSB _{INV} (V _{EE})* LSB _{INV} (V _{EE})*	MSB _{INV} (V _{EE})* LSB _{INV} (GND)	MSB _{INV} (GND) LSB _{INV} (V _{EE})*
00	-1.000	x	000 000	111 111	100 000	011 111
01	-0.968	x	000 001	111 110	100 001	011 110
—	—	x	—	—	—	—
—	—	x	—	—	—	—
—	—	x	—	—	—	—
31	-0.031	x	011 111	100 000	111 111	000 000
32	-0.000	x	100 000	011 111	000 000	111 111
33	+0.031	x	100 001	011 110	000 001	111 110
—	—	x	—	—	—	—
—	—	x	—	—	—	—
—	—	x	—	—	—	—
62	+0.938	x	111 110	000 001	011 110	100 001
63	+0.969	x	111 111	000 000	011 111	100 000
> 63	+1.000	«1»	(0) 111 111**	(0) 000 000**	(0) 011 111**	(0) 100 000**
		«0»	(1) 000 000***	(1) 111 111***	(1) 100 000***	(1) 011 111***

* V_{EE} or floating.
 ** OVINH (overflow inhibit) = GND
 *** OVINH = V_{EE} (or floating). (Overflow bit is always zero except where noted in parentheses).

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EVALUATION BOARD BLOCK DIAGRAM

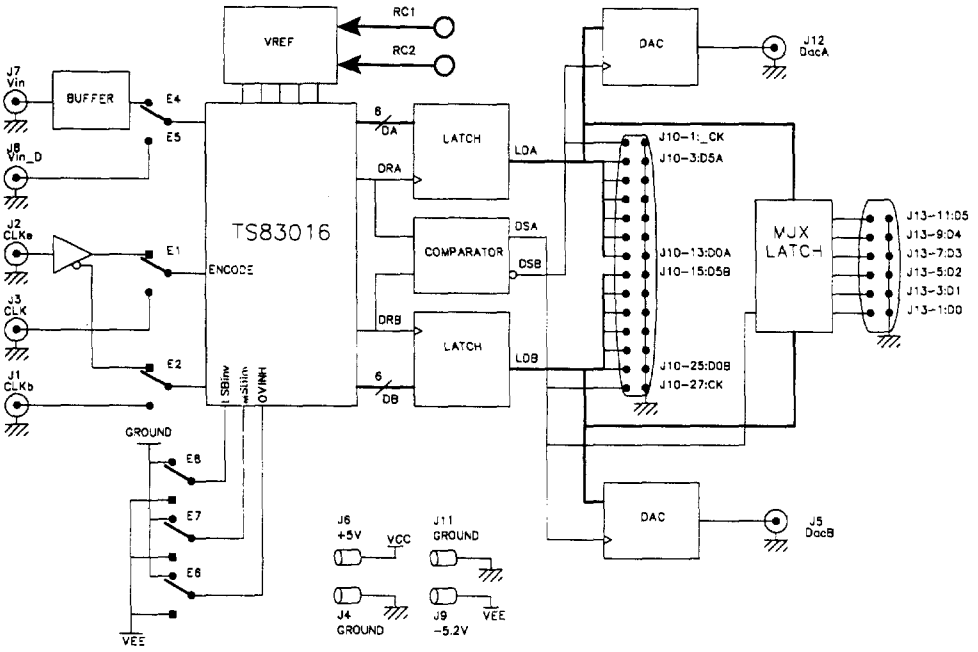


Figure 4

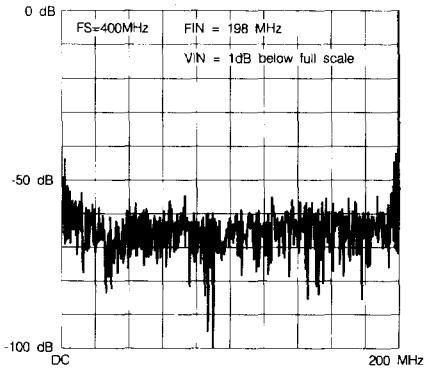


Figure 11 : FFT os TS 83016.

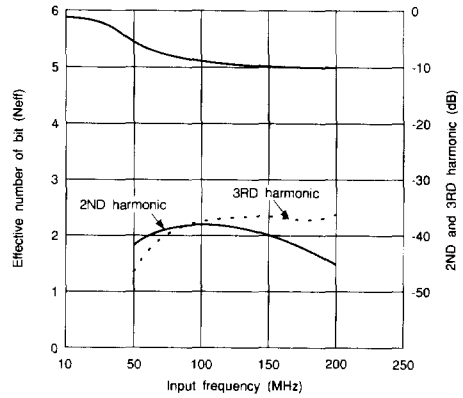


Figure 12 : Number of effective bits, 2nd and 3rd harmonics, versus input frequency.

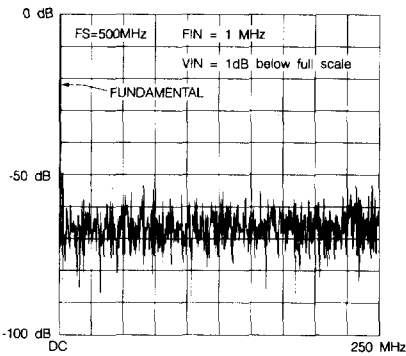


Figure 13 : FFT os TS 83016.

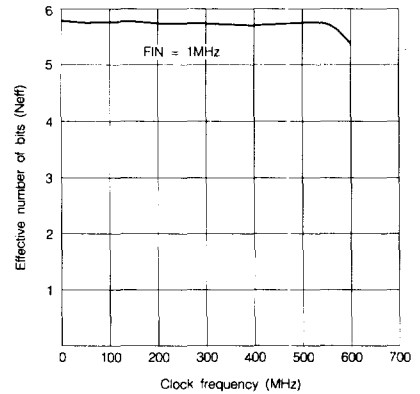


Figure 14 : Number of effective bits versus sampling rate.

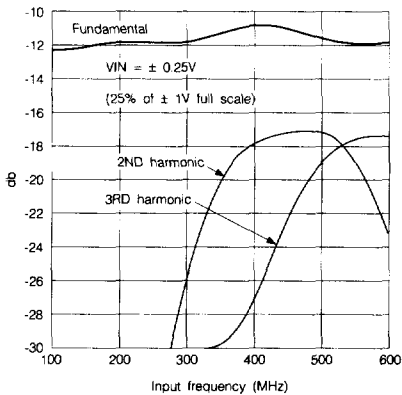


Figure 15 : Harmonics versus input frequency (small signal).

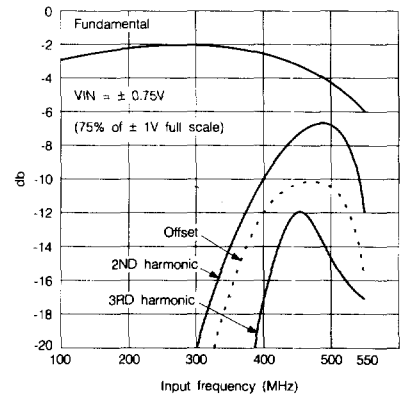
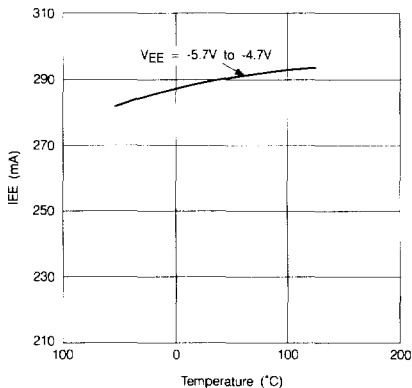
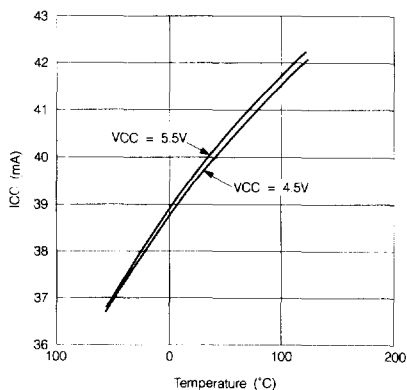


Figure 16 : Harmonics versus input frequency (large signal).

Figure 17 : I_{EE} versus temperature.Figure 18 : I_{CC} versus temperature.

DEFINITION OF TERMS

Analog bandwidth

The analog input frequency at which the fundamental component in the reconstructed output has fallen by 3 dB with respect to its low frequency value (determined by FFT analysis).

Signal to noise ratio (SNR)

The ratio of RMS signal amplitude to the RMS sum of all other spectral components, including significant harmonics except DC.

Total harmonic distortion (THD)

The ratio of the five most significant harmonic components in the spectrum of the quantized representation, to the fundamental spectral component.

Differential non-linearity (DNL)

The differential non-linearity for an output code i is the difference between the measured step size of code i and the ideal LSB step size. $DNL(i)$ is expressed in LSBs. DNL is the maximum value of all $|DNL(i)|$. DNL error specification of less than 1 LSB guarantees that there are no missing output codes, and that the transfer function is monotonic.

Integral non-linearity (INL)

The integral non-linearity for an output code i is the difference between the measured input voltage at which the transition occurs and the ideal value of this transition. $INL(i)$ is expressed in LSBs, and is the maximum value of all $|INL(i)|$.

Aperture delay (TA)

The delay between the rising edge of CLK signal and the time at which V_{IN} is sampled.

Aperture uncertainty (JITTER)

The sample to sample variation in aperture delay. The voltage error due to jitter depends on the slew rate of the signal at the sampling point.

Pipe line delay (TPD)

The delay of one clock cycle, between two successive rising edges of CLK signal (50 % points).

Output delay (TOD)

The delay between the rising edge of CLK (50 % point) and the -1.3 V point of a change in output data.

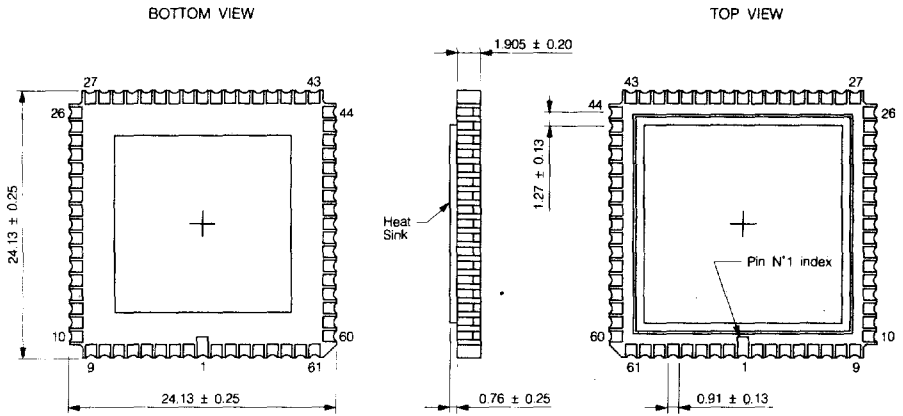
Data ready output delay (TDR)

The delay between the 50 % point of the falling edge of CLK and -1.3 V point of the leading edge of the data ready pulse.

OUTLINE DIMENSIONS

LEADLESS CERAMIC CHIP CARRIER (LCCC) - E SUFFIX

Dimensions in mm



DIE MECHANICAL INFORMATION : JTS 83016

Pad layout : V747

Pad size : 0.120×0.120 mm

Die size : 3.330×2.480 mm

Die thickness : $380 \mu\text{m}$

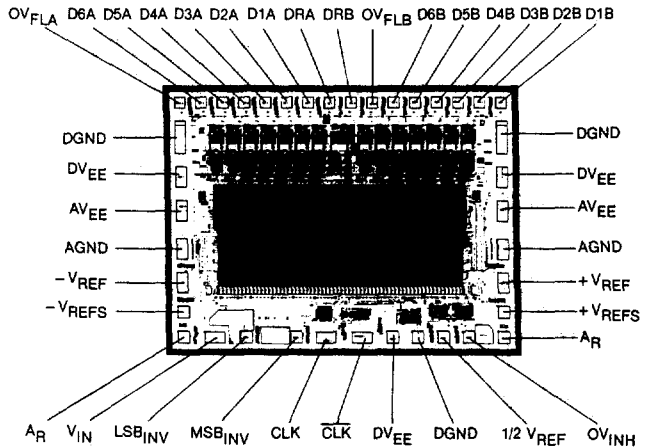
Metalization : Si (Back side)
Al-Si-Ti (Front side)

Passivation : Nitride

Revision : A

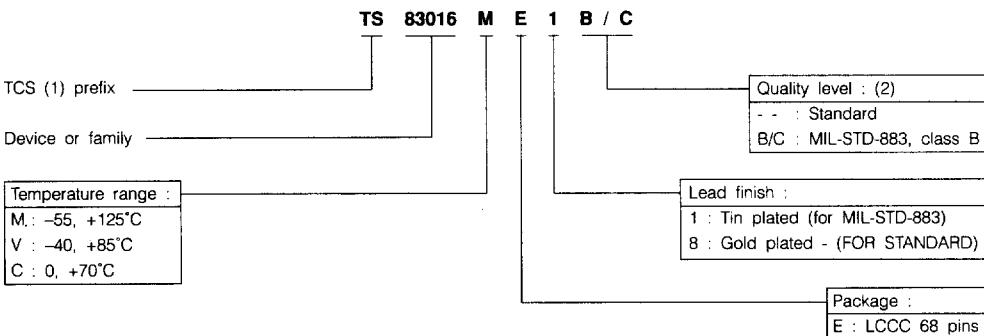
Qualification lot package : LCCC 68

Back side potential : AV_{EE}



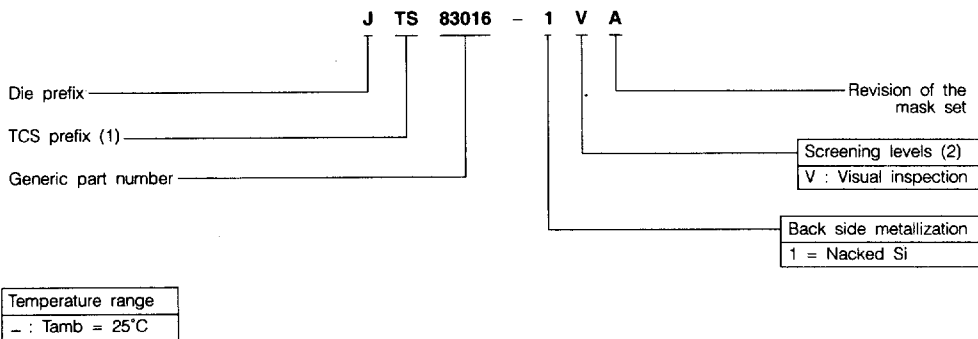
ORDERING INFORMATION

Packaged device



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Die form



Note 1 : THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES.

Note 2 : For availability of the different available versions contact your TCS sales office.