

Description

The MC-42512A36 and the MC-424512A36 are dynamic RAM modules organized as 524,288 words by 36 bits and designed to operate from a single +5-volt power supply. Advanced CMOS circuitry ensures minimum power dissipation and excellent operating margins.

The three-state output is controlled by $\overline{\text{CAS}}$ independent of $\overline{\text{RAS}}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{\text{CAS}}$ low. Data output is returned to high impedance by returning $\overline{\text{CAS}}$ high. Page read and write cycles can be executed by cycling $\overline{\text{CAS}}$. Refreshing is accomplished by means of $\overline{\text{RAS}}$ -only refresh cycles, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles, hidden refresh cycles, or by the 512 address combinations of A_0 through A_8 during an 8-ms period.

Single Inline Memory Module (SIMM™) packaging enhances reliability and reduces the size, weight, and cost of a system. Each SIMM contains 24 DRAMs and 24 power supply decoupling capacitors. The complement of DRAMs ($\mu\text{PD}424256$, 41256, 42256, 421000) and the operating mode (fast-page, page) are summarized below.

Module	DRAMs (Qty)		
	256K x 4	256K x 1	1M x 1
MC-42512A36	(16)	(8)	
B/F (fast-page)	424256	42256	
MC-424512A36	(16)	(8)	
B/F (page)	424256	41256	
MC-424512A36	(16)		(8)
BH/FH (fast-page)	424256		421000

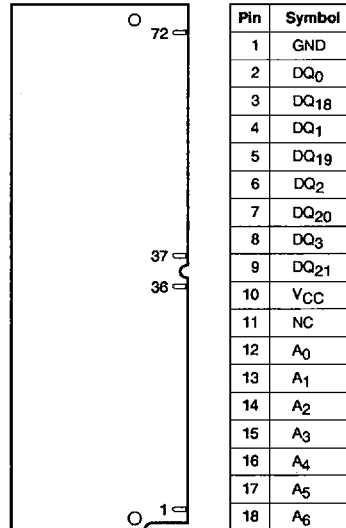
Features

- 524,288-word by 36-bit organization
- Single +5-volt power supply
- Low power dissipation (252 mW max in standby)
- $\overline{\text{RAS}}$ -only refresh cycles
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles
- Hidden refresh cycles
- 512 refresh cycles every 8 ms
- TTL-compatible inputs and outputs
- 72-pin SIMM packaging
- Fast-page mode operation (MC-42512A36B/F and MC-424512A36BH/FH)
- Page mode operation (MC-424512A36B/F)

SIMM is a trademark of Wang Laboratories.

Pin Configuration

72-Pin Socket-Mountable SIMM



Pin	Symbol
19	NC
20	DQ ₄
21	DQ ₂₂
22	DQ ₅
23	DQ ₂₃
24	DQ ₆
25	DQ ₂₄
26	DQ ₇
27	DQ ₂₅
28	A ₇
29	NC
30	V _{CC}
31	A ₈
32	NC
33	$\overline{\text{RAS}}_3$
34	$\overline{\text{RAS}}_2$
35	DQ ₂₆
36	DQ ₈

Pin	Symbol
37	DQ ₁₇
38	DQ ₃₅
39	GND
40	$\overline{\text{CAS}}_0$
41	$\overline{\text{CAS}}_2$
42	$\overline{\text{CAS}}_3$
43	$\overline{\text{CAS}}_1$
44	$\overline{\text{RAS}}_0$
45	$\overline{\text{RAS}}_1$
46	NC
47	WE
48	NC
49	DQ ₉
50	DQ ₂₇
51	DQ ₁₀
52	DQ ₂₈
53	DQ ₁₁
54	DQ ₂₉

Pin	Symbol
55	DQ ₁₂
56	DQ ₃₀
57	DQ ₁₃
58	DQ ₃₁
59	V _{CC}
60	DQ ₃₂
61	DQ ₁₄
62	DQ ₃₃
63	DQ ₁₅
64	DQ ₃₄
65	DQ ₁₆
66	NC
67	NC
68	GND
69	[Note 1]
70	[Note 1]
71	NC
72	GND

Notes:

[1] Pins 69 and 70 are defined by access time:

Pin	70 ns	80/85 ns	100 ns
69	GND	NC	GND
70	NC	GND	GND

Ordering Information

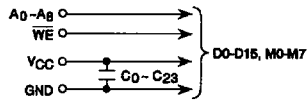
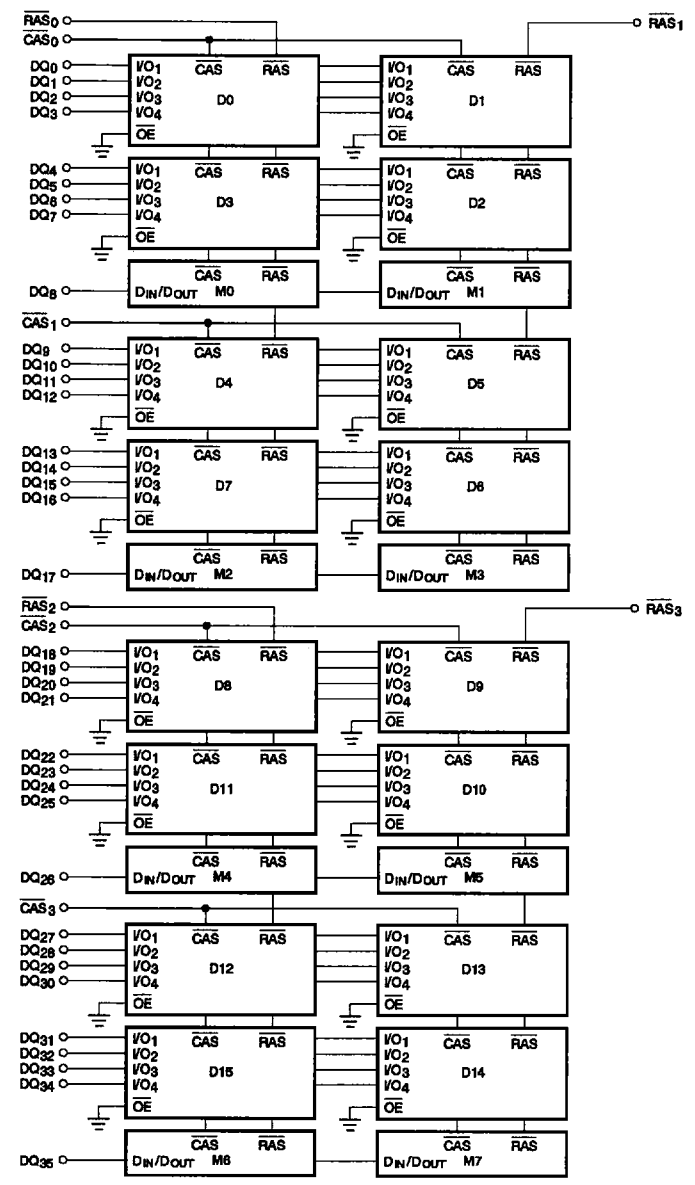
Part Number	Access Time (max)	Package	Operation	Height	Thickness	DRAMs
MC-424512A36BH-70	70 ns	72-pin socket-mountable SIMM (solder plating)	Fast-page	31.75 mm (1.25 inch)	9.3 mm (0.366 inch)	Sixteen μ PD424256LA Eight μ PD421000LA
BH-80	80 ns					
BH-10	100 ns					
MC-424512A36FH-70	70 ns	72-pin socket-mountable SIMM (gold plating)				
FH-80	80 ns					
FH-10	100 ns					
MC-42512A36B-70	70 ns	72-pin socket-mountable SIMM (solder plating)	Fast-page	25.4 mm (1.00 inch)	9.3 mm (0.366 inch)	Sixteen μ PD424256LA Eight μ PD42256L
B-80	80 ns					
B-10	100 ns					
MC-42512A36F-70	70 ns	72-pin socket-mountable SIMM (gold plating)				
F-80	80 ns					
F-10	100 ns					
MC-424512A36B-80	80 ns	72-pin socket-mountable SIMM (solder plating)	Page	25.4 mm (1.00 inch)	9.3 mm (0.366 inch)	Sixteen μ PD424256LA Eight μ PD41256L
B-85	85 ns					
B-10	100 ns					
MC-424512A36F-80	80 ns	72-pin socket-mountable SIMM (gold plating)				
F-85	85 ns					
F-10	100 ns					

Pin Identification

Name	Function
$A_0 - A_8$	Address inputs
$\overline{CAS}_0 - \overline{CAS}_3$	Column address strobes
$DQ_0 - DQ_{35}$	Common data inputs/outputs
$\overline{RAS}_0 - \overline{RAS}_3$	Row address strobes
\overline{WE}	Write enable
GND	Ground
V_{CC}	+ 5-volt power supply
NC	No connection

Connection Diagram; MC-42512A36, -424512A36

9g



D0-D15, M0-M7

Desig	DRAM
D0-D15	μPD424256LA
M0-M7	μPD421000LA
	μPD42256LA
	μPD41256L

Used On
All
MC-424512A36BH/FH
MC-42512A36B/F
MC-424512A36B/F

Absolute Maximum Ratings

Voltage on any pin relative to GND	-1.0 to +7.0 V
Operating temperature, T _{OPR}	0 to +70°C
Storage temperature, T _{STG}	-55 to +125°C
Short-circuit output current, I _{OS}	50 mA
Power dissipation, P _D	24 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V _{IH}	2.4		V _{CC} + 1.0	V
Input voltage, low	V _{IL}	-1.0		0.8	V
Supply voltage	V _{CC}	4.75	5.0	5.25	V
Ambient temperature	T _A	0		70	°C

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C _{I1}	161	pF	A ₀ - A ₉
	C _{I2}	193	pF	WE
	C _{I3}	62	pF	RAS
	C _{I4}	62	pF	CAS
Input/output capacitance	C _{I0} /C _{O0}	29	pF	DQ ₀ - DQ ₇ , DQ ₉ - DQ ₁₆ , DQ ₁₈ - DQ ₂₅ , DQ ₂₇ - DQ ₃₄
	C _{I2} /C _{O2}	39	pF	DQ ₈ , DQ ₁₇ , DQ ₂₆ , DQ ₃₅

DC Characteristics 1 (MC-42512A36B/F, -424512A36BH/FH)

T_A = 0 to +70°C; V_{CC} = +5.0 V ±5%

Parameter	Symbol	Min	Max	Unit	Test Conditions
Standby current	I _{CC2}		48	mA	RAS = CAS ≥ V _{IH} (min)
			24	mA	RAS = CAS ≥ V _{CC} - 0.2 V
Input leakage current	I _{I(L)}	-240	240	μA	V _{IN} = 0 V to V _{CC} ; all other pins not under test = 0 V
Output leakage current	I _{O(L)}	-10	10	μA	DQ ₀ to DQ ₃₅ disabled; V _{OUT} = 0 V to V _{CC}
Output voltage, low	V _{OL}		0.4	V	I _{OL} = 4.2 mA
Output voltage, high	V _{OH}	2.4		V	I _{OH} = -5 mA

AC Characteristics 1 (MC-42512A36B/F, -424512A36BH/FH)

T_A = 0 to +70°C; V_{CC} = +5.0 V ±5%

Parameter	Symbol	-70		-80		-10		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
Operating current, average	I _{CC1} (Note 17)		1040		910		780	mA	RAS and CAS cycling; t _{RC} = t _{RC} min; I _O = 0 mA (Note 5)
	I _{CC1} (Note 18)		980		860		740	mA	
Operating current, RAS-only refresh cycle, average	I _{CC3} (Note 17)		1040		910		780	mA	RAS cycling; CAS ≥ V _{IH} ; t _{RC} = t _{RC} min; I _O = 0 mA (Note 5)
	I _{CC3} (Note 18)		980		860		740	mA	
Operating current, fast-page cycle, average	I _{CC4} (Note 17)		910		780		650	mA	RAS ≤ V _{IL} ; CAS cycling; t _{PC} = t _{PC} min; I _O = 0 mA (Note 5)
	I _{CC4} (Note 18)		860		740		620	mA	
Operating current, CAS before RAS refresh cycle, average	I _{CC5} (Note 17)		1040		910		780	mA	RAS cycling; CAS before RAS; t _{RC} = t _{RC} min; I _O = 0 mA (Note 5)
	I _{CC5} (Note 18)		980		860		740	mA	
Access time from column address	t _{AA}		35		45		50	ns	(Notes 7, 9)

AC Characteristics 1 (MC-42512A36B/F, -424512A36BH/FH) (cont)

Parameter	Symbol	-70		-80		-10		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
Column address hold time referenced to $\overline{\text{RAS}}$	t_{AR}	60		60		70		ns	
Access time from $\overline{\text{CAS}}$ precharge (rising edge)	t_{ACP}		40		45		55	ns	(Notes 7, 9)
Column address setup time	t_{ASC}	0	20	0	20	0	25	ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Access time from $\overline{\text{CAS}}$ (falling edge)	t_{CAC}		20		20		25	ns	(Notes 7, 9)
Column address hold time	t_{CAH}	17		20		20		ns	
$\overline{\text{CAS}}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{\text{CAS}}$ hold time for $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle	t_{CHR}	15		15		20		ns	
$\overline{\text{CAS}}$ precharge time, fast-page cycle	t_{CP}	10	20	10	20	10	25	ns	
$\overline{\text{CAS}}$ precharge time	t_{CPN}	10		10		10		ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t_{CRP}	10		10		10		ns	(Note 12)
$\overline{\text{CAS}}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{\text{CAS}}$ setup time for $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle	t_{CSR}	10		10		10		ns	
Data-in hold time	t_{DH}	15		20		20		ns	(Note 15)
Data-in hold time referenced to $\overline{\text{RAS}}$	t_{DHR}	60		60		70		ns	
Data-in setup time	t_{DS}	0		0		0		ns	(Note 15)
Output buffer turnoff delay	t_{OFF}	0	15	0	20	0	25	ns	(Note 10)
Fast-page cycle time	t_{PC}	45		50		60		ns	(Note 6)
Access time from $\overline{\text{RAS}}$	t_{RAC}		70		80		100	ns	(Notes 7, 8)
$\overline{\text{RAS}}$ to column address delay time	t_{RAD}	15	35	17	35	17	45	ns	(Note 9)
Row address hold time	t_{RAH}	10		12		12		ns	
Column address lead time referenced to $\overline{\text{RAS}}$ (rising edge)	t_{RAL}	35		45		55		ns	
$\overline{\text{RAS}}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{\text{RAS}}$ pulse width, fast-page cycle	t_{RASp}	70	100,000	80	100,000	100	100,000	ns	
Random read or write cycle time	t_{RC}	130		160		190		ns	(Note 6)
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t_{RCD}	20	50	25	60	25	75	ns	(Note 11)
Read command hold time referenced to $\overline{\text{CAS}}$	t_{RCH}	0		0		0		ns	(Note 13)
Read command setup time	t_{RCS}	0		0		0		ns	
Refresh period	t_{REF}		8		8		8	ms	Addresses $A_0 - A_8$
$\overline{\text{RAS}}$ precharge time	t_{RP}	60		70		80		ns	
$\overline{\text{RAS}}$ precharge $\overline{\text{CAS}}$ hold time	t_{RPC}	10		10		10		ns	
Read command hold time referenced to $\overline{\text{RAS}}$	t_{RRH}	10		10		10		ns	(Note 13)
$\overline{\text{RAS}}$ hold time	t_{RSH}	20		20		25		ns	

AC Characteristics 1 (MC-42512A36B/F, -424512A36BH/FH) (cont)

Parameter	Symbol	-70		-80		-10		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
Rise and fall transition time	t_T	3	50	3	50	3	50	ns	(Note 3)
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold time referenced to \overline{RAS}	t_{WCR}	55		55		70		ns	
Write command setup time	t_{WCS}	0		0		0		ns	(Note 16)
\overline{WE} hold time	t_{WHR}	15		15		20		ns	
Write command pulse width	t_{WP}	15		15		20		ns	(Note 14)

Notes:

- (1) All voltages are referenced to GND.
- (2) An initial pause of 100 μ s is required after power-up, followed by any eight RAS cycles, before proper device operation is achieved. At the end of the initial power-up sequence, it is recommended that either a RAS-only refresh or a CAS before RAS refresh cycle be executed while $\overline{WE} \geq V_{IH}$ to ensure normal operation.
- (3) Ac measurements assume $t_T = 5$ ns.
- (4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL} .
- (5) I_{CC1} , I_{CC3} , I_{CC4} , and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during RAS-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.
- (6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range ($T_A = 0$ to $+70^\circ\text{C}$) is assured.
- (7) Load = 2 TTL (-1 mA, $+4$ mA) loads and 100 pF ($V_{OH} = 2.0$ V, $V_{OL} = 0.8$ V).
- (8) Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$ and $t_{RAD} \leq t_{RAD}(\text{max})$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.
- (9) If $t_{RAD} \geq t_{RAD}(\text{max})$, then the access time is defined by t_{AA} .
- (10) $t_{OFF}(\text{max})$ defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL} .
- (11) Operation within the $t_{RCD}(\text{max})$ limit assures that $t_{RAC}(\text{max})$ can be met. $t_{RCD}(\text{max})$ is specified as a reference point only; if t_{RCD} is greater than $t_{RCD}(\text{max})$, then access time is controlled exclusively by t_{CAC} .
- (12) The t_{CRP} requirement should be applicable for $\overline{RAS}/\overline{CAS}$ cycles preceded by any cycle.
- (13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
- (14) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.
- (15) These parameters are referenced to the falling edge of \overline{CAS} for early write cycles and to the falling edge of \overline{WE} for delayed write or read-modify-write cycles.
- (16) t_{WCS} , t_{RWD} , t_{CWD} , and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}(\text{min})$, the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle.
If $t_{CWD} \geq t_{CWD}(\text{min})$, $t_{RWD} \geq t_{RWD}(\text{min})$, and $t_{AWD} \geq t_{AWD}(\text{min})$, the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output pin (at access time and until \overline{CAS} returns to V_{IH}) is indeterminate.
- (17) MC-424512A36BH/FH
- (18) MC-42512A36B/F

DC Characteristics 2 (MC-424512A36B/F)

$T_A = 0$ to $+70^\circ\text{C}$; $V_{CC} = +5.0$ V $\pm 5\%$

Parameter	Symbol	Min	Max	Unit	Test Conditions
Standby current	I_{CC2}		72	mA	$\overline{RAS} = \overline{CAS} \geq V_{IH}(\text{min})$
			16	mA	$\overline{RAS} = \overline{CAS} \geq V_{CC} - 0.2$ V
Input leakage current	$I_{I(L)}$	-240	240	μ A	$V_{IN} = 0$ V to V_{CC} ; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	-10	10	μ A	DQ ₀ to DQ ₃₅ disabled; $V_{OUT} = 0$ V to V_{CC}
Output voltage, low	V_{OL}		0.4	V	$I_{OL} = 4.2$ mA
Output voltage, high	V_{OH}	2.4		V	$I_{OH} = -5$ mA

AC Characteristics 2 (MC-424512A36B/F)

$T_A = 0$ to $+70^\circ\text{C}$; $V_{CC} = +5.0\text{ V} \pm 5\%$

Parameter	Symbol	-80		-85		-10		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
Operating current, average	I_{CC1}		1024		872		744	mA	$\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ cycling; $t_{RC} = t_{RC} \text{ min}$; $I_O = 0 \text{ mA}$ (Note 5)
Operating current, $\overline{\text{RAS}}$ -only refresh cycle, average	I_{CC3}		1024		872		744	mA	$\overline{\text{RAS}}$ cycling; $\overline{\text{CAS}} \geq V_{IH}$; $t_{RC} = t_{RC} \text{ min}$; $I_O = 0 \text{ mA}$ (Note 5)
Operating current, fast-page cycle, average	I_{CC4}		996		828		724	mA	$\overline{\text{RAS}} \leq V_{IL}$; $\overline{\text{CAS}}$ cycling; $t_{PC} = t_{PC} \text{ min}$; $I_O = 0 \text{ mA}$ (Note 5)
Operating current, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle, average	I_{CC5}		1024		872		744	mA	$\overline{\text{RAS}}$ cycling; $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$; $t_{RC} = t_{RC} \text{ min}$; $I_O = 0 \text{ mA}$ (Note 5)
Column address hold time referenced to $\overline{\text{RAS}}$	t_{AR}	55		55		65		ns	
Column address setup time	t_{ASC}	0	20	0	20	0	25	ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Access time from $\overline{\text{CAS}}$ (falling edge)	t_{CAC}		40		40		50	ns	(Notes 7, 9)
Column address hold time	t_{CAH}	20		20		20		ns	
$\overline{\text{CAS}}$ pulse width	t_{CAS}	40	10,000	40	10,000	50	10,000	ns	
$\overline{\text{CAS}}$ hold time for $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle	t_{CHR}	15		15		20		ns	
$\overline{\text{CAS}}$ precharge time (page mode)	t_{CP}	20		20		40		ns	
$\overline{\text{CAS}}$ precharge time, nonpage cycle	t_{CPN}	25		25		25		ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t_{CRP}	10		10		10		ns	(Note 12)
$\overline{\text{CAS}}$ hold time	t_{CSH}	80		85		100		ns	
$\overline{\text{CAS}}$ setup time for $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle	t_{CSR}	10		10		10		ns	
Data-in hold time	t_{DH}	20		20		25		ns	(Note 15)
Data-in hold time referenced to $\overline{\text{RAS}}$	t_{DHR}	60		65		75		ns	
Data-in setup time	t_{DS}	0		0		0		ns	(Note 15)
Output buffer turnoff delay	t_{OFF}	0	20	0	20	0	25	ns	(Note 10)
Fast-page cycle time	t_{PC}	70		70		100		ns	(Note 6)
Access time from $\overline{\text{RAS}}$	t_{RAC}		80		85		100	ns	(Notes 7, 8)
Row address hold time	t_{RAH}	12		12		12		ns	
$\overline{\text{RAS}}$ pulse width	t_{RAS}	80	10,000	85	10,000	100	10,000	ns	
Random read or write cycle time	t_{RC}	160		165		200		ns	(Note 6)
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t_{RCD}	20	40	20	45	20	50	ns	(Note 11)
Read command hold time referenced to $\overline{\text{CAS}}$	t_{RCH}	0		0		0		ns	(Note 13)
Read command setup time	t_{RCS}	0		0		0		ns	

AC Characteristics 2 (MC-424512A36B/F) (cont)

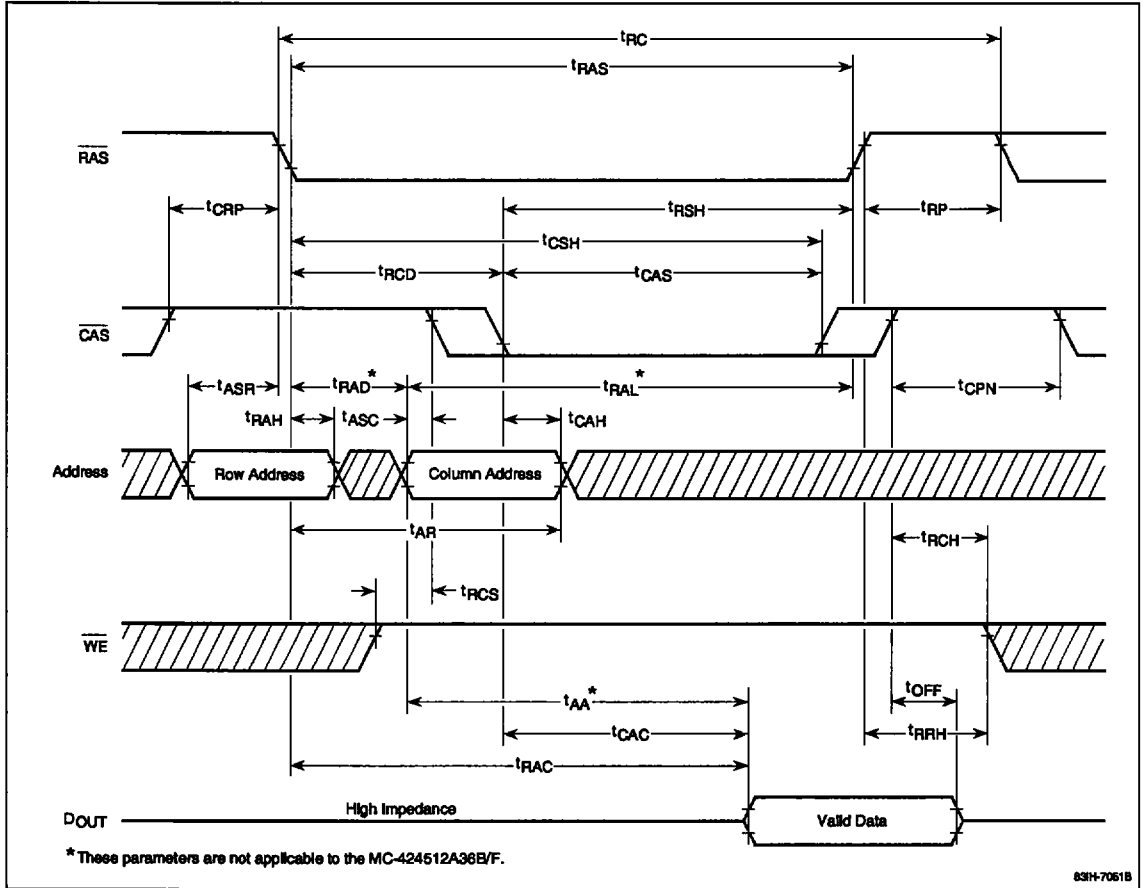
Parameter	Symbol	-80		-85		-10		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
Refresh period	t_{REF}		8		8		8	ms	Addresses $A_0 - A_8$
RAS precharge time	t_{RP}	70		70		90		ns	
RAS precharge CAS hold time	t_{RPC}	0		0		0		ns	
Read command hold time referenced to \overline{RAS}	t_{RRH}	10		10		10		ns	(Note 13)
\overline{RAS} hold time	t_{RSH}	40		40		50		ns	
Rise and fall transition time	t_T	3	50	3	50	3	50	ns	(Note 3)
Write command hold time	t_{WCH}	20		20		25		ns	
Write command hold time referenced to \overline{RAS}	t_{WCR}	60		65		75		ns	
Write command setup time	t_{WCS}	0		0		0		ns	(Note 16)
Write command pulse width	t_{WP}	15		15		15		ns	(Note 14)

Notes:

- (1) All voltages are referenced to GND.
- (2) An initial pause of 100 μ s is required after power-up, followed by any eight RAS cycles, before proper device operation is achieved. At the end of the initial power-up sequence, it is recommended that either a RAS-only refresh or a CAS before RAS refresh cycle be executed while $\overline{WE} \geq V_{IH}$ to ensure normal operation.
- (3) Ac measurements assume $t_T = 5$ ns.
- (4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL} .
- (5) I_{CC1} , I_{CC3} , I_{CC4} , and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during \overline{RAS} -only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.
- (6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range ($T_A = 0$ to $+70^\circ\text{C}$) is assured.
- (7) Load = 2 TTL (-1 mA, $+4$ mA) loads and 100 pF ($V_{OH} = 2.0$ V, $V_{OL} = 0.8$ V).
- (8) Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$ and $t_{RAD} \leq t_{RAD}(\text{max})$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.
- (9) If $t_{RAD} \geq t_{RAD}(\text{max})$, then the access time is defined by t_{AA} .
- (10) $t_{OFF}(\text{max})$ defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL} .
- (11) Operation within the $t_{RCD}(\text{max})$ limit assures that $t_{RAC}(\text{max})$ can be met. $t_{RCD}(\text{max})$ is specified as a reference point only; if t_{RCD} is greater than $t_{RCD}(\text{max})$, then access time is controlled exclusively by t_{CAC} .
- (12) The t_{CRP} requirement should be applicable for $\overline{RAS}/\overline{CAS}$ cycles preceded by any cycle.
- (13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
- (14) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.
- (15) These parameters are referenced to the falling edge of \overline{CAS} for early write cycles and to the falling edge of \overline{WE} for delayed write or read-modify-write cycles.
- (16) t_{WCS} , t_{RWD} , t_{CWD} , and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}(\text{min})$, the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle.
 If $t_{CWD} \geq t_{CWD}(\text{min})$, $t_{RWD} \geq t_{RWD}(\text{min})$, and $t_{AWD} \geq t_{AWD}(\text{min})$, the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output pin (at access time and until \overline{CAS} returns to V_{IH}) is indeterminate.

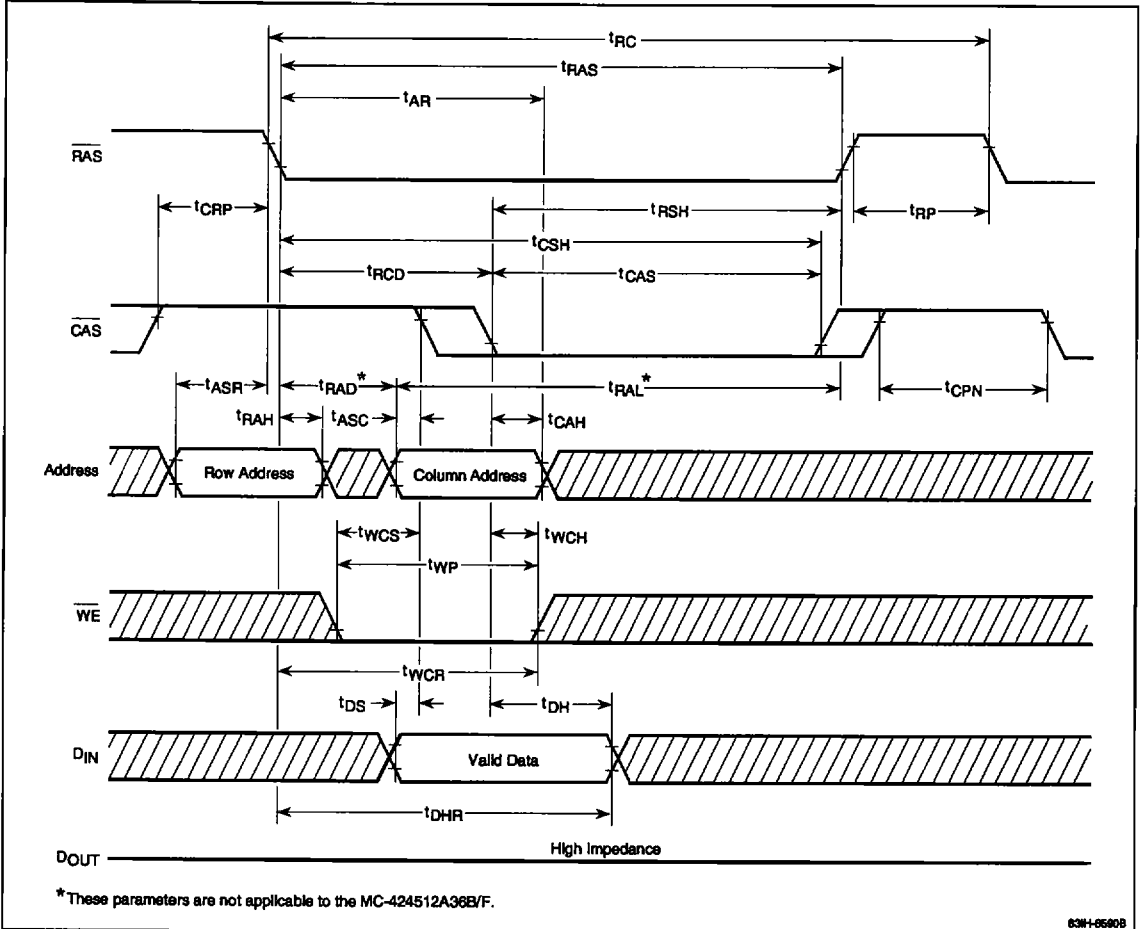
Timing Waveforms

Read Cycle



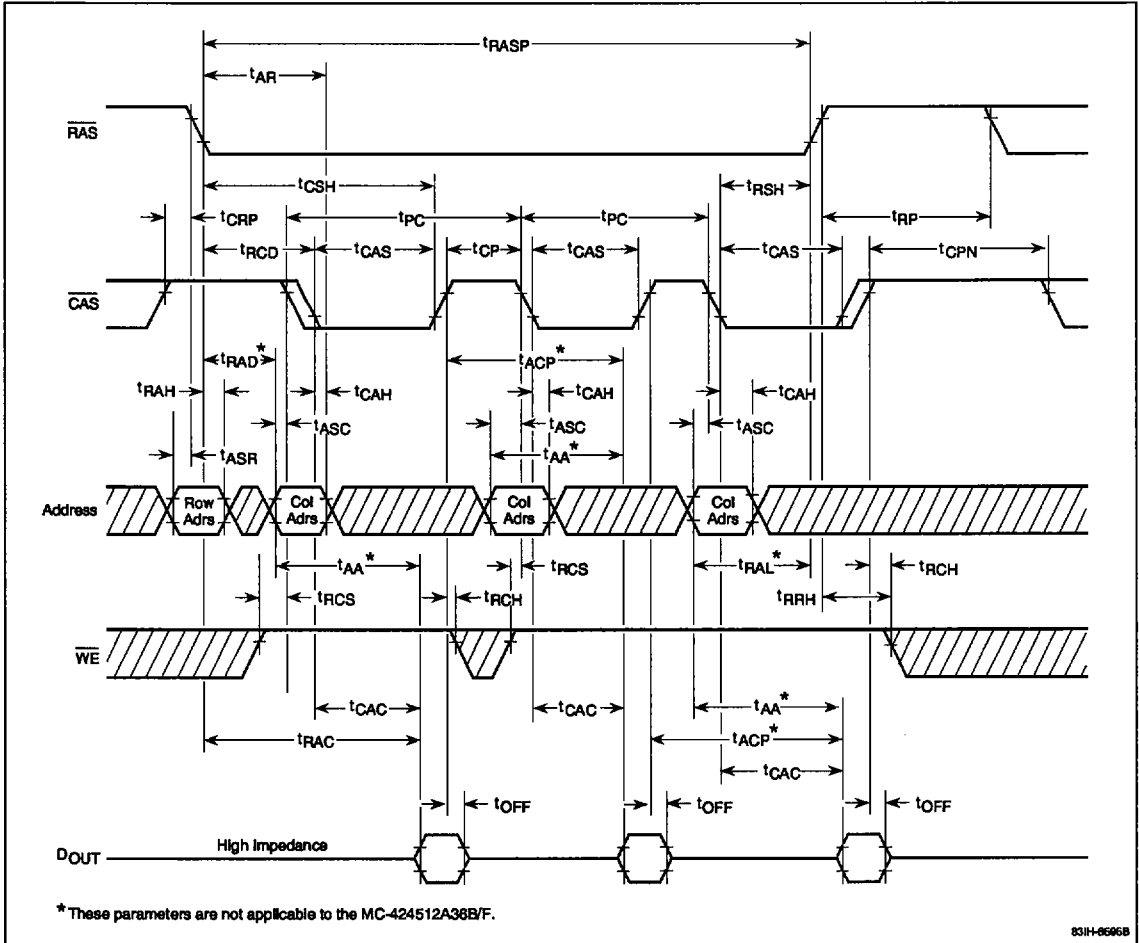
Timing Waveforms (cont)

Early Write Cycle



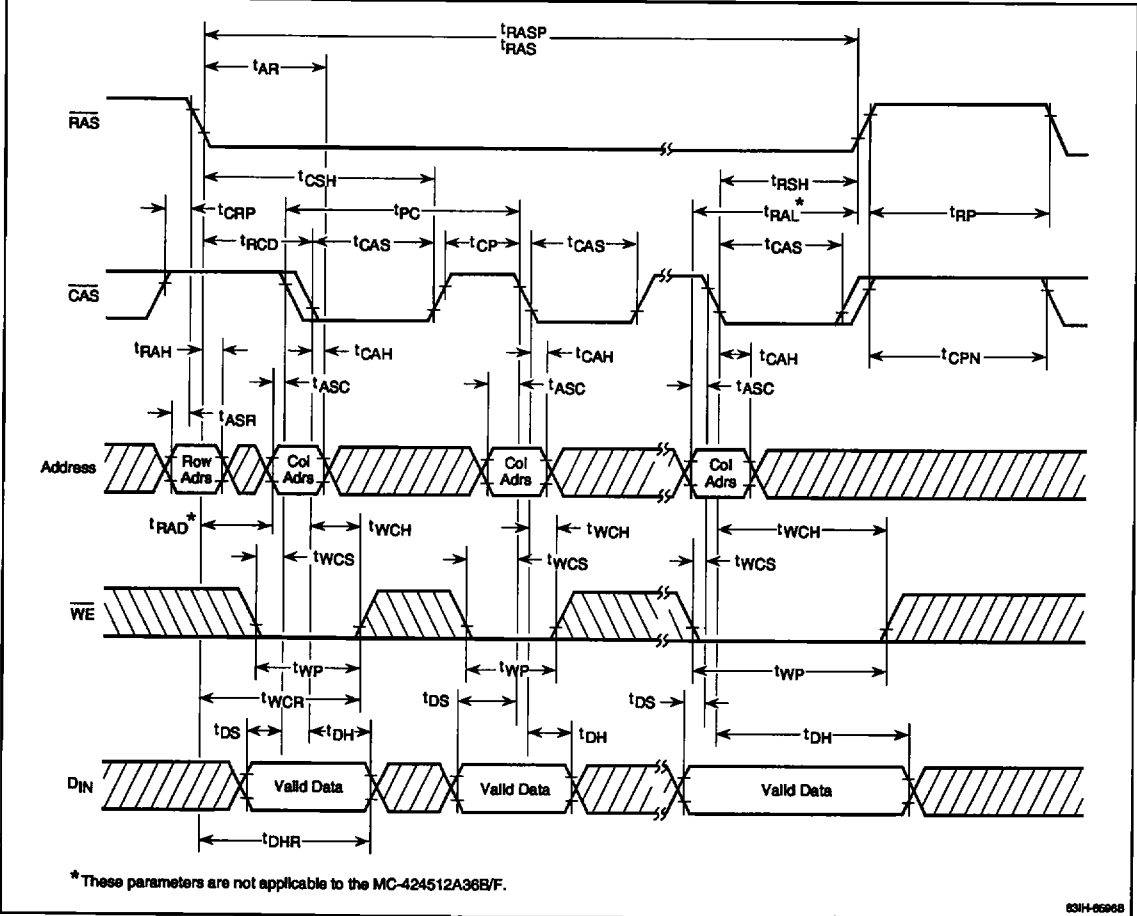
Timing Waveforms (cont)

Page/Fast-Page Read Cycle



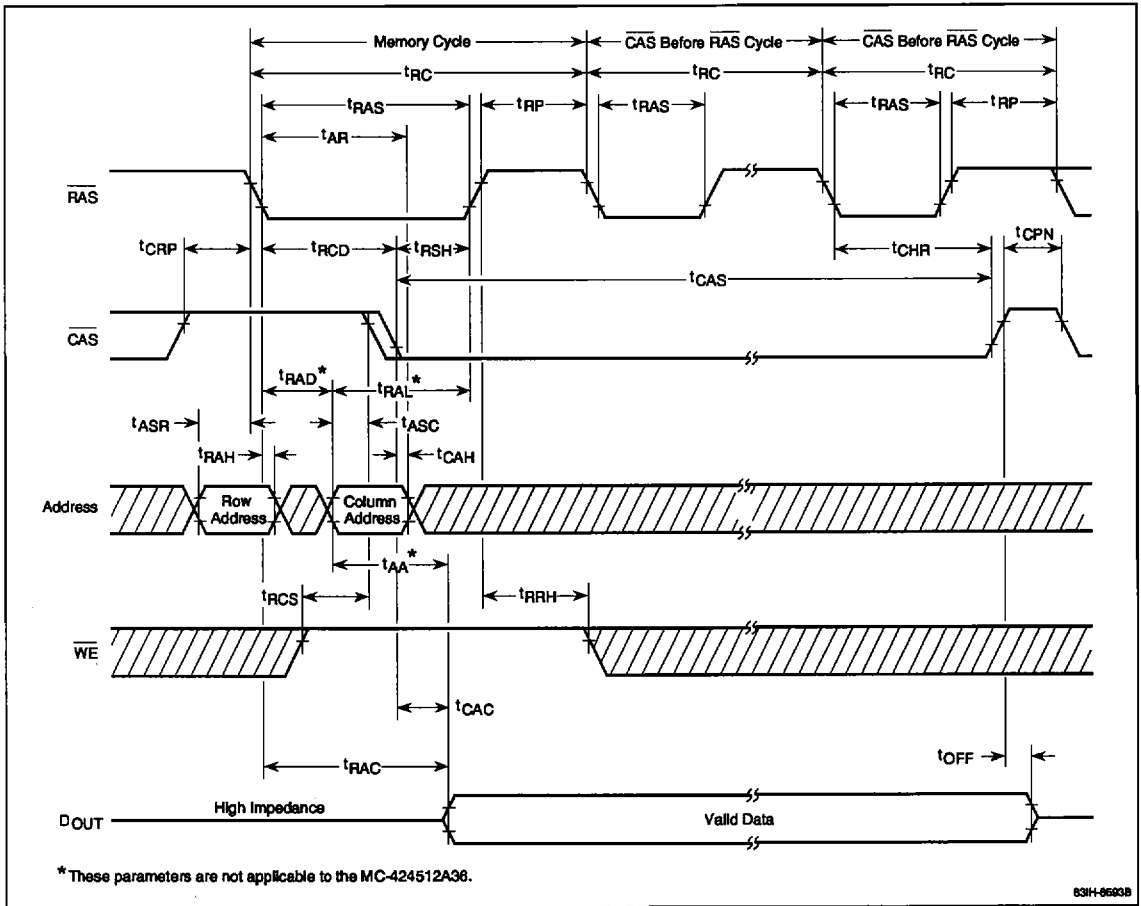
Timing Waveforms (cont)

Page/Fast-Page Early Write Cycle



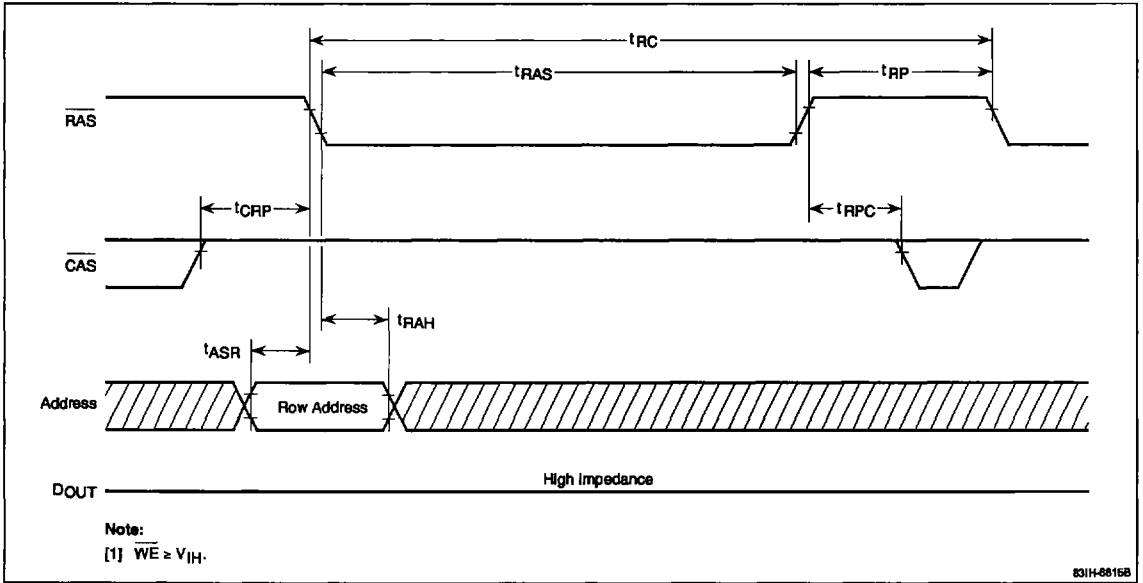
Timing Waveforms (cont)

Hidden Refresh Cycle

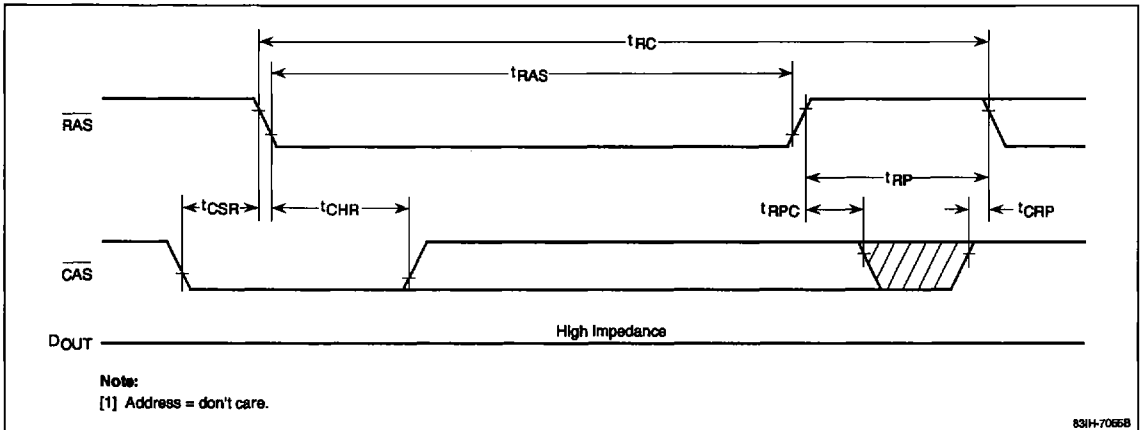


Timing Waveforms (cont)

RAS-Only Refresh Cycle



CAS Before RAS Refresh Cycle



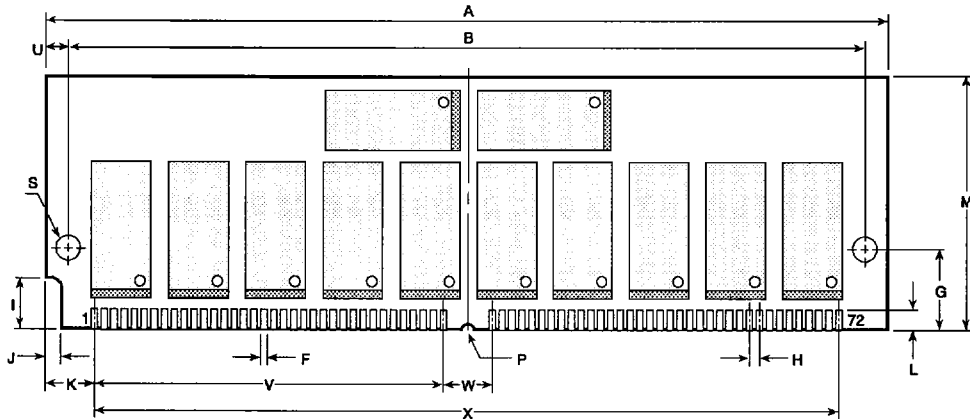
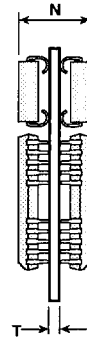
Package Drawings

72-Pin Socket-Mountable SIMM (MC-424512A36BH/FH)

9g

Item	Millimeters	Inches
A	107.95 ± 0.2	4.250 ± .008
B	101.19 ± 0.2	3.984 ± .008
F	0.75 min	.029 min
G	10.16	.400
H	1.27	.050
I	6.35	.250
J	2.03	.080
K	6.35	.250
L	2.7 min	.106 min

Item	Millimeters	Inches
M	31.75	1.250
N	9.3 max	.366 max
P	1.57 rad	.062 rad
S	3.17 dia	.125 dia
T	1.27	.050
U	3.38	.133
V	44.45	1.750
W	6.35	.250
X	95.25 ± 0.1	3.750 ± .004



MC-424512A36BH/FH

40NR-716B (3/91)

Package Drawings (cont)

72-Pin Socket-Mountable SIMM (MC-42512A36B/F and MC-424512A36B/F)

