SPT
SIGNAL PROCESSING TECHNOLOGIES

SPT1175

8-BIT, 20 AND 30 MSPS CMOS A/D CONVERTER

FEATURES

- 30 MSPS Maximum Conversion Rate
- Internal Sample-and-Hold Function
- 90 mW Power Dissipation at 20 MSPS
- Internal Voltage Reference
- Single +5.0 V Power Supply
- Three-State TTL-Outputs
- CMOS Compatible Clock

APPLICATIONS

- Video Digitizing
- Image Scanners
- Personal Computer Video
- Medical Ultrasound
- Multimedia
- Digital Television

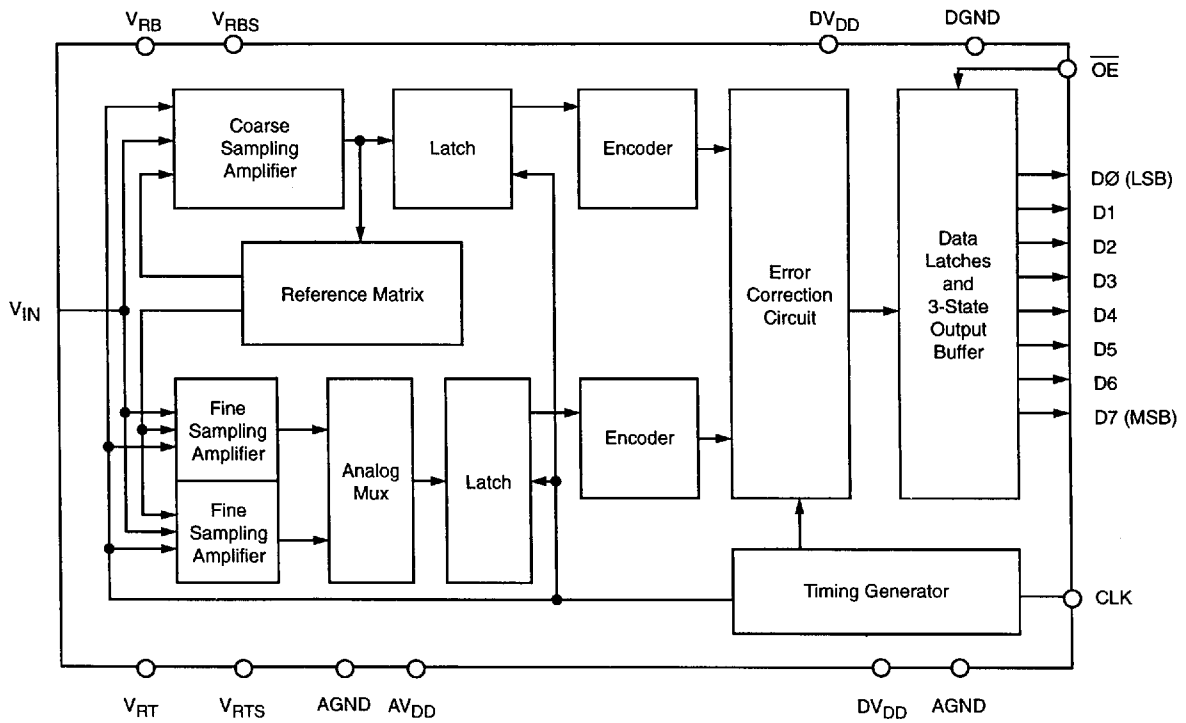
GENERAL DESCRIPTION

The SPT1175 is a CMOS two-step A/D converter capable of digitizing full scale analog input signals into 8-bit digital words at sample rates of 20 and 30 MSPS.

For most applications, no external sample-and-hold or video driving amplifiers are required due to the device's narrow aperture time, wide bandwidth, and low input capacitance.

The SPT1175 operates from a single +5.0 V power supply and has an internal voltage reference which eliminates the need for external reference circuitry. All digital inputs are CMOS compatible and the tri-state outputs are TTL-compatible. The SPT1175 is ideal for most video and image processing applications that require low power dissipation and low cost. The SPT1175 is available in 24-lead plastic SOIC, plastic DIP, ceramic DIP, PLCC and die form.

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages
V_{DD} ..... -0.5 to +7.0 V
Input Voltages
Analog Input ..... AGND to V_{DD}
Reference Input Voltage ..... AGND to V_{DD}
ESD Susceptibility(2) ..... ±1,500 V

Temperature
Operating Temperature ..... -20 to +70 °C
Junction Temperature ..... 175 °C
Lead Temperature, (soldering 10 seconds) ..... 300 °C
Storage Temperature ..... -55 to +125 °C

Notes: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.
2. 100 pF discharged through a 1.5 kΩ resistor (human body model).

ELECTRICAL SPECIFICATIONS

T_A= +25 °C, AV_{DD}=DV_{DD}=+5.0 V, AGND=DGND=0.0 V, V_{RB}=+0.6 V and V_{RT}=+2.6 V, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
Resolution			8			Bits
DC Accuracy (+25 °C)						
Integral Nonlinearity		I		±0.8	±1.2	LSB
Differential Nonlinearity		I		±0.6	±1.0	LSB
No Missing Codes		I		Guaranteed		
Analog Input						
Input Voltage Range		I	V_{RB}		V_{RT}	V
Input Bias Current		I			±5.0	µA
Input Resistance		VI	100	200		kΩ
Input Capacitance		V		15		pF
Input Bandwidth		V	12			MHz
Reference Input						
Reference Ladder Resistance		I	200	300	400	Ω
Reference Current		I	5.0	6.7	10.0	mA
Reference Input Voltage	V_{RB}	IV	0	0.6	-	V
	V_{RT}	IV	-	2.6	2.8	V
Internal Bias	V_{RB}	I	0.55	0.60	0.65	V
	V_{RT}-V_{RB}	I	1.9	2.0	2.1	V
	Short V_{RT} and V_{RTS}					
	Short V_{RB} and V_{RBS}					
Offset Voltage Error						
Top		I	-18	-25	-68	mV
Bottom		I	0	10	40	mV
Timing Characteristics						
Maximum Conversion Rate	1 MHz Input Sine Wave	I	30	40		MSPS
Output Data Delay (td)		IV		18	30	ns
Output Data Delay (Tdish, Tdisl)	(High 'Z')	IV			100	ns
Data Valid Time (Teneh, Tenel)	Tri-state circuit	IV			100	ns
Sampling Time Offset		IV		5	10	ns

NOTE: It is strongly recommended that all of the supply pins (AV_{DD}, DV_{DD}) be powered from the same source.

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PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
Dynamic Performance						
Signal-To-Noise Ratio	fs= 20 MSPS					
$f$in=1.0 MHz		I	44	46		dB
$f$in=3.58 MHz		I	43	45		dB
$f$in=10 MHz		I		44		dB
Spurious Free						
Dynamic Range	fs= 20 MSPS					
$f$in=1.0 MHz		I	44	47		dB
$f$in=3.58 MHz		I	41	44		dB
$f$in=10 MHz		I	30	33		dB
Signal-To-Noise Ratio	fs= 30 MSPS					
$f$in=1.0 MHz		I	42	44		dB
$f$in=3.58 MHz		I	41	43		dB
$f$in=10 MHz		I	40	42		dB
Spurious Free						
Dynamic Range	fs= 30 MSPS					
$f$in=1.0 MHz		I	42	45		dB
$f$in=3.58 MHz		I	35	38		dB
$f$in=10 MHz		I	30	33		dB
Differential Phase	NTSC 20 IRE Mod Ramp	I		0.7		Degrees
Differential Gain	fs= 14.3 MSPS	I		1.0		%
Digital Inputs						
Input Current, Logic High	V_{DD} = 5.25 V, V_{IH} = V_{DD}	I			1.0	µA
Input Current, Logic Low	V_{DD} = 5.25 V, V_{IL} = DGND	I			1.0	µA
Pulse Width High (CLK)		IV	15			ns
Pulse Width Low (CLK)		IV	15			ns
Voltage, Logic High		I	4.0			V
Voltage, Logic Low		I			1.0	V
Digital Outputs						
Output Current, High	V_{DD} = 4.75 V	I	-1.1			mA
Output Current, Low	V_{DD} = 4.75 V	I	3.5			mA
Output Current, High 'Z'	V_{DD} = 5.25 V, $\overline{OE}$= V_{DD}	I			16	µA
Voltage High		I	4.0			V
Voltage Low		I			0.4	V
Power Supply Requirements						
AV_{DD} (Analog Supply Voltage)		IV	+4.75	+5.0	+5.25	V
DV_{DD} (Digital Supply Voltage)		IV	+4.75	+5.0	+5.25	V
Supply Voltage Difference	(AV_{DD} -DV_{DD})	IV	-0.1	0.0	0.1	V
Supply Current	fs=20 MSPS	I		18	27	mA
Power Dissipation		I		90	135	mW

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, T_J = T_C = T_A.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

Table 1 - Output Coding

INDEX	ANALOG INPUT (V)	DIGITAL OUTPUT	
0	0.6078125	00000000	
1	0.6078125 ~ 0.6156260	00000001	V_{RB}=0.6 V
2	0.6156250 ~ 0.6234375	00000010	V_{RT}=2.6 V
....	....	....	
123	1.5921875 ~ 1.6000000	01111111	1 LSB=7.8125 mV
124	1.6000000 ~ 1.6078125	10000000	
125	1.6078125 ~ 1.6156250	10000001	
....	....	....	
254	2.5843750 ~2.5921875	11111110	
255	2.5921875 ~	11111111	

Figure 1A: Timing Diagram

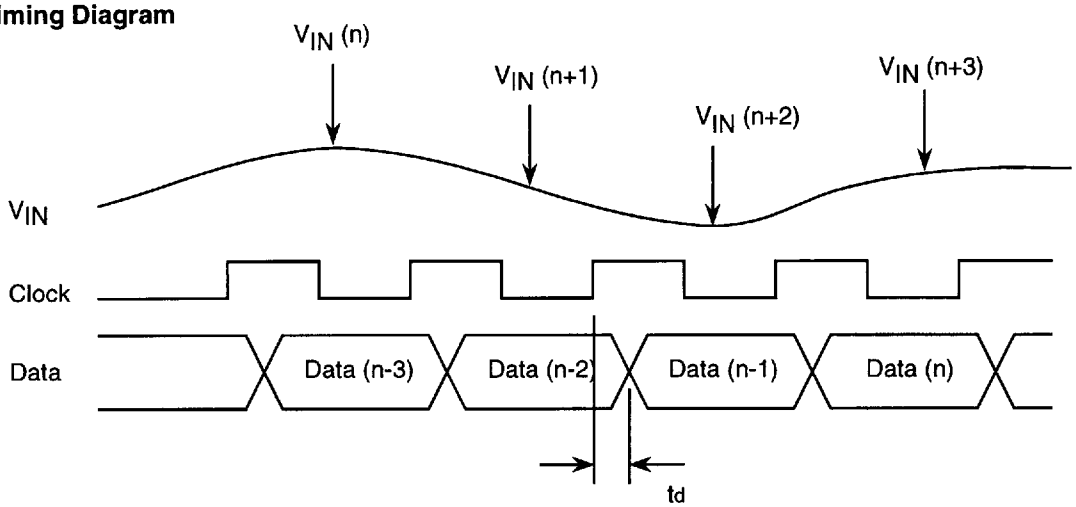
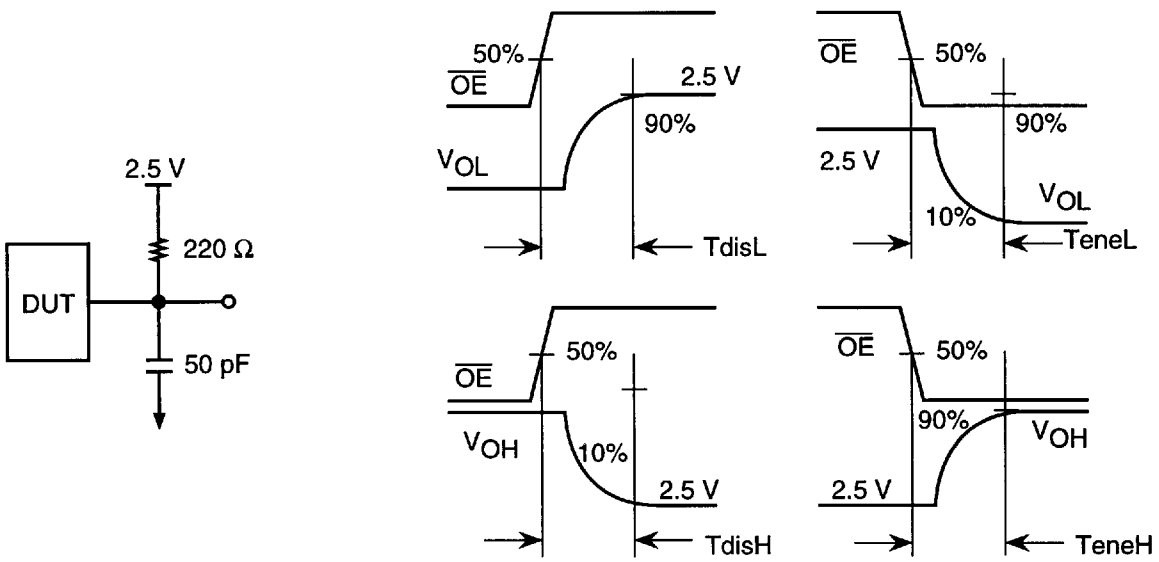


Figure 1B: Tri-State Output Timing Diagram



TYPICAL INTERFACE CIRCUIT

The SPT1175 is an 8-bit analog-to-digital converter which uses a two-step, ping-pong architecture to perform conversions up to 30 MSPS. Figure 2 shows the typical interface requirements when using the SPT1175 in normal operation. The following sections describe the function and operation of the device.

POWER SUPPLIES AND GROUNDING

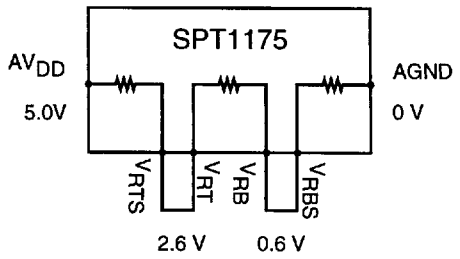
The SPT1175 operates from a single +5 V power supply. AV_{DD} and DV_{DD} must be supplied from the same source (analog +5 V) to prevent a latch-up condition due to power supply sequencing. Each power supply pin should be bypassed as closely as possible to the device. For optimal performance, both the AGND and DGND should be connected to the system's analog ground plane.

ANALOG INPUT AND VOLTAGE REFERENCE

The SPT1175 input voltage range is $V_{RT}>V_{IN}>V_{RB}$. Two reference voltages (V_{RT} and V_{RB}) are required for device operation. These voltages may be generated externally or the SPT1175's internal reference may be used.

Inside the SPT1175, reference resistors are placed between AV_{DD} and V_{RTS} and between AGND and V_{RBS} so that V_{RTS} and V_{RBS} generate the 2.6 V and 0.6 V references respectively. (See figure 3.) In order to utilize the internal self-bias reference voltage, V_{RTS} is to be shorted with V_{RT} and the V_{RBS} pin is to be shorted to the V_{RB} pin. The self-bias internal reference is not as stable over temperature and supply variations as externally generated reference voltages but will perform well in many commercial video applications.

Figure 3 - Reference Circuit Diagram



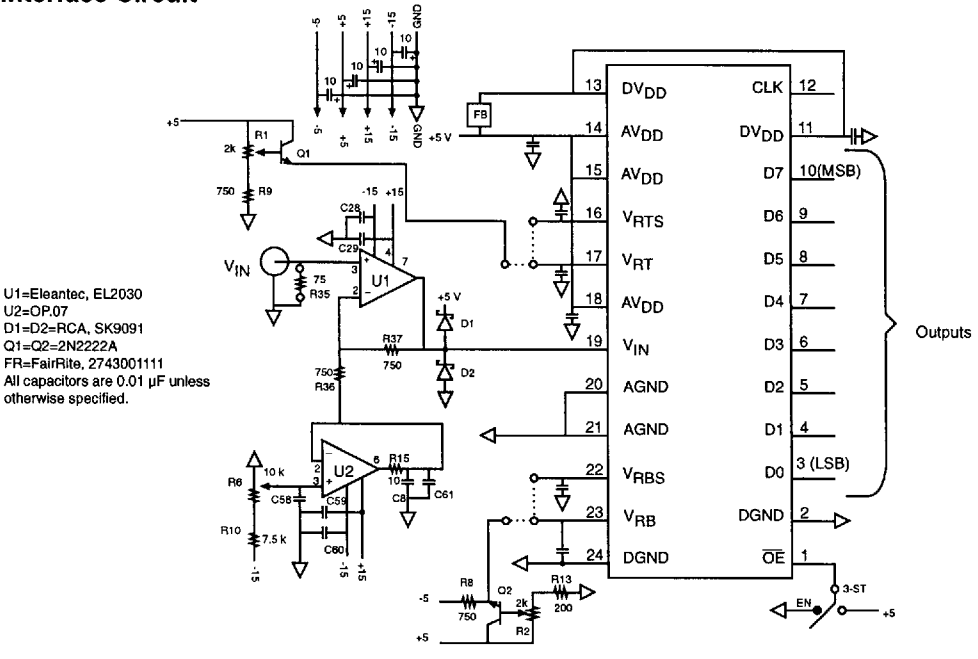
DIGITAL INPUTS AND OUTPUTS

The analog input is sampled and tracked on the first 'H' cycle of the external clock and is held from the falling edge of CLK. The output remains valid (output hold time), and the new data becomes valid (output delay time) after the rising edge of CLK, delayed by 2.5 clock cycles. The clock input and output enable input must be driven at CMOS-compatible levels.

EVALUATION BOARD

The EB1175 evaluation board is available to aid designers in demonstrating the full performance of the SPT1175. This board includes a reference circuit, clock driver circuit, output data latches, and an on-board reconstruction DAC. An application note describing the operation of the board is available. Contact the factory for price and delivery.

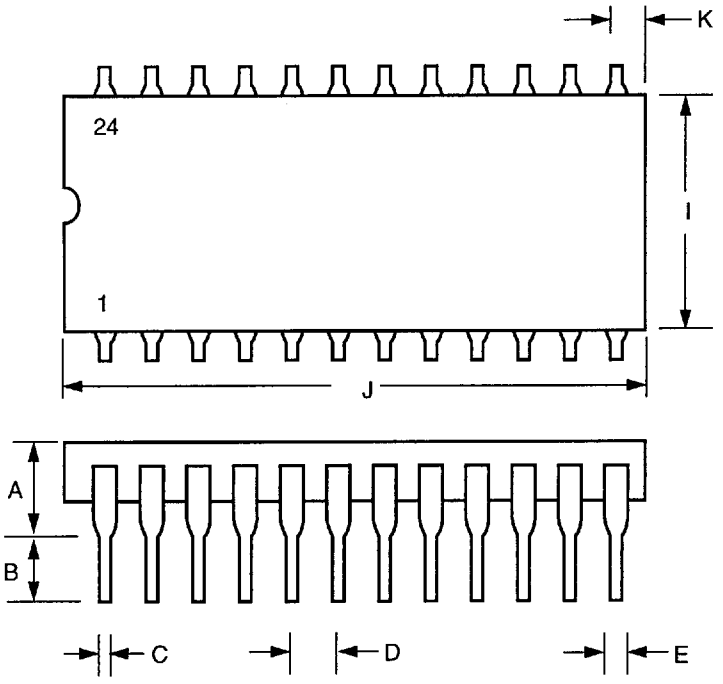
Figure 2 - Typical Interface Circuit



NOTE: AV_{DD} and DV_{DD} must be supplied from the same source (Analog +5 V) to prevent a latch-up condition due to power supply sequencing.

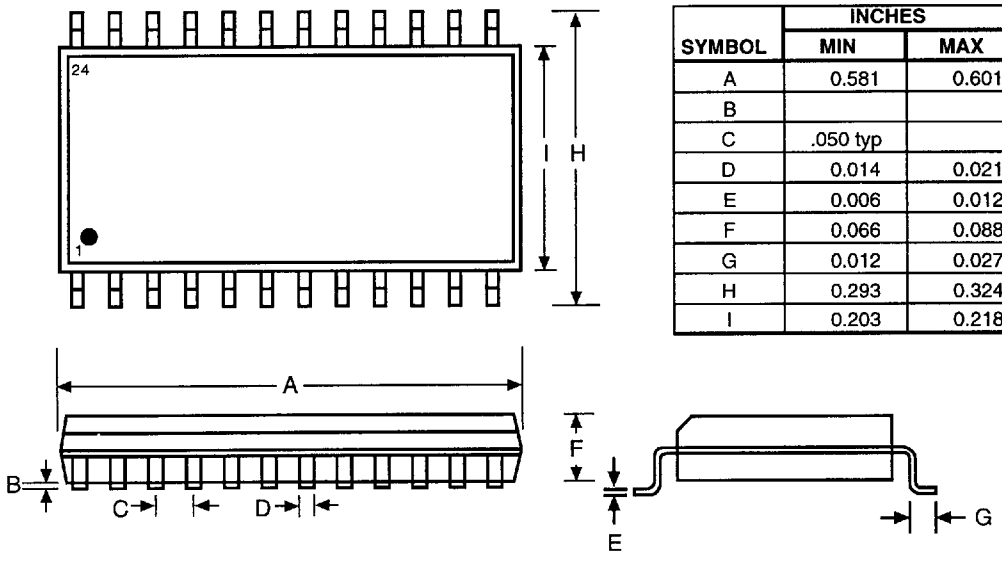
PACKAGE OUTLINES

24-Lead Plastic DIP



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.130	0.230	3.30	5.84
B	0.115	0.200	2.92	5.08
C	0.014	0.023	0.36	0.58
D	0.045	0.070	1.14	1.78
E	.100 typ		2.54	0.00
F	0.008	0.015	0.20	0.38
G	0.115	0.195	2.92	4.95
H	.30 typ		7.62	0.00
I	0.240	0.310	6.10	7.87
J	1.180	1.285	29.97	32.64
K	.005 typ		0.13	

24-Lead SOIC

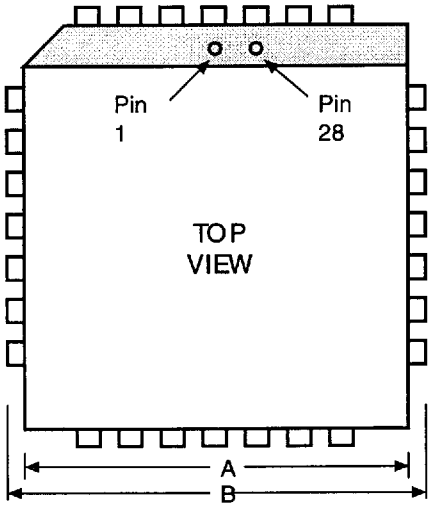


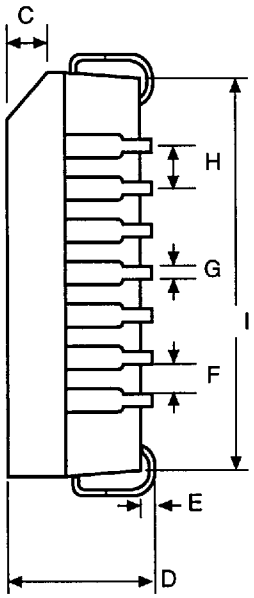
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.581	0.601	14.90	15.40
B				
C	.050 typ		1.27 typ	
D	0.014	0.021	0.35	0.55
E	0.006	0.012	0.15	0.30
F	0.066	0.088	1.70	2.25
G	0.012	0.027	0.30	0.70
H	0.293	0.324	7.50	8.30
I	0.203	0.218	5.20	5.60

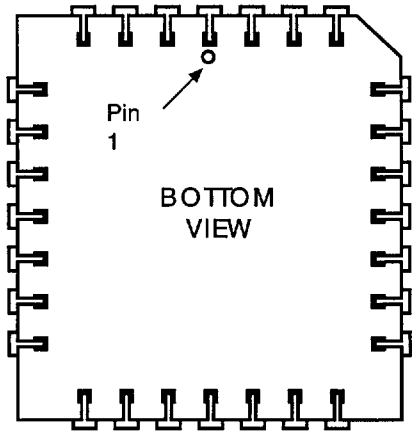
PACKAGE OUTLINES

28-Lead PLCC

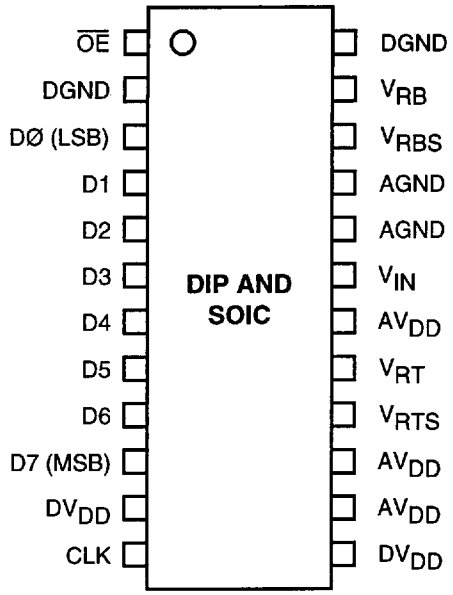
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.450	0.456	11.43	11.58
B	0.485	0.495	12.32	12.57
C	45°		45°	
D	0.165	0.175	4.19	4.45
E		0.010		0.25
F	0.022 typ		.56 typ	0.00
G	0.18 typ		4.57 typ	0.00
H	0.05 typ		1.27 typ	0.00
I	0.039	0.430	0.99	10.92

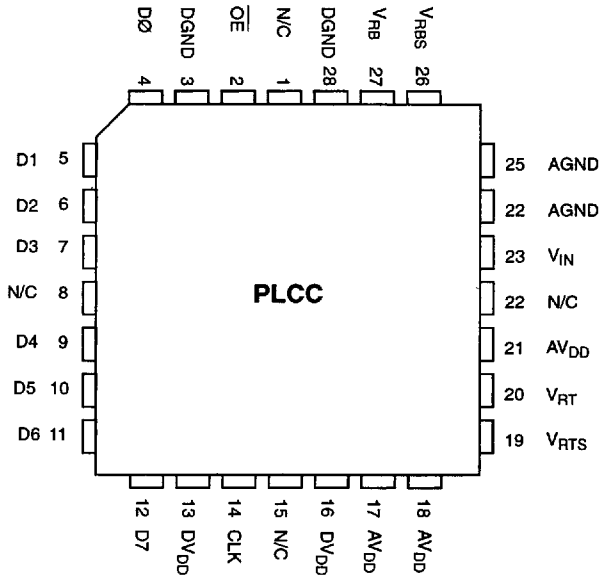






PIN ASSIGNMENTS





PIN FUNCTIONS

$\overline{OE}$	Tri-State Output Enable Tri-State When $\overline{OE}$ = DV_{DD}, Enable When $\overline{OE}$ = DGND
DGND	Digital Ground
D0	Digital Output Data (LSB)
D1-6	Digital Output Data
D7	Digital Output Data (MSB)
DV_{DD}	Digital Supply
CLK	CMOS Digital Clock Input

AV_{DD}	Analog Supply
V_{RTS}	Internal Self-Biased Reference Top Shorted with V_{RT} pin (17). Generates 2.6 V.
V_{RT}	Reference Resistor Top Side
V_{IN}	Analog Input
AGND	Analog Ground
V_{RBS}	Internal Self-Biased Reference Bottom Shorted with V_{RB} pin (23). Generates 0.6 V.
V_{RB}	Reference Resistor Bottom Side

ORDERING INFORMATION

PART NUMBER	SAMPLE RATE	PACKAGE TYPE
SPT1175ACD	20 MSPS	24L Ceramic Dip
SPT1175ACN	20 MSPS	24L Plastic Dip
SPT1175ACP	20 MSPS	28L PLCC
SPT1175ACS	20 MSPS	24L SOIC
SPT1175BCD	30 MSPS	24L Ceramic Dip
SPT1175BCN	30 MSPS	24L Plastic Dip
SPT1175BCP	30 MSPS	28L PLCC
SPT1175BCS	30 MSPS	24L SOIC
SPT1175ACU	20 MSPS	Die*

* Die are screened at +25 °C. Please consult factory for the die specifications.