Integrated Device Technology, Inc.

64K x 16
32K x 16
CMOS STATIC RAM MODULE

IDT8M624S
IDT8M612S

FEATURES:

- High-density CMOS static RAM module 64K x 16 organization (IDT8M624S) or 32K x 16 option (IDT8M612S)
- Fast access time:
  - — Commercial - 25ns (max.)
  - — Military - 35ns (max.)
- Separate upper byte (I/O_{9-16}) and lower byte (I/O_{1-8}) controls allow for greater application flexibility
- Offered in the JEDEC standard 40-pin DIP (dual in-line package)
- Leadless chip carriers (LCCs) mounted on an multi-layer ceramic substrate
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible

DESCRIPTION:

The IDT8M624S/IDT8M612S are high-speed CMOS static RAM modules constructed on an co-fired, multi-layer ceramic substrate using four 32K x 8 static RAMs (IDT8M624S) or two 32K x 8 static RAMs (IDT8M612S) in hermetic LCC packages. Functional equivalence to proposed monolithic static RAMs is achieved by utilization of an on-board decoder that interprets the higher order address A_{15} to select one of the two 32K x 16 RAMs as the x16 output and using $\overline{LB}$ and $\overline{UB}$ as two extra chip select functions for lower byte (I/O_{1-8}) and upper byte (I/O_{9-16}) control, respectively. Extremely high speeds can be achieved by the use of IDT71256 (32K x 8) static RAMs fabricated in IDT's high-performance, high-reliability technology, CEMOS™.

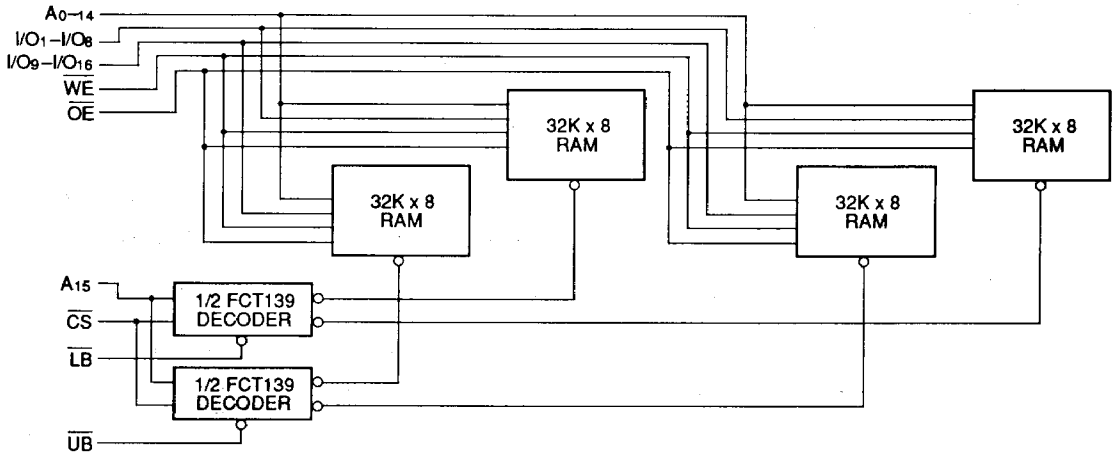
The IDT8M624S/IDT8M612S are available with access times as fast as 25ns over the commercial temperature range and 35ns over the military termperature range, with maximum operating power consumption of only 3.4W (64K x 16 commercial option). The module also offers a full standby mode of 451mW (max.).

The IDT8M624S/IDT8M612S modules are offered in the JEDEC standard 40-pin sidebrazed DIP.

All inputs and outputs of the IDT8M624S/ IDT8M612S are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

All military module semiconductor components are manufactured in compliance with the latest revision of MIL-STD-883 Class B, making them ideally suited for applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



2673 drw 01

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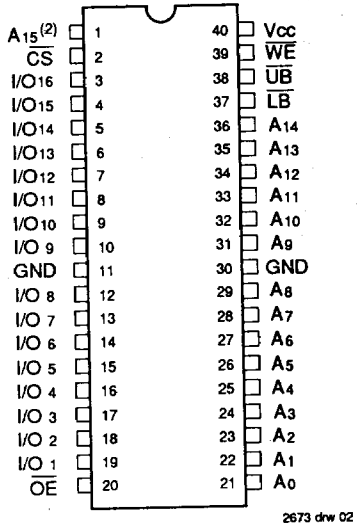
PIN CONFIGURATION[1]



2673 drw 02

DIP
TOP VIEW

NOTE:
1. For module dimensions, please refer to module drawing M11 (8M624S) and M12 (8M612S) in the packaging section.
2. For 32K x 16 option (IDT8M612S), A15 (Pin 1) must be connected to GND for proper operation of the module.

PIN NAMES

A0–15	Addresses
I/O1–16	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
Vcc	Power
GND	Ground
$\overline{OE}$	Output Enable
$\overline{UB}$	Upper Byte Control
$\overline{LB}$	Lower Byte Control

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TRUTH TABLE

Mode	$\overline{CS}$	$\overline{UB}$	$\overline{LB}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	X	X	High Z	Standby
Standby	L	H	H	X	X	High Z	Standby
Read	L	L	L	L	H	DOUT 1-16	Active
Lower Byte Read	L	H	L	L	H	DOUT 1-8	Active (X8)
Upper Byte Read	L	L	H	L	H	DOUT 9-16	Active (X8)
Read	L	L	L	H	H	High Z	Active
Lower Byte Read	L	H	L	H	H	High Z	Active (X8)
Upper Byte Read	L	L	H	H	H	High Z	Active (X8)
Write	L	L	L	X	L	DIN 1-16	Active
Lower Byte Write	L	H	L	X	L	DIN 1-8	Active (X8)
Upper Byte Write	L	L	H	X	L	DIN 9-16	Active (X8)

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ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTES: 2673 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	8MP624 Max.	8MP612 Max.	Unit
$C_{IN(D)}$	Input Capacitance (Data)	V_{IN} = 0V	25	14	pF
$C_{IN(A1)}$	Input Capacitance (A0–14, $\overline{OE}$, $\overline{WE}$)	V_{IN} = 0V	50	25	pF
$C_{IN(C)}$	Input Capacitance (A15, $\overline{CS}$)	V_{IN} = 0V	23	23	pF
$C_{IN(C)}$	Input Capacitance ($\overline{LB}$, $\overline{UB}$)	V_{IN} = 0V	13	13	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	25	14	pF

NOTE: 2673 tbl 07

1. This parameter is guaranteed by design, but not tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commerical	0°C to +70°C	0V	5.0V ± 10%
Military	-55°C to +125°C	0V	5.0V ± 10%

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RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

NOTE: 2673 tbl 08

1. V_{IL} (min) = –3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C or -55°C to +125°C)

Symbol	Parameter	Test Conditions	IDT8M624S			IDT8M612S			Unit
			Min.	Max.(1)	Max.(2)	Min.	Max.(1)	Max.(2)	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	20	15	—	10	15	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max.; $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	15	—	5	15	µA
I_{CCX16}	Dynamic Operating Current in X16 Mode	V_{CC} = Max., $\overline{CS}$, $\overline{UB}$ and $\overline{LB}$ = V_{IL}, f = f_{MAX}; Output Open	—	450	340	—	400	300	mA
I_{CCX8}	Dynamic Operating Current in X8 Mode	$\overline{CS}$, $\overline{UB}$ or $\overline{LB}$ = V_{IL}, V_{CC} = Max., f = f_{MAX}, Output Open	—	275	200	—	225	170	mA
I_{SB}	Standby Supply Current	$\overline{CS}$ ≥ V_{IH} or $\overline{UB}$ ≥ V_{IL} and $\overline{LB}$ ≥ V_{IH}	—	100	80	—	50	40	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS}$ ≥ V_{CC} – 0.2V; V_{IN} > V_{CC} – 0.2V or < 0.2V	—	60	80	—	30	40	mA
V_{OL}	Output Low Voltage	V_{CC} = Min. I_{OL} = 8mA	—	0.4	0.4	—	0.4	0.4	mA
V_{OH}	Output High Voltage	V_{CC} = Min. I_{OH} = –4mA	2.4	—	—	2.4	—	—	mA

NOTES: 2673 tbl 11

1. t_{AA} = 25, 30, 35ns.
2. t_{AA} = 40, 45, 50, 60, 70, 85, 100ns.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2673 tbl 09

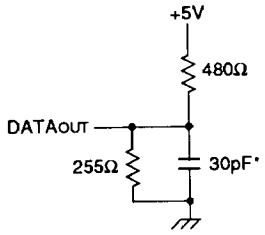

Figure 1. Output Load

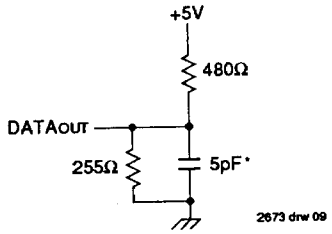

Figure 2. Output Load
(for tOLZ, tOHZ, tWHZ, and tOW)

*Including scope and jig.

AC ELECTRICAL CHARACTERISTICS

(VCC = 5V ±10%, TA = 0°C to +70°C or -55°C to +125°C)

Symbol	Parameter	8M612S25 8M624S25		8M612S30 8M624S30		8M612S35 8M624S35		8M612S40 8M624S40		8M612S45 8M624S45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle												
tRC	Read Cycle Time	25	—	30	—	35	—	40	—	45	—	ns
tAA	Address Access Time	—	25	—	30	—	35	—	40	—	45	ns
tACS	Chip Select Access Time	—	25	—	30	—	35	—	40	—	45	ns
tCLZ(1)	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
tOE	Output Enable to Output Valid	—	10	—	11	—	13	—	25	—	25	ns
tOLZ(1)	Chip Deselection to Output in High Z	2	—	2	—	2	—	5	—	5	—	ns
tCHZ(1)	Chip Select to Output in High Z	—	15	—	16	—	20	—	20	—	20	ns
tOHZ(1)	Output Disable to Output in High Z	—	8	—	10	—	15	—	20	—	20	ns
tOH	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	ns
tPU(1)	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	0	—	ns
tPD(1)	Chip Deselect to Power-Down Time	—	25	—	30	—	35	—	40	—	45	ns
Write Cycle												
tWC	Write Cycle Time	25	—	30	—	35	—	40	—	45	—	ns
tCW	Chip Select to End of Write	20	—	25	—	30	—	35	—	40	—	ns
tAW	Address Valid to End of Write	20	—	25	—	30	—	35	—	40	—	ns
tAS	Address Set-up Time	3	—	3	—	3	—	5	—	5	—	ns
tWP	Write Pulse Width	15	—	20	—	23	—	30	—	35	—	ns
tWR	Write Recovery Time	2	—	2	—	2	—	5	—	5	—	ns
tWHZ(1)	Write Enable to Output in High Z	—	10	—	11	—	15	—	15	—	15	ns
tDW	Data to Write Time Overlap	11	—	13	—	14	—	15	—	20	—	ns
tDH	Data Hold from Write Time	3	—	3	—	3	—	3	—	5	—	ns
tOW(1)	Output Active from End of Write	5	—	5	—	5	—	5	—	5	—	ns

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AC ELECTRICAL CHARACTERISTICS (Continued)

(V_{CC} = 5V ±10%, T_A = 0° to +70°C or −55°C to +125°C)

Symbol	Parameter	8M612S50 8M624S50		8M612S60 8M624S60		8M612S70 8M624S70		8M612S85 8M624S85		8M612S100 8M624S100		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle												
t_{RC}	Read Cycle Time	50	—	60	—	70	—	85	—	100	—	ns
t_{AA}	Address Access Time	—	50	—	60	—	70	—	85	—	100	ns
t_{ACS}	Chip Select Access Time	—	50	—	60	—	70	—	85	—	100	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	30	—	35	—	40	—	50	—	60	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{CHZ}[1]	Chip Select to Output in High Z	—	20	—	25	—	30	—	35	—	40	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	20	—	25	—	30	—	35	—	40	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	ns
t_{PU}[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power-Down Time	—	50	—	60	—	70	—	85	—	70	ns
Write Cycle												
t_{WC}	Write Cycle Time	50	—	60	—	70	—	85	—	100	—	ns
t_{CW}	Chip Select to End of Write	45	—	55	—	65	—	75	—	90	—	ns
t_{AW}	Address Valid to End of Write	45	—	55	—	65	—	75	—	90	—	ns
t_{AS}	Address Set-up Time	5	—	5	—	5	—	5	—	5	—	ns
t_{WP}	Write Pulse Width	40	—	50	—	60	—	70	—	80	—	ns
t_{WR}	Write Recovery Time	5	—	5	—	5	—	10	—	10	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	20	—	25	—	30	—	35	—	40	ns
t_{DW}	Data to Write Time Overlap	20	—	25	—	30	—	35	—	40	—	ns
t_{DH}	Data Hold from Write Time	5	—	5	—	5	—	5	—	5	—	ns
t_{OW}[1]	Output Active from End of Write	5	—	5	—	5	—	5	—	5	—	ns

NOTE:
1. This parameter is guaranteed by design, but not tested.

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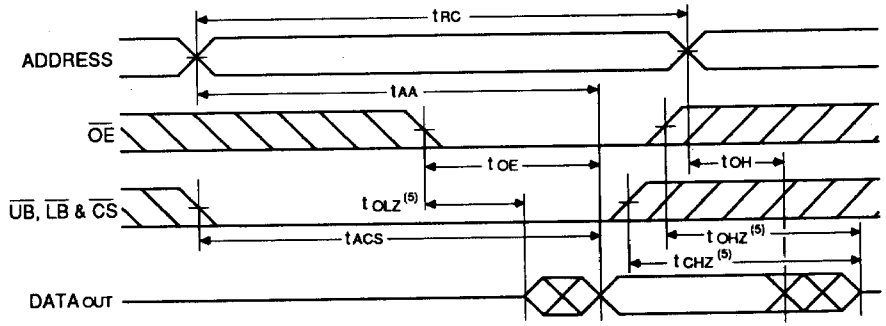
TIMING WAVEFORM OF READ CYCLE NO. 1(1)



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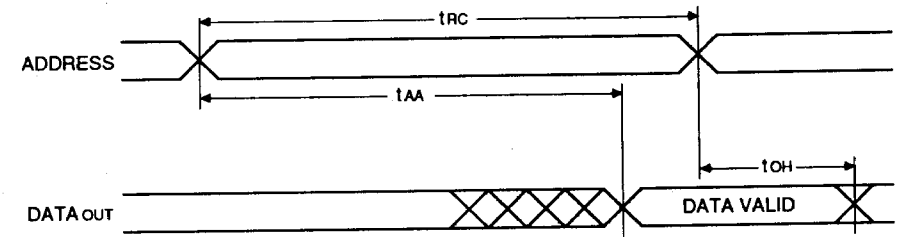
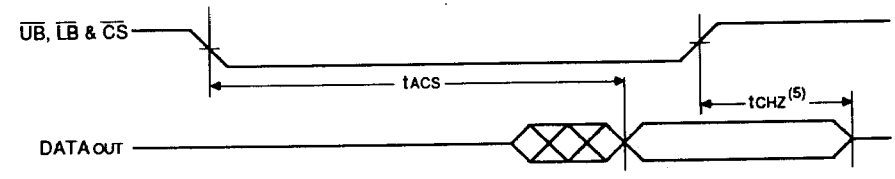
TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



2673 drw 04

TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



2673 drw 05

NOTES:
1. $\overline{WE}$ is high for Read cycle.
2. Device is continuously selected, $\overline{CS}$ = VIL and $\overline{UB}$, $\overline{LB}$ = VIL for 16 output active.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = VIL.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design, but not tested.

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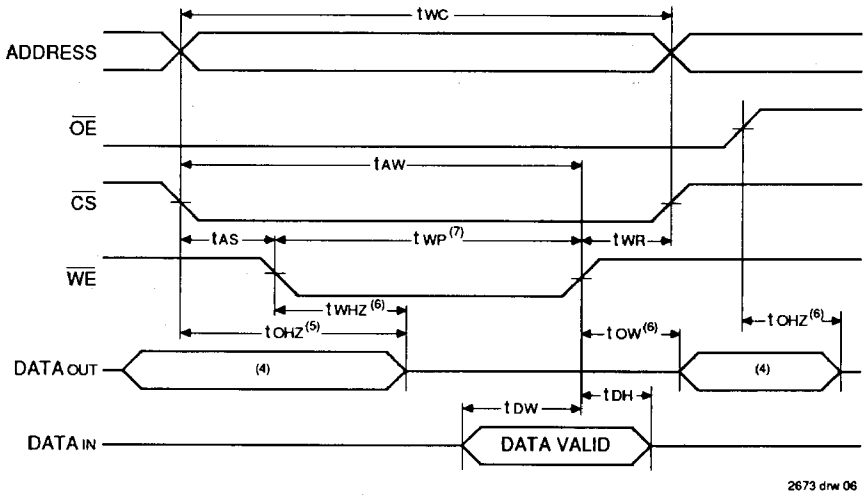
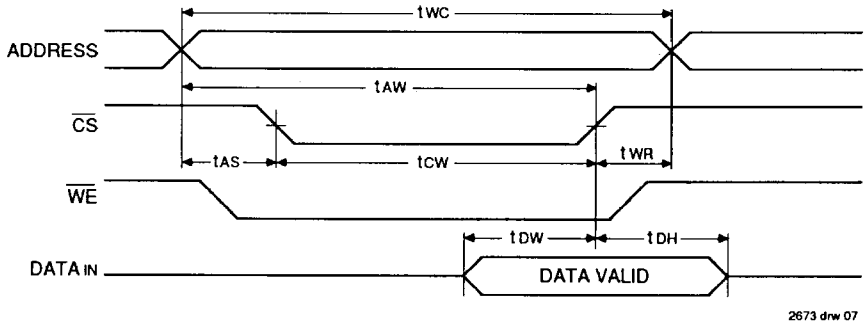
TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)

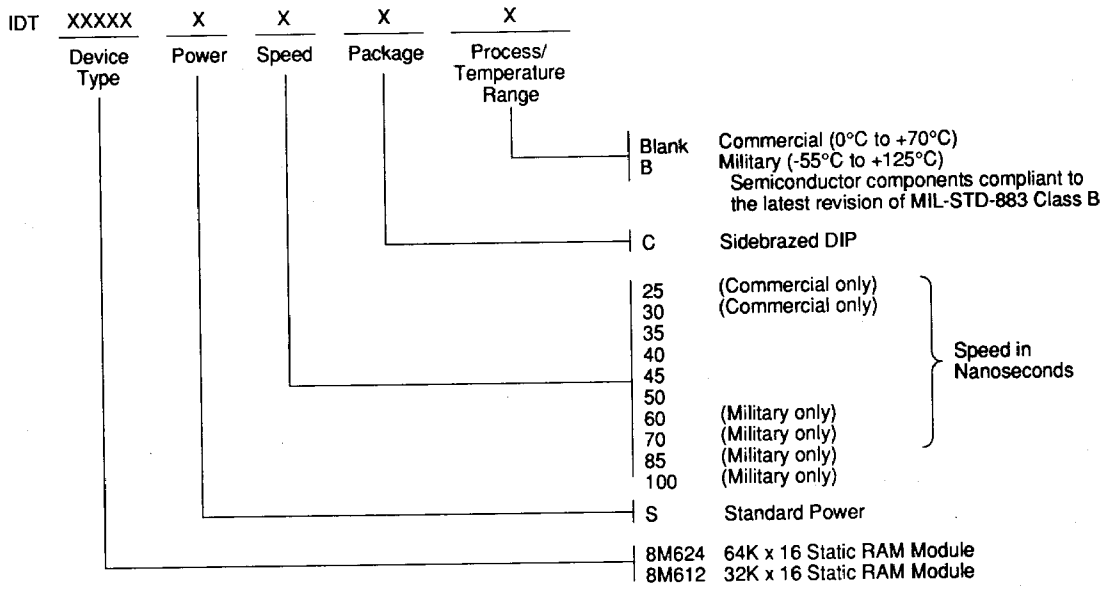


TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transactions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. During a $\overline{WE}$ controlled write cycle, write pulse ((tWP) > tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

ORDERING INFORMATION



2673 drw 10

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