HEWLETT PACKARD

PIN Diodes for RF Power Switching/Attenuating

Technical Data

5082-3101
5082-3102
5082-3201
5082-3202
5082-3303
5082-3304

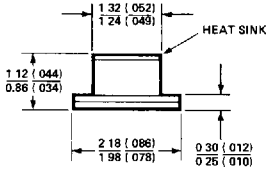
Features

- **High Isolation**
  Greater than 25 dB
- **Low Insertion Loss**
- **High Control Signal Dynamic Range**
  10,000: 1 RF Resistance Change
- **Low Harmonic Distortion**
- **Both Anode and Cathode Heat Sink Models Available**

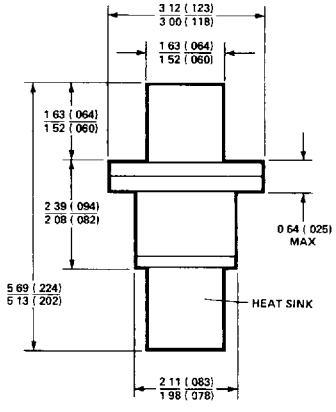
Description/ Applications

HP 5082-3101/02, 5082-3201/02, 5082-3303/04 PIN diodes are silicon devices manufactured using modern processing techniques to provide optimum characteristics for RF switching, signal conditioning and control. These devices are of planar passivated design. Both anode and cathode heat sink models are available.

PIN diodes provide a variable RF resistance with DC bias current. The main advantages of a PIN diode over PN switching diodes are the low forward resistance and the low device capacitance.



Outline 38



Outline 31

Maximum Ratings

Junction Operating and Storage
Temperature Range ..... -65°C to +150°C
DC Power Dissipation at 25°C
(Derate linearly to zero at 150°C)
HP 5082-3101, 3102 ..... 1.0 W
HP 5082-3201, 3202, 3303, 3304 ..... 3.0 W

These HP PIN diodes are intended for use in RF switching, multiplexing, modulating, phase shifting, and attenuating applications from approximately 10 MHz to frequencies well into the microwave region. Due to their low parasitic capacitance and inductance, both HP Package Outline 31 and 38 are well suited for broadband circuits up to 1 GHz and for resonated circuits up to 8 GHz.

These devices are especially useful where the lowest residual series resistance and junction capacitance are required for high on-to-off switching ratios.

Mechanical Specifications

The HP Package Outline 31 has a metal ceramic hermetic seal. The heat sink stud is gold-plated copper. The opposite stud is gold-plated kovar. Typical package inductance is 1.0 nH and typical package capacitance is 0.2 pF.

The HP Package Outline 38 also has a metal ceramic hermetic seal. The heat sink contact is gold plated copper. The opposite contact is gold-plated kovar. Typical package inductance is 0.4 nH and typical package capacitance is 0.2 pF.

The maximum soldering temperature for diodes in either package is 230°C for 5 seconds.

RF Power Switching/Attenuating

Electrical Specifications at T_A = 25°C

Part Number 5082-	Package Outline	Heat Sink	Minimum Breakdown Voltage V_{BR} (V)	Maximum Total Capacitance C_T (pF)	Maximum Residual Series Resistance R_S (Ω)	Minimum Carrier Lifetime τ (ns)	Typical Reverse Recovery Time t_{rr} (ns)	Typical CW Power Handling Capability P_A (W)
3101	38	Anode	200	0.32	1.2	100	100	40
3102	38		300	0.30	1.2	100	100	40
3201	31		200	0.35	1.2	100	100	120
3202	31		300	0.32	1.2	100	100	120
3303	31	Cathode	200	0.40	1.2	100	100	120
3304	31		250	0.32	1.2	100	100	120
Test Conditions			$V_R = V_{BR}$, meas. $I_R \leq 10$ μA	V_R = 50 V, f = 1 MHz	I_F = 100 mA f = 100 MHz	I_F = 50 mA I_R = 250 mA	I_F = 20 mA V_R = 10 V 90% Recovery	Series* Switch in 50 Ω System

*Divide by four for a shunt switch.

Typical Parameters

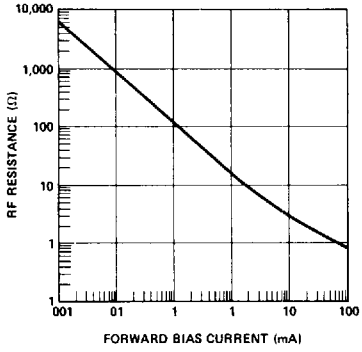


Figure 1. Typical RF Resistance vs. Forward Bias Current.

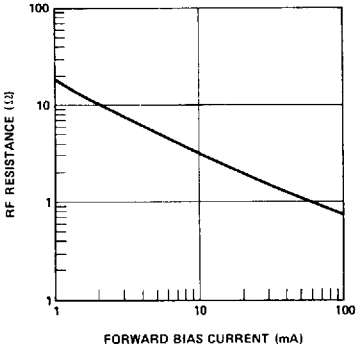


Figure 2. Typical RF Resistance vs. Forward Bias Current.

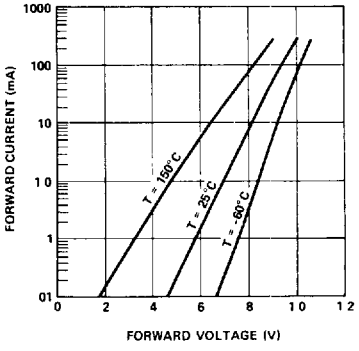


Figure 3. Typical Forward Characteristics.

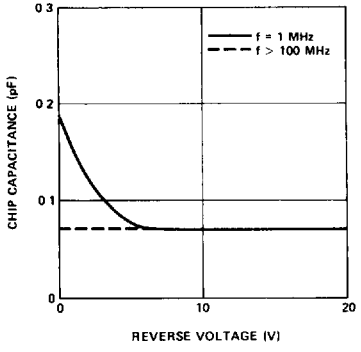
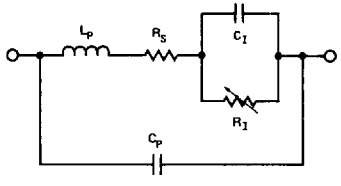


Figure 4. Typical Chip Capacitance vs. Reverse Voltage.



C_P = Package Capacitance
L_P = Package Inductance
R_S = Residual Series Resistance
R_I = I Layer Resistance
C_I = I Layer Capacitance

TYPICAL VALUES FOR C_P AND L_P ARE GIVEN UNDER "MECHANICAL SPECIFICATIONS" WITH REVERSE BIAS, $R_I \geq 10k\ \Omega$. TOTAL CAPACITANCE IS C_T AND IS GIVEN IN "ELECTRICAL SPECIFICATIONS." WITH FORWARD BIAS C_I IS NO LONGER PRESENT. R_I DECREASES WITH INCREASING FORWARD BIAS TO APPROXIMATELY ZERO AT 100 mA.

Figure 5. Device Equivalent Circuit.