

UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER

DESCRIPTION

The ST16C1450/51 is a universal asynchronous receiver and transmitter. A programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 448kHz.

The ST16C1450/51 is an improved version of the SSI 73M1550 and SSI 73M2550 UART with higher operating speed and lower access time. The ST16C1450/51 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C1450/51 provides internal loop-back capability for on board diagnostic testing.

The ST16C1450/51 is fabricated in an advanced 0.6µ CMOS process to achieve low drain power and high speed requirements.

FEATURES

- Pin to pin and functional compatible to SSI 73M1450/2450
- Modem control signals (CTS*, RTS*, DSR*, DTR*, RI*, CD*)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- Software compatible with INS8250, NS16C450
- 460.8 kHz transmit/receive operation with 7.372 MHz crystal or external clock source
- 28 Pin plastic-Dip and PLCC package
- Pin-to-pin compatible to ST16C1550/1551

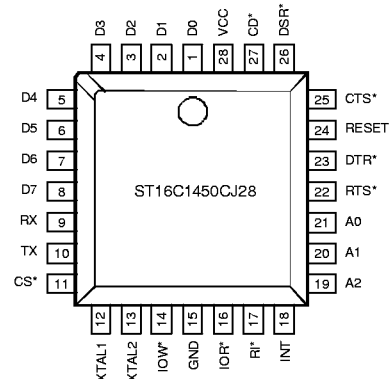
ORDERING INFORMATION

Part number	Package	Operating temperature
ST16C1450CP28	Plastic-DIP	0° C to + 70° C
ST16C1450CJ28	PLCC	0° C to + 70° C
ST16C1450CQ48	TQFP	0° C to + 70° C
ST16C1451CP28	Plastic-DIP	0° C to + 70° C
ST16C1451CJ28	PLCC	0° C to + 70° C
ST16C1451CQ48	TQFP	0° C to + 70° C

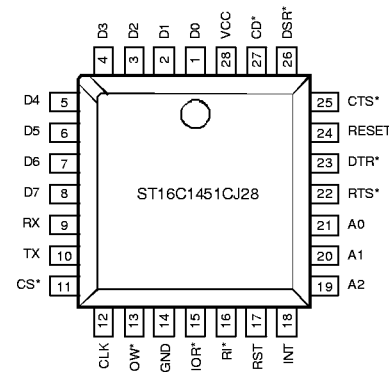
*Industrial operating range are available.

Rev. 2.2

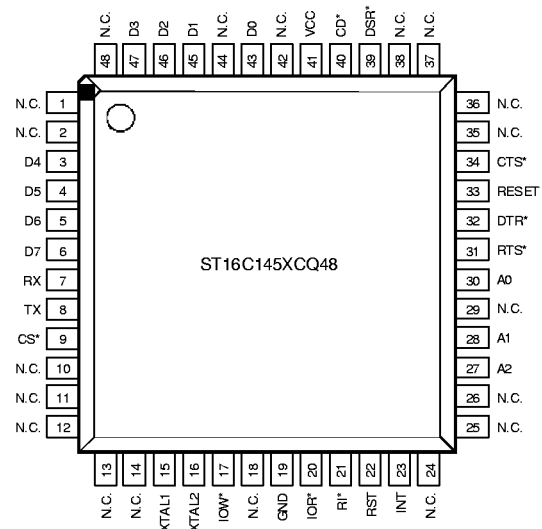
ST16C1450 PLCC Package



ST16C1451 PLCC Package

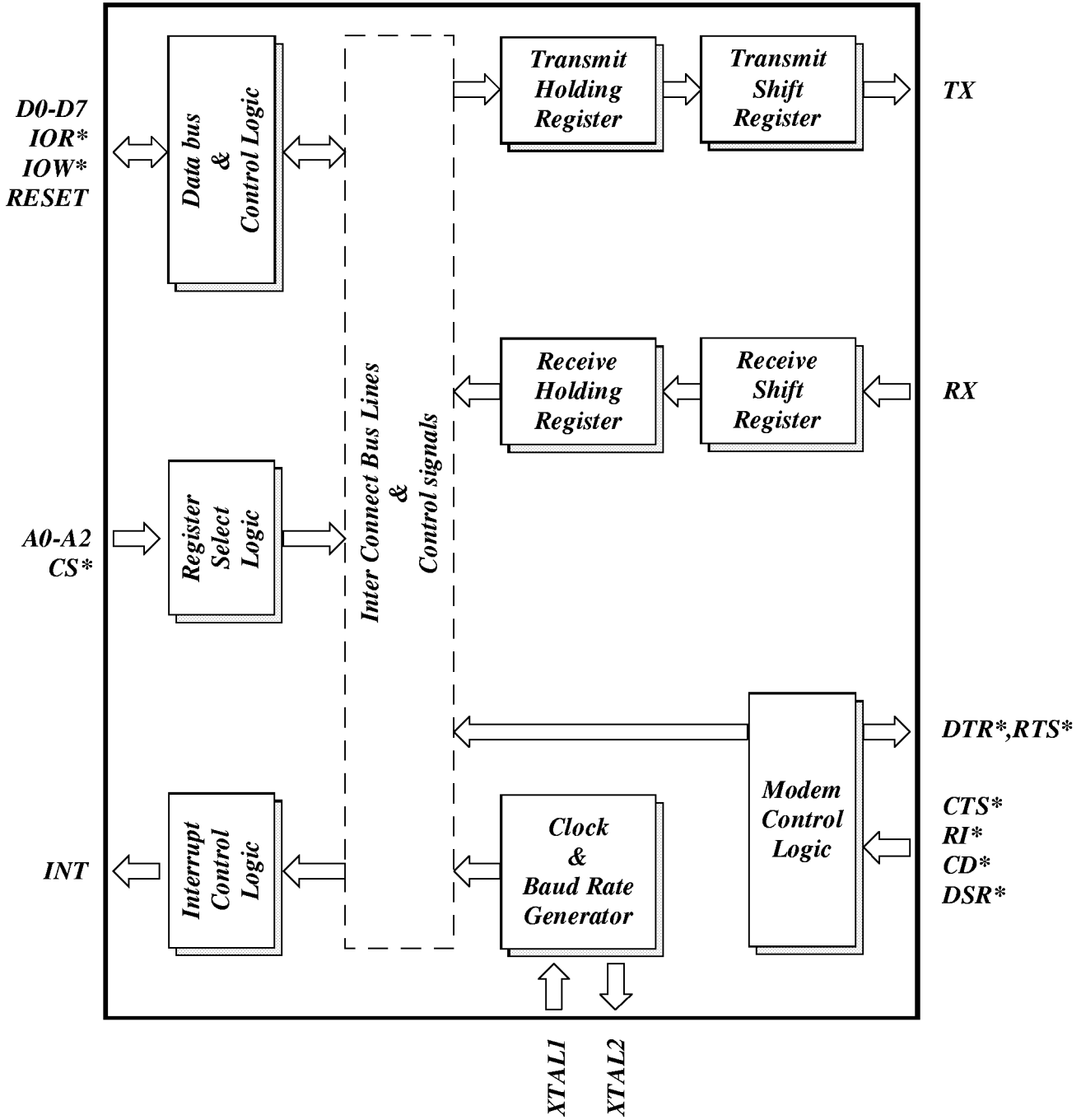


ST16C145X QFP Package



ST16C1450 ST16C1451

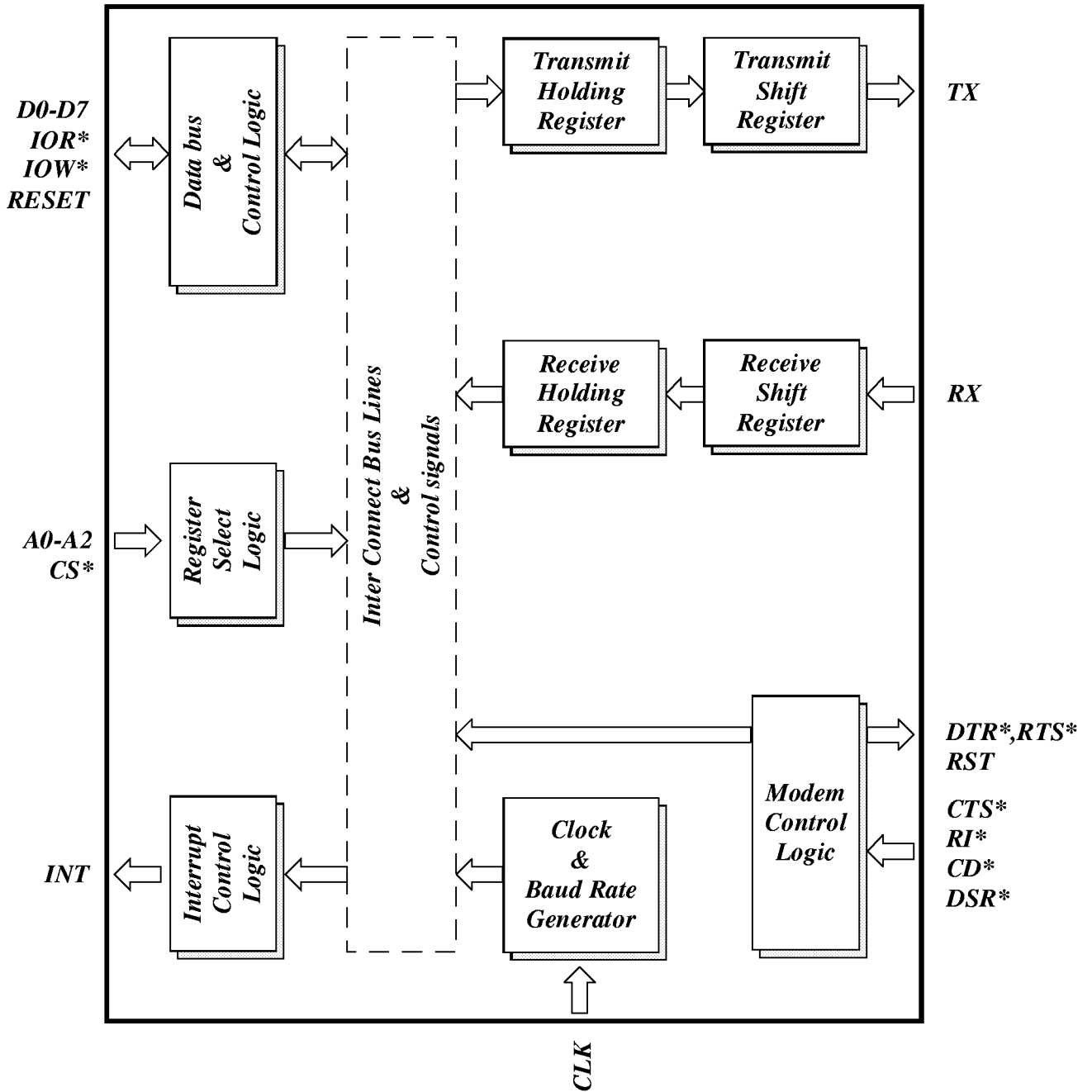
ST16C1450 BLOCK DIAGRAM



ST16C1450 ST16C1451

ST16C1450/51

ST16C1451 BLOCK DIAGRAM



ST16C1450

ST16C1451

SYMBOL DESCRIPTION (ST16C1450 - ST16C1451)

Symbol	Pin		Signal Type	Pin Description
	28	28		
D0-D7	1-8	1-8	I/O	Bi-directional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
RX	9	9	I	Serial data input. The serial information (data) received from serial port to ST16C145X receive input circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
TX	10	10	O	Serial data output. The serial data is transmitted via this pin with additional start , stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
CS*	11	11	I	Chip select (active low). A low at this pin enables the ST16C145X / CPU data transfer operation.
XTAL1	12	-	I	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
CLK	-	12	I	External clock input. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
XTAL2	13	-	O	Crystal input 2 or buffered clock output. See XTAL1.
IOW*	14	13	I	Write strobe (active low). A low on this pin will transfer the contents of the CPU data bus to the addressed register.
GND	15	14	O	Signal and power ground.
IOR*	16	15	I	Read strobe (active low). A low level on this pin transfers the contents of the ST16C145X data bus to the CPU..
RI*	17	16	I	Ring detect indicator (active low). A low on this pin indicates

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SYMBOL DESCRIPTION (ST16C1450 - ST16C1451)

Symbol	Pin		Signal Type	Pin Description
	28	28		
RST	-	17	O	the modem has received a ringing signal from telephone line. Reset output (active high). The ST16C1451 provides a buffered reset output which is gated internally with MCR bit-2.
INT	18	18	O	Interrupt output. (three state / active high) This pin goes high (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.
A0-A2	21-19	21-19	I	Address select line. To select internal registers.
RTS*	22	22	O	Request to send (active low). To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation.
DTR*	23	23	O	Data terminal read (active low). To indicate that ST16C145X is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset. Note that this pin does not have any effect on the transmit or receive operation.
RESET	24	24	I	Master reset (active high). A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
CTS*	25	25	I	Clear to send (active low). The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR bit-4. CTS* has no effect on the transmit or receive operation.
DSR*	26	26	I	Data set ready (active low). A low on this pin indicates the MODEM is ready to exchange data with UART. This pin

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SYMBOL DESCRIPTION (ST16C1450 - ST16C1451)

Symbol	Pin		Signal Type	Pin Description
	28	28		
CD*	27	27	I	does not have any effect on the transmit or receive operation. Carrier detect (active low). A low on this pin indicates the carrier has been detected by the modem.
VCC	28	28	I	Power supply input.

All unused input pins should be tied to VCC or GND.

PROGRAMMING TABLE

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1	0	Interrupt Status Register	
0	1	1		Line Control Register
1	0	0		Modem Control Register
1	0	1	Line Status Register	
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
0	0	0		LSB of Divisor Latch
0	0	1		MSB of Divisor Latch

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ST16C1450/51 ACCESSIBLE REGISTERS

A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER	0	0	0/ special mode	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	ISR	0	0	0	0	0	int priority bit-1	int priority bit-0	int status
0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR	0/power down	0	0	loop back	INT enable	SOFT reset	RTS*	DTR*
1 0 1	LSR	0	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1 1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	DLL	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	DLM	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

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REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register (THR) will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set.

On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the Line Status Register.

PROGRAMMABLE BAUD RATE GENERATOR

The ST16C1450/51 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-24 MHz and dividing it by any divisor from 1 to $2^{16}-1$. The output frequency of the Baudout* is equal to 16X of transmission baud rate (Baudout*=16 x Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

IER BIT-0:

0=disable the receiver ready interrupt.
1=enable the receiver ready interrupt.

IER BIT-1:

0=disable the transmitter empty interrupt.
1=enable the transmitter empty interrupt.

IER BIT-2:

0=disable the receiver line status interrupt.
1=enable the receiver line status interrupt.

IER BIT-3:

0=disable the modem status register interrupt.
1=enable the modem status register interrupt.

IER BIT-5:

0=normal ST16C450 mode.
1=special mode. Enable power down and SOFT rest.

IER BIT 4,6-7:

All these bits are set to logic zero.

INTERRUPT STATUS REGISTER (ISR)

The ST16C1450/51 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the ST16C1450/51 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority levels

P	D2	D1	D0	Source of the interrupt
1	1	1	0	LSR (Receiver Line Status Register)
2	1	0	0	RXRDY (Received Data Ready)
3	0	1	0	TXRDY(Transmitter Holding Register Empty)
4	0	0	0	MSR (Modem Status Register)

ISR BIT-0:

0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
1=no interrupt pending.

ISR BIT 1-2:

Logical combination of these bits, provides the highest priority interrupt pending.

ISR bit 3-7:

Not used

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:

These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
0	1	6
1	0	7
1	1	8

LCR BIT-2:

The number of stop bits can be specified by this bit.

BIT-2	Word length	Stop bit(s)
0	5,6,7,8	1
1	5	1-1/2
1	6,7,8	2

LCR BIT-3:

Parity or no parity can be selected via this bit.
0=no parity
1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4:

If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0=ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format.
1= EVEN parity bit is generated by forcing an even the number of 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5:

If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:

Break control bit. It causes a break condition to be transmitted (the TX is forced to low state).
0=normal operating condition.
1=forces the transmitter output (TX) to go low to alert the communication terminal.

LCR BIT-7:

The internal baud rate counter latch enable (DLEN).
0=normal operation.
1=select divisor latch register.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:

0=force DTR* output to high.
1=force DTR* output to low.

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MCR BIT-1:

0=force RTS* output to high.
1=force RTS* output to low.

MCR BIT-2:

0=normal operation.
1=software reset, set RST output to high.

MCR BIT-3:

0=set INT output pin to three state mode.
1=set INT output pin to normal operation mode.

MCR BIT-4:

0=normal operating mode.
1=enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX), CTS*, DSR*, CD*, and RI* are disabled. Internally the transmitter output is connected to the receiver input and DTR*, RTS*, SOFT reset and INT enable are connected to modem control inputs.

In this mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER.

MCR BIT 5-6:

Not used. Are set to zero permanently.

MCR bit-7:

0=normal mode.
1=power down mode. XTAL1, XTAL2, and baud rate generators are disabled.

LINE STATUS REGISTER (LSR)

This register provides the status of data transfer to CPU.

LSR BIT-0:

0=no data in receive holding register
1=data has been received and saved in the receive

holding register.

LSR BIT-1:

0=no overrun error (normal).
1=overrun error, next character arrived before receive holding register was emptied.

LSR BIT-2:

0=no parity error (normal).
1=parity error, received data does not have correct parity information.

LSR BIT-3:

0=no framing error (normal).
1=framing error received, received data did not have a valid stop bit.

LSR BIT-4:

0=no break condition (normal).
1=receiver received a break signal (RX was low for one character time frame).

LSR BIT-5:

0=transmit holding register is full. ST16C1450/51 will not accept any data for transmission.
1=transmit holding register is empty. CPU can load the next character.

LSR BIT-6:

0=transmitter holding and shift registers are full.
1=transmitter holding and shift registers are empty.

LSR BIT-7:

Not used.

MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:

Indicates that the CTS* input to the ST16C1450/51 has changed state since the last time it was read.

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MSR BIT-1:

Indicates that the DSR* input to the ST16C1450/51 has changed state since the last time it was read.

MSR BIT-2:

Indicates that the RI* input to the ST16C1450/51 has changed from a low to a high state.

MSR BIT-3:

Indicates that the CD* input to the ST16C1450/51 has changed state since the last time it was read.

MSR BIT-4:

This bit is equivalent to RTS in the MCR during local loop-back mode. It is the compliment of the CTS* input.

MSR BIT-5:

This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR* input.

MSR BIT-6:

This bit is equivalent to SOFT reset in the MCR during local loop-back mode. It is the compliment of the RI* input.

MSR BIT-7:

This bit is equivalent to INT enable in the MCR during local loop-back mode. It is the compliment to the CD* input.

Note: Whenever MSR BIT3-0: is set to logic "1", a MODEM Status Interrupt is generated.

SCRATCHPAD REGISTER (SR)

ST16C1450/51 provides a temporary data register to store 8 bits of information for variable use.

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	0.026
75	1536	
110	1047	
150	768	
300	384	
600	192	
1200	96	
2400	48	
3600	32	
4800	24	
7200	16	2.77
9600	12	
19.2K	6	
38.4K	3	
56K	2	
115.2K	1	

ST16C1450/51 EXTERNAL RESET CONDITION

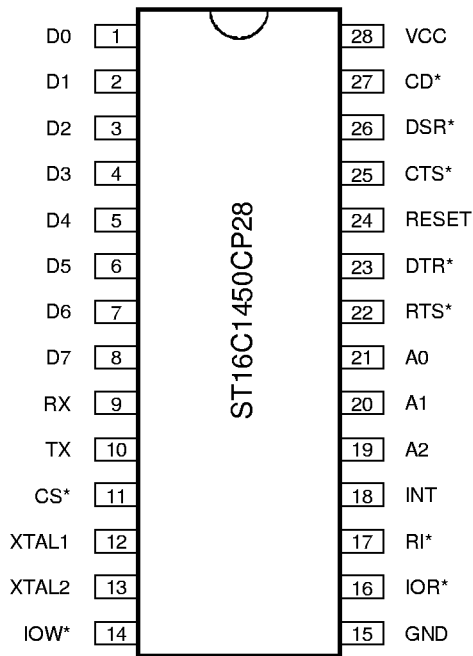
REGISTERS	RESET STATE
IER	IER BITS 0-7=0 ISR BIT-0=1, ISR BITS 1-7=0 LCR BITS 0-7=0 MCR BITS 0-7=0 LSR BITS 0-4=0, LSR BITS 5-6=1 LSR, BIT 7=0 MSR BITS 0-3=0, MSR BITS 4-7=input signals
ISR	
LCR	
MCR	
LSR	
MSR	

SIGNALS	RESET STATE
TX	High
SOFT reset	High
RTS*	High
DTR*	High
INT	Three state mode

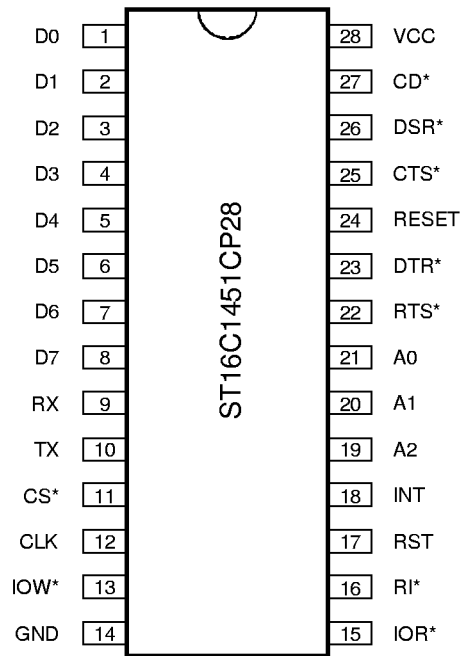
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ST16C1450 Plastic-DIP Package



ST16C1451 Plastic-DIP Package



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AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C (-40° - +85° C for IP, IJ,IQ packages), V_{CC}=3.3 - 5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		Min	Typ	Max		
T _{1w}	Clock high pulse duration	20			ns	
T _{2w}	Clock low pulse duration	20			ns	
T _{3w}	Oscillator/Clock speed			24	MHz	V _{CC} =5.0V
T _{3w}	Oscillator/Clock speed			8	MHz	V _{CC} =3.0V
T _{4w}	Address strobe width	15			ns	
T _{5s}	Address setup time	8			ns	
T _{5h}	Address hold time	0			ns	
T _{6s}	Chip select setup time	8			ns	
T _{6h}	Chip select hold time	0			ns	
T _{7d}	IOR* delay from chip select	7			ns	
T _{7w}	IOR* strobe width	40			ns	
T _{7h}	Chip select hold time from IOR*	0			ns	
T _{9d}	Read cycle delay	40			ns	
T _{12s}	Delay from IOR* to data	15			ns	
T _{12h}	Data hold time			5	ns	
T _{13d}	IOW* delay from chip select	7			ns	
T _{13w}	IOW* strobe width	40			ns	
T _{13h}	Chip select hold time from IOW*	0			ns	
T _{15d}	Write cycle delay	40			ns	
T _{16s}	Data setup time	10			ns	
T _{16h}	Data hold time	5			ns	
T _{17d}	Delay from IOW* to output			50	ns	100 pF load
T _{18d}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T _{19d}	Delay to reset interrupt from IOR*			70	ns	100 pF load
T _{20d}	Delay from stop to set interrupt			1 _{Rclk}	*	100 pF load
T _{21d}	Delay from IOR* to reset interrupt			200	ns	100 pF load
T _{22d}	Delay from stop to interrupt			100	ns	
T _{23d}	Delay from initial INT reset to transmit start	8		24	*	
T _{24d}	Delay from IOW* to reset interrupt			175	ns	
T _{25d}	Delay from stop to set RxRdy			1	Clk	
T _{26d}	Delay from IOR* to reset RxRdy			1	µs	
T _{27d}	Delay from IOW* to set TxRdy			175	ns	
T _{28d}	Delay from start to reset TxRdy			8	*	
T _R	Reset pulse width	10			ns	
N	Baud rate divisor	1		2 ₁₆₋₁	Rclk	

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ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

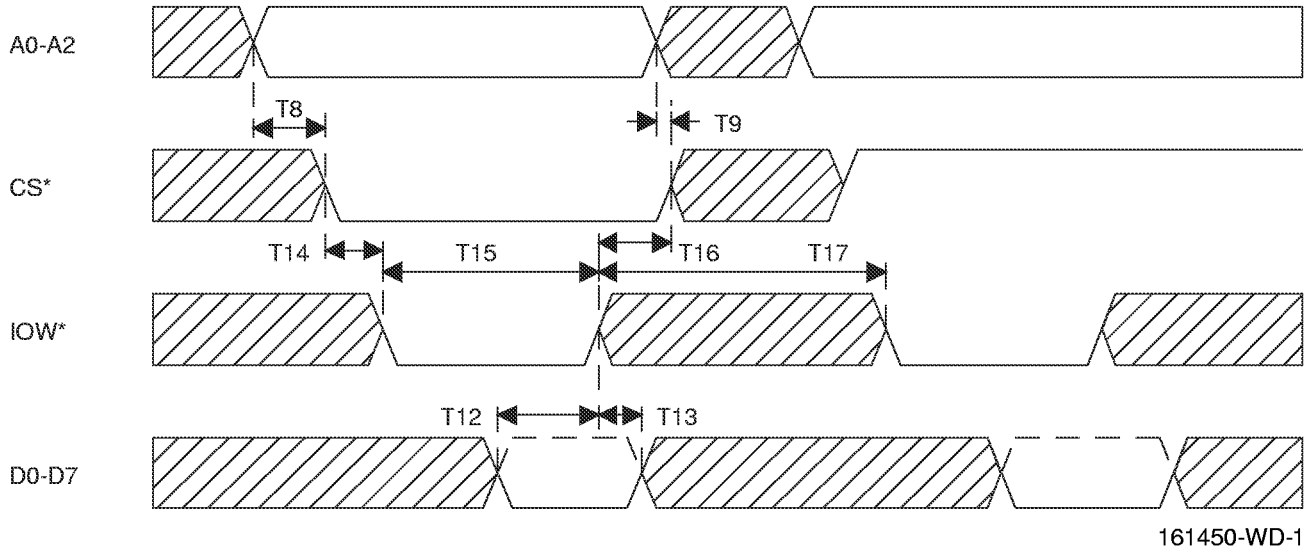
$T_A=0^\circ - 70^\circ \text{ C}$ ($-40^\circ - +85^\circ \text{ C}$ for IP, IJ,IQ packages), $V_{CC}=3.3 - 5.0 \text{ V} \pm 10\%$ unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		Min	Typ	Max		
V_{ILCK}	Clock input low level	-0.5		0.6	V	$V_{CC}=5.0 \text{ V}$
V_{IHCK}	Clock input high level	3.0		VCC	V	$V_{CC}=5.0 \text{ V}$
V_{IL}	Input low level	-0.5		0.8	V	$V_{CC}=5.0 \text{ V}$
V_{IH}	Input high level	2.2		VCC	V	$V_{CC}=5.0 \text{ V}$
V_{OL}	Output low level on all outputs			0.4	V	$I_{OL}= 6 \text{ mA}$
V_{OH}	Output high level	2.4			V	$I_{OH}= -6 \text{ mA}$
I_{IL}	Input leakage			± 10	μA	
I_{CL}	Clock leakage			± 10	μA	
I_{CC}	Avg power supply current		1.2	1.5	mA	$V_{CC}=5.0 \text{ V}$
C_P	Input capacitance		2	5	pF	
V_{ILCK}	Clock input low level	-0.3		0.8	V	$V_{CC}=3.0 \text{ V}$
V_{IHCK}	Clock input high level	2.4		VCC	V	$V_{CC}=3.0 \text{ V}$
V_{IL}	Input low level	-0.3		0.8	V	$V_{CC}=3.0 \text{ V}$
V_{IH}	Input high level	2.0		VCC	V	$V_{CC}=3.0 \text{ V}$
V_{OL}	Output low level on all outputs			0.4	V	$V_{CC}=3.0 \text{ V}$, $I_{OL}= 4.2 \text{ mA}$
V_{OH}	Output high level	2.0			V	$V_{CC}=3.0 \text{ V}$, $I_{OH}= -1 \text{ mA}$
I_{CC}	Avg power supply current		0.6	0.8	mA	$V_{CC}=3.0 \text{ V}$

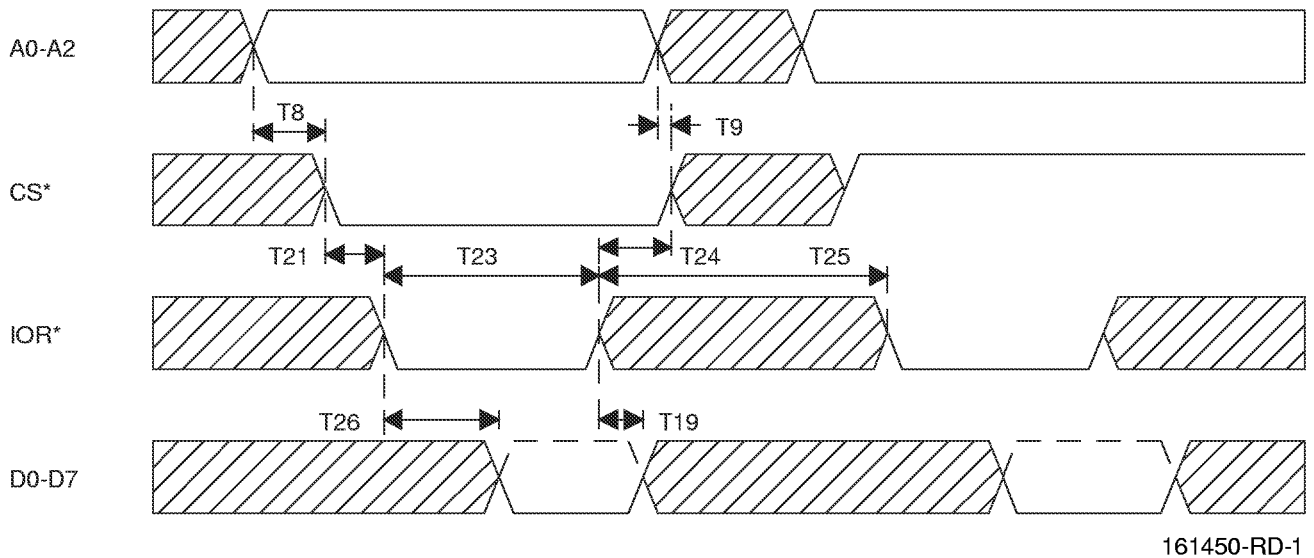
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GENERAL WRITE TIMING



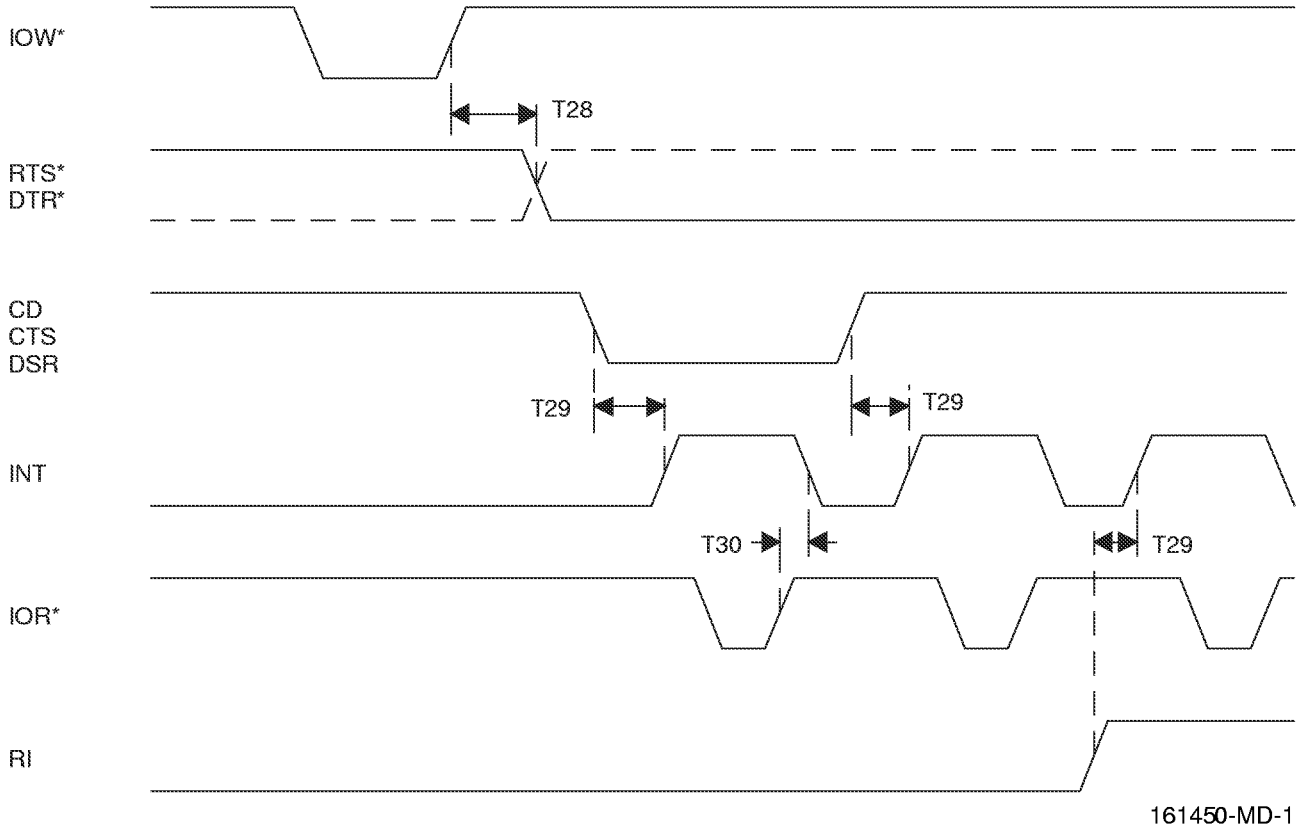
GENERAL READ TIMING



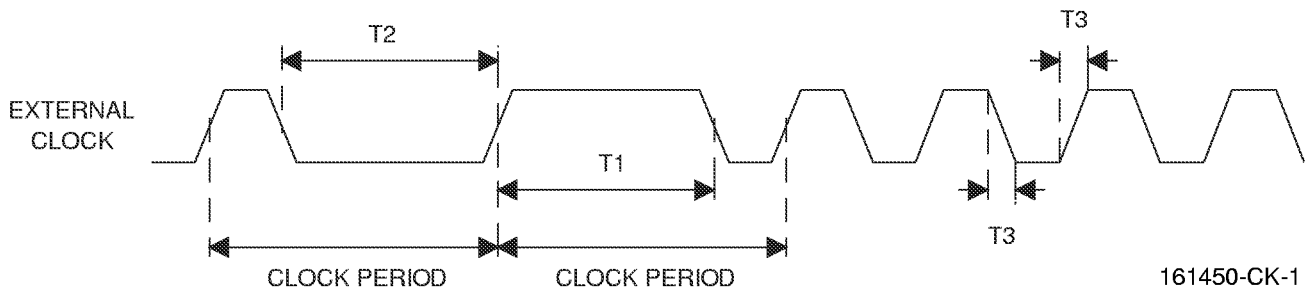
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MODEM TIMING



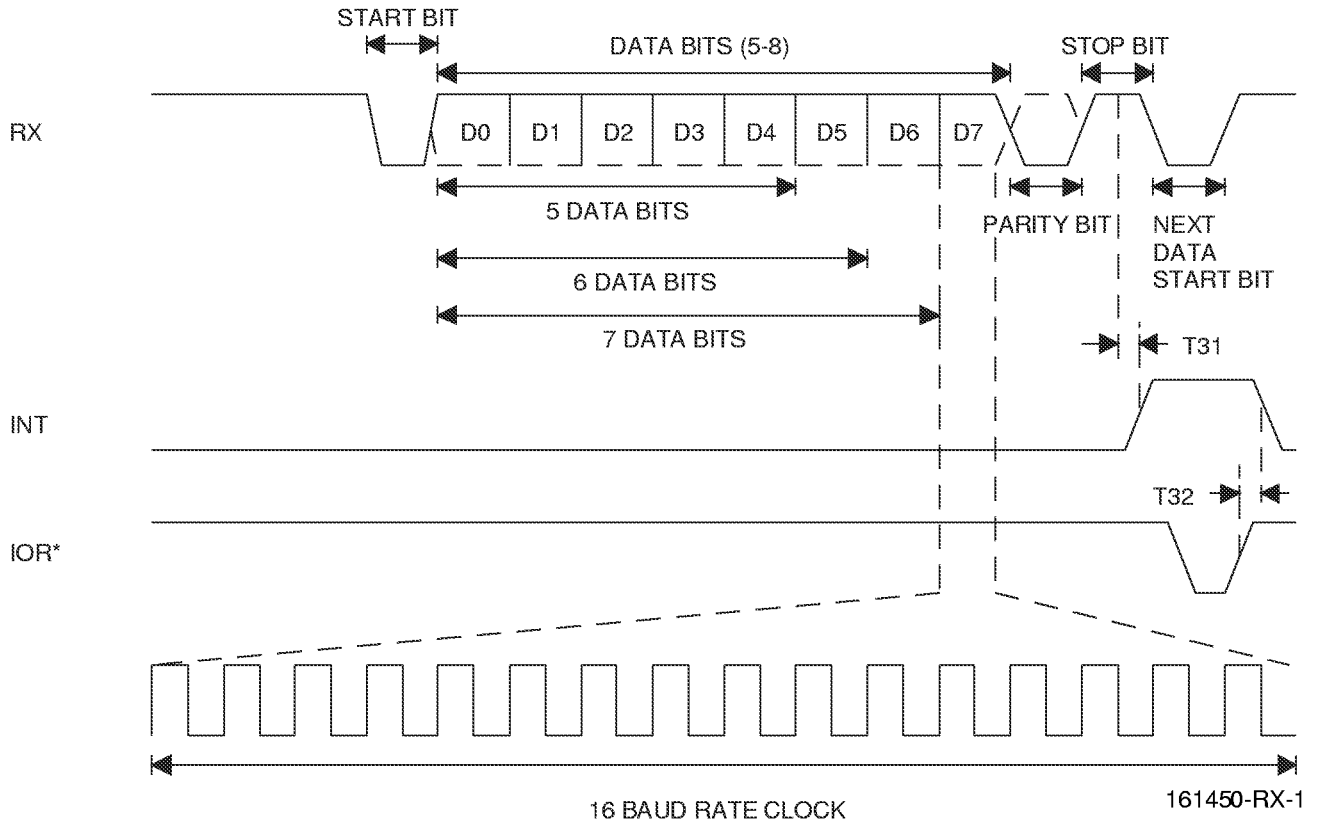
CLOCK TIMING



ST16C1450 ST16C1451

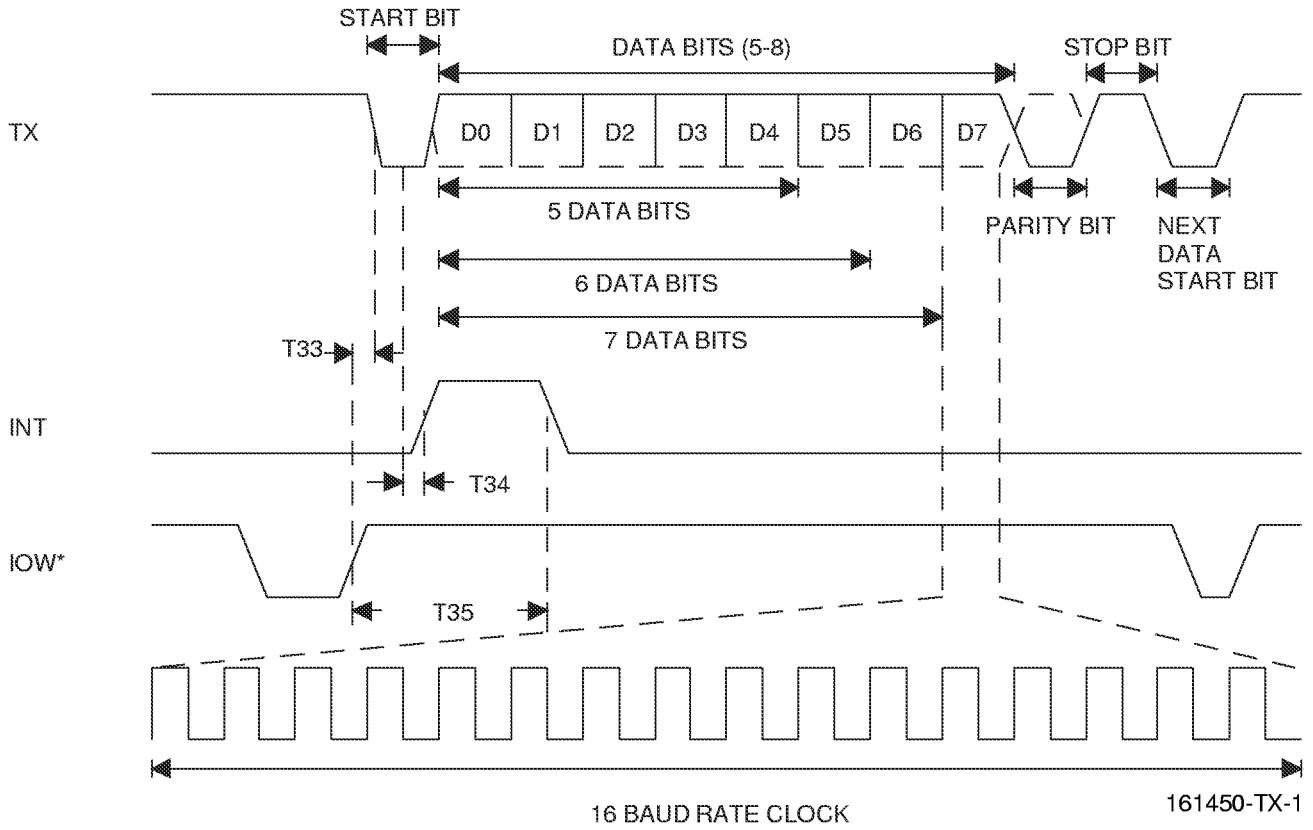
ST16C1450/51

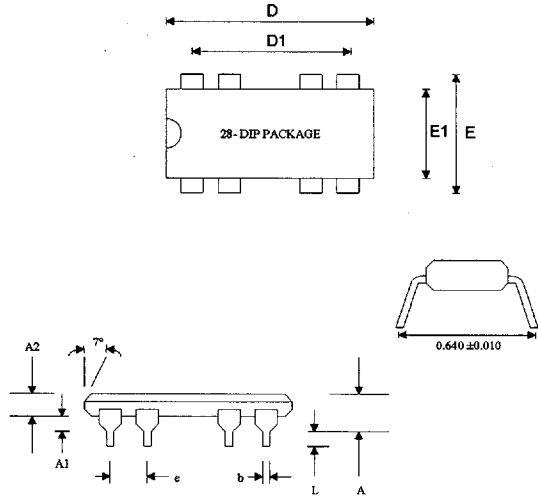
RECEIVE TIMING



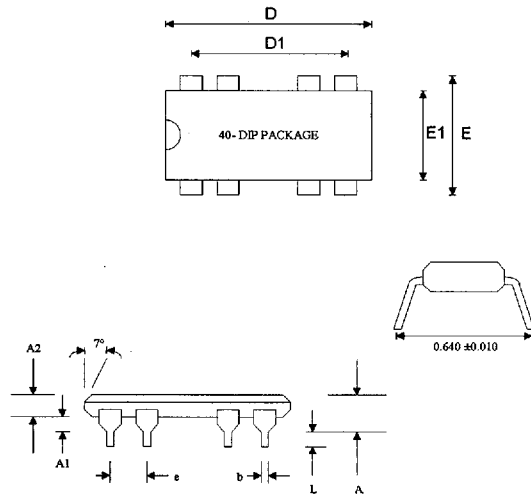
ST16C1450 ST16C1451

TRANSMIT TIMING

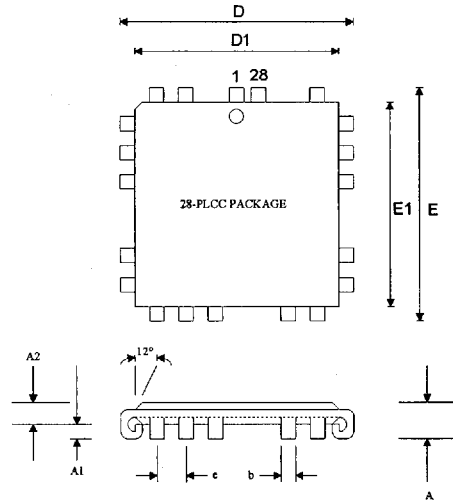




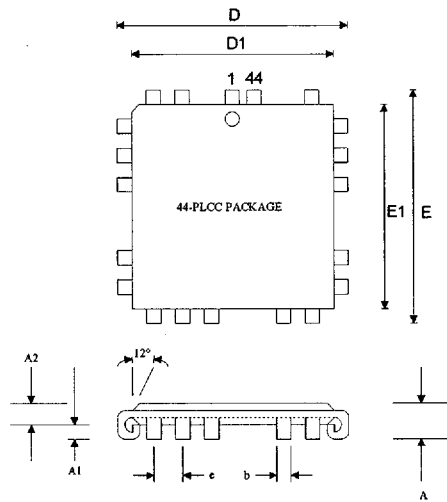
DIMENSIONS	TOLERANCE (MIL)
A	0.200 ± 0.010
A1	0.015
A2	0.150 ± 0.005
D	1.450 ± 0.005
D1	1.300
E	0.610 ± 0.010
E1	0.550 ± 0.005
L	0.125 ± 0.020
e	0.100
b	0.17 ± 0.02



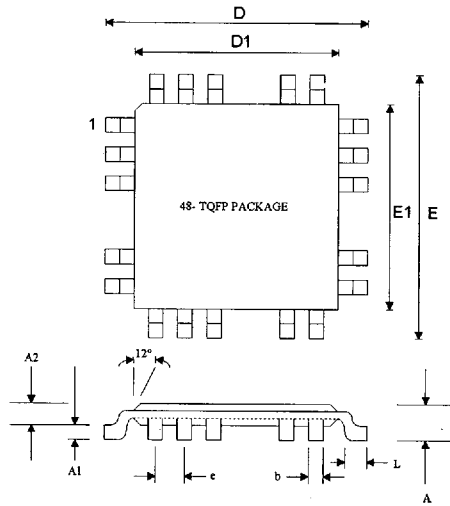
DIMENSIONS	TOLERANCE (MIL)
A	0.200 ± 0.010
A1	0.015
A2	0.150 ± 0.005
D	2.050 ± 0.005
D1	1.900
E	0.610 ± 0.010
E1	0.550 ± 0.005
L	0.125 ± 0.020
e	0.100
b	0.17 ± 0.02



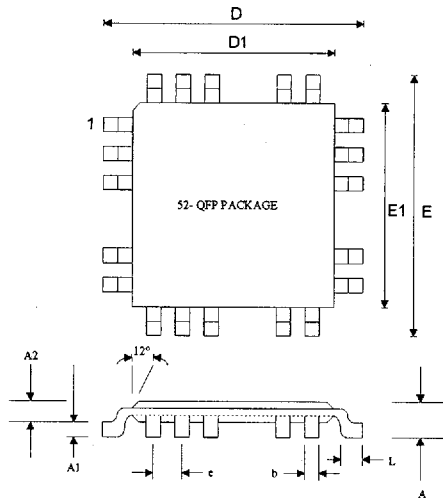
DIMENSIONS	TOLERANCE (mil)
A	0.170±0.005
A1	0.020
A2	0.150±0.002
D	0.490±0.005
D1	0.454±0.002
E	0.490±0.005
E1	0.454±0.002
c	0.050±0.002
b	0.030±0.005



DIMENSIONS	TOLERANCE (mil)
A	0.170±0.005
A1	0.020
A2	0.150±0.002
D	0.690±0.005
D1	0.654±0.002
E	0.690±0.005
E1	0.654±0.002
c	0.050±0.002
b	0.030±0.005



DIMENSIONS	TOLERANCE (mm)
A	1.20
A1	0.05 - 0.10
A2	1.0 ±0.5
D	9.0 ±0.25
D1	7.0 ±0.10
E	9.00 ±0.25
E1	7.0 ±0.10
L	0.6 ±0.15
c	0.5
b	0.22 ±0.05



DIMENSIONS	TOLERANCE (mm)
A	2.26 ±0.13
A1	0.23 ±0.07
A2	2.03 ±0.06
D	14.1 ±0.20
D1	10 ±0.10
E	14.1 ±0.20
E1	10 ±0.10
L	0.88 ±0.15
c	0.65
b	0.30 ±0.08