HM11S140

129 COM / 128 SEG DRIVER & CONTROLLER
FOR 4 GRAY SCALE STN LCD

Hynix Semiconductor, Inc.

1. INTRODUCTION

The HM11S140 is a driver & controller LSI for 4-level gray scale graphic dot-matrix liquid crystal display systems. It contains 128 segment and 129 common driver circuits.

This chip is connected directly to a microprocessor (MPU), accepts serial or 8-bit parallel display data and stores in an on-chip display data RAM (DDRAM) of 128 x 129 x 2 bits.

It performs display data RAM read/write operation with no external operating clock to minimize power consumption. In addition, because it contains power supply circuits necessary to drive liquid crystal, it is possible to make a display system with the fewest components.

2. FEATURES

Driver output circuits

-. 129 common outputs / 128 segment outputs

4-level (White, Light Gray, Dark Gray, Black) Gray scale display with PWM and FRC methods

DDRAM data [2n: 2n+1]	00	01	10	11
Gray scale	White	Light gray	Dark gray	Black

(Accessible column address, n = 0, 1, 2, …… ,125, 126, 127)

Applicable duty-ratios

Duty ratio	Applicable LCD bias	Maximum display area
1/16 ~ 1/128 (ICON disabled)	1/5 to 1/12	128 x 128
1/17 ~ 1/129 (ICON enabled)		129 x 128

-. Various partial displays

-. Partial window moving & data scrolling

On-chip display data RAM (DDRAM)

-. Capacity: 129 x 128 x 2 = 33,024 bits

-. Bit data " 1" : a dot of display is illuminated

-. Bit data " 0" : a dot of display is not illuminated

Microprocessor interface

-. 8-bit parallel bi-directional interface with 6800-series or 8080-series

-. Serial interface (only write operation)

On-chip low power analog circuit

-. On-chip oscillator circuit for display clock

-. Voltage converter (x3, x4, x5 or x6)

-. Voltage regulator (temperature coefficient: -0.1%/°C or external input)

-. On-chip electronic contrast control function (64 steps)

-. Voltage follower (LCD bias : 1/5 to 1/12)

Operating voltage range

-. Supply voltage (V_{DD}): 2.4 to 3.6V

-. LCD driving voltage (V_{LCD} = V0 - VSS): 4.0 to 15.0 V

Low power consumption

-. TBD μA Max. (operation)

-. 2μA Max. (sleep mode)

Package type

-. Slim chip for TCP / COF

3. BLOCK DIAGRAM

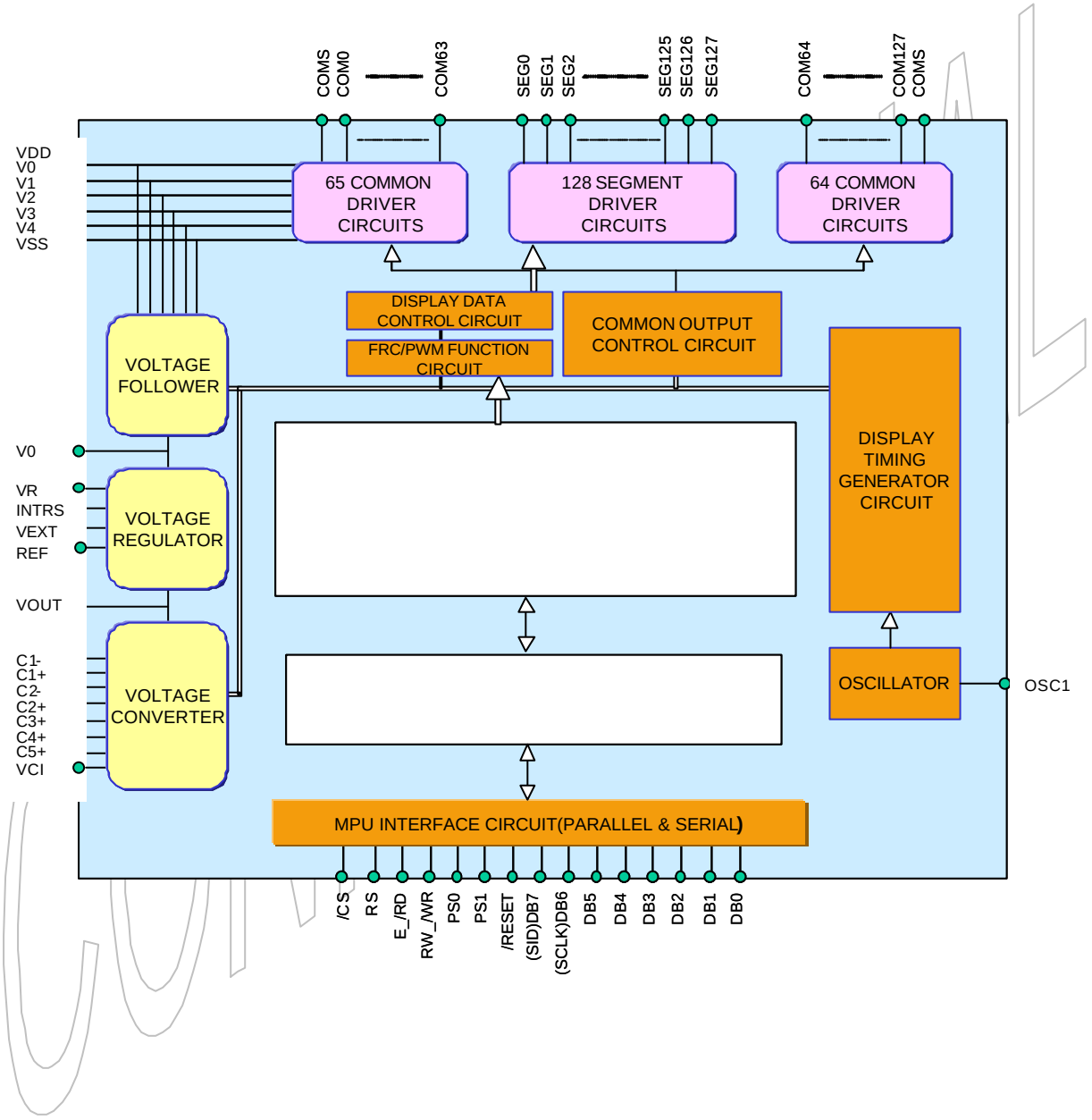

Figure 3-1. Block diagram

4. PAD CONFIGURATION

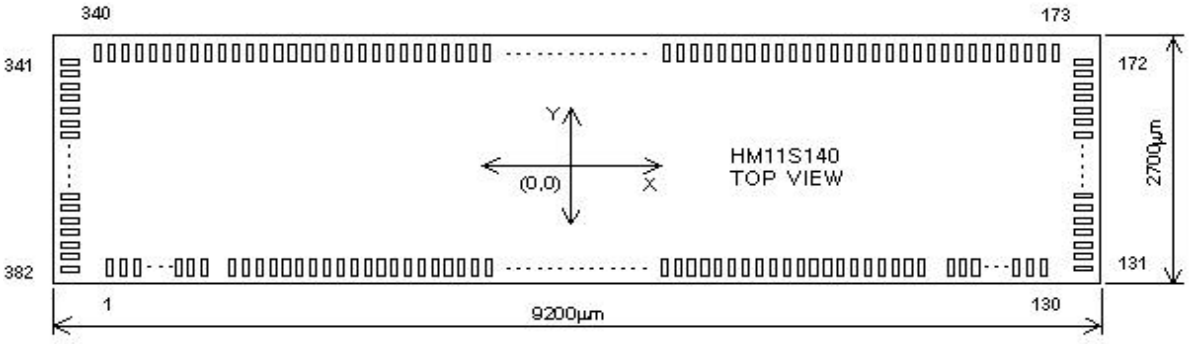

Figure 4-1. HM11S140 Chip configuration

Table 4-1. HM11S140 Pad dimensions

ITEM	Pad No.	Size		Unit
		X	Y	
Chip size (without S/L)	-	9200	2700	µm
Pad pitch	16~115	70		
	1~15, 116~130, 131~172, 173~340, 341~382	52		
	15~16, 115~116	149		
Bumped pad size (Bottom)	16~115	50	102	
	1~15, 116~130, 173~340	34	78	
	131~172, 341~382	78	34	
Bumped pad height	All pad	18 ±3 (Typ.)		

5. PAD CENTER COORDINATES

Table 5-1. Pad center coordinates [Unit: mm]

PAD No.	Pad name	X	Y	PAD No.	Pad name	X	Y	PAD No.	Pad name	X	Y
1	DUMMY0	-4342	-1256	51	TEST12	-1015	-1256	101	V4	2485	-1256
2	DUMMY1	-4290	-1256	52	TEST13	-945	-1256	102	V3	2555	-1256
3	COM118	-4238	-1256	53	TEST14	-875	-1256	103	V3	2625	-1256
4	COM119	-4186	-1256	54	TEST15	-805	-1256	104	V2	2695	-1256
5	COM120	-4134	-1256	55	TEST16	-735	-1256	105	V2	2765	-1256
6	COM121	-4082	-1256	56	TEST17	-665	-1256	106	V1	2835	-1256
7	COM122	-4030	-1256	57	TEST18	-595	-1256	107	V1	2905	-1256
8	COM123	-3978	-1256	58	TEST19	-525	-1256	108	V0	2975	-1256
9	COM124	-3926	-1256	59	TEST20	-455	-1256	109	V0	3045	-1256
10	COM125	-3874	-1256	60	VDD	-385	-1256	110	VR	3115	-1256
11	COM126	-3822	-1256	61	VDD	-315	-1256	111	VR	3185	-1256
12	COM127	-3770	-1256	62	VDD	-245	-1256	112	VSS	3255	-1256
13	COMS	-3718	-1256	63	VDD	-175	-1256	113	VSS	3325	-1256
14	DUMMY2	-3666	-1256	64	VDD	-105	-1256	114	VDD	3395	-1256
15	DUMMY3	-3614	-1256	65	VDD	-35	-1256	115	OSC1	3465	-1256
16	VDD	-3465	-1256	66	VCI	35	-1256	116	DUMMY4	3614	-1256
17	TESTCK	-3395	-1256	67	VCI	105	-1256	117	DUMMY5	3666	-1256
18	VSS	-3325	-1256	68	VSS	175	-1256	118	COM63	3718	-1256
19	PS	-3255	-1256	69	VSS	245	-1256	119	COM62	3770	-1256
20	VDD	-3185	-1256	70	VSS	315	-1256	120	COM61	3822	-1256
21	C68	-3115	-1256	71	VSS	385	-1256	121	COM60	3874	-1256
22	VSS	-3045	-1256	72	VSS	455	-1256	122	COM59	3926	-1256
23	/CS	-2975	-1256	73	VSS	525	-1256	123	COM58	3978	-1256
24	/RESET	-2905	-1256	74	VSS	595	-1256	124	COM57	4030	-1256
25	VDD	-2835	-1256	75	VOUT	665	-1256	125	COM56	4082	-1256
26	RS	-2765	-1256	76	VOUT	735	-1256	126	COM55	4134	-1256
27	RW_/WR	-2695	-1256	77	C5+	805	-1256	127	COM54	4186	-1256
28	VSS	-2625	-1256	78	C5+	875	-1256	128	COM53	4238	-1256
29	E_/RD	-2555	-1256	79	C3+	945	-1256	129	DUMMY6	4290	-1256
30	VDD	-2485	-1256	80	C3+	1015	-1256	130	DUMMY7	4342	-1256
31	DB0	-2415	-1256	81	C1-	1085	-1256	131	DUMMY8	4506	-1066
32	DB1	-2345	-1256	82	C1-	1155	-1256	132	DUMMY9	4506	-1014
33	DB2	-2275	-1256	83	C1+	1225	-1256	133	DUMMY10	4506	-962
34	DB3	-2205	-1256	84	C1+	1295	-1256	134	COM52	4506	-910
35	DB4	-2135	-1256	85	C2+	1365	-1256	135	COM51	4506	-858
36	DB5	-2065	-1256	86	C2+	1435	-1256	136	COM50	4506	-806
37	DB6	-1995	-1256	87	C2-	1505	-1256	137	COM49	4506	-754
38	DB7	-1925	-1256	88	C2-	1575	-1256	138	COM48	4506	-702
39	TEST0	-1855	-1256	89	C4+	1645	-1256	139	COM47	4506	-650
40	TEST1	-1785	-1256	90	C4+	1715	-1256	140	COM46	4506	-598
41	TEST2	-1715	-1256	91	VDD	1785	-1256	141	COM45	4506	-546
42	TEST3	-1645	-1256	92	VDD	1855	-1256	142	COM44	4506	-494
43	TEST4	-1575	-1256	93	REF	1925	-1256	143	COM43	4506	-442
44	TEST5	-1505	-1256	94	VSS	1995	-1256	144	COM42	4506	-390
45	TEST6	-1435	-1256	95	VEXT	2065	-1256	145	COM41	4506	-338
46	TEST7	-1365	-1256	96	VDD	2135	-1256	146	COM40	4506	-286
47	TEST8	-1295	-1256	97	INTRS	2205	-1256	147	COM39	4506	-234
48	TEST9	-1225	-1256	98	VSS	2275	-1256	148	COM38	4506	-182
49	TEST10	-1155	-1256	99	VSS	2345	-1256	149	COM37	4506	-130
50	TEST11	-1085	-1256	100	V4	2415	-1256	150	COM36	4506	-78

Table 5-2. Pad center coordinates (continued) [Unit: mm]

PAD No.	Pad name	X	Y	PAD No.	Pad name	X	Y	PAD No.	Pad name	X	Y
151	COM35	4506	-26	201	SEG8	2886	1256	251	SEG58	286	1256
152	COM34	4506	26	202	SEG9	2834	1256	252	SEG59	234	1256
153	COM33	4506	78	203	SEG10	2782	1256	253	SEG60	182	1256
154	COM32	4506	130	204	SEG11	2730	1256	254	SEG61	130	1256
155	COM31	4506	182	205	SEG12	2678	1256	255	SEG62	78	1256
156	COM30	4506	234	206	SEG13	2626	1256	256	SEG63	26	1256
157	COM29	4506	286	207	SEG14	2574	1256	257	SEG64	-26	1256
158	COM28	4506	338	208	SEG15	2522	1256	258	SEG65	-78	1256
159	COM27	4506	390	209	SEG16	2470	1256	259	SEG66	-130	1256
160	COM26	4506	442	210	SEG17	2418	1256	260	SEG67	-182	1256
161	COM25	4506	494	211	SEG18	2366	1256	261	SEG68	-234	1256
162	COM24	4506	546	212	SEG19	2314	1256	262	SEG69	-286	1256
163	COM23	4506	598	213	SEG20	2262	1256	263	SEG70	-338	1256
164	COM22	4506	650	214	SEG21	2210	1256	264	SEG71	-390	1256
165	COM21	4506	702	215	SEG22	2158	1256	265	SEG72	-442	1256
166	COM20	4506	754	216	SEG23	2106	1256	266	SEG73	-494	1256
167	COM19	4506	806	217	SEG24	2054	1256	267	SEG74	-546	1256
168	COM18	4506	858	218	SEG25	2002	1256	268	SEG75	-598	1256
169	COM17	4506	910	219	SEG26	1950	1256	269	SEG76	-650	1256
170	DUMMY11	4506	962	220	SEG27	1898	1256	270	SEG77	-702	1256
171	DUMMY12	4506	1014	221	SEG28	1846	1256	271	SEG78	-754	1256
172	DUMMY13	4506	1066	222	SEG29	1794	1256	272	SEG79	-806	1256
173	DUMMY14	4342	1256	223	SEG30	1742	1256	273	SEG80	-858	1256
174	DUMMY15	4290	1256	224	SEG31	1690	1256	274	SEG81	-910	1256
175	COM16	4238	1256	225	SEG32	1638	1256	275	SEG82	-962	1256
176	COM15	4186	1256	226	SEG33	1586	1256	276	SEG83	-1014	1256
177	COM14	4134	1256	227	SEG34	1534	1256	277	SEG84	-1066	1256
178	COM13	4082	1256	228	SEG35	1482	1256	278	SEG85	-1118	1256
179	COM12	4030	1256	229	SEG36	1430	1256	279	SEG86	-1170	1256
180	COM11	3978	1256	230	SEG37	1378	1256	280	SEG87	-1222	1256
181	COM10	3926	1256	231	SEG38	1326	1256	281	SEG88	-1274	1256
182	COM9	3874	1256	232	SEG39	1274	1256	282	SEG89	-1326	1256
183	COM8	3822	1256	233	SEG40	1222	1256	283	SEG90	-1378	1256
184	COM7	3770	1256	234	SEG41	1170	1256	284	SEG91	-1430	1256
185	COM6	3718	1256	235	SEG42	1118	1256	285	SEG92	-1482	1256
186	COM5	3666	1256	236	SEG43	1066	1256	286	SEG93	-1534	1256
187	COM4	3614	1256	237	SEG44	1014	1256	287	SEG94	-1586	1256
188	COM3	3562	1256	238	SEG45	962	1256	288	SEG95	-1638	1256
189	COM2	3510	1256	239	SEG46	910	1256	289	SEG96	-1690	1256
190	COM1	3458	1256	240	SEG47	858	1256	290	SEG97	-1742	1256
191	COM0	3406	1256	241	SEG48	806	1256	291	SEG98	-1794	1256
192	COMS	3354	1256	242	SEG49	754	1256	292	SEG99	-1846	1256
193	SEG0	3302	1256	243	SEG50	702	1256	293	SEG100	-1898	1256
194	SEG1	3250	1256	244	SEG51	650	1256	294	SEG101	-1950	1256
195	SEG2	3198	1256	245	SEG52	598	1256	295	SEG102	-2002	1256
196	SEG3	3146	1256	246	SEG53	546	1256	296	SEG103	-2054	1256
197	SEG4	3094	1256	247	SEG54	494	1256	297	SEG104	-2106	1256
198	SEG5	3042	1256	248	SEG55	442	1256	298	SEG105	-2158	1256
199	SEG6	2990	1256	249	SEG56	390	1256	299	SEG106	-2210	1256
200	SEG7	2938	1256	250	SEG57	338	1256	300	SEG107	-2262	1256

Table 5-3. Pad center coordinates (continued) [Unit: ㎜]

PAD No.	Pad name	X	Y	PAD No.	Pad name	X	Y	PAD No.	Pad name	X	Y
301	SEG108	-2314	1256	351	COM89	-4506	546				
302	SEG109	-2366	1256	352	COM90	-4506	494				
303	SEG110	-2418	1256	353	COM91	-4506	442				
304	SEG111	-2470	1256	354	COM92	-4506	390				
305	SEG112	-2522	1256	355	COM93	-4506	338				
306	SEG113	-2574	1256	356	COM94	-4506	286				
307	SEG114	-2626	1256	357	COM95	-4506	234				
308	SEG115	-2678	1256	358	COM96	-4506	182				
309	SEG116	-2730	1256	359	COM97	-4506	130				
310	SEG117	-2782	1256	360	COM98	-4506	78				
311	SEG118	-2834	1256	361	COM99	-4506	26				
312	SEG119	-2886	1256	362	COM100	-4506	-26				
313	SEG120	-2938	1256	363	COM101	-4506	-78				
314	SEG121	-2990	1256	364	COM102	-4506	-130				
315	SEG122	-3042	1256	365	COM103	-4506	-182				
316	SEG123	-3094	1256	366	COM104	-4506	-234				
317	SEG124	-3146	1256	367	COM105	-4506	-286				
318	SEG125	-3198	1256	368	COM106	-4506	-338				
319	SEG126	-3250	1256	369	COM107	-4506	-390				
320	SEG127	-3302	1256	370	COM108	-4506	-442				
321	COM64	-3354	1256	371	COM109	-4506	-494				
322	COM65	-3406	1256	372	COM110	-4506	-546				
323	COM66	-3458	1256	373	COM111	-4506	-598				
324	COM67	-3510	1256	374	COM112	-4506	-650				
325	COM68	-3562	1256	375	COM113	-4506	-702				
326	COM69	-3614	1256	376	COM114	-4506	-754				
327	COM70	-3666	1256	377	COM115	-4506	-806				
328	COM71	-3718	1256	378	COM116	-4506	-858				
329	COM72	-3770	1256	379	COM117	-4506	-910				
330	COM73	-3822	1256	380	DUMMY21	-4506	-962				
331	COM74	-3874	1256	381	DUMMY22	-4506	-1014				
332	COM75	-3926	1256	382	DUMMY23	-4506	-1066				
333	COM76	-3978	1256								
334	COM77	-4030	1256								
335	COM78	-4082	1256								
336	COM79	-4134	1256								
337	COM80	-4186	1256								
338	COM81	-4238	1256								
339	DYMMY16	-4290	1256								
340	DUMMY17	-4342	1256								
341	DUMMY18	-4506	1066								
342	DUMMY19	-4506	1014								
343	DUMMY20	-4506	962								
344	COM82	-4506	910								
345	COM83	-4506	858								
346	COM84	-4506	806								
347	COM85	-4506	754								
348	COM86	-4506	702								
349	COM87	-4506	650								
350	COM88	-4506	598								

6. PIN DESCRIPTION

Table 6-1. Pin description

<table>
<tr><td colspan="3">Power supply</td></tr>
<tr><td>Name</td><td>I/O</td><td>Description</td></tr>
<tr><td>VDD</td><td rowspan="2">Supply</td><td>Power supply</td></tr>
<tr><td>VSS</td><td>Ground</td></tr>
<tr><td>V0
V1
V2
V3
V4</td><td>I/O</td><td>LCD driver supply voltages
The voltage determined by LCD pixel is impedance-converted by an operational amplifier for application.
Voltages should have the following relationship;
V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ VSS
When the internal power circuit is active, these voltages are generated as following table according to the state of LCD bias.
<table>
<tr><th>LCD bias</th><th>V1</th><th>V2</th><th>V3</th><th>V4</th></tr>
<tr><td>1/N bias</td><td>(N-1) / N x V0</td><td>(N-2) / N x V0</td><td>(2/N) x V0</td><td>(1/N) x V0</td></tr>
<tr><td colspan="5">Note: N = 5 to 12</td></tr>
</table></td></tr>
<tr><td colspan="3">LCD driver supply</td></tr>
<tr><td>Name</td><td>I/O</td><td>Description</td></tr>
<tr><td>C1+</td><td rowspan="7">O</td><td>Capacitor 1 positive connection pin for voltage converter</td></tr>
<tr><td>C1-</td><td>Capacitor 1 negative connection pin for voltage converter</td></tr>
<tr><td>C2+</td><td>Capacitor 2 positive connection pin for voltage converter</td></tr>
<tr><td>C2-</td><td>Capacitor 2 negative connection pin for voltage converter</td></tr>
<tr><td>C3+</td><td>Capacitor 3 positive connection pin for voltage converter</td></tr>
<tr><td>C4+</td><td>Capacitor 4 positive connection pin for voltage converter</td></tr>
<tr><td>C5+</td><td>Capacitor 5 positive connection pin for voltage converter</td></tr>
<tr><td>VOUT</td><td>I/O</td><td>Voltage converter input / output pin</td></tr>
<tr><td>VCI</td><td>I</td><td>Voltage converter input voltage pin</td></tr>
<tr><td>VR</td><td>I</td><td>V0 voltage adjustment pin
It is valid only when on-chip resistors are not used (INTRS = "L")
When using internal resistors (INTRS = "H"), open this pin</td></tr>
<tr><td>REF</td><td>I</td><td>Selects the external VREF voltage via the VEXT pin
– REF = “ H” : using the internal VREF
– REF = “ L” : using the external VREF</td></tr>
<tr><td>VEXT</td><td>I</td><td>Externally input reference voltage (VREF) for the internal voltage regulator
It is valid only when REF is "L"
When using internal voltage regulator, connect to VDD, VSS or open this pin</td></tr>
<tr><td>OSC1</td><td>I</td><td>When using internal clock oscillator, connect a resistor between OSC1 and VDD.</td></tr>
</table>

Table 6-1. Pin description (continued)

<table>
<tr><td colspan="3">System control</td></tr>
<tr><td>Name</td><td>I/O</td><td>Description</td></tr>
<tr><td>INTRS</td><td>I</td><td>Internal resistor select pin
This pin selects the resistors for adjusting V0 voltage level
– INTRS = "H": use the internal resistors.
– INTRS = "L": use the external resistors
VR pin and external resistive divider control V0 voltage</td></tr>
<tr><td colspan="3">Microprocessor Interface</td></tr>
<tr><td>Name</td><td>I/O</td><td>Description</td></tr>
<tr><td>/RESET</td><td>I</td><td>Reset input pin
When /RESET is “L”, initialization is executed.</td></tr>
<tr><td>PS</td><td>I</td><td>Parallel / Serial select input pin.
<table>
<tr><th>PS</th><th>Interface mode</th><th>Chip Select</th><th>Data/ Instruction</th><th>Data</th><th>Read/ Write</th><th>Serial</th></tr>
<tr><td>H</td><td>Parallel</td><td>/CS</td><td>RS</td><td>DB7 to DB0</td><td>E_/RD, RW_/WR</td><td>-</td></tr>
<tr><td>L</td><td>Serial</td><td>/CS</td><td>RS</td><td>DB7 (SID)</td><td>Write only</td><td>DB6 (SCLK)</td></tr>
</table>
*Note: In serial mode, it is impossible to read data from the on-chip RAM. And DB0 to DB5 are high impedance and E_/RD and RW_/WR must be fixed to either “H” or “L”.</td></tr>
<tr><td>C68</td><td>I</td><td>Microprocessor interface select input pin
– PS = “H”, C68 = "H": 6800-series parallel MPU interface
– PS = “H”, C68 = "L": 8080-series parallel MPU interface
– PS = “L”, C68 = "H": 4 pin-SPI MPU interface
– PS = “L”, C68 = "L": No operation (Don’t use)</td></tr>
<tr><td>/CS</td><td>I</td><td>Chip select input pins
Data/instruction I/O is enabled only when /CS is "L". When chip select is non-active, DB0 to DB7 may be high impedance.</td></tr>
<tr><td>RS</td><td>I</td><td>Register select input pin.
RS = “H”: The data on DB7 to DB0 is used the display data.
RS = “L”: The data on DB7 to DB0 is used the control data.</td></tr>
<tr><td>RW_/WR</td><td>I</td><td>Read / Write execution control pin
<table>
<tr><th>C68</th><th>MPU type</th><th>RW_/WR</th><th>Description</th></tr>
<tr><td>H</td><td>6800-series</td><td>RW</td><td>Read / Write control input pin
– RW = “H” : read
– RW = “L” : write</td></tr>
<tr><td>L</td><td>8080-series</td><td>/WR</td><td>Write enable clock input pin
The data on DB0 to DB7 are latched at the rising edge of the /WR signal.</td></tr>
</table></td></tr>
</table>

Table 6-1. Pin description (continued)

<table>
<tr><th colspan="3">Microprocessor interface (continued)</th></tr>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>E_/RD</td><td>I</td><td>Read / Write execution control pin
<table>
<tr><th>C68</th><th>MPU Type</th><th>E_/RD</th><th>Description</th></tr>
<tr><td>H</td><td>6800-series</td><td>E</td><td>Read / Write control input pin
– RW = “ H” : When E is “ H” , DB0 to DB7 are in an output status.
– RW = “ L” : The data on DB0 to DB7 are latched at the falling edge of the E signal.</td></tr>
<tr><td>L</td><td>8080-series</td><td>/RD</td><td>Read enable clock input pin
When /RD is “ L” , DB0 to DB7 are in an output status.</td></tr>
</table></td></tr>
<tr><td>DB0
to
DB7</td><td>I/O</td><td>8-bit bi-directional data bus that is connected to the standard 8-bit microprocessor data bus. When the serial interface selected (PS = "L");
– DB0 to DB5: high impedance
– DB6: serial input clock (SCLK)
– DB7: serial input data (SID)
When chip select is not active, DB0 to DB7 may be high impedance.</td></tr>
<tr><td>TESTCK

TEST20
to
TEST0</td><td>O</td><td>Test pins
Don’ t use this pin, open this pin</td></tr>
</table>

Table 6-1. Pin description (continued)

<table>
<tr><th colspan="3">LCD driver output</th></tr>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>SEG0
to
SEG127</td><td>O</td><td>LCD driver output for segment.
The display data and the M signal control the output voltage of segment driver.
<table>
<tr><th rowspan="2">Display data</th><th rowspan="2">M (Internal)</th><th colspan="2">Segment driver output voltage</th></tr>
<tr><th>Normal Display</th><th>Reverse Display</th></tr>
<tr><td>H</td><td>H</td><td>V0</td><td>V2</td></tr>
<tr><td>H</td><td>L</td><td>VSS</td><td>V3</td></tr>
<tr><td>L</td><td>H</td><td>V2</td><td>V0</td></tr>
<tr><td>L</td><td>L</td><td>V3</td><td>VSS</td></tr>
<tr><td colspan="2">Power save mode</td><td colspan="2">VSS</td></tr>
</table></td></tr>
<tr><td>COM0
to
COM127</td><td>O</td><td>LCD driver output for common.
The internal scanning data and M signal control the output voltage of common driver.
<table>
<tr><th>Scan data</th><th>M (Internal)</th><th>Common driver output voltage</th></tr>
<tr><td>H</td><td>H</td><td>VSS</td></tr>
<tr><td>H</td><td>L</td><td>V0</td></tr>
<tr><td>L</td><td>H</td><td>V1</td></tr>
<tr><td>L</td><td>L</td><td>V4</td></tr>
<tr><td colspan="2">Power save mode</td><td>VSS</td></tr>
</table></td></tr>
<tr><td>COMS</td><td>O</td><td>Common output for the icons
The output signals of two pins are same. When not used, these pins should be left open.</td></tr>
</table>

Note: DUMMY – These pins should be opened (floated).

7. FUNCTIONAL DESCRIPTION

7-1. MICROPROCESSOR INTERFACE

Chip select input

There is /CS pin for chip selection. The HM11S140 can interface with an MPU when /CS is "L".

When these pins are set to any other combination, RS, E_/RD, and RW_/WR inputs are disabled and DB0 to DB7 are to be high impedance.

And, in case of serial interface, the internal shift register and the counter are reset.

Parallel / Serial interface mode

HM11S140 has three types of interface with an MPU, which are one serial and two parallel interfaces.

This parallel or serial interface is determined by PS pin as shown in table 7-1.

Table 7-1. Parallel / Serial interface mode

PS	Type	C68	/CS	Interface mode
H	Parallel	H	/CS	6800-series MPU mode
		L		8080-series MPU mode
L	Serial	H	/CS	Serial MPU mode

Parallel interface (PS = "H")

The 8-bit bi-directional data bus is used in parallel interface and the type of MPU is selected by PS as shown in table 7-2.

The type of data transfer is determined by signals at RS, E_/RD and RW_/WR as shown in table 7-3.

Table 7-2. Microprocessor selection for parallel interface

C68	/CS	RS	E_/RD	RW_/WR	DB7 to DB0	MPU bus
H	/CS	RS	E	RW	DB7 to DB0	6800-series
L	/CS	RS	/RD	/WR	DB7 to DB0	8080-series

Table 7-3. Parallel data transfer

Common	6800-series		8080-series		Description
RS	E_/RD (E)	RW_/WR (RW)	E_/RD (/RD)	RW_/WR (/WR)	
H	H	H	L	H	Display data read out
H	H	L	H	L	Display data write
L	H	H	L	H	Register status read
L	H	L	H	L	Writes to internal register(instruction)

Note: When E_/RD pin is always pulled high for 6800-series interface, it can be used /CS for enable signal. In this case, interface data is latched at the rising edge of /CS and the type of data transfer is determined by signals at RS, RW_/WR as in case of 6800-series mode.

Serial interface (PS = "L" , C68 = "H")

When the HM11S140 is active and serial interface has been selected, the serial data (DB7) and the serial clock (DB6) inputs are enabled.

And HM11S140 is not active, the internal 8-bit shift register and the 3-bit counter are reset.

The serial data can be read on the rising edge of the serial clock going into DB6 and processed as 8-bit parallel data on the eighth serial clock.

The serial data input is display data when RS is high and control data when RS is low.

Reading is not possible while serial interface mode is activated.

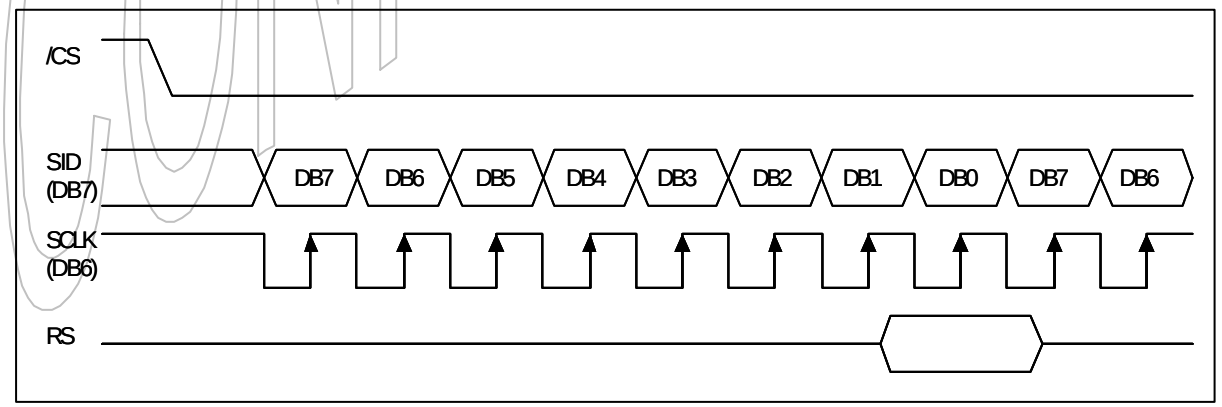

Figure 7-1. Serial interface timing

Busy flag

The busy flag indicates whether the HM11S140 is operating or not.

When DB7 is "H" in read status operation, this device is in busy status and will accept only read status instruction. If the cycle time is correct, the MPU needs not to check this flag before each instruction, which improves the MPU performance.

Data accessing

The HM11S140 uses bus holder and internal data bus for data read and data write with the MPU.

When writing data from the MPU to on-chip RAM, data is automatically transferred from the bus holder to the RAM as shown in figure 7-3. And when reading data from on-chip RAM to the MPU, the data for the initial read cycle is stored in the bus holder (dummy read) and the MPU reads this stored data from bus holder for the next data read cycle as shown in figure 7-4. This means that a dummy read cycle must be inserted between each pair of address sets when a sequence of address sets is executed. Therefore, the data of the specified address cannot be output with the read display data instruction right after the address sets, but can be output at the second read of data.

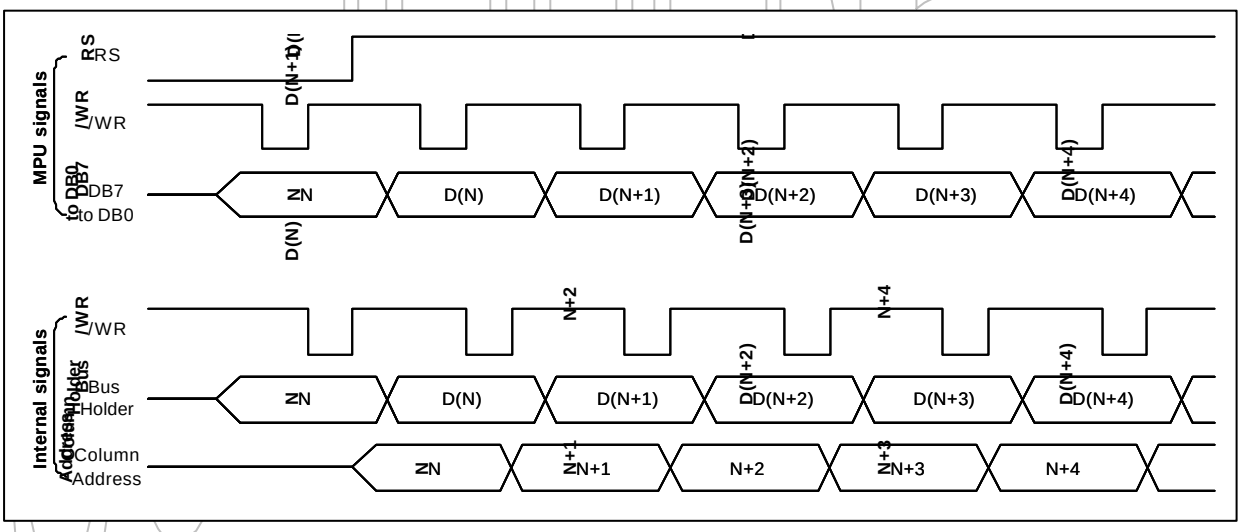

Figure 7-3. Write timing

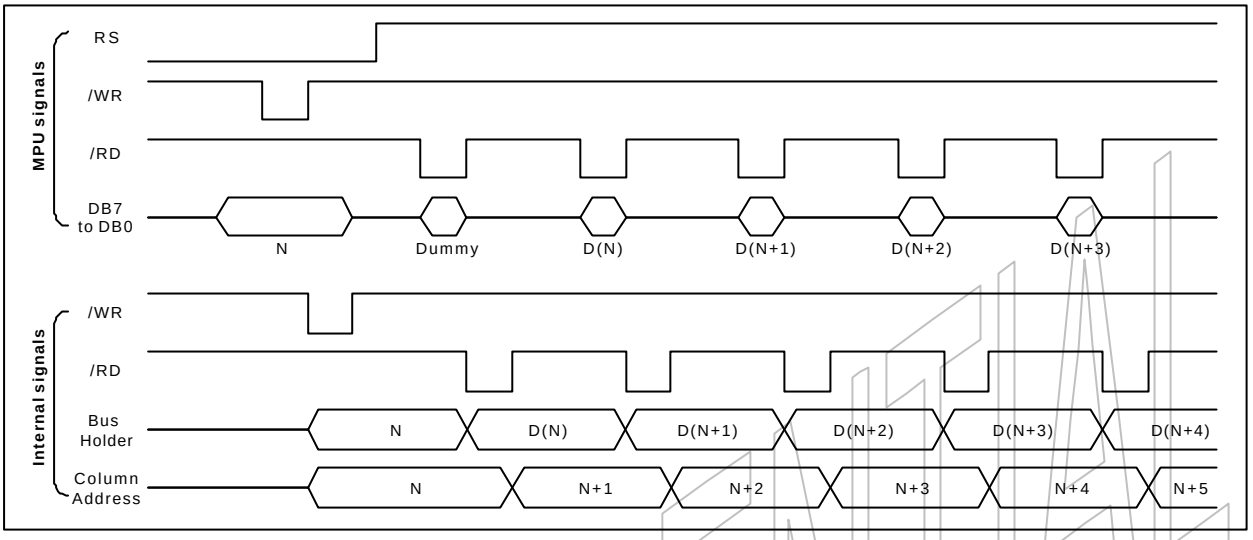

Figure 7-4. Read timing

7-2. DISPLAY DATA RAM (DDRAM)

The Display Data RAM stores pixel data for the LCD.

It is 129-row (17 page by 8 bits) by 128-column addressable array.

Each pixel can be selected when the page and column addresses are specified.

The 129 rows are divided into 16 pages of 8 lines and the 17th page with a single line (DB0 only).

Data is read from or written to the 8 lines of each page directly through DB0 to DB7.

The display data of DB0 to DB7 from the microprocessor correspond to the LCD common lines.

The microprocessor can read from and write to RAM through the I/O buffer.

Since the LCD controller operates independently, data can be written into RAM at the same time as data is being displayed without causing the LCD flicker.

Page address circuit

This circuit is for providing a Page Address to Display Data RAM shown in figure 7-6. It incorporates 4-bit Page Address register changed by only the " Set Page" instruction. Page Address 16 is a special RAM area for the icons and display data DB0 is only valid.

Line address circuit

This circuit assigns DDRAM a Line Address corresponding to the first line (COM0) of the display. Therefore, by setting Line Address repeatedly, it is possible to realize the screen scrolling and page switching without changing the contents of on-chip RAM as shown in figure 7-6. It incorporates 7-bit Line Address register changed by only the initial display line instruction and 7-bit counter circuit. At the beginning of each LCD frame, the contents of register are copied to the line counter which is increased by CL signal and generates the line address for transferring the 128-bit RAM data to the display data latch circuit. When icon is enabled by setting icon control register, display data of icons are not scrolled because the MPU can not access Line Address of icons.

Column address circuit

Column Address Circuit has a 8-bit preset counter that provides Column Address to the Display Data RAM as shown in figure 7-6.

When set Column Address MSB / LSB instruction is issued, 7-bit [Y7:Y1] are set and lowest bit, Y0 is set to "0". Since this address is increased by 1 each a read or write data instruction, microprocessor can access the display data continuously. The increment of the column address stops with 7FH

And, the counter is not increased and locked if a non-existing address above 80H.

It is unlocked if a column address is set again by set Column Address MSB / LSB instruction.

And the column address counter is independent of page address register.

ADC select instruction makes it possible to invert the relationship between the Column Address and the segment outputs.

It is necessary to rewrite the display data on built-in RAM after issuing ADC select instruction.

Refer to the following figure 7-5.

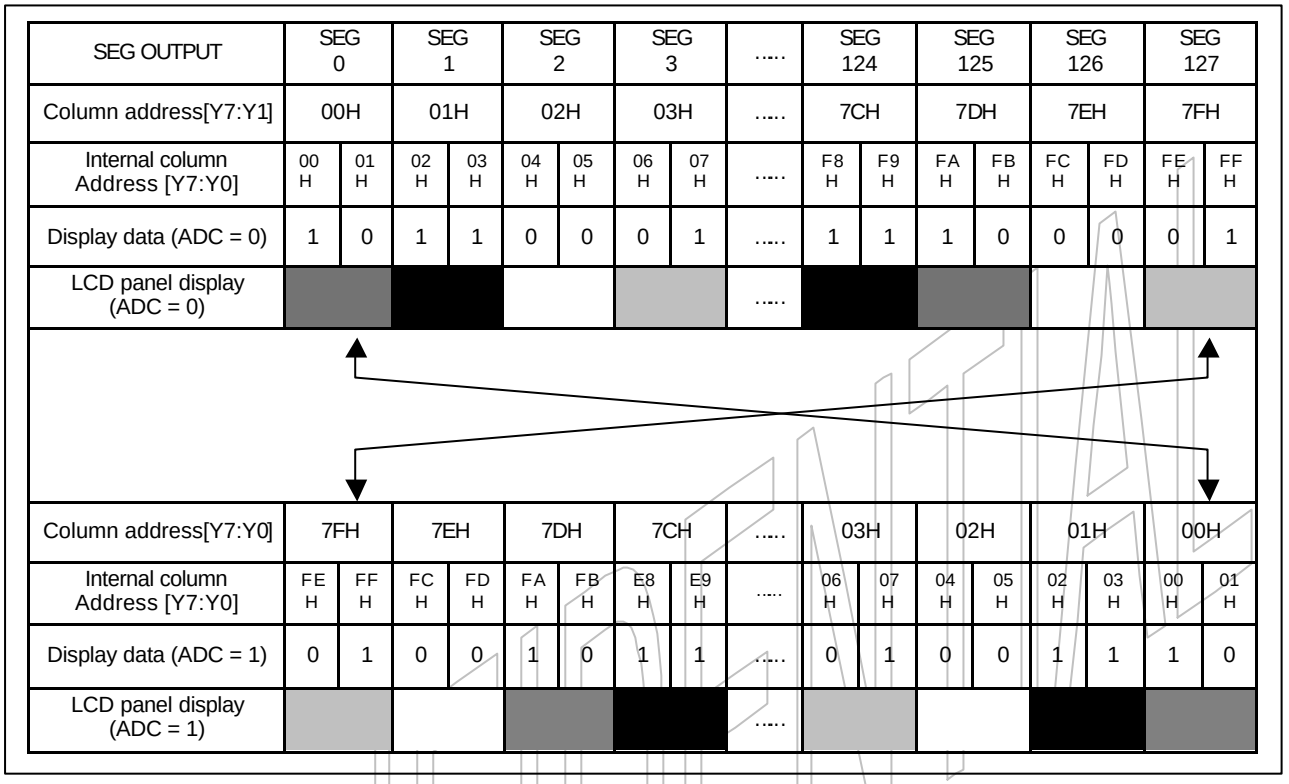

Figure 7-5. The relationship between the column address and the segment outputs

Segment control circuit

This circuit controls the display data by the display ON / OFF, reverse display ON / OFF and entire display ON / OFF instructions without changing the data in the display data RAM.

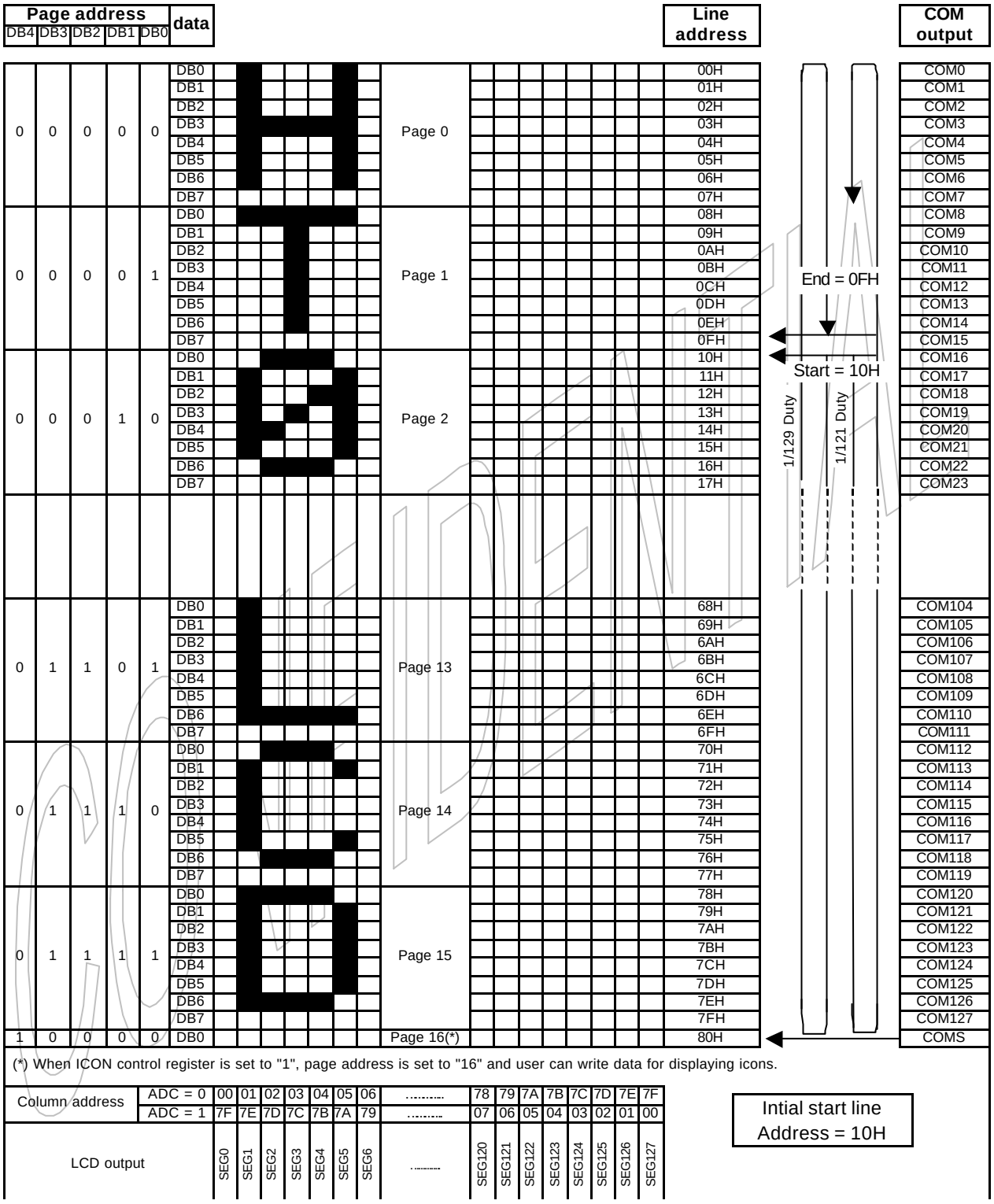

Figure 7-6. Display data RAM map

7-3. LCD DISPLAY CIRCUITS

FRC (frame rate control) and PWM (Pulse width modulation) function circuit

The HM11S140 incorporates an FRC function and a PWM function circuit to display a 4-level gray scale. The FRC function and PWM utilize liquid crystal characteristics whose transmittance is changed by an effective value of applied voltage. The HM11S140 provides four 4-bit palette-registers to assign the desired gray level. These registers are set by the instructions and the /RESET.

– **Gray scale table of 4 FRC (Frame rate control)**

Gray Scale Level	MSB (DB7 to DB4)	LSB (DB3 to DB0)
White	2nd FR (FR2)	1st FR (FR1)
	4th FR (FR4)	3rd FR (FR3)
Light gray	2nd FR (FR2)	1st FR (FR1)
	4th FR (FR4)	3rd FR (FR3)
Dark gray	2nd FR (FR2)	1st FR (FR1)
	4th FR (FR4)	3rd FR (FR3)
Black	2nd FR (FR2)	1st FR (FR1)
	4th FR (FR4)	3rd FR (FR3)

– **Gray scale table of 3 FRC (Frame rate control)**

Gray Scale Level	MSB (DB7 to DB4)	LSB (DB3 to DB0)
White	2nd FR (FR2)	1st FR (FR1)
	x x x x	3rd FR (FR3)
Light gray	2nd FR (FR2)	1st FR (FR1)
	x x x x	3rd FR (FR3)
Dark gray	2nd FR (FR2)	1st FR (FR1)
	x x x x	3rd FR (FR3)
Black	2nd FR (FR2)	1st FR (FR1)
	x x x x	3rd FR (FR3)

- **Gray scale table of 15 PWM (Pulse width modulation)**

Dec	Hex	4-bits	PWM (on width)	Note
0	00	0000	0 (0/15)	Brighter
1	01	0001	1/15	
2	02	0010	2/15	
3	03	0011	3/15	
4	04	0100	4/15	
5	05	0101	5/15	
6	06	0110	6/15	
7	07	0111	7/15	
8	08	1000	8/15	
9	09	1001	9/15	
10	0A	1010	10/15	
11	0B	1011	11/15	
12	0C	1100	12/15	
13	0D	1101	13/15	
14	0E	1110	14/15	
15	0F	1111	1 (15/15)	Darker

- **Gray scale table of 12 PWM (Pulse width modulation)**

Dec	Hex	4-bits	PWM (on width)	Note
0	00	0000	0 (0/12)	Brighter
1	01	0001	1/12	
2	02	0010	2/12	
3	03	0011	3/12	
4	04	0100	4/12	
5	05	0101	5/12	
6	06	0110	6/12	
7	07	0111	7/12	
8	08	1000	8/12	
9	09	1001	9/12	
10	0A	1010	10/12	
11	0B	1011	11/12	
12	0C	1100	1 (12/12)	Darker
13	0D	1101	0/12	This area is selected to OFF level (0/12 level)
14	0E	1110	0/12	
15	0F	1111	0/12	

- **Gray scale table of 9 PWM (Pulse width modulation)**

Dec	Hex	4-bits	PWM (on width)	Note
0	00	0000	0 (0/9)	Brighter
1	01	0001	1/9	
2	02	0010	2/9	
3	03	0011	3/9	
4	04	0100	4/9	
5	05	0101	5/9	
6	06	0110	6/9	
7	07	0111	7/9	
8	08	1000	8/9	
9	09	1001	1 (9/9)	Darker
10	0A	1010	0/9	This area is selected to OFF level (0/9 level)
11	0B	1011	0/9	
12	0C	1100	0/9	
13	0D	1101	0/9	
14	0E	1110	0/9	
15	0F	1111	0/9	

Oscillator

This is on-chip Oscillator with external resistor.

Its frequency is controlled by external resistor between OSC1 and VDD.

This oscillator signal is used in the voltage converter and display timing generation circuit.

Display timing generator circuit

This circuit generates some signals to be used for displaying LCD.

The display clock, CL(internal), generated by oscillation clock, generates the clock for the line counter and the signal for the display data latch.

The line address of on-chip RAM is generated in synchronization with the display clock and the display data latch circuit latches the 128-bit display data in synchronization with the display clock.

The display data, which is read to the LCD driver, is completely independent of the access to the display data RAM from the microprocessor.

The display clock generates an LCD AC signal (M) which enables the LCD driver to make a AC drive waveform, and also generates an internal common timing signal and start signal to the common driver.

The frame signal or the line signal changes the M by setting internal instruction. Driving waveform and internal timing signal are shown in Figure 7-7.

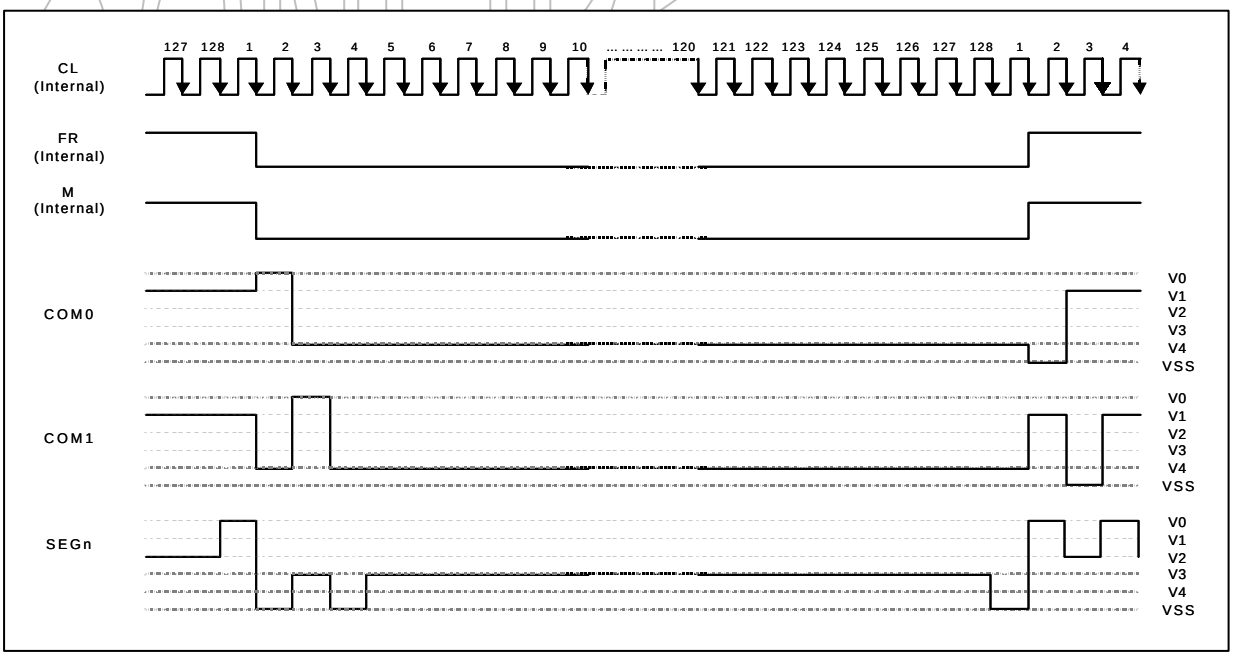

Figure 7-7. 2-Frame AC driving waveform (Duty ratio = 1/128)

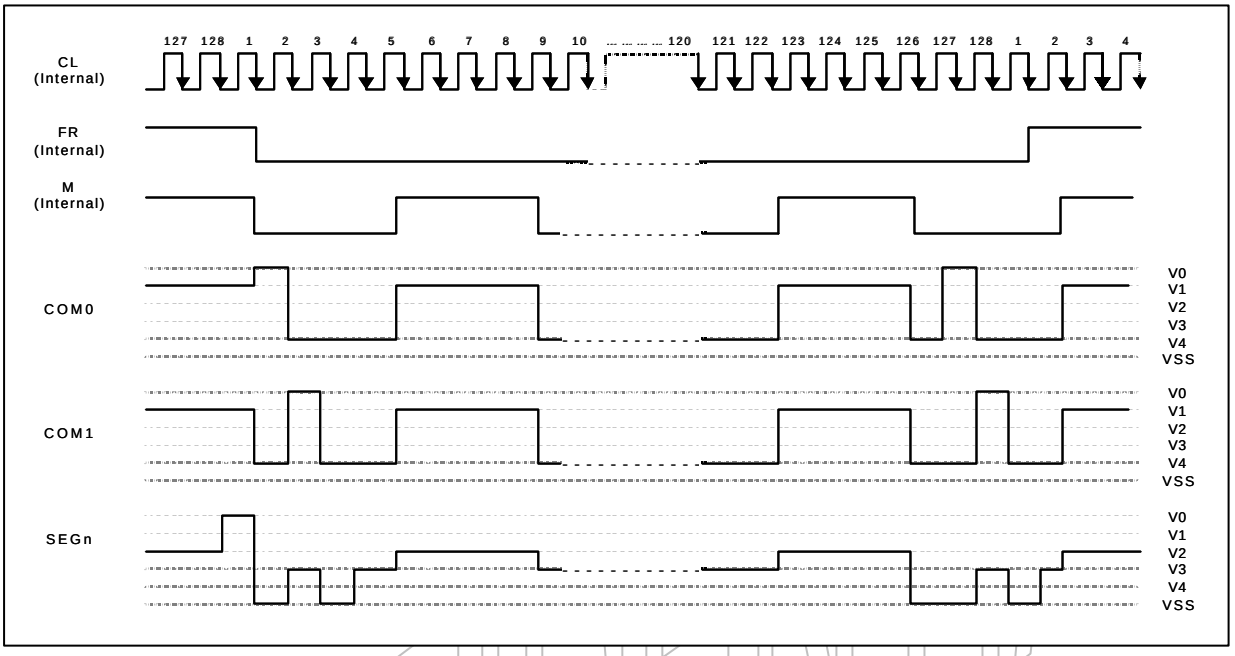

Figure 7-8. N-Line inversion driving waveform (N = 5, Duty ratio = 1/128)

7-4. LCD DRIVER CIRCUIT

This driver circuit is configured by 129-channel common drivers and 128-channel segment drivers.

This LCD panel driver voltage depends on the combination of display data and M signal.

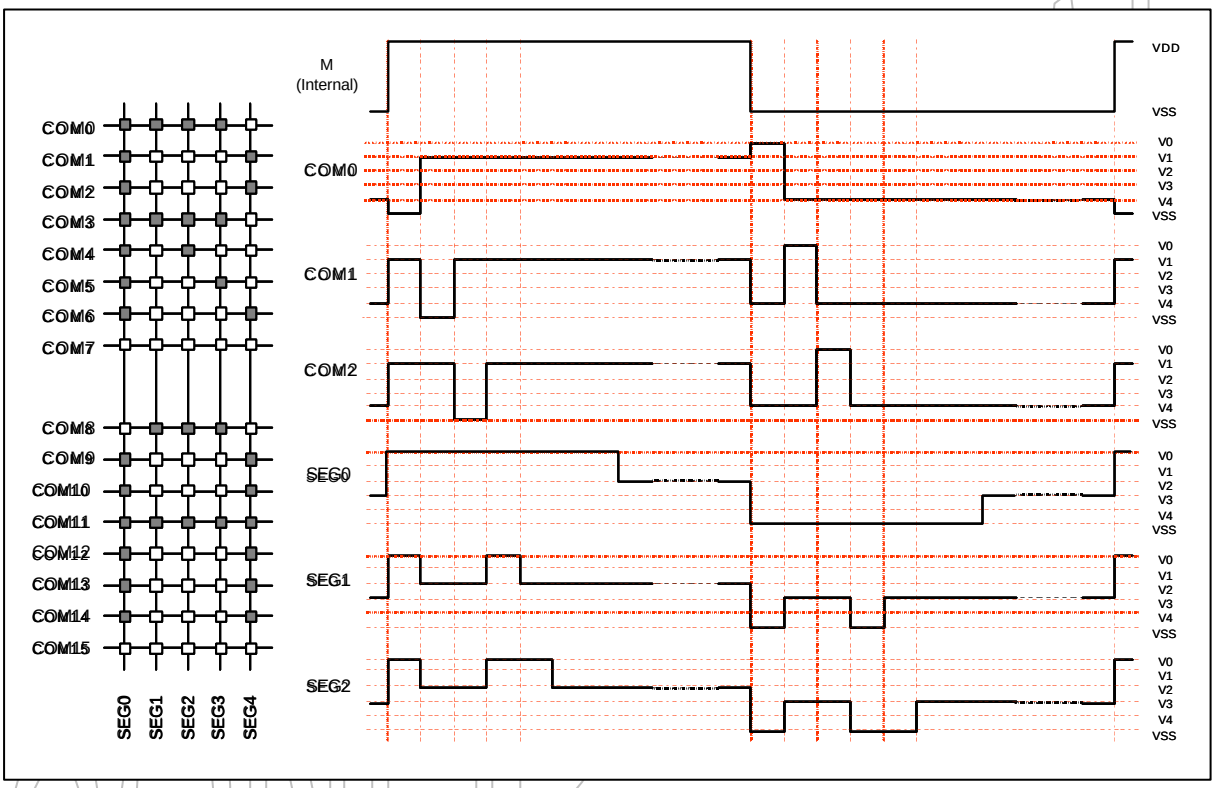

Figure 7-9. Segment and common timing

Partial display on LCD

The HM11S140 realizes the Partial Display function on LCD with low-duty driving for saving power consumption and showing the various display duty.

To show the various display duty on LCD, LCD driving duty and bias are programmable via the instruction.

And, built-in power supply circuits are controlled by the instruction for adjusting the LCD driving voltages

7-5. POWER SUPPLY CIRCUITS

The Power Supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low power consumption and the fewest components.

There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits.

They are controlled by power control instruction.

For details, refers to "Instruction Description". Table 7-4 shows the referenced combinations in using Power Supply circuits.

Table 7-4. Recommended power supply combinations

User setup	Power Control (VC VR VF)	Voltage converter	Voltage regulator	Voltage follower	VOUT	V0	V1 to V4
Only the internal power supply circuits are used	1, 1, 1	ON	ON	ON	Open	Open	Open
Only the voltage regulator circuits and voltage follower circuits are used	0, 1, 1	OFF	ON	ON	External input	Open	Open
Only the voltage follower circuits are used	0 , 0, 1	OFF	OFF	ON	Open	External input	Open
Only the external power supply circuits are used	0, 0, 0	OFF	OFF	OFF	Open	External input	External input

Voltage converter circuits

These circuits boost up the electric potential between VCI and Vss to 3, 4, 5 or 6 times toward positive side and boosted voltage is outputted from VOUT pin.

It is possible to select the lower boosting level in any boosting circuit by "Set DC-DC Step-up" instruction. When the higher level is selected by instruction, VOUT voltage is not valid.

(C1 = 1.0 to 4.7μF)

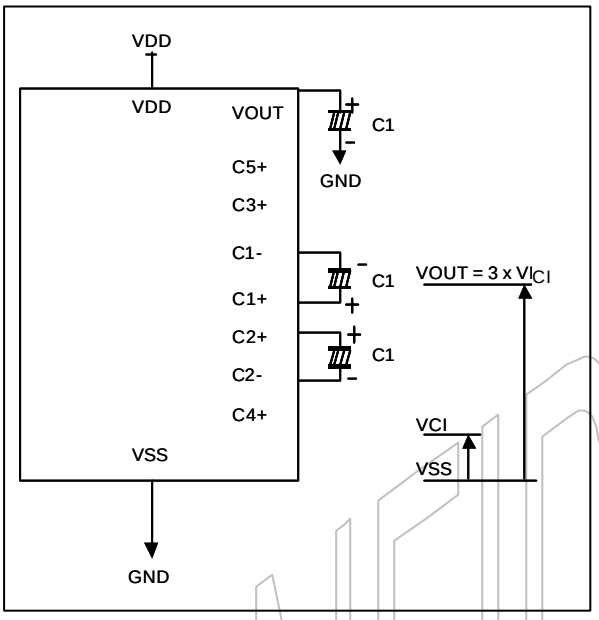

Figure 7-13. Three times boosting circuit

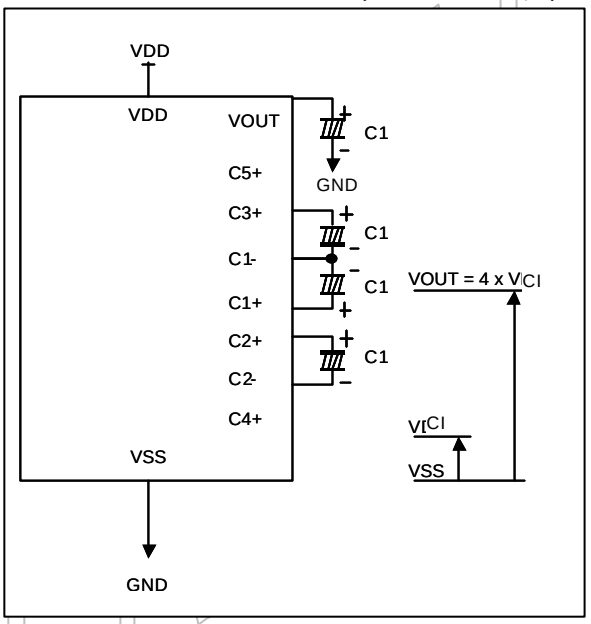

Figure 7-14. Four times boosting circuit

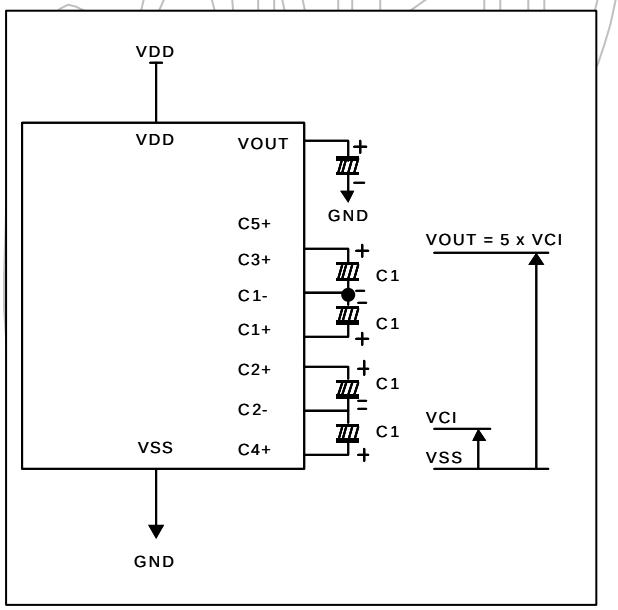

Figure 7-15. Five times boosting circuit

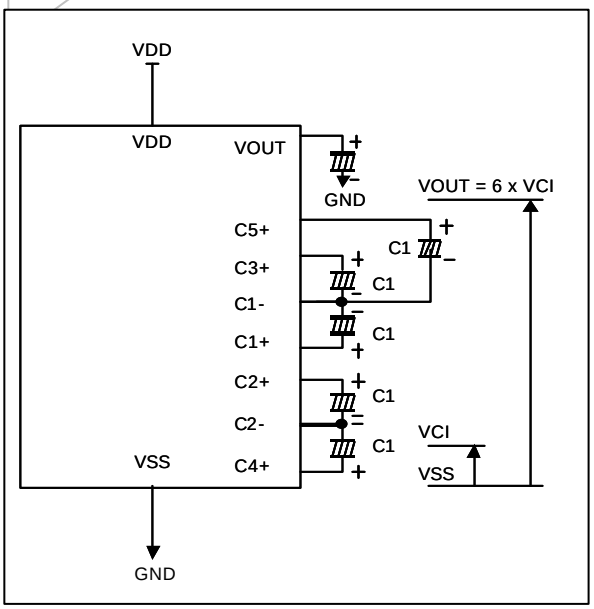

Figure 7-16. Six times boosting circuit

*. The voltage converter input voltage range must be set so that the VOUT voltage does not exceed the absolute maximum rated value

Voltage regulator circuits

The function of the internal Voltage Regulator circuits is to determine liquid crystal operating voltage, V0, by adjusting resistors, Ra and Rb, within the range of |V0| < |VOUT|.

Because VOUT is the operating voltage of operational-amplifier circuits shown in figure 7-17, it is necessary to be applied internally or externally.

For the Equation. 1, we determine V0 by Ra, Rb and V_{EV}. The Ra and Rb are connected internally or externally by INTRS pin.

And V_{EV} called the voltage of electronic volume is determined by Equation. 2, where the parameter α is the value selected by instruction, "Set Reference Voltage Register", within the range 0 to 63. VREF voltage at Ta= 25°C is shown in Table 7-5.

$$V0 = \left(1 + \frac{Rb}{Ra}\right) \times V_{EV} \quad [V] \quad \text{------ (Equation 1)}$$

$$V_{EV} = \left(1 - \frac{(63-\alpha)}{210}\right) \times VREF \quad [V] \quad \text{------ (Equation 2)}$$

Table 7-5. VREF Voltage at Ta = 25 °C

REF	Temp. coefficient	VREF [V]
1	-0.1% / °C	2.1
0	External input	VEXT

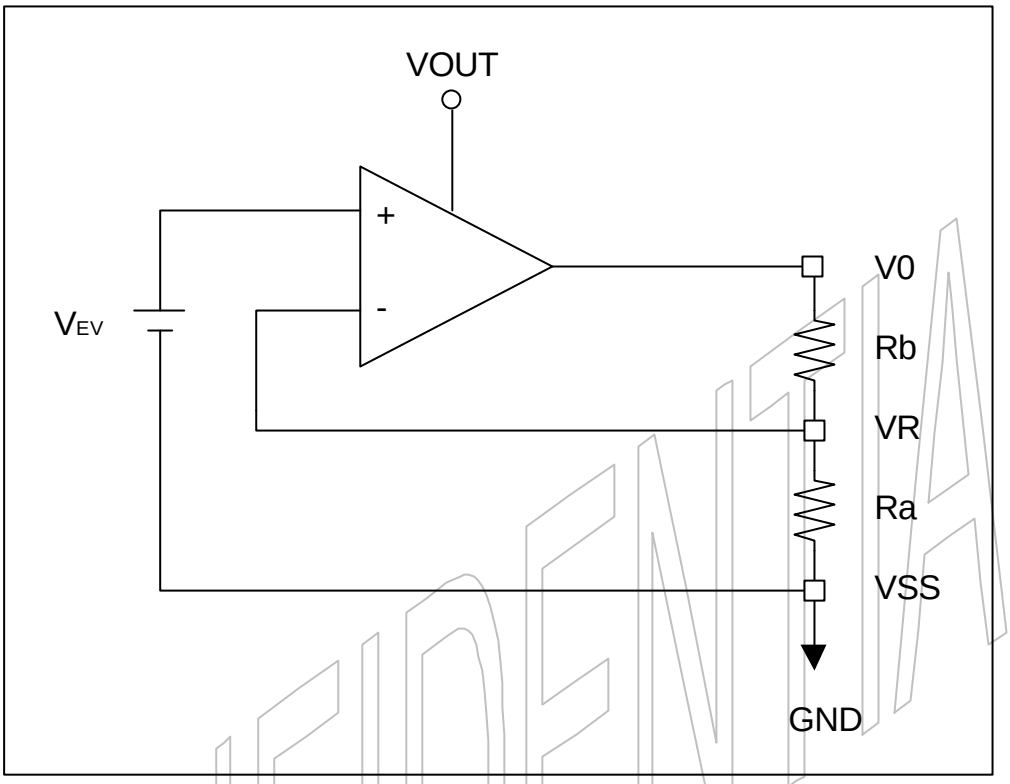

Figure 7-17. Internal voltage regulator circuit

In case of using internal resistors, Ra and Rb (INTRS = "H")

When INTRS pin is "**H**", resistor Ra is connected internally between VR pin and VSS, and Rb is connected between V0 and VR.

We determine V0 by two instructions, "Regulator Resistor Select" and "Set Reference Voltage".

Table 7-6. Internal Rb / Ra Ratio depending on 3-bit data (R2, R1, R0)

	3-bit data settings (R2 R1 R0)							
	000	**001**	**010**	**011**	**100**	**101**	**110**	**111**
1+(Rb / Ra)	2.3	3.0	3.7	4.4	5.1	5.8	6.5	7.2

Figure 7-18 Shows V0 voltage measured by adjusting internal regulator register ratio (Rb / Ra) and 6-bit electronic volume registers for each temperature coefficient at Ta = 25 °C.

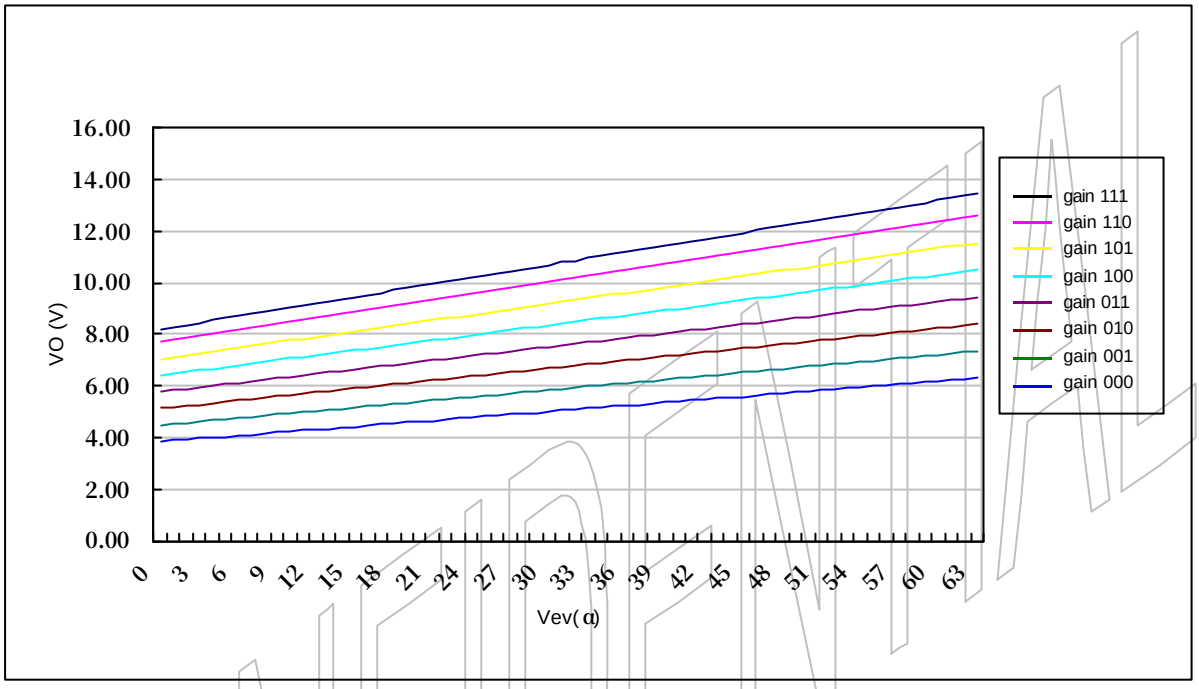

Figure 7-18. Electronic volume level (Temp. Coefficient = -0.1% / °C)

*. The voltage regulator operating voltage range (1+Rb/Ra and α) must be set so that the V0 voltage does not exceed the absolute maximum rated value

In case of using external resistors, Ra and Rb. (INTRS = "L")

When INTRS pin is " L", it is necessary to connect external regulator resistor Ra between VR and VSS, and Rb between V0 and VR.

Example: For the following requirements

1. LCD driver voltage, V0 = 10V
2. 6-bit reference voltage register = (1, 0, 0, 0, 0, 0, α = 32)
3. Maximum current flowing Ra, Rb = 1[μA]

From equation 1

$$10 = \left(1 + \frac{Rb}{Ra} \right) \times V_{EV} \quad [V] \quad \text{------} \quad \text{(Equation 3)}$$

From equation 2

$$V_{EV} = \left(1 - \frac{(63-32)}{210} \right) \times 2.1 = 1.79 \quad [V] \text{ ------ (Equation 4)}$$

From equation 3

$$\frac{10}{(Ra + Rb)} = 1[\mu A] \quad \text{------ (Equation 5)}$$

From equation 3,4 and 5

Ra = 1.79 [MΩ]

Rb = 8.21 [MΩ]

Table 7-7 Shows the range of V0 depending on the above requirements.

Table 7-7. The range of V0

	Electric Volume Level						
	0	**1**	**------**	**32**	**-------**	**62**	**63**
V0	8.21	8.27	------	10.00	------	11.68	11.73

Voltage follower circuits

VLCD voltage (V0) is resistively divided into four voltage levels (V1, V2, V3 and V4), and those output impedance are converted by the Voltage Follower for increasing drive capability.

Table 7-8 shows the relationship between V1 to V4 level and each duty ratio.

Table 7-8. The relationship between V1 to V4 level and each duty ratio

LCD bias	V1	V2	V3	V4
1/N	(N-1)/N × V0	(N-2)/N × V0	2/N × V0	1/N × V0

* N = 5 to 12

7-6. REFERECE CIRCUIT EXAMPLS

(C1 = 1.0 to 4.7 [μF], C2 = 0.47 to 2.0 [μF])

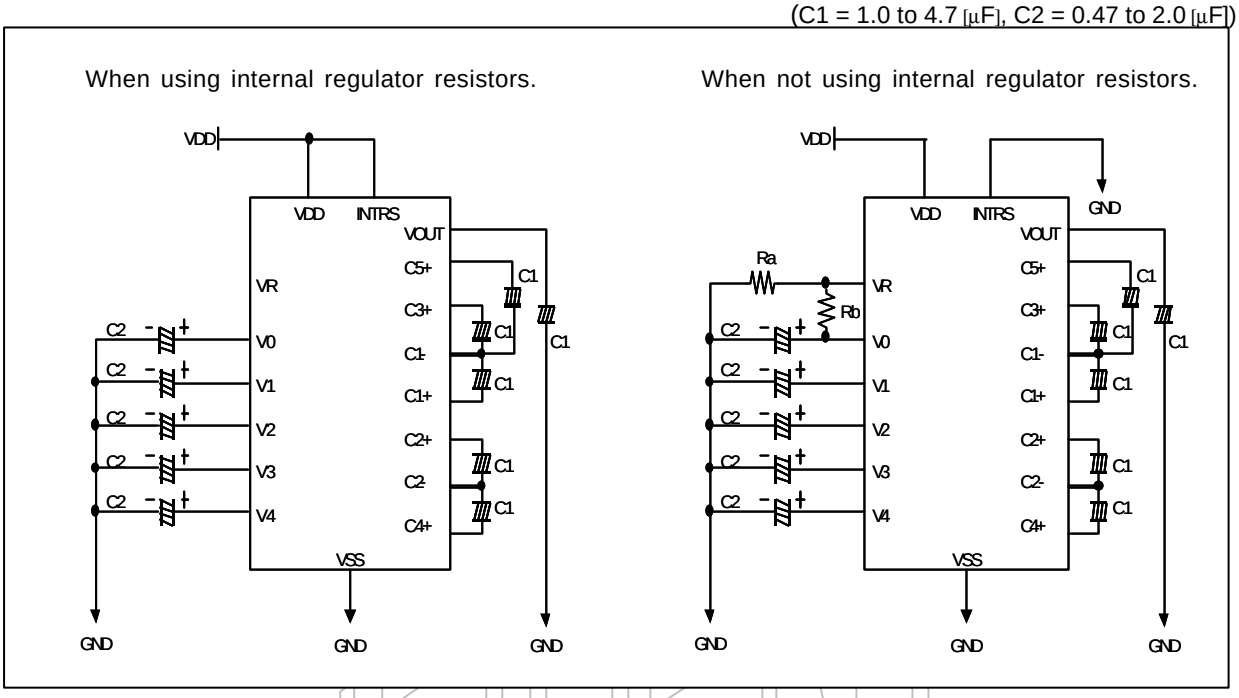

Figure 7-19. When using all LCD power circuits (6-Time V/C: ON, V/R: ON, V/F: ON)

(C2 = 0.47 to 2.0 [μF])

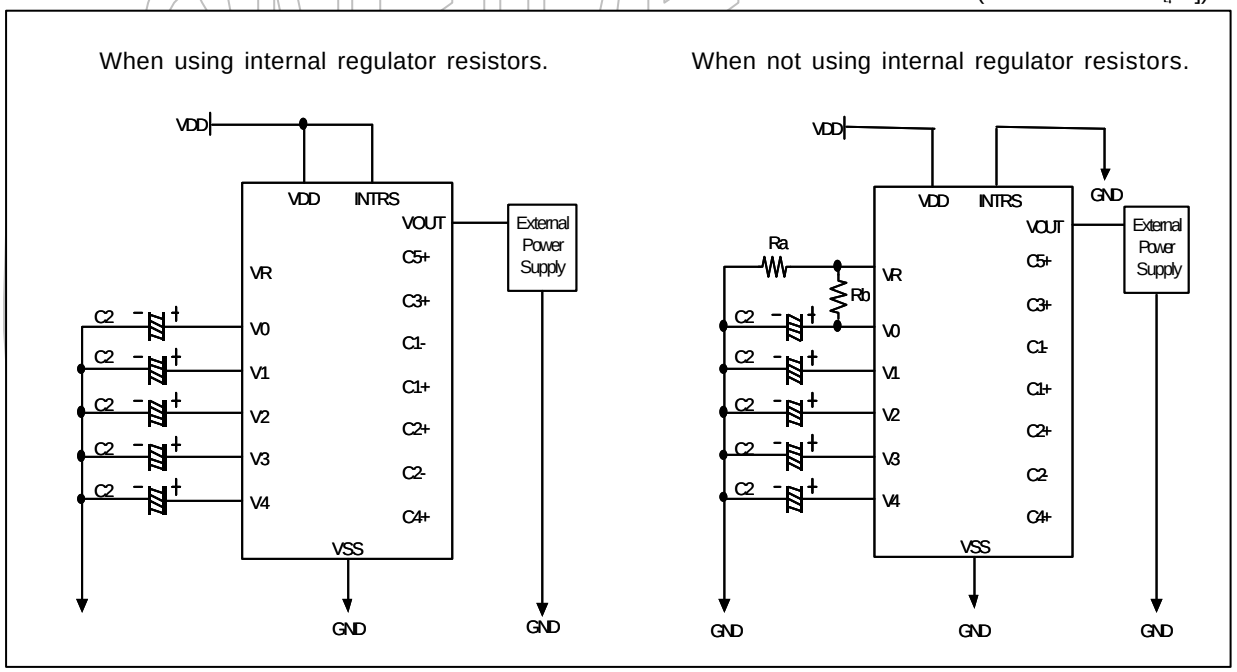

Figure 7-20. When using some LCD power circuits (V/C: OFF, V/R: ON, V/F: ON)

(C2 = 0.47 to 2.0 [μF])

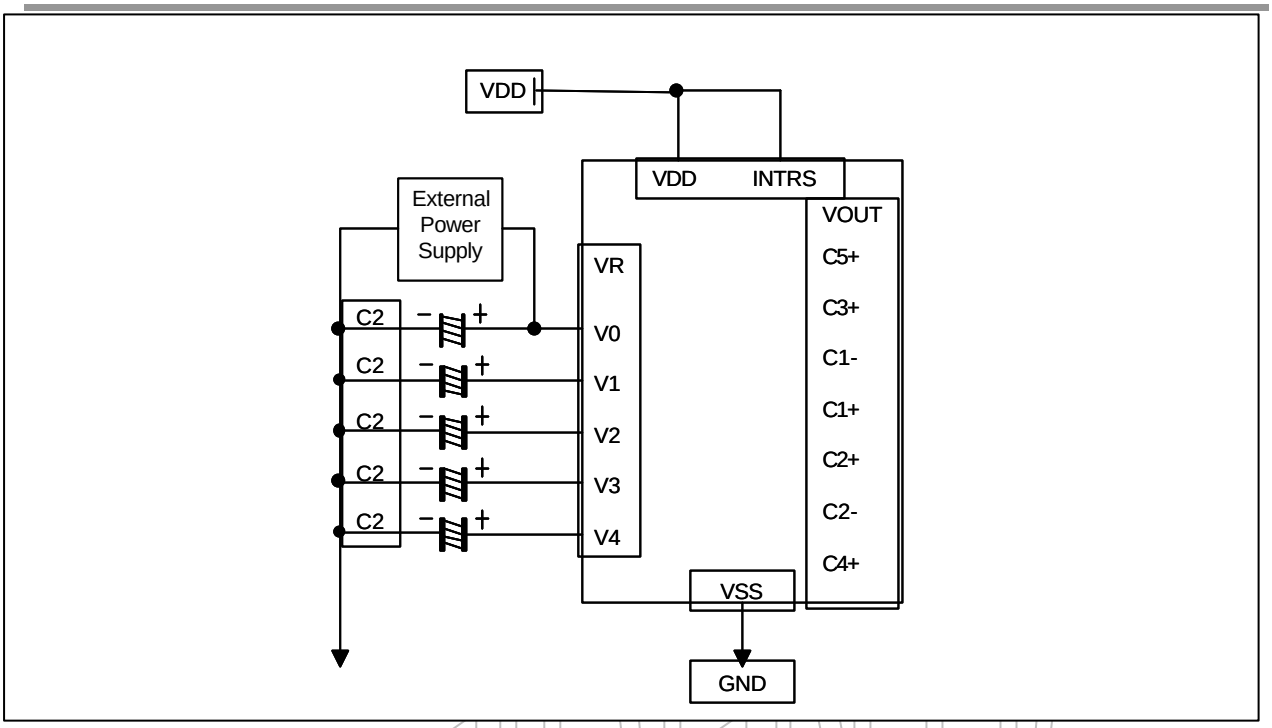

Figure 7-21. When using some LCD power circuits (V/C: OFF, V/R: OFF, V/F: ON)

(C2 = 0.47 to 2.0 [μF])

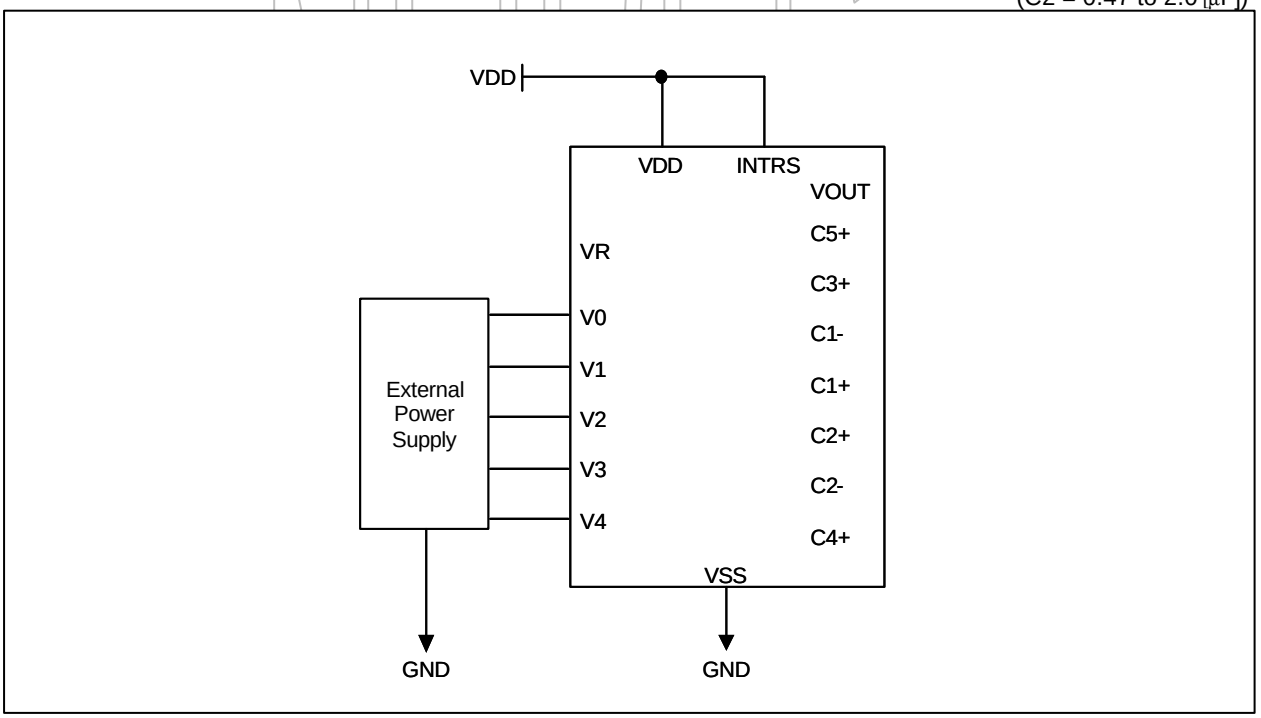

Figure 7-22. When not using any internal LCD power supply circuits (V/C: OFF, V/R: OFF, V/F: OFF)

7-7. RESET CIRCUIT

Setting /RESET to " L" or Reset instruction can initialize internal function.

When /RESET becomes " L" , following procedure is occurred.

- Page address: 0
- Column address: 0
- Read-modify-write: OFF
- Display ON / OFF: OFF
- Initial display line: 0 (first)
- Initial COM0 register: 0 (COM0)
- Partial display duty ratio: 1/128
- Reverse display ON / OFF: OFF (normal)
- N-line inversion register: 0 (disable)
- Entire display ON/OFF: OFF
- ICON control register ON/OFF: OFF (ICON disable)
- Power control register (VC, VR, VF) = (0, 0, 0)
- DC-DC converter circuit = (0, 0)
- Regulator resistor select register: (R2, R1, R0) = (0, 0, 0)
- Contrast Level: 32
- LCD bias ratio: 1/12
- COM scan direction: 0
- ADC select: 0
- Oscillator: OFF
- Power save mode: Release
- White mode set: OFF
- White palette register (WG3, WG2, WG1, WG0) = (0, 0, 0, 0)
- Light gray mode set: OFF
- Light gray palette register (LG3, LG2, LG1, LG0) = (0, 0, 0, 0)
- Dark gray mode set: OFF
- Dark gray palette register (DG3, DG2, DG1, DG0) = (1, 1, 1, 1)
- Black mode set: OFF
- Black palette register (BG3, BG2, BG1, BG0) = (1, 1, 1, 1)
- FRC, PWM mode: 4FRC, 9PWM

When RESET instruction is issued, following procedure is occurred.

Page address: 0

Column address: 0

Read-modify-write: OFF

Initial display line: 0 (First)

Regulator resistor select register: (R2, R1, R0) = (0, 0, 0)

Contrast level: 32

White mode set: OFF

White palette register (WG3, WG2, WG1, WG0) = (0, 0, 0, 0)

Light gray mode set: OFF

Light gray palette register (LG3, LG2, LG1, LG0) = (0, 0, 0, 0)

Dark gray mode set: OFF

Dark gray palette register (DG3, DG2, DG1, DG0) = (1, 1, 1, 1)

Black mode set: OFF

Black palette register (BG3, BG2, BG1, BG0) = (1, 1, 1, 1)

FRC, PWM mode: 4FRC, 9PWM

While /RESET is " L" or reset instruction is executed, no instruction except read status can be accepted. Reset status appears at DB4.

After DB4 becomes " L" , any instruction can be accepted. /RESET must be connected to the reset pin of the MPU, and initialize the MPU and this LSI at the same time.

The initialization by /RESET is essential before used.

8. INSTRUCTION DESCRIPTION

Table 8-1. Instruction table

x : Don't care

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
Read display data	1	1	Read data								Read data from DDRAM
Write display data	1	0	Write data								Write data into DDRAM
Read status	0	1	BUSY	DISP	RES	0	0	0	1	0	Read the internal status
ICON control register ON / OFF	0	0	1	0	1	0	0	0	1	ICON	ICON = 0: ICON disable (default) ICON=1:ICON enable & set the page address to 16
Set page adress	0	0	1	0	1	1	P3	P2	P1	P0	Set page address
Set column address MSB / LSB	0	0	0	0	0	1	0	Y7	Y6	Y5	Set column address MSB
	0	0	0	0	0	0	Y4	Y3	Y2	Y1	Set column address LSB
Set modify-read	0	0	1	1	1	0	0	0	0	0	Set modify-read mode
Reset modify-read	0	0	1	1	1	0	1	1	1	0	Reset modify-read mode
Display ON/OFF	0	0	1	0	1	0	1	1	1	D	D=0: display OFF D=1: display ON
Set initial display line register	0	0	0	1	0	0	0	0	X	X	2-byte instruction to specify the initial display line to realize vertical scrolling
	0	0	X	S6	S5	S4	S3	S2	S1	S0	
Set initial COM0 register	0	0	0	1	0	0	0	1	X	X	2-byte instruction to specify the initial COM0 to realize window scrolling
	0	0	X	C6	C5	C4	C3	C2	C1	C0	
Set partial display duty ratio	0	0	0	1	0	0	1	0	X	X	2-byte instruction to set partial display duty ratio
	0	0	D7	D6	D5	D4	D3	D2	D1	D0	
Set N-line inversion	0	0	0	1	0	0	1	1	X	X	2-byte instruction to set N-line inversion register
	0	0	X	X	X	N4	N3	N2	N1	N0	
Release N-line inversion	0	0	1	1	1	0	0	1	0	0	Release N-line inversion mode
Reverse display ON/OFF	0	0	1	0	1	0	0	1	1	REV	REV=0: normal display, REV=1: reverse display
Entire display ON/OFF	0	0	1	0	1	0	0	1	0	EON	EON=0: normal display. EON=1: entire display ON
Power control	0	0	0	0	1	0	1	VC	VR	VF	Control power circuit operation
Select DC-DC step-up	0	0	0	1	1	0	0	1	DC1	DC0	Select the step-up of the internal voltage converter
Select regulator resistor	0	0	0	0	1	0	0	R2	R1	R0	Select internal resistance ratio of the regulator resistor
Set electronic volume register	0	0	1	0	0	0	0	0	0	1	2-byte instruction to specify the Reference voltage
	0	0	X	X	EV5	EV4	EV3	EV2	EV1	EV0	
Select LCD bias	0	0	0	1	0	1	0	B2	B1	B0	Select LCD bias
SHL select	0	0	1	1	0	0	SHL	X	X	X	COM bi-directional selection SHL = 0 : normal direction SHL = 1 : reverse direction

Table 8-1. Instruction table (Continued)

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
ADC select	0	0	1	0	1	0	0	0	0	ADC	SEG bi-directional selection ADC=0: normal direction ADC=1: reverse direction
Oscillator on start	0	0	1	0	1	0	1	0	1	1	Start the built-in oscillator
Set power save mode	0	0	1	0	1	0	1	0	0	PS	PS=0: normal mode PS=1: sleep mode
Release power save mode	0	0	1	1	1	0	0	0	0	1	Release power save mode
Reset	0	0	1	1	1	0	0	0	1	0	Initialize the internal functions
Set FRC and PWM mode	0	0	1	0	0	1	0	FRC	PWM 1	PWM 0	Set FRC and PWM mode
Set white mode and 1st /2nd frame, set pulse width	0	0	1	0	0	0	1	0	0	0	Set white mode and 1st /2nd frame
	0	0	WB3	WB2	WB1	WB0	WA3	WA2	WA1	WA0	
Set white mode and 3rd /4th frame, set pulse width	0	0	1	0	0	0	1	0	0	1	Set white mode and 3rd /4th frame
	0	0	WD3	WD2	WD1	WD0	WC	WC2	WC1	WC0	
Set light gray mode and 1st /2nd frame, set pulse width	0	0	1	0	0	0	1	0	1	0	Set light gray mode and 1st /2nd frame
	0	0	LB3	LB2	LB1	LB0	LA3	LA2	LA1	LA0	
Set light gray mode and 3rd /4th frame, set pulse width	0	0	1	0	0	0	1	0	1	1	Set light gray mode and 3rd /4th frame
	0	0	LD3	LD2	LD1	LD0	LC3	LC2	LC1	LC0	
Set dark gray mode and 1st /2nd frame, set pulse width	0	0	1	0	0	0	1	1	0	0	Set dark gray mode and 1st /2nd frame
	0	0	DB3	DB2	DB1	DB0	DA3	DA2	DA1	DA0	
Set dark gray mode and 3rd /4th frame, set pulse width	0	0	1	0	0	0	1	1	0	1	Set dark gray mode and 3rd /4th frame
	0	0	DD3	DD2	DD1	DD0	DC3	DC2	DC1	DC0	
Set black mode and 1st /2nd frame, set pulse width	0	0	1	0	0	0	1	1	1	0	Set black mode and 1st /2nd frame
	0	0	BB3	BB2	BB1	BB0	BA3	BA2	BA1	BA0	
Set black mode and 3rd /4th frame, set pulse width	0	0	1	0	0	0	1	1	1	1	Set black mode and 3rd /4th frame
	0	0	BD3	BD2	BD1	BD0	BC3	BC2	BC1	BC0	
NOP	0	0	1	1	1	0	0	0	1	1	No operation
Test instruction	0	0	1	1	1	1	X	X	X	X	Don' t use this instruction.

Read display data

8-bit data from Display Data RAM specified by the column address and page address can be read by this instruction. As the column address is increased by 1 automatically after each this instruction, the microprocessor can continuously read data from the addressed page.

A dummy read is required after loading an address into the column address register.

Display Data cannot be read through the serial interface.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	Read data							

Write display data

8-bit data of Display Data from the microprocessor can be written to the RAM location specified by the column address and page address.

The column address is increased by 1 automatically so that the microprocessor can continuously write data to the addressed page.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	Write data							

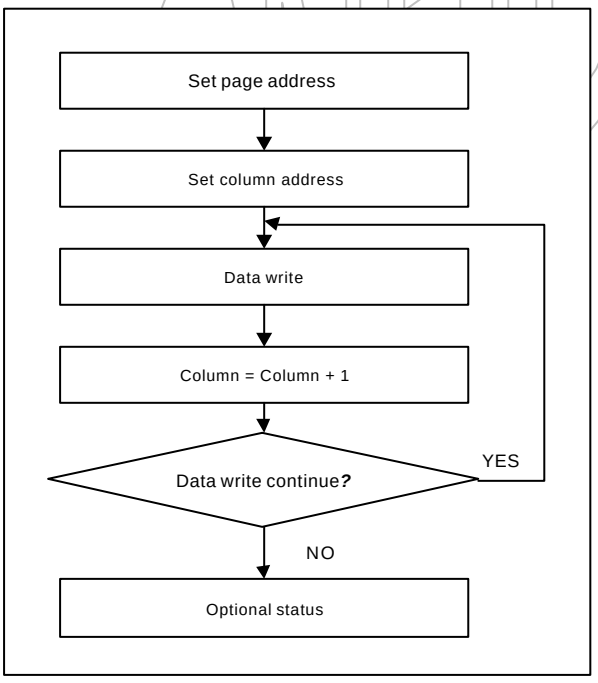

Figure 8-1. Sequence for writing display data

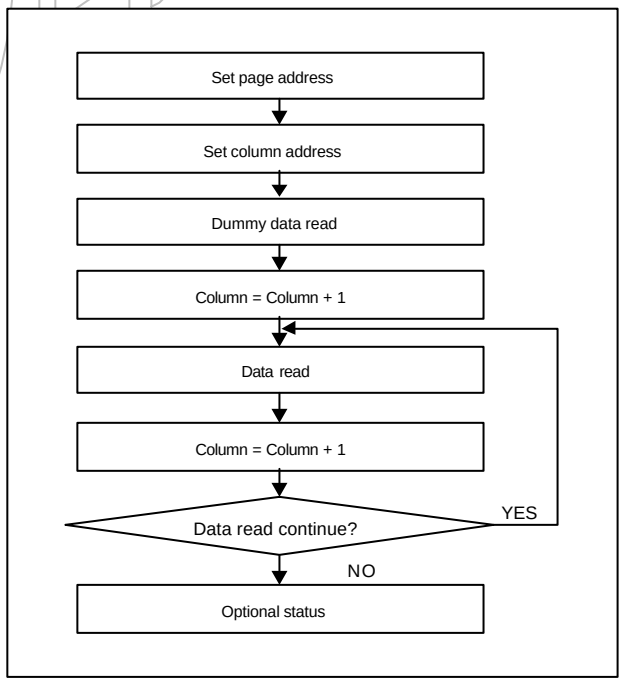

Figure 8-2. Sequence for reading display data

Read status

Indicates the internal status of the HM11S140.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BUSY	DISP	RES	0	0	0	1	0

Flag	Description
BUSY	The device is busy when internal operation or reset. Any instruction is rejected until BUSY goes Low. 0: chip is active, 1: chip is being busy.
DISP	Indicates display ON / OFF status 0: display OFF, 1: display ON
RESET	Indicates the initialization is in progress by RESET signal. 0: chip is active, 1: chip is being reset

ICON control register ON/OFF

This instruction makes ICON enable or disable. By default, ICON display is disabled (ICON= 0).

When ICON control register is set to " 1" , ICON display is enabled and page address is set to " 16" .

Then user can write data for icons.

It is impossible to set the page address to " 16" by Set Page Address instruction.

Therefore, when writing data for icons, ICON control register ON instruction would be used to set the page address to " 16" .

When ICON control register is set to " 0" , ICON display is disabled.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	1	ICON

ICON=0: ICON disable (default)

ICON=1: ICON enable & set the page address to 16

Set page address

Sets the Page Address of display data RAM from the microprocessor into the page address register.

Any RAM data bit can be accessed when its Page Address and column address are specified.

Along with the column address, the Page Address defines the address of the display RAM to write or read display data.

Changing the Page Address doesn't effect to the display status.

Set Page Address instruction can not be used to set the page address to " 16" . Use ICON control register ON/OFF instruction to set the page address to " 16" .

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	P3	P2	P1	P0

P 3	P 2	P 1	P 0	Page
0	0	0	0	0
0	0	0	0	1
:	:	:	:	:
1	1	1	0	14
1	1	1	1	15

Set column address

Sets the Column Address of display RAM from the microprocessor into the column address register. Along with the Column Address, the Column Address defines the address of the display RAM to write or read display data. When the microprocessor reads or writes display data to or from display RAM, Column Addresses are automatically increased.

Set column address MSB

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	0	Y7	Y6	Y5

Set column address LSB

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	Y4	Y3	Y2	Y1

Y7	Y6	Y5	Y4	Y3	Y2	Y1	Column address [Y7:Y1]
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
:	:	:	:	:	:	:	:
1	1	1	1	1	1	0	126
1	1	1	1	1	1	1	127

Set modify-read

This instruction stops the automatic increment of the column address by the read display data instruction, but the column address is still increased by the write display data instruction.

And it reduces the load of microprocessor when the data of a specific area is repeatedly changed during cursor blinking or others.

This mode is canceled by the reset Modify-Read instruction.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	0	0

Reset modify-read

This instruction cancels the modify-read mode, and makes the column address return to its initial value just before the set modify-read instruction is started.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	1	1	1	0

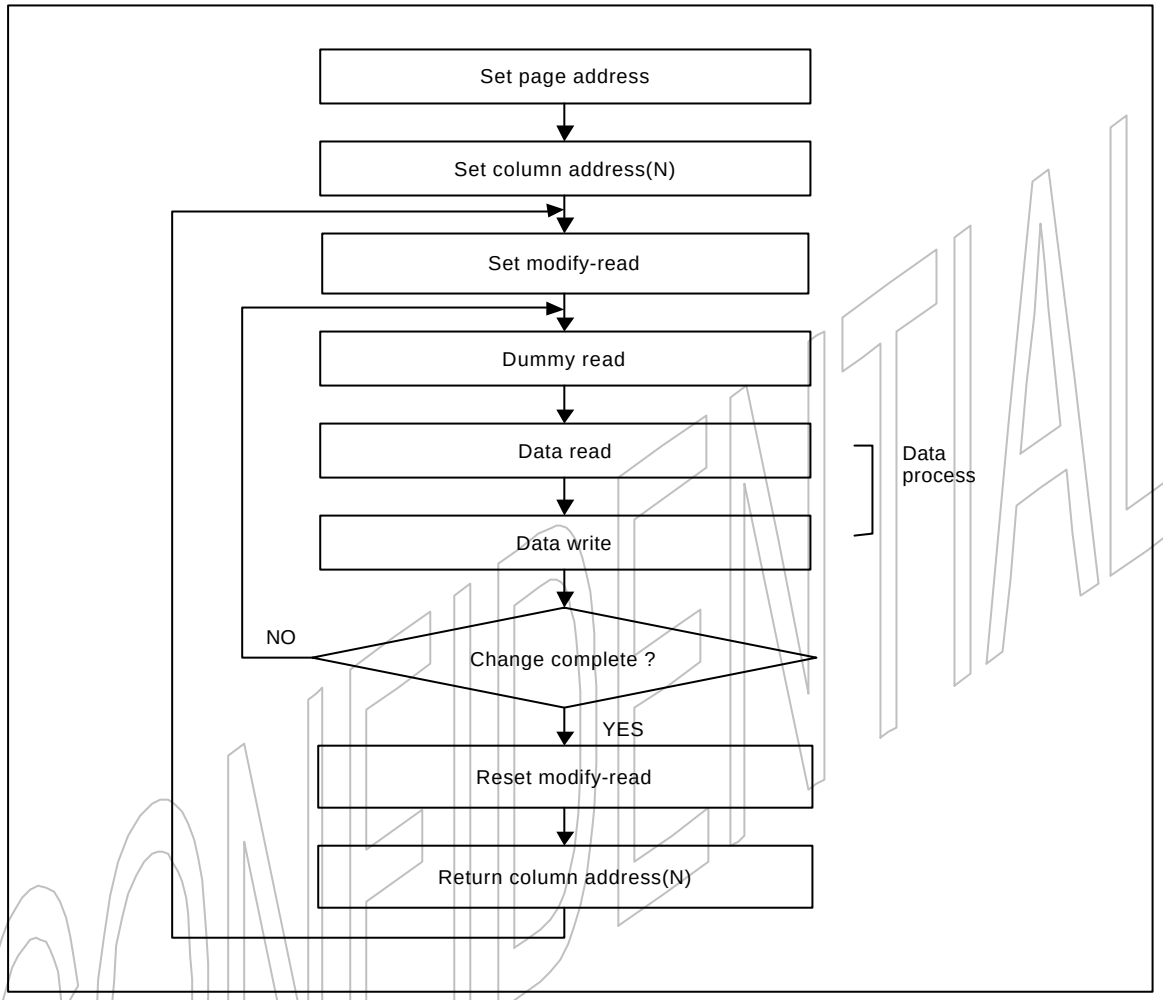

Figure 8-3. Sequence for cursor display

Display ON / OFF

Turns the display ON or OFF.

This command has priority over Entire Display On/Off and Reverse Display On/Off. Commands are accepted while the display is off, but the visual state of the display does not change.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	1	1	DON

DON = 1: display ON
DON = 0: display OFF

Set initial display line register

Sets the line address of display RAM to determine the initial display line using 2-byte instruction. The RAM display data is displayed at the top of row(COM0) of LCD panel.

The 1st Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	0	0	X	X

The 2nd Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	X	S6	S5	S4	S3	S2	S1	S0

S6	S5	S4	S3	S2	S1	S0	Line address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
0	0	0	0	0	1	0	2
:	:	:	:	:	:	:	:
1	1	1	1	1	0	1	125
1	1	1	1	1	1	0	126
1	1	1	1	1	1	1	127

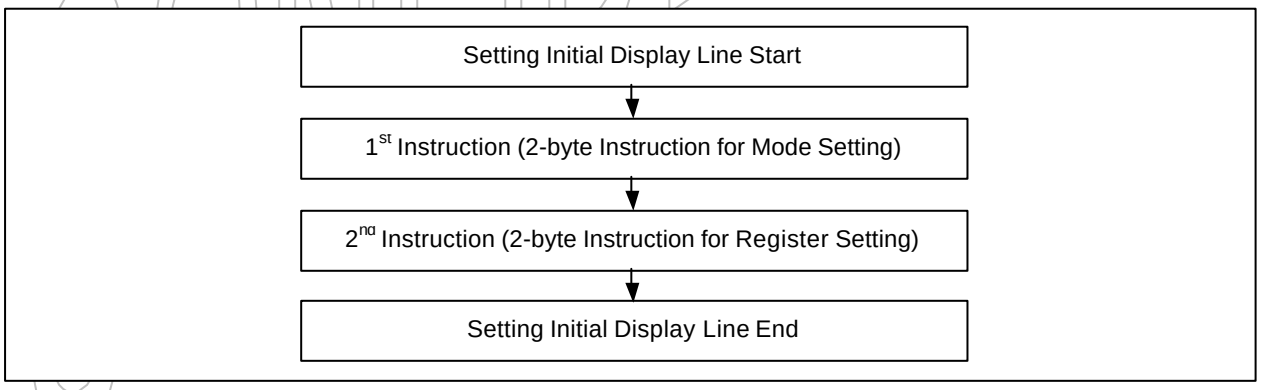

Figure 8-4. The sequence for setting the initial display line

Set initial COM0 register

Sets the initial row (COM) of the LCD panel using the 2-byte instruction.

By using this instruction, it is possible to realize the window moving without the change of display data.

The 1st Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	0	1	X	X

The 2nd Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	X	C6	C5	C4	C3	C2	C1	C0

C6	C5	C4	C3	C2	C1	C0	Initial COM0
0	0	0	0	0	0	0	COM0
0	0	0	0	0	0	1	COM1
0	0	0	0	0	1	0	COM2
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	0	1	COM125
1	1	1	1	1	1	0	COM126
1	1	1	1	1	1	1	COM127

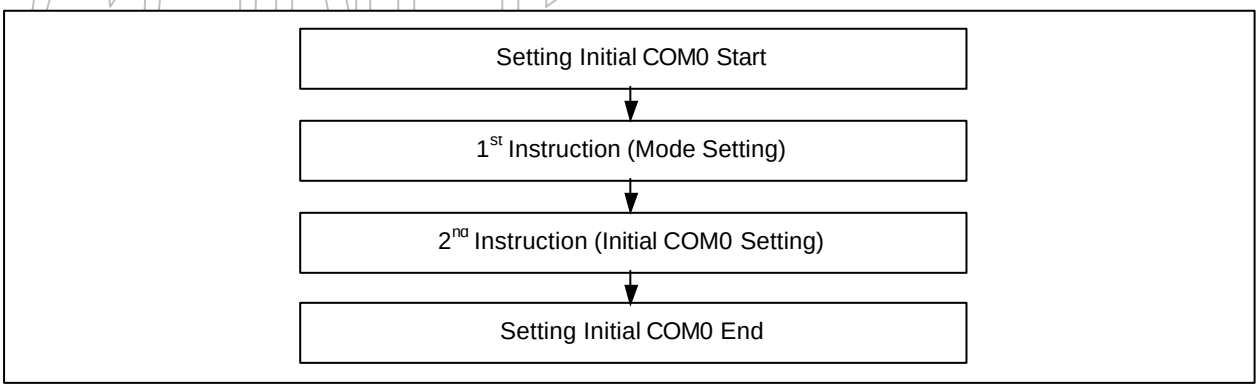

Figure 8-5. Sequence for setting the initial COM0

Set partial display duty ratio

Sets the duty ratio within range of 16 to 128 (ICON disabled) or 17 to 129 (ICON enabled) to realize partial display by using the 2-byte instruction.

The 1st Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	1	0	X	X

The 2nd Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	D7	D6	D5	D4	D3	D2	D1	D0

D7	D6	D5	D4	D3	D2	D1	D0	Selected partial duty ratio (ICON disabled)	Selected partial duty ratio (ICON enabled)
0	0	0	0	0	0	0	0	No operation	No operation
:	:	:	:	:	:	:	:		
0	0	0	0	1	1	1	1		
0	0	0	1	0	0	0	0	1/16	1/17
0	0	0	1	0	0	0	1	1/17	1/18
:	:	:	:	:	:	:	:	:	:
0	1	1	1	1	1	1	1	1/127	1/128
1	0	0	0	0	0	0	0	1/128	1/129
1	0	0	0	0	0	0	1	No operation	No operation
:	:	:	:	:	:	:	:		
1	1	1	1	1	1	1	1		

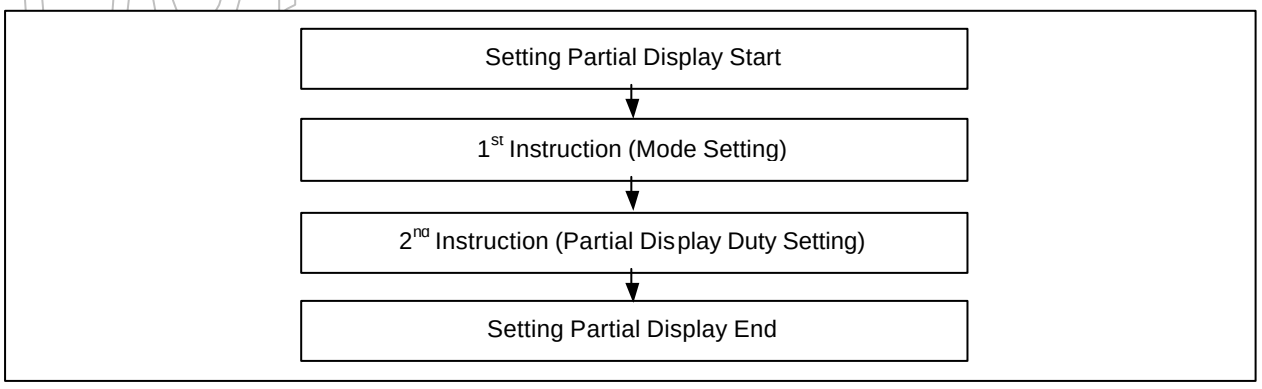

Figure 8-6. Sequence for setting partial display

Set N-line inversion register

Sets the inverted line number within range of 3 to 33 to improve the display quality by controlling the phase of the internal LCD AC signal (M) by using the 2-byte instruction.

The DC-bias problem could be occurred if K is even number. So, we recommend customers to set K to be odd number. K = D/N

D : The number of display duty ratio (D is selectable by customers)

N : N for N-line inversion (N is selectable by customers).

The 1st Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	1	1	X	X

The 2nd Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	X	X	X	N4	N3	N2	N1	N0

N4	N3	N2	N1	N0	Selected n-line inversion
0	0	0	0	0	0-line inversion (frame inversion)
0	0	0	0	1	3-line inversion
0	0	0	1	0	4-line inversion
:	:	:	:	:	:
1	1	1	0	1	32-line inversion
1	1	1	1	0	33-line inversion

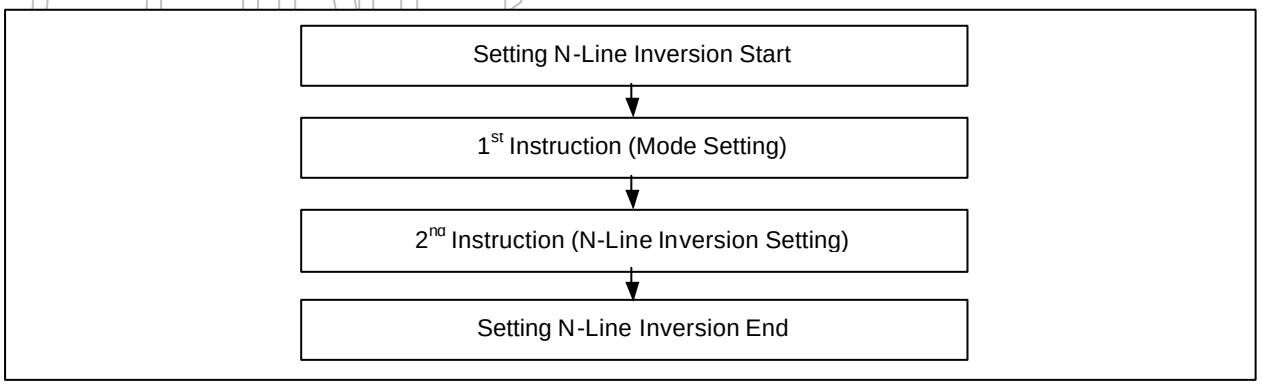

Figure 8-7. Sequence for N-line inversion

Release N-line Inversion

Returns to the frame inversion condition from the n-line inversion.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	1	0	0

Reverse display ON / OFF

Reverses the display status on LCD panel without rewriting the contents of the DDRAM.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	1	REV

REV	DDRAM data = "00" (White)	DDRAM data = "01" (Light gray)	DDRAM data = "10" (Dark gray)	DDRAM data = "11" (Black)
0(Normal)	White (" 00")	Light gray (" 01")	Dark gray (" 10")	Black (" 11")
1(Reverse)	Black (" 11")	Dark gray (" 10")	Light gray (" 01")	White (" 00")

Entire display ON / OFF

Forces the whole LCD panel to be turned on regardless of the contents of the display data RAM.

At this time, the contents of the display data RAM are held.

This instruction has priority over the Reverse Display ON / OFF instruction.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	0	EON

EON	DDRAM data = "00" (White)	DDRAM data = "01" (Light gray)	DDRAM data = "10" (Dark gray)	DDRAM data = "11" (Black)
0(Normal)	White (" 00")	Light gray (" 01")	Dark gray (" 10")	Black (" 11")
1(Entire)	Black (" 11")	Black (" 11")	Black (" 11")	Black (" 11")

Power control

Selects one of eight power circuit functions by using 3-bit register. An external power supply and part of internal power supply functions can be used simultaneously.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	1	VC	VR	VF

VC	VR	VF	Status of internal power supply circuits
0 1			Internal voltage converter circuit is OFF Internal voltage converter circuit is ON
	0 1		Internal voltage regulator circuit is OFF Internal voltage regulator circuit is ON
		0 1	Internal voltage follower circuit is OFF Internal voltage follower circuit is ON

Select DC-DC step-up

Selects one of 4 DC-DC step-up to reduce the power consumption by this instruction.

It is very useful to realize the partial display function.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	0	0	1	DC1	DC0

DC1	DC0	Selected DC-DC converter circuit
0	0	3 times boosting circuit
0	1	4 times boosting circuit
1	0	5 times boosting circuit
1	1	6 times boosting circuit

Select regulator resistor

Selects resistance ratio of the internal resistor used in the internal voltage regulator.

See voltage regulator section in power supply circuit. Refer to the table 7-6.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	0	R2	R1	R0

R2	R1	R0	1+ Rb/Ra)
0	0	0	2.3 (default)
0	0	1	3.0
0	1	0	3.7
0	1	1	4.4
1	0	0	5.1
1	0	1	5.8
1	1	0	6.5
1	1	1	7.2

Set electronic volume register

Consist of 2-byte Instructions

The 1st instruction set Reference Voltage mode, the 2nd one updates the contents of reference voltage register. After second instruction, Reference Voltage mode is released.

The 1st Instruction: Set reference voltage select mode

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	0	0	0	1

The 2nd Instruction: Set reference voltage register

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	X	X	EV5	EV4	EV3	EV2	EV1	EV0

EV5	EV4	EV3	EV2	EV1	EV0	Reference voltage parameter (a)
0	0	0	0	0	0	0
0	0	0	0	0	1	1
:	:	:	:	:	:	:
1	0	0	0	0	0	32 (default)
:	:	:	:	:	:	:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

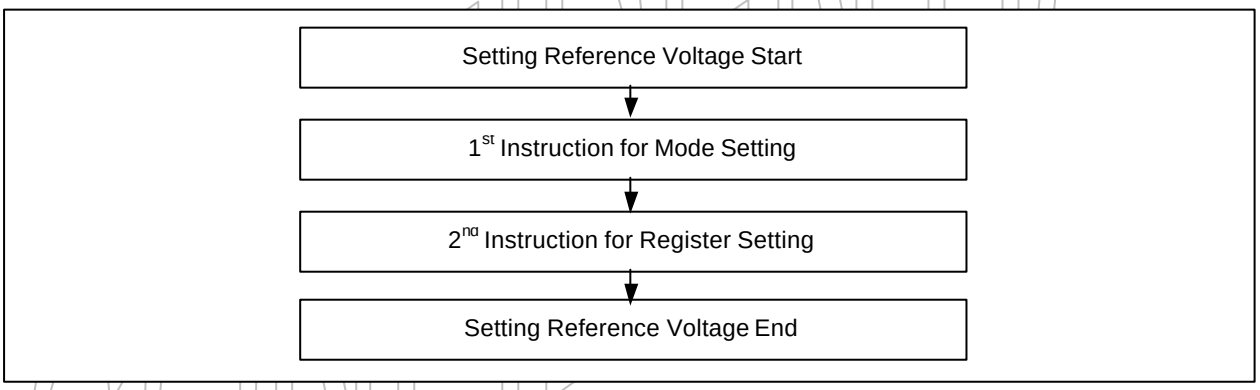

Figure 8-8. Sequence for setting the electronic volume

Select LCD bias

Selects LCD bias ratio of the voltage required for driving the LCD.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	1	0	B2	B1	B0

B2	B1	B0	LCD bias
0	0	0	1/5
0	0	1	1/6
0	1	0	1/7
0	1	1	1/8
1	0	0	1/9
1	0	1	1/10
1	1	0	1/11
1	1	1	1/12

SHL select

COM output scanning direction is selected by this instruction which determines the LCD driver output status.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	0	0	SHL	X	X	X

SHL = 0: normal direction (COM0 → COM127)
SHL = 1: reverse direction (COM127 → COM0)

X: Don't care

ADC select

Changes the relationship between RAM column address and segment driver. The direction of segment driver output pins could be reversed by software. This makes IC layout flexible in LCD module assembly.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	0	ADC

ADC = 0: normal direction (SEG0 → SEG127)
ADC = 1: reverse direction (SEG127 → SEG0)

Oscillator ON start

This instruction enables the built-in oscillator circuit.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	1	1

Power save

The HM11S140 enters the Power Save status to reduce the power consumption to the static power consumption value and returns to the normal operation status by the following instructions.

Set power save mode

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	0	P

PS = 0: normal mode
PS = 1: sleep mode

Release power save mode

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	0	1

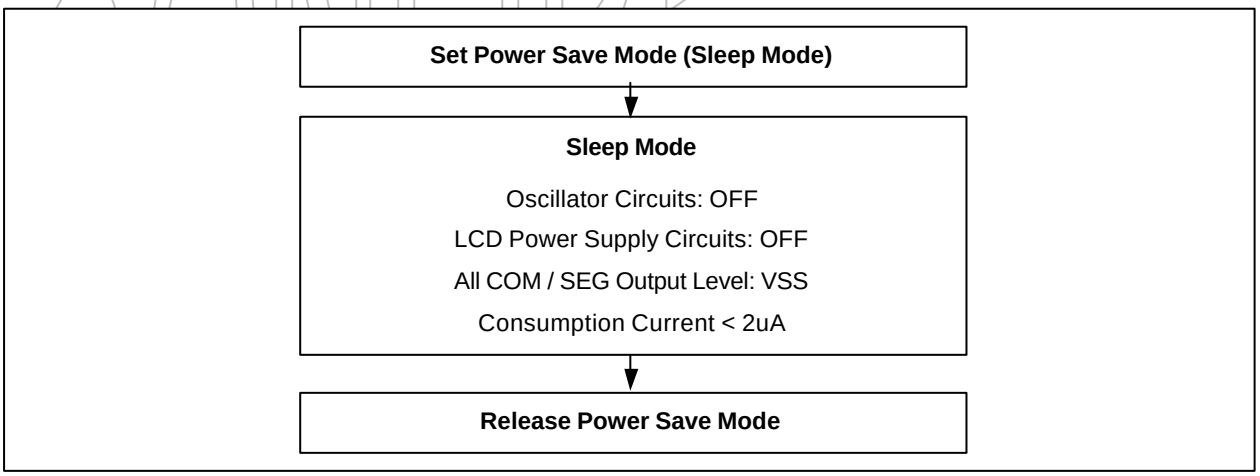

Figure 8-9. Power save routine

Reset

This instruction resets initial display line, column address, page address, and common output status select to their initial status, but dose not affect the contents of display data RAM.

This instruction cannot initialize the LCD power supply, which is initialized by the /RESET pin.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	0

Set PWM & FRC mode

Selects 3 / 4 FRC and 9 / 12 / 15 PWM

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	FRC	PWM1	PWM0

FRC	PWM1	PWM0	Status of internal power supply circuits
0			4FRC
1			3FRC
	0	0	9PWM
	0	1	9PWM
	1	0	12PWM
	1	1	15PWM

Set gray scale mode & register

Consists of 2 bytes instruction. The first byte sets grayscale mode and the second byte updates the contents of gray scale register without issuing any other instruction.

– **Set gray scale mode**

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	1	GM2	GM1	GM0

GM2	GM1	GM0	Description
0	0	0	In case of setting white mode and 1st/ 2nd frame
0	0	1	In case of setting white mode and 3rd /4th frame
0	1	0	In case of setting light gray mode and 1st/ 2nd frame
0	1	1	In case of setting light gray mode and 3rd /4th frame
1	0	0	In case of setting dark gray mode and 1st/ 2nd frame
1	0	1	In case of setting dark gray mode and 3rd /4th frame
1	1	0	In case of setting black mode and 1st/ 2nd frame
1	1	1	In case of setting black mode and 3rd /4th frame

– **Set gray scale register**

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	GB3	GB2	GB1	GB0	GA3	GA2	GA1	GA0
0	0	GD3	GD2	GD1	GD0	GC3	GC2	GC1	GC0

GA3, GB3, GC3, GD3	GA2, GB2, GC2, GD2	GA1, GB1, GC1, GD1	GA0, GB0, GC0, GD0	Pulse width (9PWM)	Pulse width (12PWM)	Pulse width (15PWM)
0	0	0	0	0/9	0/12	0/15
0	0	0	0	1/9	1/12	1/15
:	:	:	:	:	:	:
:	:	:	:	:	:	:
1	0	0	1	9/9	9/12	9/15
1	0	1	0	0/9	10/12	10/15
1	0	1	1	0/9	11/12	11/15
1	1	0	0	0/9	12/12	12/15
1	1	0	1	0/9	0/12	13/15
1	1	1	0	0/9	0/12	14/15
1	1	1	1	0/9	0/12	15/15

* GA3=WA3,LA3,DA3,BA3 GA2=WA2,LA2,DA2,BA2 GA1=WA1,LA1,DA1,BA1 GA0=WA0,LA0,DA0,BA0
  GB3=WB3,LB3,DB3,BB3 GA2=WB2,LB2,DB2,BB2 GA1=WB1,LB1,DB1,BB1 GA0=WB0,LB0,DB0,BB0
  GC3=WC3,LC3,DC3,BC3 GA2=WC2,LC2,DC2,BC2 GA1=WC1,LC1,DC1,BC1 GA0=WC0,LC0,DC0,BC0
  GD3=WD3,LD3,DD3,BD3 GA2=WD2,LD2,DD2,BD2 GA1=WD1,LD1,DD1,BD1 GA0=WD0,LD0,DD0,BD0

NOP

No operation

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	1

Test instruction

This instruction is for testing IC. Please do not use it.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	X	X	X	X

Referential instruction set-up flow: Initializing with the built-in power supply circuits

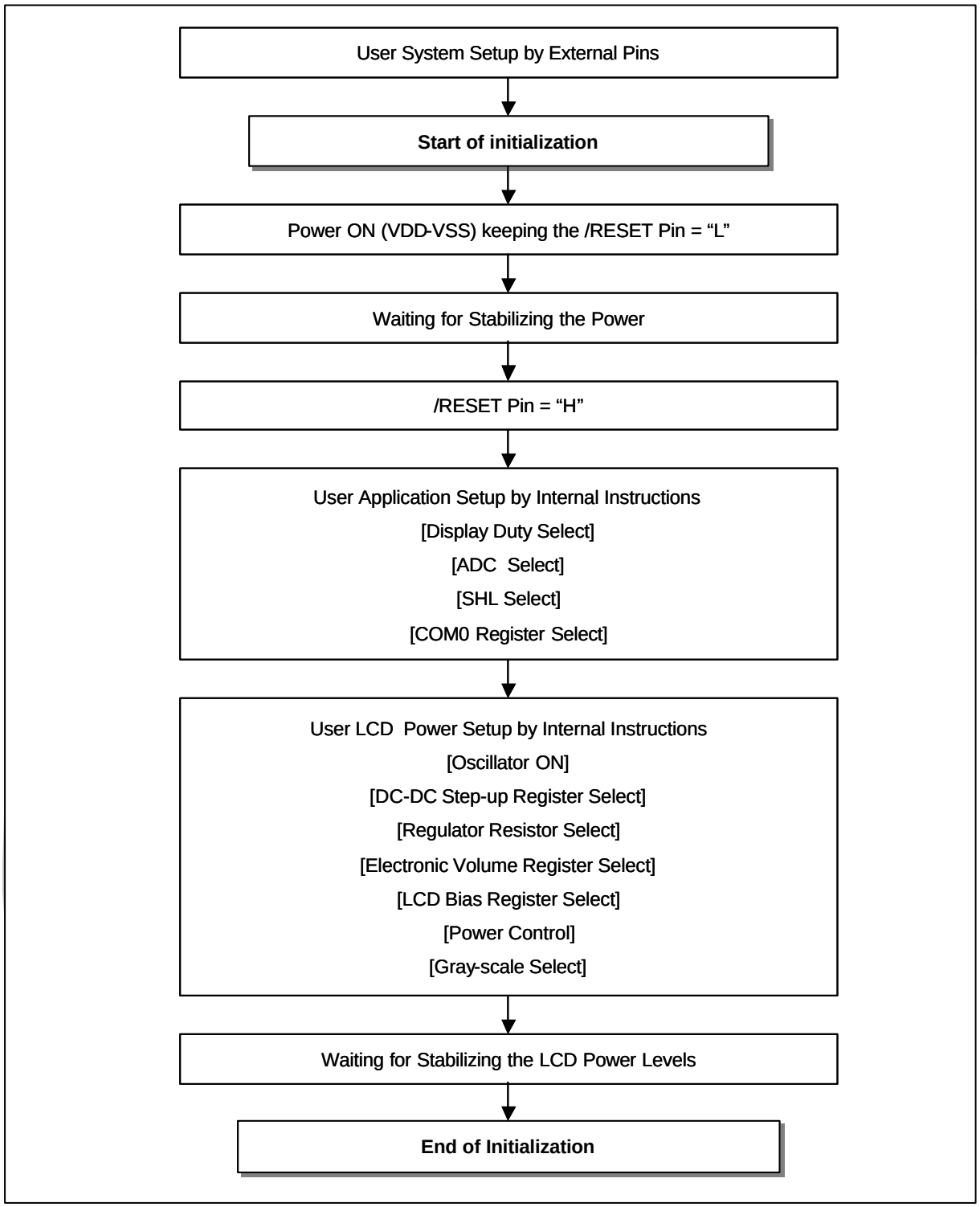

Figure 8-10. Initializing with the built-in power supply circuits

Referential instruction set-up flow: Initializing without the built-in power supply circuits

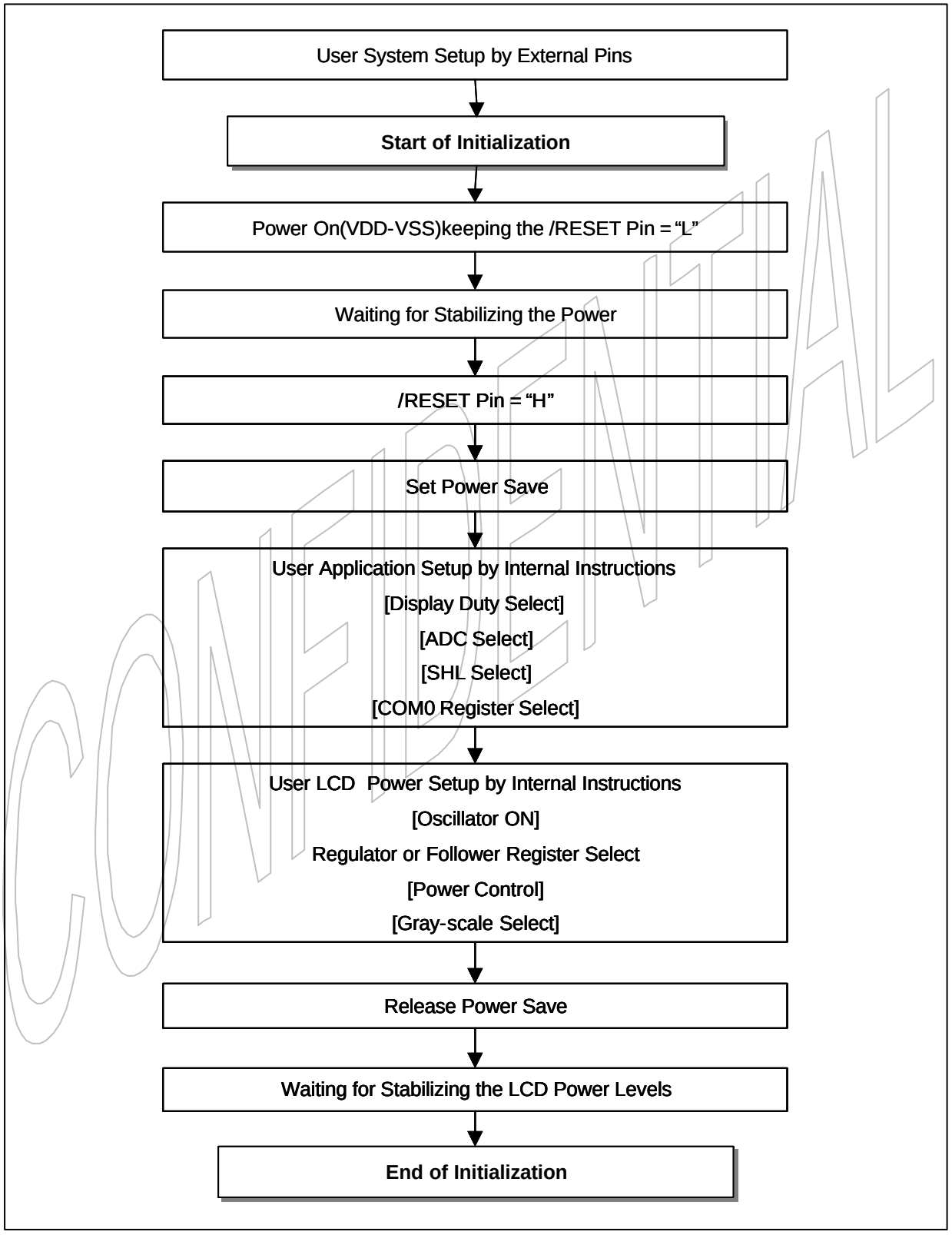

Figure 8-11. Initializing without the built-in power supply circuits

Referential instruction set-up flow: data displaying

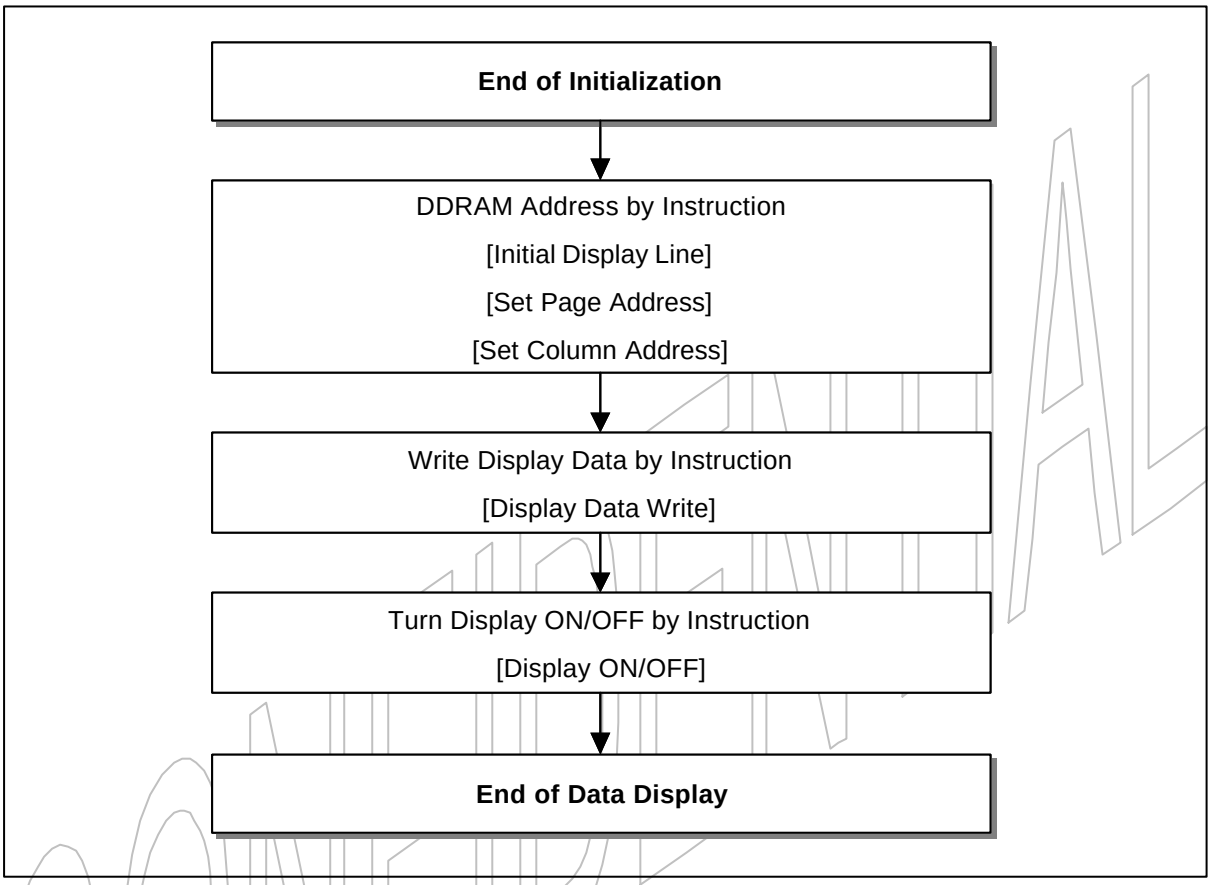

Figure 8-12. Data displaying

Referential instruction set-up flow: Power OFF

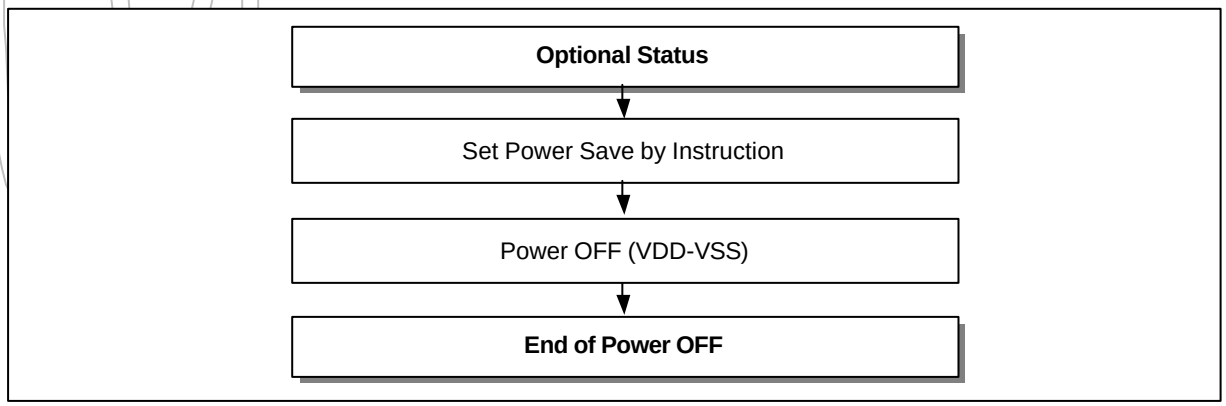

Figure 8-13. Power OFF

Referential instruction set-up flow: Partial duty changing

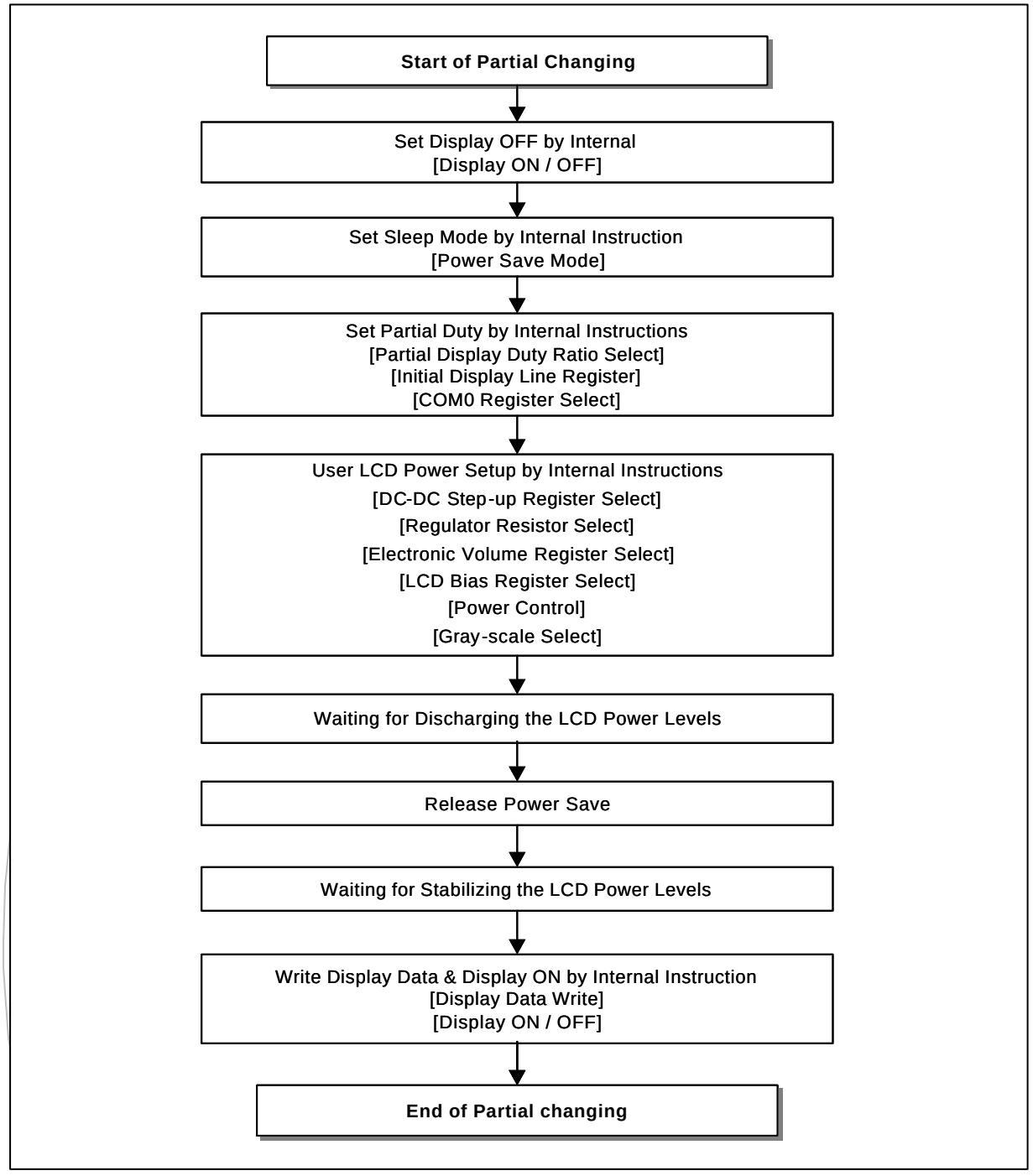

Figure 8-14. Partial duty changing

9. SPECIFICATIONS

9-1. ABSOLUTE MAXIMUM RATINGS

Table9-1. Absolute maximum ratings (VSS = 0V)

Parameter	Symbol	Rating	Unit
Supply voltage range	VDD	-0.3 to +7.0	V
	V0, VOUT	-0.3 to +17.0	
	V1, V2, V3, V4	-0.3 to V0 +0.3	
Input voltage range	V_{IN}	-0.3 to VDD +0.3	
External reference voltage	VEXT	+0.3 to VDD	V
Operating temperature range	T_{OPR}	-40 to +85	°C
Storage temperature range	T_{STR}	-55 to +125	

Notes:

1. VDD, V0, VOUT, V1 to V4 and VEXT are based on VSS = 0V.
2. Voltages V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ VSS must always be satisfied.(VLCD = V0 – VSS)
3. If supply voltage exceeds its absolute maximum range, this LSI may be damaged permanently. It is desirable to use this LSI under electrical characteristic conditions during general operation. Otherwise, this LSI may malfunction or reduced LSI reliability may result.

9-2. DC CHARACTERISTICS

Table 9-2. DC Characteristics (V_{SS} = 0V, V_{DD} = 2.4V to 3.6V, Ta = -40 to +85°C)

Item		Symbol	Condition	Min	Typ	Max	Unit	Pin Used
Operating voltage(1)		VDD		2.4	-	3.6	V	VDD *1
Operating voltage(2)		V0		4.0	-	15.0		V0 *2
Input voltage	High	VIH		0.8VDD	-	VDD		*3
	Low	VIL		VSS	-	0.2VDD		
Output voltage	High	VOH	IOH=-0.5mA	0.8VDD	-	VDD		*4
	Low	VOL	IOL=0.5mA	VSS	-	0.2VDD		
Input leakage current		IIL	VIN=VDD or VSS	-1.0	-	+1.0	μA	*3
Output leakage current		IOZ	VIN=VDD or VSS	-3.0	-	+3.0		*5
LCD driver ON resistance		RON	Ta = 25°C V0 = 8V	-	2.0	3.0	kΩ	COMn SEGn *6
Operating frequency		fFR	Ta = 25° C 1/128 Duty, 9 PWM REXT = TBDkΩ	70	85	100	Hz	*7
Voltage converter Input voltage		VCI	x 3	2.4	-	5.3	V	VCI
			x 4	2.4	-	4.0		
			x 5	2.4	-	3.2		
			x 6	2.4	-	2.6		
Voltage converter Output voltage		VOUT	x3 / x4 / x5 / x6 voltage conversion (no-load)	95	99	-	%	VOUT
Voltage regulator operating voltage		VOUT	-	5.4	-	16.0	V	VOUT
Voltage follower operating voltage		V0	-	4.0	-	15.0		V0 *8
Reference voltage		VREF	Ta = 25° C	2.04	2.10	2.16		*9

Table 9-2. DC Characteristics (Continued) (VDD = 3.0V, Ta = 25° C)

Item	Symbol	Condition	Min	Typ	Max	Unit	Pin Used
Dynamic current consumption(1) when the internal power supply is OFF (External power is used)							
Dynamic current consumption (1)	I_{DD1}	V0 - VSS = 12.0V duty = 1/128 (Display Off)	-	TBD	TBD	μA	*10
Dynamic current consumption (2) when the internal power supply is ON (internal power)							
Dynamic current consumption (2)	I_{DD2}	V0 – VSS = 12.0V, x5 boosting, duty = 1/128, (Display Off)	-	TBD	TBD	μA	*10
		V0 – VSS = 12.0V, x5 boosting, duty = 1/128 (Display On , Checker Pattern)	-	TBD	TBD	μA	*10
Current consumption during power save mode							
Sleep mode current	I_{DDS1}	During sleep	-	-	2	μA	*10

Table 9-3. The relationship between oscillation frequency and frame frequency

Duty ratio	Item	f_{CL}	fosc
1/N	On-chip oscillator circuit is used	f_{FR} x N	f_{FR} x PWM x 2 x N

*(f_{OSC}: oscillation frequency, f_{CL}: display clock frequency, f_{FR}: frame frequency, N = 16 to 129)

[* Remark solves]

*1. Though the wide range of operating voltages is guaranteed, a spike voltage change may affect the voltage assurance during access from the MPU.
*2. In case of external power supply is applied.
*3. /CS, RS, DB0 to DB7, E_/RD, RW_/WR, /RESET, PS, C68, INTRS and REF
*4. DB0 to DB7
*5. Applies when the DB0 to DB7 pins are in high impedance.
*6. Resistance value when -0.1[mA] is applied during the ON status of the output pin SEGn or COMn.
RON [kΩ] = ΔV[V] / 0.1[mA] (ΔV : voltage change when -0.1[mA] is applied in the ON status.)
*7. See Table 9-3 for the relationship between oscillation frequency and frame frequency.
*8. The voltage regulator circuit adjusts V0 within the voltage follower operating voltage range.
*9. On-chip reference voltage source of the voltage regulator circuit to adjust V0.
*10. Applies to the case where the on-chip oscillation circuit is used and no access is made from the MPU.
The current consumption, when the built-in power supply circuit is ON.
The current flowing through voltage regulation resistors(Rb and Ra) is not included.
It does not include the current of the LCD panel capacity, wiring capacity, etc.
Other conditions are 1/12 bias, 3 FRC, 9 PWM, Frame inversion, Frame freq. = 85HZ,
BL=(9,9,9,0), DG=(6,6,6,0), LG=(3,3,3,0), WH=(0,0,0,0).
*11. Applies when PWM method is used.
When both PWM and FRC method are used, frame frequency should be increased up to more than 130Hz. So, oscillator resistor value between OSC1 and VDD pin should be reduced.

9-3. AC CHARACTERISTICS

Read / Write characteristics (8080-series MPU)

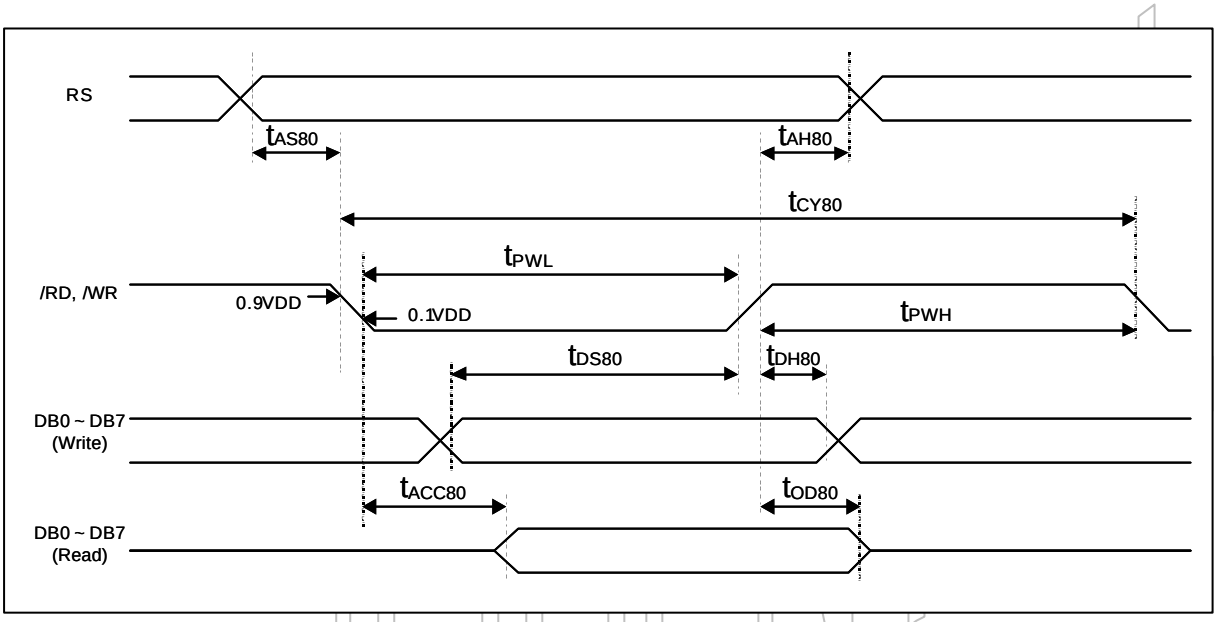

Figure 9-1. Read / Write characteristics (8080-series MPU)

(VDD = 2.4V to 3.6V, Ta = -40 to +85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time Address hold time	RS RW	tAS80 tAH80		0 0	-	ns
System cycle time for write System cycle time for read		tCY80 tCY80		100 166	-	ns
Pulse width low Pulse width high	/WR /RD	tPWL tPWH		40 40	-	ns
Data setup time Data hold time	DB0 to DB7	tDS80 tDH80		30 5	-	ns
Read access time Output disable time		tACC80 tOD80	CL = 100 pF	15 10	- 50	ns

Note: *1. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
(tr + tf) < (tCY80 - tPWLW - tPWHW) for write, (tr + tf) < (tCY80 - tPWLR - tPWHR) for read

Read / Write characteristics (6800-series microprocessor)

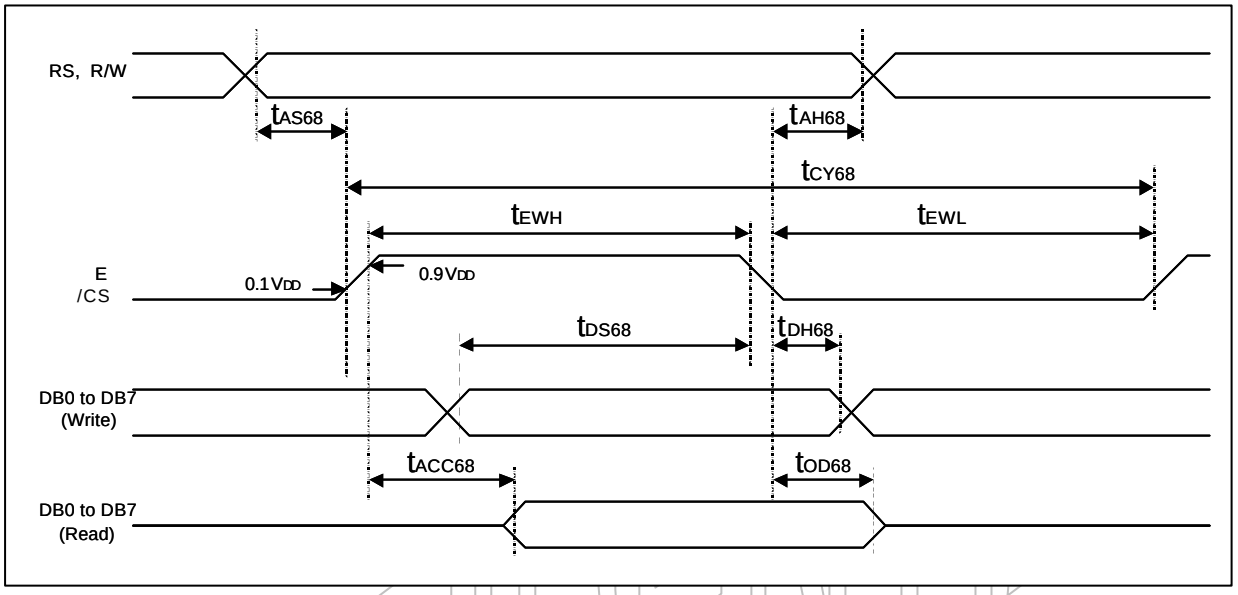

Figure 9-2. Read / Write characteristics (6800-series microprocessor)

(VDD = 2.4V to 3.6V, Ta = -40 to +85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time Address hold time	RS RW	tAS68 tAH68		0 0	-	ns
System cycle time for write System cycle time for read		tCY68 tCY68		100 166	-	ns
Pulse width low Pulse width high	E_RD (E)	tEWH tEWL		40 40	-	ns
Data setup time Data hold time	DB0 to DB7	tDS68 tDH68		30 5	-	ns
Read access time Output disable time		tACC68 tOD68	C_L = 100 pF	15 10	- 50	ns

Note: *1. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
(tr + tf) < (t CY68 - tEWHW - tEWLW) for write, (tr + tf) < (t CY68 - tEWHR - tEWLR) for read

Serial interface characteristics

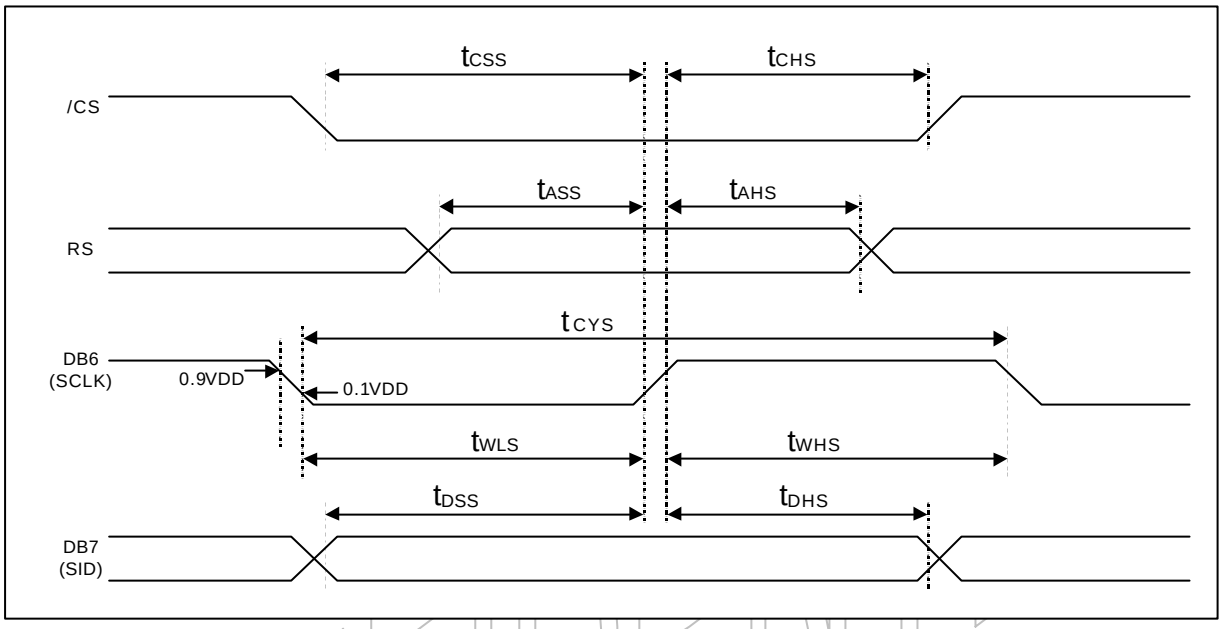

Figure 9-3. Serial interface characteristics

(VDD = 2.4V to 3.6V, Ta = -40 to +85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock cycle SCLK high pulse width SCLK low pulse width	DB6 (SCLK)	t_{CYS} t_{WHS} t_{WLS}		58.8 30 30	-	ns
Address setup time Address hold time	RS	t_{ASS} t_{AHS}		30 30	-	ns
Data setup time Data hold time	DB7 (SID)	t_{DSS} t_{DHS}		30 30	-	ns
/CS setup time /CS hold time	CSB	t_{CSS} t_{CHS}		30 1/2 *t_{CYS}	-	ns

Note: *1. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

Reset Input Timing

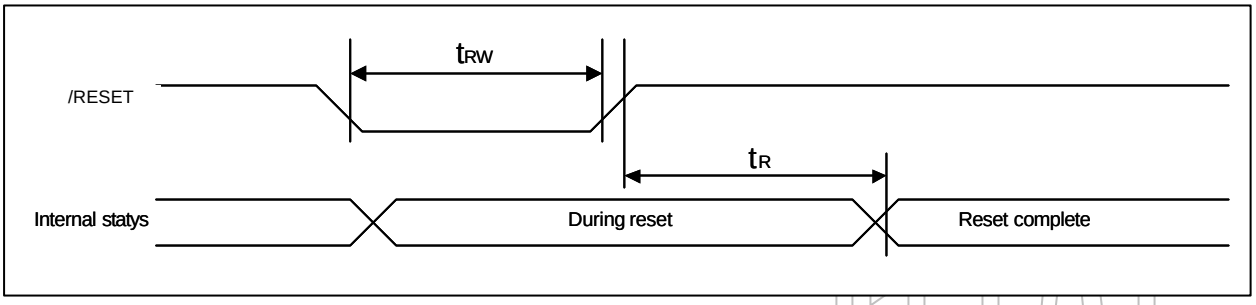

Figure 9-4. Reset input timing

(VDD = 2.4V to 3.6V, Ta = -40 to +85° C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Reset low pulse width	/RESET	tRW		1000	-	Ns
Reset time	-	tR		-	1000	ns

10. REFERENCE APPLICATIONS

10-1. MICROPROCESSOR INTERFACE

In case of interfacing with 6800-series (PS = “H”, C68 = “H”)

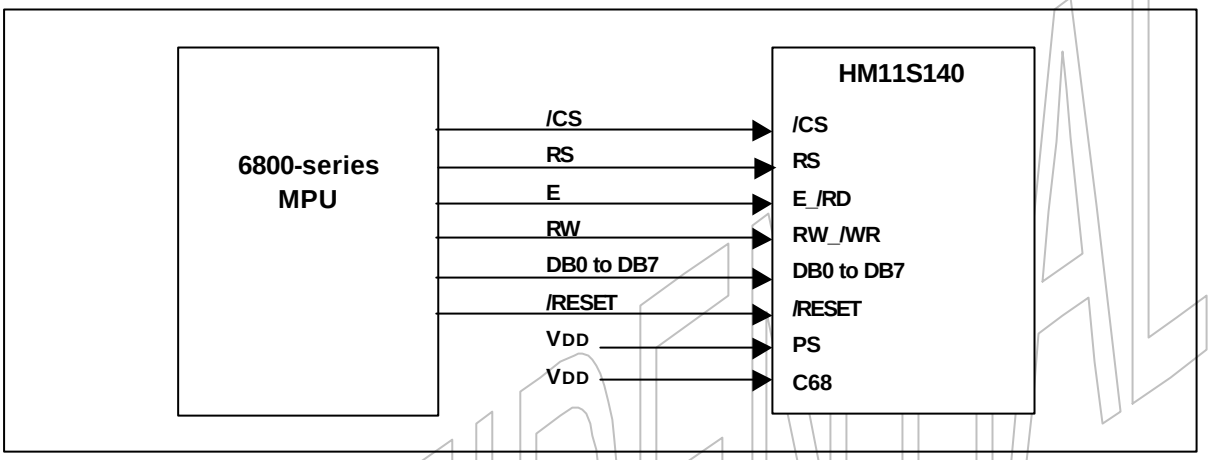

Figure 10-1. Interfacing with 6800-series (PS = “H”, C68 = “H”)

In case of interfacing with 8080-series (PS = “H”, C68 = “L”)

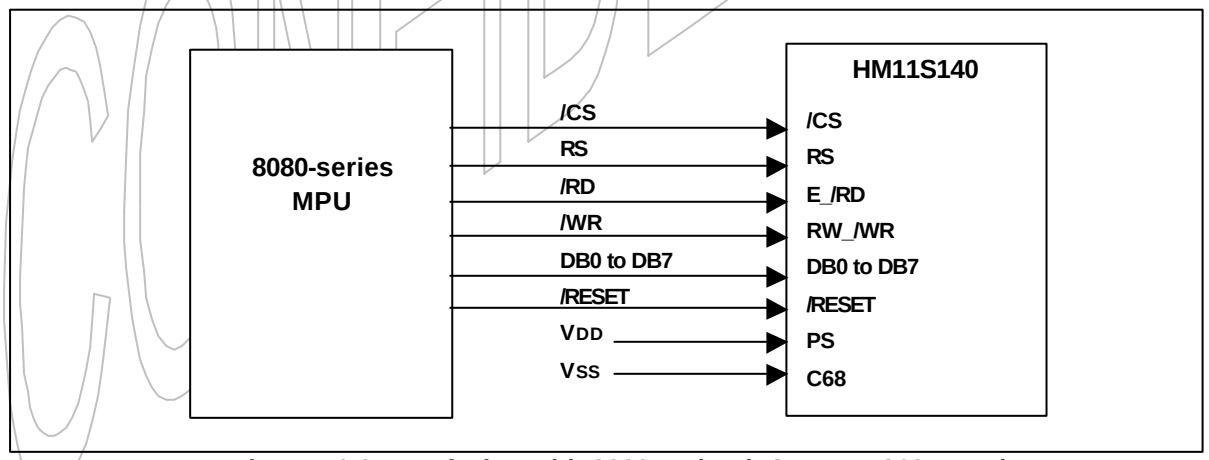

Figure 10-2. Interfacing with 8080-series (PS = “H”, C68 = “L”)

In case of serial (PS = "L" , C68 = "H")

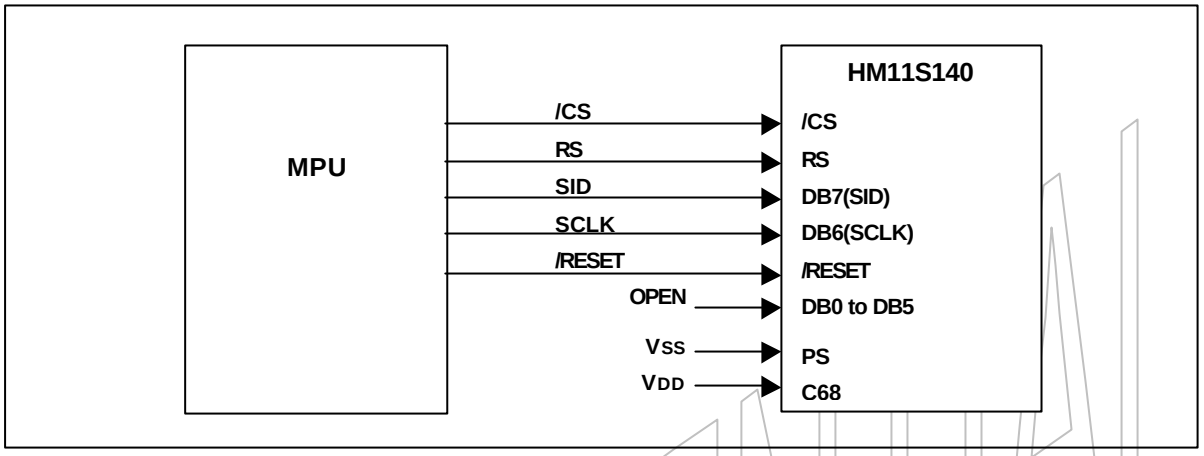

Figure 10-3. Serial interface (PS = “L”, C68 = “H”)

10-2. CONNECTIONS BETWEEN HM11S140 AND LCD PANEL

Single chip configuration (1/129 Duty configurations)

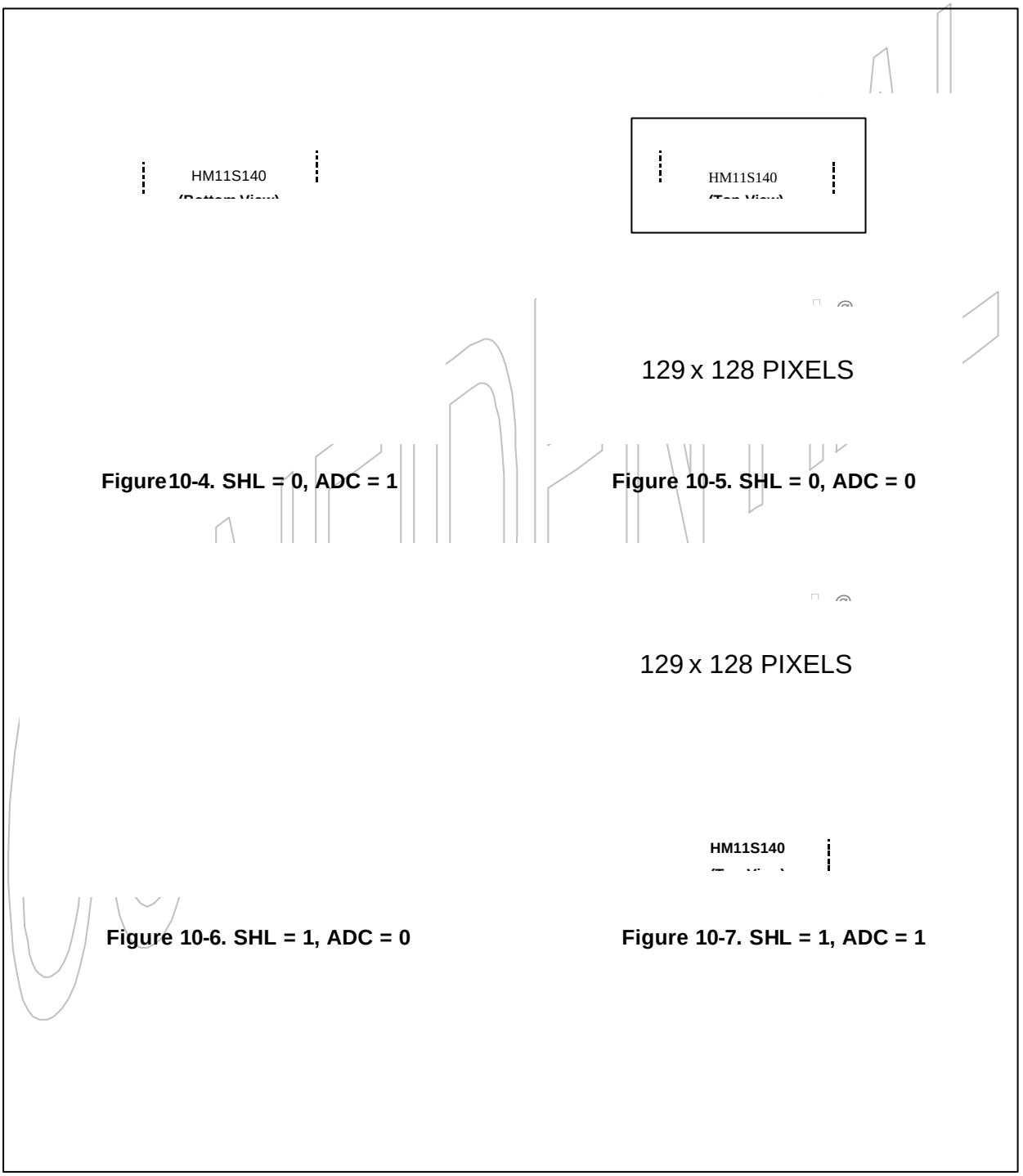

Figure 10-4. SHL = 0, ADC = 1

Figure 10-5. SHL = 0, ADC = 0

Figure 10-6. SHL = 1, ADC = 0

Figure 10-7. SHL = 1, ADC = 1