

10-Bit 200MSPS 0.18 μ m Digital-to-Analog Converter IP

nDA10200-18

FEATURES

- Complementary current output
- Update rate: 200MSPS
- Low power (max 36mW@1.8V)
- 1.8V power supply
- SFDR > 70dB for ($f_{in} = 5$ MHz)
- Internal voltage reference
- Adjustable full-scale current
- Edge-triggered input latches
- Small footprint (0.38mm²)

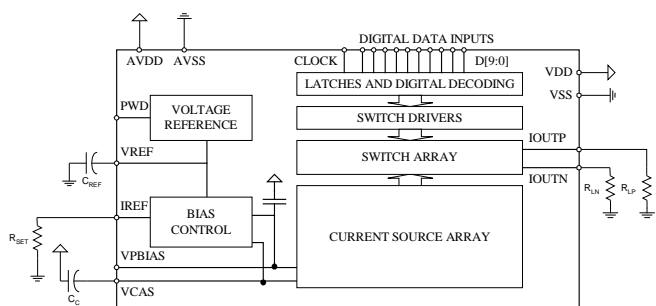
APPLICATIONS

- Communications transmit channel:
 - W-CDMA
 - Direct IF synthesis
 - Base stations
- Direct digital synthesis
- Digital Radio Link
- Set top boxes
- Instrumentation
- Digital video systems

GENERAL DESCRIPTION

The nDA10200-18 is a compact, high performance 10-bit resolution digital-to-analog converter (DAC), implemented as a 0.18 μ m CMOS IP. Excellent spurious free dynamic range performance in combination with high speed makes it ideal for transmit signal path of a communication systems. It consumes only 36mW from a 1.8V supply operating at 200MHz-update rate.

FUNCTIONAL BLOCK DIAGRAM



The nDA10200-18 is a current-output DAC with a nominal full-scale output current of 15mA and an output impedance greater than 100K Ω . Differential current output is provided to support both single ended and differential applications.

QUICK REFERENCE DATA

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V _{DD}	Supply Voltage		1.6	1.8	2.0	V
I _{DD}	Supply Current	200 MSPS			20	mA
P _D	Power Dissipation	200 MSPS, 1.8V			36	mW
DNL	Differential nonlinearity			± 0.1	± 0.5	LSB
INL	Integral nonlinearity			± 0.4	± 1.0	LSB
f _{clk,max}	Maximum update rate		200			MHz
SFDR	Spurious free dynamic range	190 MSPS, f _{OUT} = 60 MHz f _{OUT} = 5 MHz		62 71		dBc dBc
I _{FSR}	Full-scale Output Current		5		15	mA
N	Resolution				10	bit



GENERAL DESCRIPTION (Continued)

Matching between the two current outputs further enhances the dynamic performance for differential output configuration. The current outputs may be tied directly to external output resistors to provide two complementary voltage outputs, or fed directly into a transformer. Single ended voltage compliance range is then 0 - 0.75V at each output or $\pm 0.75V$ differentially.

Edge triggered input latches, internal voltage reference and bias control is integrated to provide a complete monolithic DAC solution. The on-chip bias is configured for maximum accuracy and flexibility. It supports adjustment of the full-scale current range from 5mA to 15mA. Power consumption can then be reduced to a mere 18mW at 5mA full-scale current, and thus make it ideal for portable and handheld applications.

The nDA10200-18 is provided as 21-pin 0.18 μ m CMOS IP, specified over the temperature range $-50^{\circ}C$ to $125^{\circ}C$

ELECTRICAL SPECIFICATIONS

DC SPECIFICATIONS

($T_A = 25^{\circ}C$, $V_{DD} = 1.8V$, $I_{FS} = 15mA$)

Symbol	Parameter	Min.	Typ.	Max.	Units
DC Accuracy					
DNL	Differential Nonlinearity		± 0.1	± 0.5	LSB
INL	Integral Nonlinearity		± 0.4	± 1.0	LSB
Monotonicity		Guaranteed			
Analog Output					
I_{FSR}	Full-scale Output Current	2		15	mA
V_{FSR}	Output compliance range	0		0.75	V
R_{OUT}	Output resistance		100		k Ω
C_{OUT}	Output capacitance		5		pF
ϵ_{offset}	Offset error	-0.03		0.03	% FSR
ϵ_{gain}	Gain error	-10		10	% FSR
Reference Voltage					
V_{ref}	Reference Voltage	0.88	0.91	0.95	V
	Reference Voltage Drift			100	ppm/ $^{\circ}C$
Power Supply					
V_{DD}	Positive supply voltage	1.6	1.8	2.0	V
I_{DD}	Supply current		18.5	20	mA
V_{SS}	Negative supply voltage		GND		
P_D	Power dissipation(@1.8V)			36	mW
T	Junction operating temperature	-40		+125	$^{\circ}C$

Table 1 DC Specifications



AC SPECIFICATIONS

($T_A = 25^\circ\text{C}$, $V_{DD} = 1.8\text{V}$, $I_{FS} = 15\text{mA}$, 50Ω doubly terminated, transformer coupled differential output)

Symbol	Parameter	Min.	Typ.	Max.	Units
Dynamic Performance					
f_{max}	Maximum output update rate	200			MSPS
E_{glitch}	Glitch impulse energy		5		pV-s
t_{rise}	Output Rise time		2.3		ns
t_{fall}	Output Fall time		2.3		ns
onoise	Output noise ($I_{FSR}=15\text{mA}$)		50		$\text{pA}/\text{Hz}^{1/2}$
onoise	Output noise ($I_{FSR}=2\text{mA}$)		30		$\text{pA}/\text{Hz}^{1/2}$
AC Linearity					
SFDR	Spurious Free Dynamic Range				
	$f_{\text{CLK}}=80\text{MHz}$ $f_{\text{OUT}} = 5 \text{ MHz}$		73		dBc
	$f_{\text{CLK}}=80\text{MHz}$ $f_{\text{OUT}} = 10 \text{ MHz}$		70		dBc
	$f_{\text{CLK}}=80\text{MHz}$ $f_{\text{OUT}} = 20 \text{ MHz}$		64		dBc
	$f_{\text{CLK}}=80\text{MHz}$ $f_{\text{OUT}} = 30 \text{ MHz}$		59		dBc
	$f_{\text{CLK}}=80\text{MHz}$ $f_{\text{OUT}} = 39.5 \text{ MHz}$		60		dBc
	$f_{\text{CLK}}=190\text{MHz}$ $f_{\text{OUT}} = 5 \text{ MHz}$		71		dBc
	$f_{\text{CLK}}=190\text{MHz}$ $f_{\text{OUT}} = 20 \text{ MHz}$		69		dBc
	$f_{\text{CLK}}=190\text{MHz}$ $f_{\text{OUT}} = 40 \text{ MHz}$		62.5		dBc
	$f_{\text{CLK}}=190\text{MHz}$ $f_{\text{OUT}} = 60 \text{ MHz}$		62		dBc
	$f_{\text{CLK}}=190\text{MHz}$ $f_{\text{OUT}} = 80 \text{ MHz}$		58.5		dBc
	$f_{\text{CLK}}=190\text{MHz}$ $f_{\text{OUT}} = 94 \text{ MHz}$		59		dBc

Table 2 AC Specifications

DIGITAL SPECIFICATIONS ($T_A = 25^\circ\text{C}$, $V_{DD} = 1.8\text{V}$)

Parameter	Min.	Typ.	Max.	Units
Logic '1'		1.8		V
Logic '0'		0		V
Input capacitance (data)		0.002		pF
Input capacitance (clock)		0.04		pF
Input setup time (t_s)		0.075		ns
Input hold time (t_H)		0.035		ns

Table 3 Digital Specifications



TIMING DIAGRAM

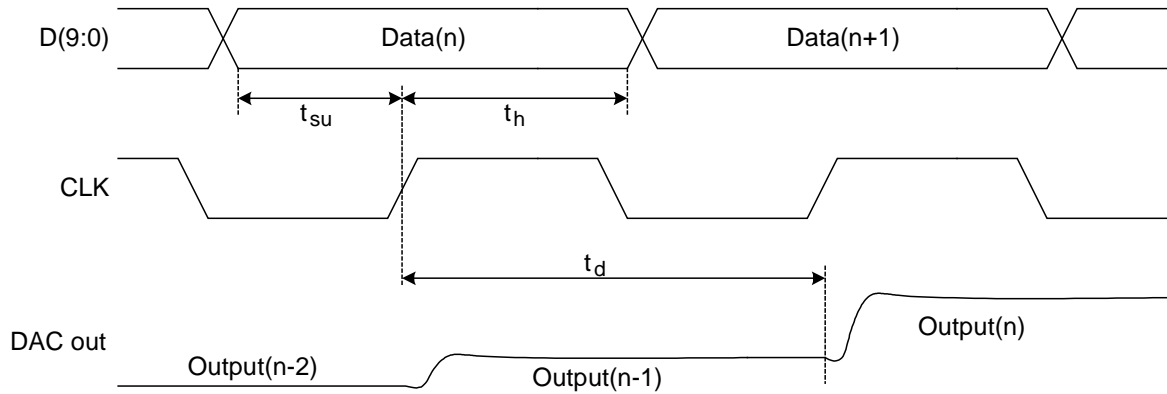


Figure 1 Timing diagram¹

IP BLOCK LAYOUT

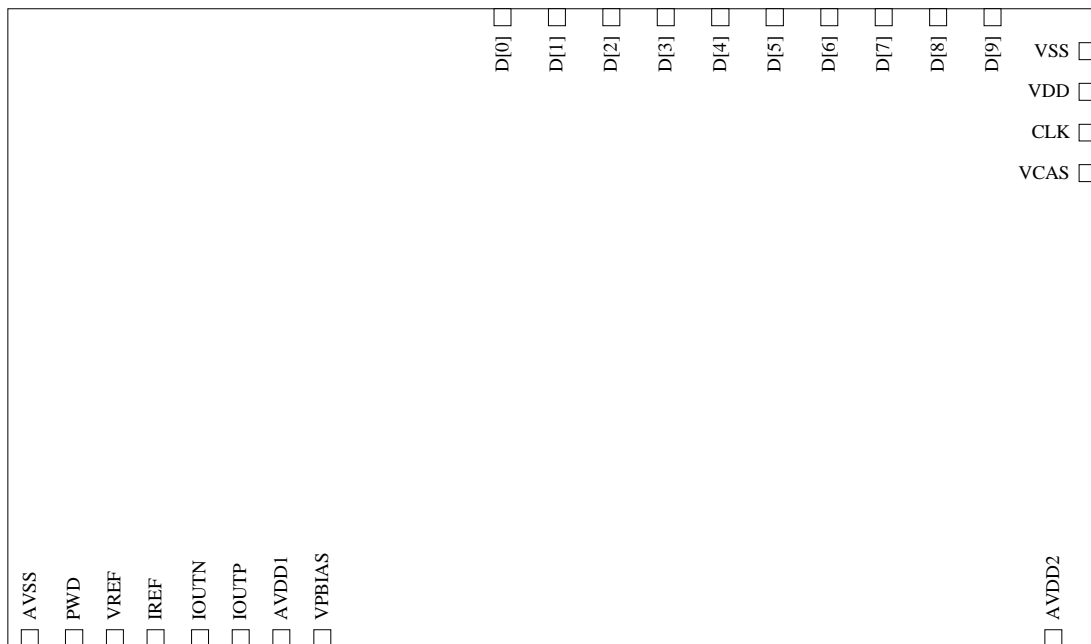


Figure 2: Size and pin placement for nDA10200-18 IP. The height and width of the layout is $X=805.1\mu m$ and $Y=471.1\mu m$ respectively in the $0.18\mu m$ CMOS process.

¹ t_{su} and t_h is defined in Table 3 Digital Specifications



PIN FUNCTIONS

PIN LABEL	Function
IOUTP, IOUTN	Complementary current outputs.
D[9:0]	Input data bits MSB:LSB. Offset binary code.
CLK	Clock input. Data latched on positive edge of clock.
IREF	Full-scale current adjustment pin. Full-scale current is thirty two times the current flowing through this pin.
VREF	Voltage reference input/output. Serves as 0.9-volt reference when internal reference is enabled.
VPBIAS	Leave unconnected.
VCAS	Decoupling pin. Decouple with at least 10nF to ground.
AVDD1,AVDD2	Analog supply voltage (+1.8V).
VDD	Digital supply voltage (+1.8V).
AVSS	Analog ground.
VSS	Digital ground.
PWD	Power down pin. Turns off internal reference when high.

Table 4 Pin functions

FUNCTIONAL DESCRIPTION

Figure 3 shows a simplified block diagram of the nDA10200-18 IP. It consists of a large PMOS current source array capable of delivering up to 15mA of current. The array is divided into 31 equal current sources that makes up the 5 most significant bits and 5 binary weighted current sources that makes up the 5 least significant bits. This configuration minimises the glitch energy and improves the DNL of the DAC.

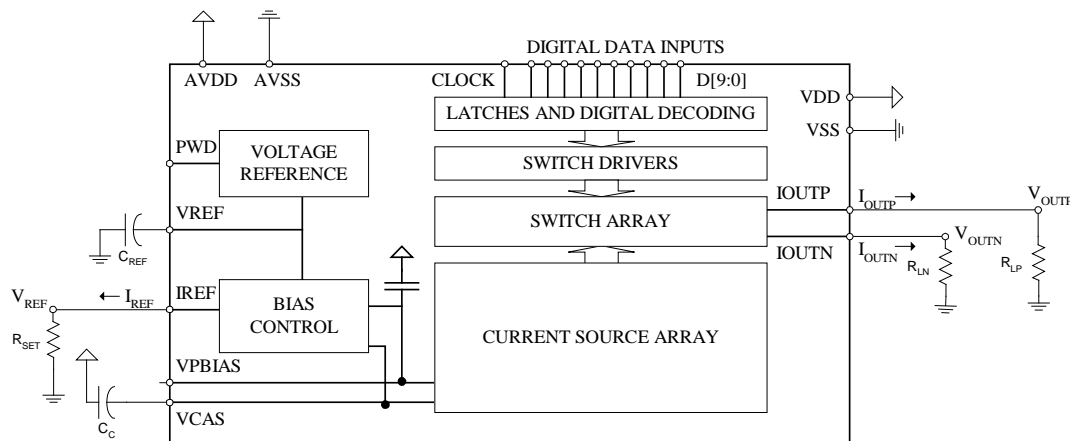


Figure 3 Functional block diagram

The current sources are switched to one or the other of the two output nodes (IOUTP or IOUTN) via PMOS differential current switches. These switches are driven by carefully designed and laid out latches that synchronises the driving signal, and thus ensures good dynamic performance.

The full-scale current is set between 5mA and 15mA by the internal bias circuit and an external resistor, R_{SET}. Combinations of the voltage reference V_{REF} and bias control circuit and the R_{SET} resistor sets the reference current I_{REF}, which is mirrored over to



the segmented current sources with the proper scaling factor. The full-scale current I_{FS} is thirty two times the value of I_{REF} .

TRANSFER FUNCTION

The nDA10200-18 provides complementary current outputs I_{OUTP} and I_{OUTN} . I_{OUTP} provides full-scale current, I_{FS} , when all input bits are high. (code 1023) while I_{OUTN} provides no current. The current appearing at the complementary current outputs is a function of both the input code and the full-scale current I_{FS} and can be expressed as:

$$I_{OUTP} = \text{code}/1024 \times I_{FS} \quad (1)$$

$$I_{OUTN} = (1023 - \text{code})/1024 \times I_{FS} \quad (2)$$

Where code is the decimal representation of the D[9:0] input signal, coded decimally from 0 to 1023. Consequently the sum of the two is equal to the full-scale current for all codes. This can be expressed as:

$$I_{OUTP} + I_{OUTN} = I_{FS} \text{ for all codes} \quad (3)$$

The full-scale current is a scaled version of the reference current I_{REF} , which is set by the reference voltage and the external resistor R_{SET} . This can be expressed as:

$$I_{FS} = 32 \times I_{REF} \quad (4)$$

$$I_{REF} = V_{REF} / R_{SET} \quad (5)$$

In a configuration where the current outputs drive resistive loads, either directly or through a transformer, the single ended voltage appearing at the outputs will be:

$$V_{OUTP} = I_{OUTP} \times R_{LP} \quad (6)$$

$$V_{OUTN} = I_{OUTN} \times R_{LN} \quad (7)$$

Where R_{LP} and R_{LN} are the equivalent load seen by I_{OUTP} and I_{OUTN} . For differential operation R_{LP} and R_{LN} should be equal. Thus, the differential voltage V_{DIFF} , appearing across I_{OUTP} and I_{OUTN} can be expressed as:

$$V_{DIFF} = (I_{OUTP} - I_{OUTN}) \times R_L \quad (8)$$

Where $R_{LP}=R_{LN}=R_L$. This equation shows the advantages of operating the DAC differentially. The differential signal swing is twice the single-ended swing, thus providing twice the signal power to the load. It also significantly reduces common-mode errors such as noise, distortion and DC offset at the outputs. Note that the single-ended full-scale voltage swing at the outputs must never exceed 0.75V to maintain specified distortion and linearity performance.



VOLTAGE REFERENCE OPERATION

The VREF pin serves as either an input or output pin depending whether internal or external reference is selected. A 1.2V bandgap reference is integrated in the nDA10200-18 core. A matched internal resistor ladder is used to divide it down to 0.9V which is supplied to the VREF pin. If PWD is set low, the internal reference is activated and VREF provides a 0.9V output. In this case the internal reference should be bypassed to ground with a 0.1 μ F ceramic capacitor.

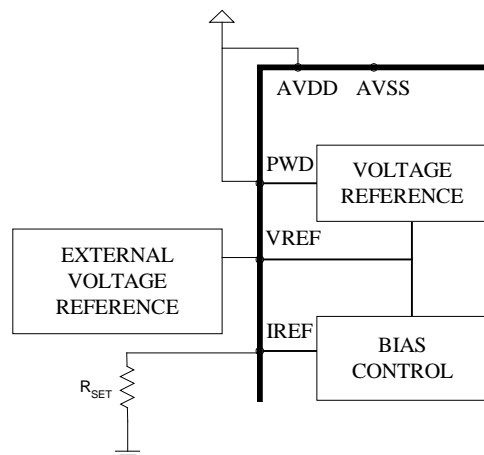


Figure 4 External reference configuration

Setting PWD to logic high disables the internal reference. In this case an external reference can be applied to the VREF pin. The external reference may provide either a fixed voltage to enhance accuracy and drift performance or a varying voltage for gain control. When using an external reference it is not necessary to bypass the VREF pin with a capacitor.

BIAS CONTROL OPERATION

The bias control is used to regulate the full-scale current of the nDA10200-18. It operates by copying the voltage appearing at the VREF pin to the IREF pin. The reference current I_{REF} flowing through the IREF pin is set by the external set resistor R_{SET} . I_{REF} is copied over to the current source array with the proper scaling factor to set the full-scale current I_{FS} .

The bias circuit allows a wide adjustment range of the full-scale current. The current through the IREF pin can be adjusted between 156.25 μ A and 468.75 μ A which is equivalent to a 5mA to 15mA full-scale current range at the output. This has several application benefits. First of all it provides a useful power versus performance trade-off. It is also very useful for applications requiring gain control.

ANALOG OUTPUTS

The nDA10200-18 produces two complementary current outputs, I_{OUTP} and I_{OUTN} , which may be configured single-ended or differentially. The current outputs can be converted to complementary single-ended voltages via load resistors, as described in the DAC transfer function section. The differential voltage appearing across the output terminals can be converted to single ended voltage through a transformer or a differential amplifier.

I_{OUTP} and I_{OUTN} have a negative and positive voltage compliance range that must be adhered in order to achieve optimum performance. The negative compliance range



of 0V is set by the breakdown limits of the CMOS process. Operation beyond this maximum may damage the current output, and thereby affect the reliability of the DAC. The positive compliance range is maximum 0.75V for 15mA full-scale current. Operation beyond this range will dramatically affect the distortion performance of the converter.

The output impedance of IOUTP and IOUTN is determined by the equivalent parallel combination of the switches associated with each current source, which means that the output impedance of each output is strongly dependent on number of switches turned on. Maximum output impedance of one output is achieved when the output conducts no current, minimal impedance is when the output conducts all the current. Due to the nature of the PMOS devices, the output impedance will also be slightly dependent on the voltage level appearing at the output. High voltage will give lower output impedance.

DIGITAL INPUTS

10 data input pins and one clock input pin comprises the digital interface to the nDA10200-18. The 10 bit parallel data input is coded with standard offset binary coding where D[9] is the most significant bit and D[0] is the least significant bit. IOUTP conducts the full-scale current when all data inputs are logic 1.

The nDA10200-18 is capable of update rates up to 200MSPS, consequently is the quality of the clock and data input critical in achieving the optimum performance. Fast clock edges will help minimising any jitter that will manifest it-self as phase noise on the reconstructed waveform. The clock can be operated at any duty cycle that meets the specified latch pulse width. Any set-up and hold time can be used as long as the specified minimum times are met, although the location of the transitions may affect the digital feed-through and distortion. The duty cycle need not to be 50%, the requirement is that the spacing between positive and negative transition and vice verse is minimum 2.5ns.

POWER DISSIPATION

The power dissipation of nDA10200-18 depends on several factors. Analog supply current I_{AVDD} depends only on the full-scale current I_{FS} , of which it is directly proportional. The digital supply current I_{VDD} depends on the update rate and the input waveform. Since the digital supply current is negligible compared to the analog supply current, an estimate of the typical total supply current is:

$$I_{TOTAL} = 3.5mA + I_{FS} \quad (9)$$

Where the update rate and waveform dependencies of the digital supply current are ignored. The power consumption from a 1.8V supply can then be expressed as:

$$P_{TOTAL} = 6.3mW + I_{FS} \times 1.8V \quad (10)$$



DEFINITIONS OF SPECIFICATIONS

Integral Non Linearity (INL)

Defined as the maximum deviation of the actual analog output from the ideal output. Ideal output is a straight line drawn from zero to full-scale

Differential Non Linearity (DNL)

Defined as the maximum deviation of the actual step size, associated with a change in 1 LSB in digital output, from the ideal step-size.

Spurious Free Dynamic Range (SFDR)

Defined as the difference, in dB, between the rms amplitude of the output signal and the highest harmonic distortion component. The repeated spectral images of the output frequency are not considered harmonic distortion.

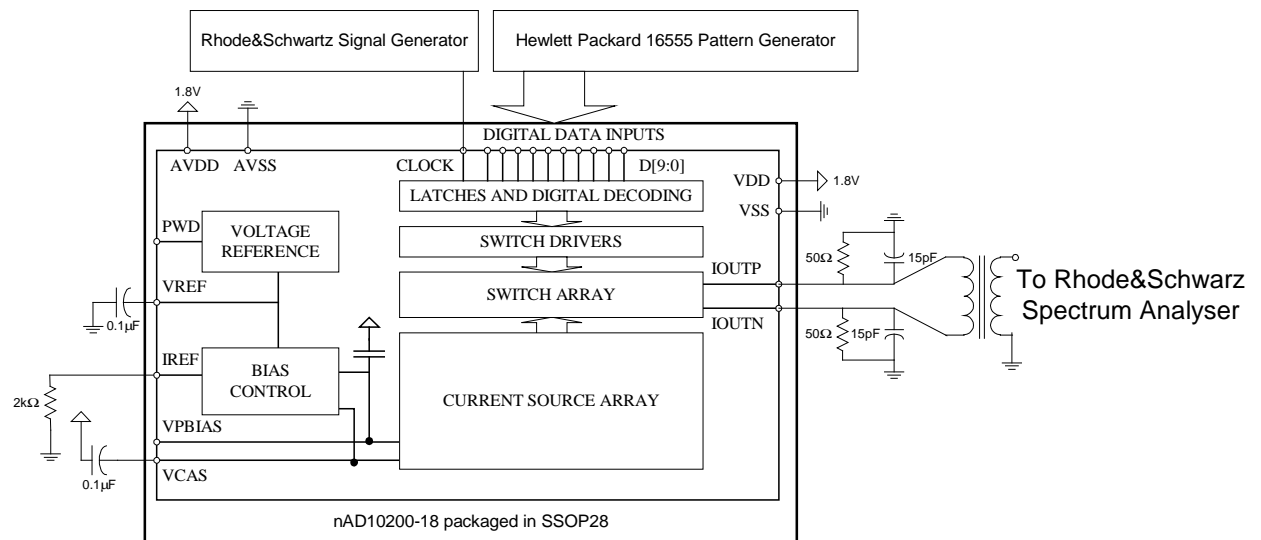
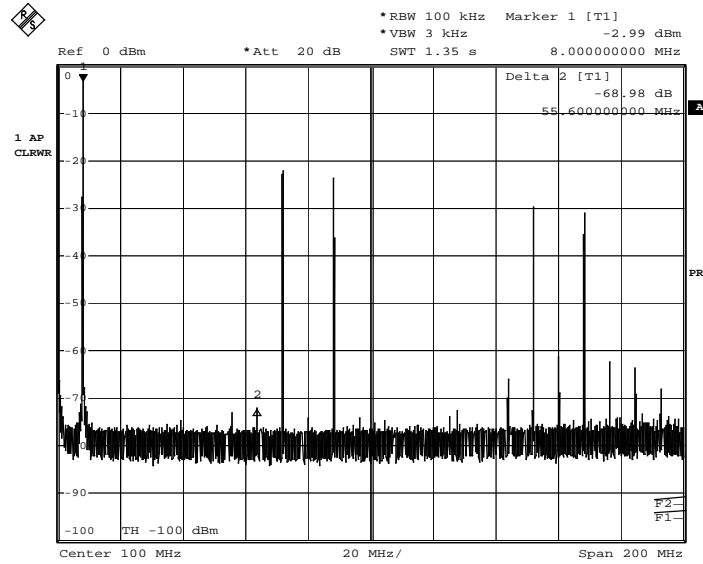


Figure 5 Basic AC Characterisation set-up



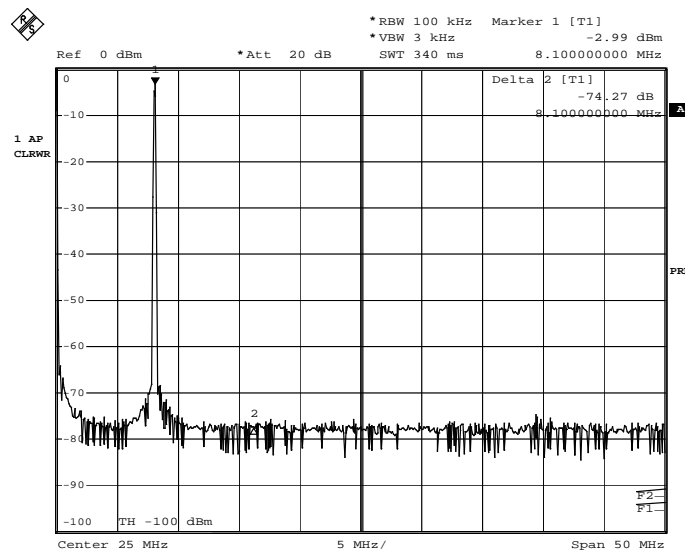
TYPICAL AC CHARACTERIZATION CURVES

($T_A = 25^\circ\text{C}$, $V_{DD} = 1.8\text{V}$, Full scale range = 15mA, 50Ω doubly terminated, differential output)



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Figure 6 Spectrum plot @ 80 MSPS, $F_{OUT} = 8.125\text{ MHz}$. 200 MHz bandwidth



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Figure 7 Spectrum plot @ 80 MSPS, $F_{OUT} = 8.125\text{ MHz}$. 50 MHz bandwidth

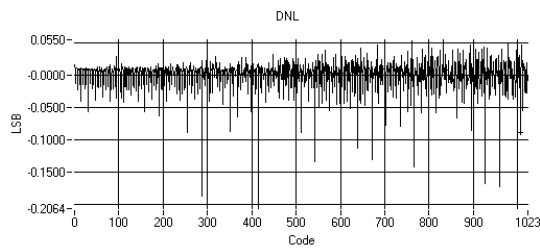


Figure 8 Typical DNL

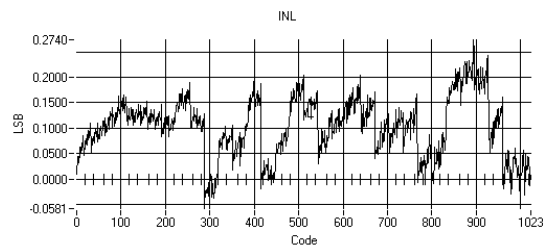


Figure 9 Typical INL

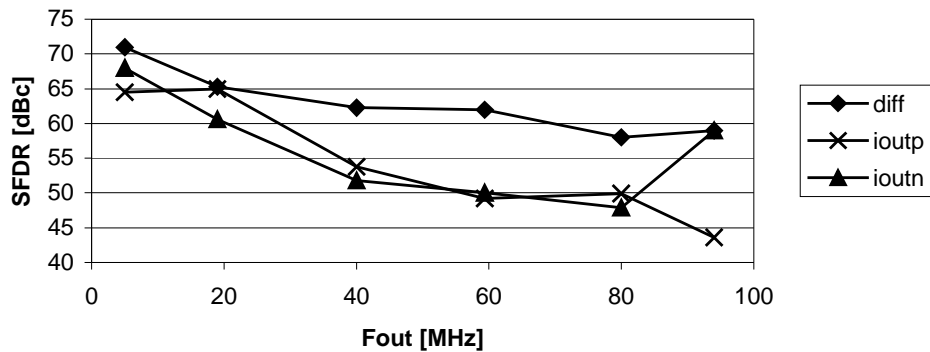


Figure 10 SFDR vs. F_{OUT} @ 190MSPS

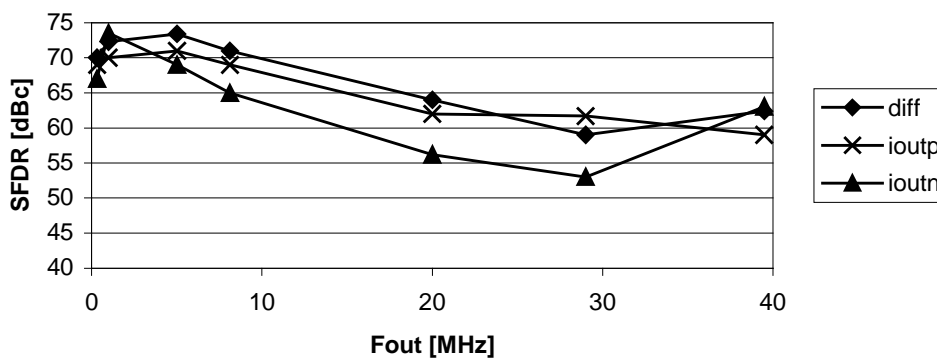


Figure 11 SFDR vs. F_{OUT} @ 80MSPS

OUTPUT CONFIGURATIONS

The complementary current outputs of the nDA10200-18 can, dependent on the application, be configured in various ways. The following sections illustrate some typical configurations. A differential configuration is highly preferable for application requiring optimal high frequency performance. A transformer configuration is suitable for applications allowing AC coupling. Application requiring DC coupling, signal gain or level shifting should use the differential op amp solution.

A unipolar output voltage can be provided using a single-ended output solution. A simple load resistor R_L is connected to IOU TP or IOU TN and referred to ground. This configuration is suitable for single-supply system requiring a DC-coupled ground



referred output voltage. A negative unipolar voltage can be generated using an amplifier as I-V converter.

Differential coupling using a transformer

Figure 12 shows a typical differential to single ended configuration using a RF transformer. This configuration provides the optimum performance in terms of distortion, common mode rejection and noise. It also provides electrical isolation and the ability to deliver twice the power to the load.

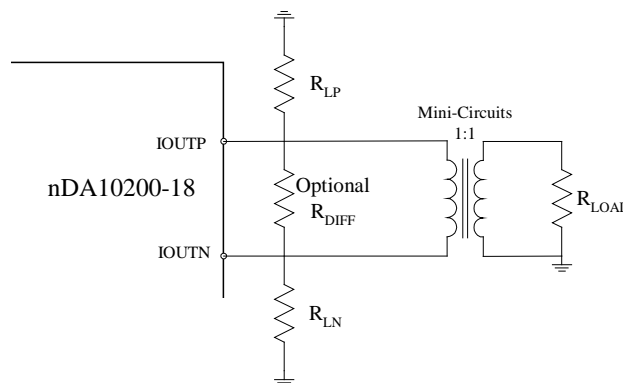


Figure 12 Differential output with transformer

A differential resistor R_{DIFF} , may be connected between the IOUTP and IOUTN pins to provide the proper source termination. Note that the complementary voltages V_{OUTP} and V_{OUTN} appearing at the IOTP and IOUTN pins respectively swing symmetrically around ground. This swing must be maintained within the specified compliance range of the DAC.

Differential coupling using an op amp

Another way to perform the differential to single-ended conversion is with an op amp, as shown is Figure 13. The differential voltage across IOUTP and IOUTN is converted to a single ended signal via the differential op amp configuration. Scaling of the gain setting resistors of the op amp can provide extra signal gain.

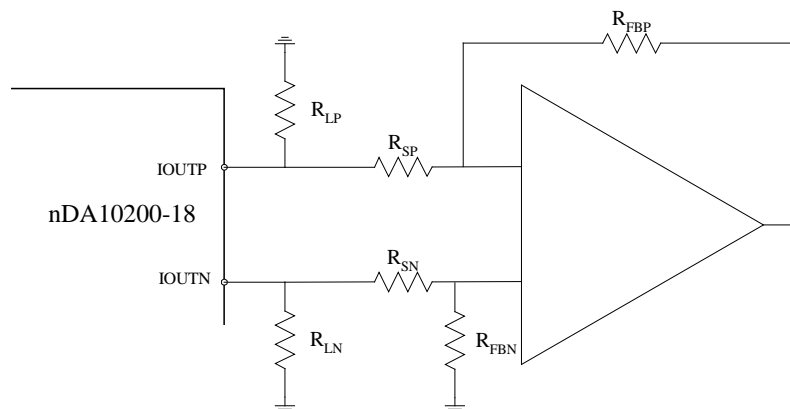


Figure 13 Differential output with op amp



Single-ended unbuffered voltage output

A pure resistive load can be used to provide a unipolar single ended output voltage. Either of the two outputs can be chosen. The unused output can be connected to ground directly or through a matched resistor. This configuration is shown in Figure 14, where R_{LP} is used to generate the output voltage V_{OUTP} . Different values of R_{LP} and I_{FS} can be selected as long as the positive compliance range is adhered to.

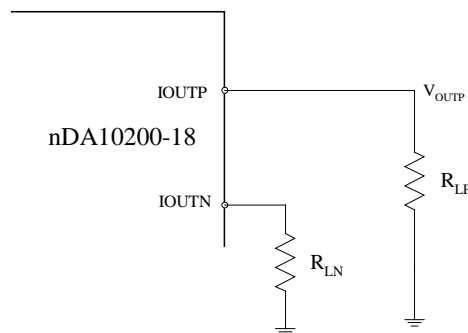


Figure 14 Unbuffered voltage output

Single-ended buffered voltage output

The configuration in Figure 15 can be used if the application requires a buffered output. The op amp performs the I-V conversion on the output current of IOUTP. In this configuration the op amp will maintain IOUTP at virtual ground, thus minimising the nonlinear output impedance effect on the DACs INL. The op amp output provides a negative unipolar output with a swing of $I_{FS} \times R_{FBP}$.

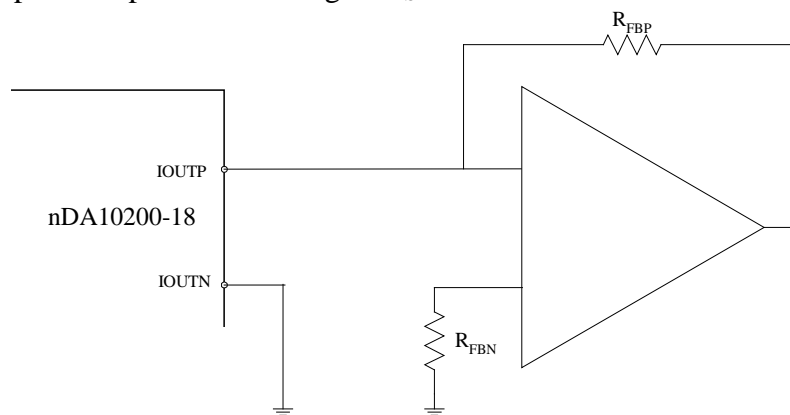


Figure 15 Single-ended buffered voltage output



APPLICATION NOTES

Using the nDA10200-18 for QAM modulation

QAM is one of the techniques in digital communication systems. It can be found in FDM and CDMA based most used digital modulation systems. The QAM modulation technique is based on both modulation in amplitude (AM) and modulation in phase (PM). It consists of two components at the same frequency, but with 90° phase shift. The sum of the in-phase component (I), and the 90° phase shift quadrature (Q) component makes up the QAM signal.

A typical implementation of a QAM modulator is shown in Figure 16. In this implementation the QAM modulation is performed in the analog domain. Two DACs are used to generate the I and Q components. Each of the components is typically applied to a Nyquist filter before they are fed into the quadrature mixer. The quadrature mixer modulates the I and Q components with an in-phase and quadrature phase carrier and sum the two outputs to provide the QAM signal.

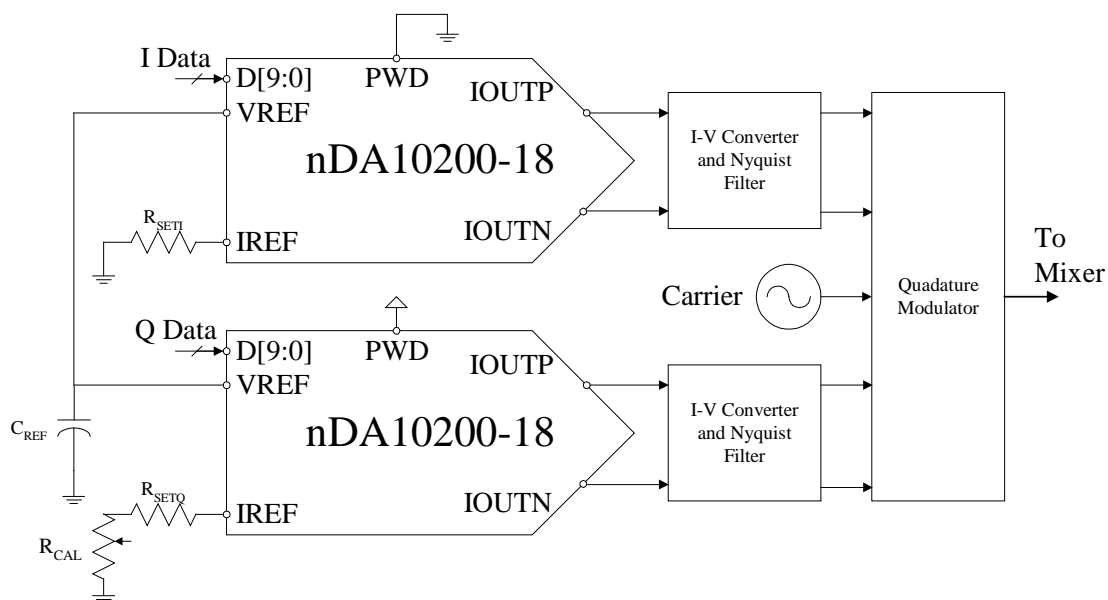


Figure 16 Typical Analog QAM Configuration

One of the most critical requirements for a QAM system is proper matching of the phase and gain of the I and Q channels. In the configuration shown in Figure 16 this is ensured by sharing the voltage reference provided by the I channel between both channels. Further enhancement in gain matching is achieved by using separate matched resistor networks for setting the full-scale current of each DAC. The R_{CAL} resistor is used to calibrate for mismatch arising from both initial mismatches between the DACs, the set resistors, the I-V converters and the Nyquist filters. To minimise phase mismatch, should the clock path to each of the channel DACs be matched.

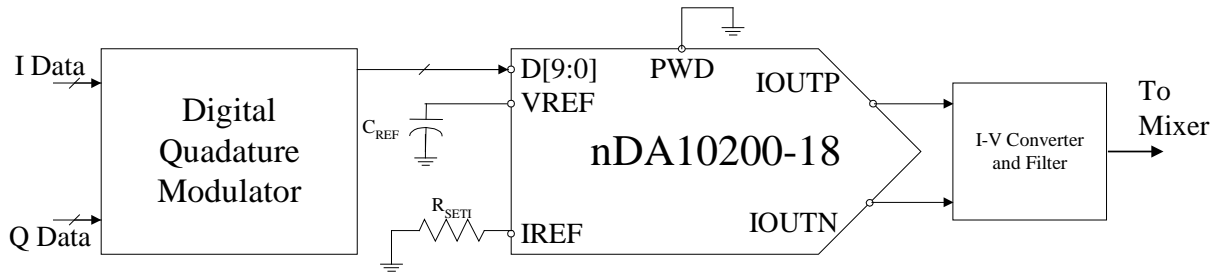


Figure 17 Typical Digital QAM Configuration

Another approach to QAM modulation is to generate the QAM signal completely in the digital domain. A typical configuration is shown in Figure 17. The greatest benefit of doing it this way is that it guaranties perfectly matched I and Q components in terms of gain and phase. However, the single DAC must operate at sufficiently high update rate to accommodate for the highest specified QAM carrier frequency.



DELIVERABLES AND INTEGRATION SUPPORT

Deliverable	Notes
Stream File	Flat GDS2
LVS Netlist	SPICE compatible
Timing Description	Synopsys LIB file
Footprint File	LEF format
HDL Model	Verilog/VHDL/SystemC
Extended documentation	Full characterisation report, integration instructions.

Table 5 Standard deliverables

An IP purchase also includes 40 hours of support from our highly experienced engineers.

DEFINITIONS

Data sheet status	
Objective product specification	This datasheet contains target specifications for product development.
Preliminary product specification	This datasheet contains preliminary data; supplementary data may be published from Nordic VLSI ASA later.
Product specification	This datasheet contains final product specifications.
Limiting values	
Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Specifications sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

Table 3. Definitions

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Nordic VLSI ASA customers using or selling these products for use in such applications do so at their own risk and agree fully indemnify Nordic VLSI ASA for any damages resulting from such improper use or sale.

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PRODUCT SPECIFICATION



nDA10200-18 10 Bit 200 MSPS DAC IP

E-mail: For further information regarding our state of the art data converters, please e-mail us at datacon@nvlsi.no.

World Wide Web/Internet: Visit our site at <http://www.nvlsi.no>.

ORDERING INFORMATION

Type number	Description	Price
nDA10200-18-IC	nDA10200-18 sample in SSOP28 package (limited availability)	USD 50
nDA10200-18-EVB	nDA10200-18 evaluation board including characterisation report and user guide	USD 300

Table 4. Ordering information

Product Specification. Revision Date: September 9th, 2002

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