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# HD66702/HD66701

(Dot Matrix Liquid Crystal Display Controller/Driver)

# HITACHI

ADE-207-304(Z)  
'99.9  
Rev. 0.0

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## Description

The HD66701/2 dot-matrix liquid crystal display controller and driver LSI displays alphanumerics, Japanese kana characters, and symbols. It can be configured to drive a dot-matrix liquid crystal display under the control of a 4- or 8-bit microprocessor. Since all the functions required for driving a dot-matrix liquid crystal display are internally provided on one chip, a minimal system can be interfaced with this controller/driver.

A single HD66702 can display up to two 20-character lines, and a single HD66701 can display up to two 16-character lines.

The low 3-V power supply of the HD66701/2 is suitable for any portable battery-driven product requiring low power dissipation.

## Features

- $5 \times 7$  and  $5 \times 10$  dot matrix possible
- $80 \times 8$ -bit display RAM (80 characters max.)
- 7,200-bit character generator ROM
  - 160 character fonts ( $5 \times 7$  dot)
  - 32 character fonts ( $5 \times 10$  dot)
- $64 \times 8$ -bit character generator RAM
  - 8 character fonts ( $5 \times 7$  dot)
  - 4 character fonts ( $5 \times 10$  dot)
- 16-common  $\times$  100-segment (HD66702) or 80-segment (HD66701) liquid crystal display driver
- Programmable duty cycles
  - 1/8 for one line of  $5 \times 7$  dots with cursor
  - 1/11 for one line of  $5 \times 10$  dots with cursor
  - 1/16 for two lines of  $5 \times 7$  dots with cursor

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- Maximum display characters
  - One line  
1/8 duty cycle, 20-char. × 1-line (HD66702), 16-char. × 1-line (HD66701)  
1/11 duty cycle, 20-char. × 1-line (HD66702), 16-char. × 1-line (HD66701)
  - Two lines  
1/16 duty cycle, 20-char. × 2-line (HD66702), 16-char. × 2-line (HD66701)
- Wide range of instruction functions
  - Display clear, cursor home, display on/off, cursor on/off, display character blink, cursor shift, display shift
- Choice of power supply ( $V_{CC}$ ): 4.5 to 5.5V (standard), 2.7 to 5.5V (low voltage)
- Automatic reset circuit that initializes the controller/driver after power on (standard version only)
- Independent LCD drive voltage driven off of the logic power supply ( $V_{CC}$ ): 3.0 to 8.3V
- Low power dissipation
- LQFP2020-144-pin (HD66702), chip, chip with bump

## Ordering Information

| Type No.       | Package                | Operating Voltage | ROM Font             |
|----------------|------------------------|-------------------|----------------------|
| HCD66702RA00L  | 144-pin-chip           | 2.7 to 5.5V       | Standard Japanese    |
| HCD66702RA00BP | 144-pin-chip with bump | 2.7 to 5.5V       | Standard Japanese    |
| HCD66702RA01L  | 144-pin-chip           | 2.7 to 5.5V       | Communication system |
| HCD66702RA02L  | 144-pin-chip           | 2.7 to 5.5V       | European font        |
| HD66702RA00F   | FP-144A                | 4.5 to 5.5V       | Standard Japanese    |
| HD66702RA00FL  | FP-144A                | 2.7 to 5.5V       | Standard Japanese    |
| HD66702RA01F   | FP-144A                | 4.5 to 5.5V       | Communication font   |
| HD66702RA02F   | FP-144A                | 4.5 to 5.5V       | European font        |
| HCD66701A00    | 124-pin-chip           | 2.7 to 5.5V       | Standard Japanese    |

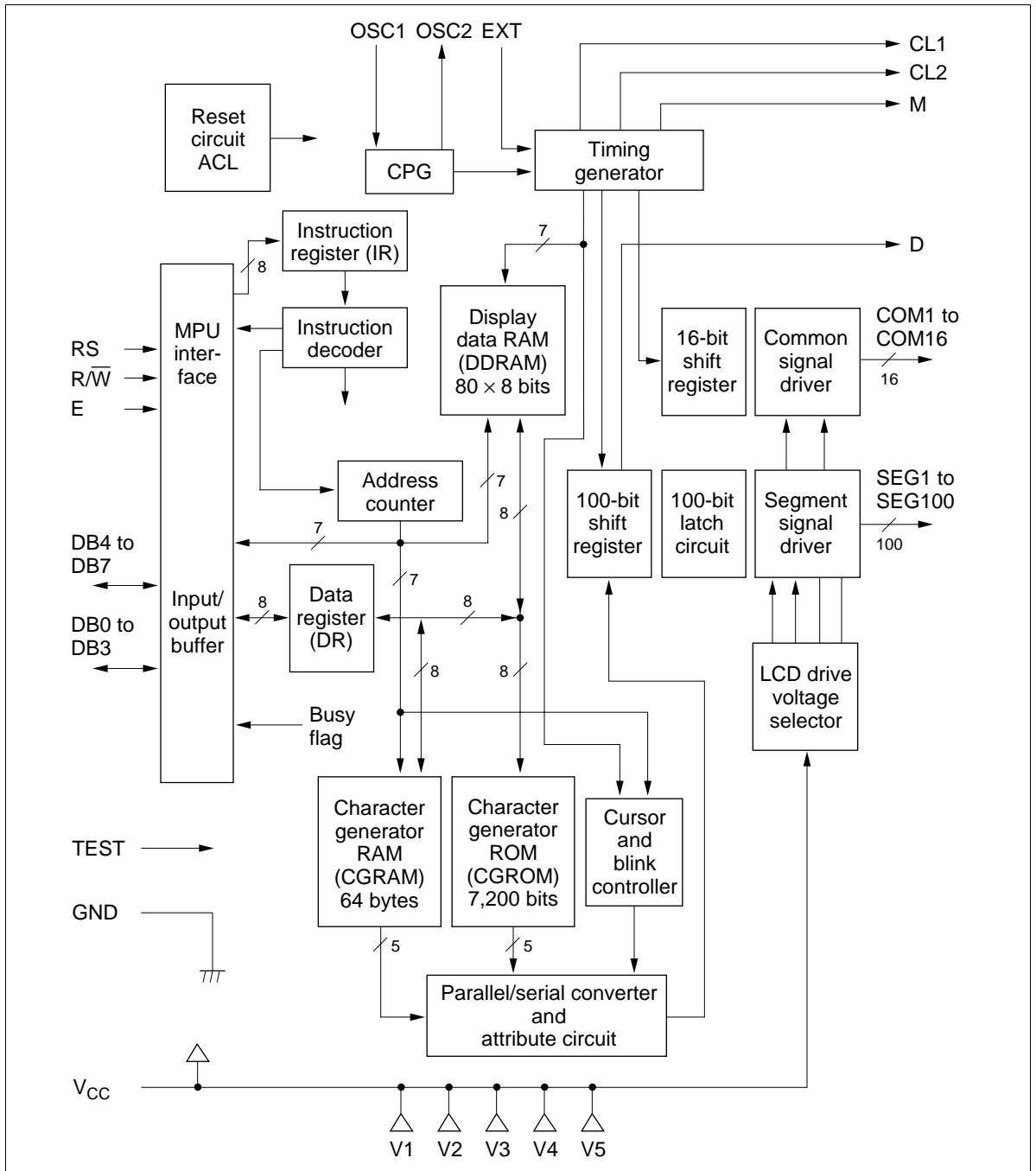
**LCD-II Family Comparison**

| <b>Item</b>  | <b>LCD-II<br/>(HD44780U)</b>  | <b>HD66702<br/>HD66701</b>  | <b>HD66710</b>   | <b>HD66712U</b>  |
|--|---|---|--|--|
| Power supply voltage                                   | 2.7V to 5.5V  | 5 V $\pm$ 10 %<br>(standard)<br>2.7 V to 5.5V<br>(low voltage)  | 2.7V to 5.5V   | 2.7V to 5.5V   |
| Liquid crystal drive voltage                           | 3.0V to 11 V  | 3.0V to 8.3V  | 3.0V to 13.0V  | 2.7V to 11.0V  |
| Maximum display digits per chip                        | 8 characters<br>$\times$ 2 lines  | 20 characters<br>$\times$ 2 lines (HD66702)<br>16 characters<br>$\times$ 2 lines (HD66701)                | 16 characters $\times$<br>2 lines/<br>8 characters $\times$<br>4 lines                             | 24 characters $\times$<br>2 lines/<br>12 characters $\times$<br>4 lines                            |
| Segment display  | None  | None  | 40 segments  | 60 segments  |
| Display duty cycle                                     | 1/8, 1/11, and 1/16   | 1/8, 1/11, and 1/16   | 1/17 and 1/33  | 1/17 and 1/33  |
| CGROM  | 9,920 bits<br>(208 $5 \times 8$ dot<br>characters and 32<br>$5 \times 10$ dot<br>characters)              | 7,200 bits<br>(160 $5 \times 7$ dot<br>characters and 32<br>$5 \times 10$ dot<br>characters)              | 9,600 bits<br>(240 $5 \times 8$ dot<br>characters)   | 9,600 bits<br>(240 $5 \times 8$ dot<br>characters)   |
| CGRAM  | 64 bytes  | 64 bytes  | 64 bytes   | 64 bytes   |
| DDRAM  | 80 bytes  | 80 bytes  | 80 bytes   | 80 bytes   |
| SEGRAM   | None  | None  | 8 bytes  | 16 bytes   |
| Segment signals  | 40  | 100 (HD66702)<br>80 (HD66701)   | 40   | 60   |
| Common signals   | 16  | 16  | 33   | 34   |
| Liquid crystal drive waveform                          | A   | B   | B  | B  |
| Bleeder resistor for LCD power supply                  | External<br>(adjustable)  | External<br>(adjustable)  | External<br>(adjustable)   | External<br>(adjustable)   |
| Clock source   | External resistor or<br>external clock  | External resistor or<br>external clock  | External resistor<br>or external clock   | External resistor or<br>external clock   |
| R <sub>f</sub> oscillation frequency (frame frequency) | 270 kHz $\pm$ 30%<br>(59 to 110 Hz for<br>1/8 and 1/16 duty<br>cycle; 43 to 80 Hz<br>for 1/11 duty cycle) | 320 kHz $\pm$ 30%<br>(70 to 130 Hz for<br>1/8 and 1/16 duty<br>cycle; 51 to 95 Hz<br>for 1/11 duty cycle) | 270 kHz $\pm$ 30%<br>(56 to 103 Hz for<br>1/17 duty cycle;<br>57 to 106 Hz for<br>1/33 duty cycle) | 270 kHz $\pm$ 30%<br>(56 to 103 Hz for<br>1/17 duty cycle;<br>57 to 106 Hz for<br>1/33 duty cycle) |
| R <sub>f</sub> resistance                              | 91 k $\Omega$ : 5-V<br>operation;<br>75 k $\Omega$ : 3-V<br>operation                                     | 68 k $\Omega$ : 5-V<br>operation;<br>56 k $\Omega$ : (3-V<br>operation)                                   | 91 k $\Omega$ : 5-V<br>operation;<br>75 k $\Omega$ : 3-V<br>operation                              | 130 k $\Omega$ : 5-V<br>operation<br>110 k $\Omega$ : 3-V<br>operation                             |

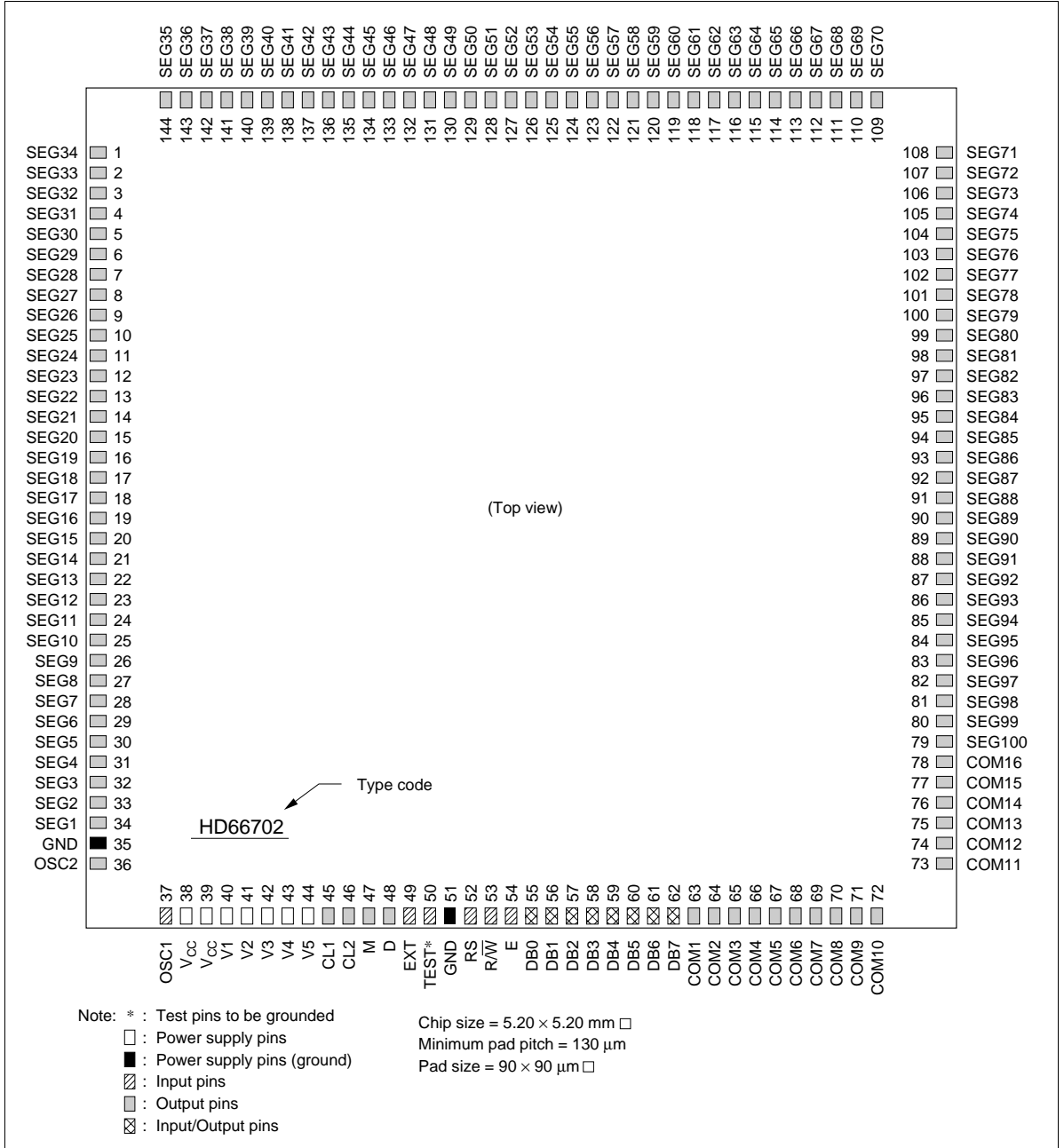
# HD66702/HD66701

| Item                                   | LCD-II<br>(HD44780)                           | HD66702<br>HD66701                              | HD66710  | HD66712U                                      |
|--|---|---|--|---|
| Liquid crystal voltage booster circuit | None  | None  | 2-3 times step-up circuit                          | 2-3 times step-up circuit                     |
| Extension driver control signal        | Independent control signal                    | Independent control signal (HD66702)            | Used in common with a driver output pin            | Independent control signal                    |
| Reset function                         | Power on automatic reset                      | Power on automatic reset                        | Power on automatic reset                           | Power on automatic reset or Reset input       |
| Instructions                           | LCD-II (HD44780)                              | Fully compatible with the LCD-II                | Uppercompatible with the LCD-II                    | Upper compatible with the LCD-II              |
| Number of displayed lines              | 1 or 2  | 1 or 2  | 1, 2, or 4   | 1, 2, or 4                                    |
| Low power mode                         | None  | None  | Available  | Available                                     |
| Horizontal scroll                      | Character unit                                | Character unit                                  | Dot unit   | Dot unit                                      |
| Bus interface                          | 4 bits/8 bits                                 | 4 bits/8 bits                                   | 4 bits/8 bits                                      | Serial;<br>4 bits/8 bits                      |
| CPU bus timing                         | 2 MHz: 5-V operation;<br>1 MHz: 3-V operation | 1 MHz   | 2 MHz: 5-V operation;<br>1 MHz: 3-V operation      | 2 MHz: 5-V operation;<br>1 MHz: 3-V operation |
| Package                                | QFP-1420-80<br>80-pin bare chip               | LQFP-2020-144<br>(HD66702)<br>144-pin bare chip | QFP-1420-100<br>TQFP-1414-100<br>100-pin bare chip | TCP-128<br>128-pin bare chip                  |

HD66702 Block Diagram



## HD66702 Pad Arrangement



## HCD66702 Pad Location Coordinates

| Pad No. | Pad Name | X ( $\mu\text{m}$ ) | Y ( $\mu\text{m}$ ) |
|---------|----------|---------------------|---------------------|
| 1       | SEG34    | -2475               | 2350                |
| 2       | SEG33    | -2475               | 2205                |
| 3       | SEG32    | -2475               | 2065                |
| 4       | SEG31    | -2475               | 1925                |
| 5       | SEG30    | -2475               | 1790                |
| 6       | SEG29    | -2475               | 1655                |
| 7       | SEG28    | -2475               | 1525                |
| 8       | SEG27    | -2475               | 1395                |
| 9       | SEG26    | -2475               | 1265                |
| 10      | SEG25    | -2475               | 1135                |
| 11      | SEG24    | -2475               | 1005                |
| 12      | SEG23    | -2475               | 875                 |
| 13      | SEG22    | -2475               | 745                 |
| 14      | SEG21    | -2475               | 615                 |
| 15      | SEG20    | -2475               | 485                 |
| 16      | SEG19    | -2475               | 355                 |
| 17      | SEG18    | -2475               | 225                 |
| 18      | SEG17    | -2475               | 95                  |
| 19      | SEG16    | -2475               | -35                 |
| 20      | SEG15    | -2475               | -165                |
| 21      | SEG14    | -2475               | -295                |
| 22      | SEG13    | -2475               | -425                |
| 23      | SEG12    | -2475               | -555                |
| 24      | SEG11    | -2475               | -685                |
| 25      | SEG10    | -2475               | -815                |
| 26      | SEG9     | -2475               | -945                |
| 27      | SEG8     | -2475               | -1075               |
| 28      | SEG7     | -2475               | -1205               |
| 29      | SEG6     | -2475               | -1335               |
| 30      | SEG5     | -2475               | -1465               |

| Pad No. | Pad Name        | X ( $\mu\text{m}$ ) | Y ( $\mu\text{m}$ ) |
|---------|-----------------|---------------------|---------------------|
| 31      | SEG4            | -2475               | -1600               |
| 32      | SEG3            | -2475               | -1735               |
| 33      | SEG2            | -2475               | -1870               |
| 34      | SEG1            | -2475               | -2010               |
| 35      | GND             | -2475               | -2180               |
| 36      | OSC2            | -2475               | -2325               |
| 37      | OSC1            | -2445               | -2475               |
| 38      | V <sub>cc</sub> | -2305               | -2475               |
| 39      | V <sub>cc</sub> | -2165               | -2475               |
| 40      | V1              | -2025               | -2475               |
| 41      | V2              | -1875               | -2475               |
| 42      | V3              | -1745               | -2475               |
| 43      | V4              | -1595               | -2475               |
| 44      | V5              | -1465               | -2475               |
| 45      | CL1             | -1335               | -2475               |
| 46      | CL2             | -1185               | -2475               |
| 47      | M               | -1055               | -2475               |
| 48      | D               | -905                | -2475               |
| 49      | EXT             | -775                | -2475               |
| 50      | TEST            | -625                | -2475               |
| 51      | GND             | -495                | -2475               |
| 52      | RS              | -345                | -2475               |
| 53      | R/W             | -195                | -2475               |
| 54      | E               | -45                 | -2475               |
| 55      | DB0             | 85                  | -2475               |
| 56      | DB1             | 235                 | -2475               |
| 57      | DB2             | 365                 | -2475               |
| 58      | DB3             | 515                 | -2475               |
| 59      | DB4             | 645                 | -2475               |
| 60      | DB5             | 795                 | -2475               |

# HD66702/HD66701

| Pad No. | Pad Name | X (μm) | Y (μm) |
|---------|----------|--------|--------|
| 61      | DB6      | 925    | -2475  |
| 62      | DB7      | 1075   | -2475  |
| 63      | COM1     | 1205   | -2475  |
| 64      | COM2     | 1335   | -2475  |
| 65      | COM3     | 1465   | -2475  |
| 66      | COM4     | 1595   | -2475  |
| 67      | COM5     | 1725   | -2475  |
| 68      | COM6     | 1855   | -2475  |
| 69      | COM7     | 1990   | -2475  |
| 70      | COM8     | 2125   | -2475  |
| 71      | COM9     | 2265   | -2475  |
| 72      | COM10    | 2410   | -2475  |
| 73      | COM11    | 2475   | -2290  |
| 74      | COM12    | 2475   | -2145  |
| 75      | COM13    | 2475   | -2005  |
| 76      | COM14    | 2475   | -1865  |
| 77      | COM15    | 2475   | -1730  |
| 78      | COM16    | 2475   | -1595  |
| 79      | SEG100   | 2475   | -1465  |
| 80      | SEG99    | 2475   | -1335  |
| 81      | SEG98    | 2475   | -1205  |
| 82      | SEG97    | 2475   | -1075  |
| 83      | SEG96    | 2475   | -945   |
| 84      | SEG95    | 2475   | -815   |
| 85      | SEG94    | 2475   | -685   |
| 86      | SEG93    | 2475   | -555   |
| 87      | SEG92    | 2475   | -425   |
| 88      | SEG91    | 2475   | -295   |
| 89      | SEG90    | 2475   | -165   |
| 90      | SEG89    | 2475   | -35    |

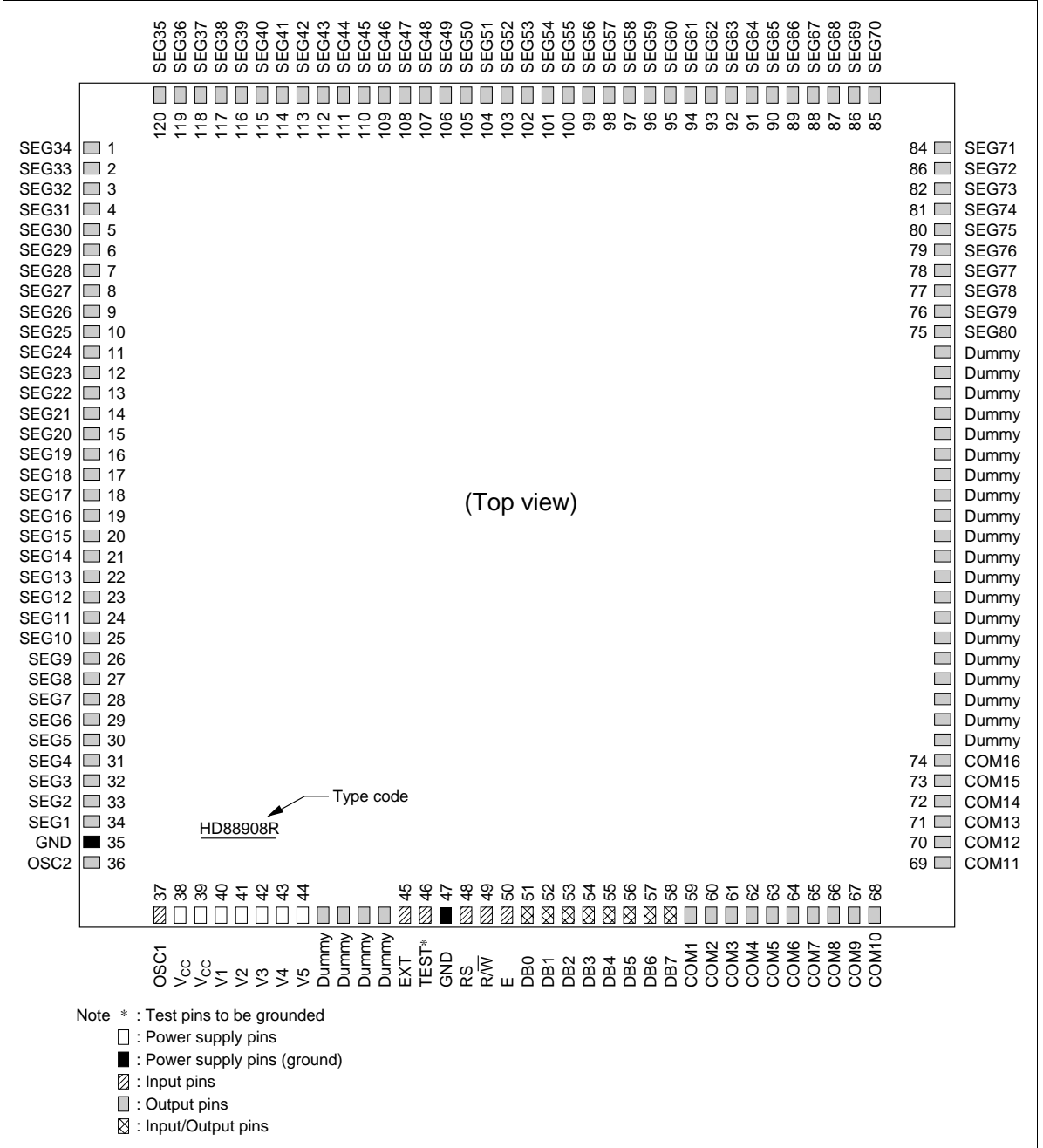
| Pad No. | Pad Name | X (μm) | Y (μm) |
|---------|----------|--------|--------|
| 91      | SEG88    | 2475   | 95     |
| 92      | SEG87    | 2475   | 225    |
| 93      | SEG86    | 2475   | 355    |
| 94      | SEG85    | 2475   | 485    |
| 95      | SEG84    | 2475   | 615    |
| 96      | SEG83    | 2475   | 745    |
| 97      | SEG82    | 2475   | 875    |
| 98      | SEG81    | 2475   | 1005   |
| 99      | SEG80    | 2475   | 1135   |
| 100     | SEG79    | 2475   | 1265   |
| 101     | SEG78    | 2475   | 1395   |
| 102     | SEG77    | 2475   | 1525   |
| 103     | SEG76    | 2475   | 1655   |
| 104     | SEG75    | 2475   | 1790   |
| 105     | SEG74    | 2475   | 1925   |
| 106     | SEG73    | 2475   | 2065   |
| 107     | SEG72    | 2475   | 2205   |
| 108     | SEG71    | 2475   | 2350   |
| 109     | SEG70    | 2320   | 2475   |
| 110     | SEG69    | 2175   | 2475   |
| 111     | SEG68    | 2035   | 2475   |
| 112     | SEG67    | 1895   | 2475   |
| 113     | SEG66    | 1760   | 2475   |
| 114     | SEG65    | 1625   | 2475   |
| 115     | SEG64    | 1495   | 2475   |
| 116     | SEG63    | 1365   | 2475   |
| 117     | SEG62    | 1235   | 2475   |
| 118     | SEG61    | 1105   | 2475   |
| 119     | SEG60    | 975    | 2475   |
| 120     | SEG59    | 845    | 2475   |

| <b>Pad No.</b> | <b>Pad Name</b> | <b>X (μm)</b> | <b>Y (μm)</b> | <b>Pad No.</b> | <b>Pad Name</b> | <b>X (μm)</b> | <b>Y (μm)</b> |
|----------------|-----------------|---------------|---------------|----------------|-----------------|---------------|---------------|
| 121            | SEG58           | 715           | 2475          | 133            | SEG46           | -845          | 2475          |
| 122            | SEG57           | 585           | 2475          | 134            | SEG45           | -975          | 2475          |
| 123            | SEG56           | 455           | 2475          | 135            | SEG44           | -1105         | 2475          |
| 124            | SEG55           | 325           | 2475          | 136            | SEG43           | -1235         | 2475          |
| 125            | SEG54           | 195           | 2475          | 137            | SEG42           | -1365         | 2475          |
| 126            | SEG53           | 65            | 2475          | 138            | SEG41           | -1495         | 2475          |
| 127            | SEG52           | -65           | 2475          | 139            | SEG40           | -1625         | 2475          |
| 128            | SEG51           | -195          | 2475          | 140            | SEG39           | -1760         | 2475          |
| 129            | SEG50           | -325          | 2475          | 141            | SEG38           | -1895         | 2475          |
| 130            | SEG49           | -455          | 2475          | 142            | SEG37           | -2035         | 2475          |
| 131            | SEG48           | -585          | 2475          | 143            | SEG36           | -2175         | 2475          |
| 132            | SEG47           | -715          | 2475          | 144            | SEG35           | -2320         | 2475          |

Notes: 1. Coordinates originate from the chip center.

2. The above are preliminary specifications, and may be subject to change.

## HD66701 Pad Arrangement



## HCD66701 Pad Location Coordinates

Chip size :  $5.2 \times 5.2 \text{ mm}^2$ , Coordinate : PAD CENTER ( $\mu\text{m}$ ),  
 Orgin : CHIP CENTER, Pad Size :  $90 (\pm 10) \times 90 (\pm 10) \mu\text{m}^2$   
 (The aperture area of a bonding pad)

| Pad No. | Pad Name | X ( $\mu\text{m}$ ) | Y ( $\mu\text{m}$ ) |
|---------|----------|---------------------|---------------------|
| 1       | SEG34    | -2475               | 2350                |
| 2       | SEG33    | -2475               | 2205                |
| 3       | SEG32    | -2475               | 2065                |
| 4       | SEG31    | -2475               | 1925                |
| 5       | SEG30    | -2475               | 1790                |
| 6       | SEG29    | -2475               | 1655                |
| 7       | SEG28    | -2475               | 1525                |
| 8       | SEG27    | -2475               | 1395                |
| 9       | SEG26    | -2475               | 1265                |
| 10      | SEG25    | -2475               | 1135                |
| 11      | SEG24    | -2475               | 1005                |
| 12      | SEG23    | -2475               | 875                 |
| 13      | SEG22    | -2475               | 745                 |
| 14      | SEG21    | -2475               | 615                 |
| 15      | SEG20    | -2475               | 485                 |
| 16      | SEG19    | -2475               | 355                 |
| 17      | SEG18    | -2475               | 225                 |
| 18      | SEG17    | -2475               | 95                  |
| 19      | SEG16    | -2475               | -35                 |
| 20      | SEG15    | -2475               | -165                |
| 21      | SEG14    | -2475               | -295                |
| 22      | SEG13    | -2475               | -425                |
| 23      | SEG12    | -2475               | -555                |
| 24      | SEG11    | -2475               | -685                |
| 25      | SEG10    | -2475               | -815                |
| 26      | SEG9     | -2475               | -945                |
| 27      | SEG8     | -2475               | -1075               |
| 28      | SEG7     | -2475               | -1205               |
| 29      | SEG6     | -2475               | -1335               |
| 30      | SEG5     | -2475               | -1465               |

| Pad No. | Pad Name        | X ( $\mu\text{m}$ ) | Y ( $\mu\text{m}$ ) |
|---------|-----------------|---------------------|---------------------|
| 31      | SEG4            | -2475               | -1600               |
| 32      | SEG3            | -2475               | -1735               |
| 33      | SEG2            | -2475               | -1870               |
| 34      | SEG1            | -2475               | -2010               |
| 35      | GND             | -2475               | -2180               |
| 36      | OSC2            | -2475               | -2325               |
| 37      | OSC1            | -2475               | -2475               |
| 38      | V <sub>cc</sub> | -2305               | -2475               |
| 39      | V <sub>cc</sub> | -2165               | -2475               |
| 40      | V1              | -2025               | -2475               |
| 41      | V2              | -1875               | -2475               |
| 42      | V3              | -1745               | -2475               |
| 43      | V4              | -1595               | -2475               |
| 44      | V5              | -1465               | -2475               |
| —       | Dummy           | -1335               | -2475               |
| —       | Dummy           | -1185               | -2475               |
| —       | Dummy           | -1055               | -2475               |
| —       | Dummy           | -905                | -2475               |
| 45      | EXT             | -775                | -2475               |
| 46      | TEST            | -625                | -2475               |
| 47      | GND             | -495                | -2475               |
| 48      | RS              | -345                | -2475               |
| 49      | R/W             | -195                | -2475               |
| 50      | E               | -45                 | -2475               |
| 51      | DB0             | 85                  | -2475               |
| 52      | DB1             | 235                 | -2475               |
| 53      | DB2             | 365                 | -2475               |
| 54      | DB3             | 515                 | -2475               |
| 55      | DB4             | 645                 | -2475               |
| 56      | DB5             | 795                 | -2475               |

**HD66702/HD66701**

| <b>Pad No.</b> | <b>Pad Name</b> | <b>X (μm)</b> | <b>Y (μm)</b> |
|----------------|-----------------|---------------|---------------|
| 57             | DB6             | 925           | -2475         |
| 58             | DB7             | 1075          | -2475         |
| 59             | COM1            | 1205          | -2475         |
| 60             | COM2            | 1335          | -2475         |
| 61             | COM3            | 1465          | -2475         |
| 62             | COM4            | 1595          | -2475         |
| 63             | COM5            | 1725          | -2475         |
| 64             | COM6            | 1855          | -2475         |
| 65             | COM7            | 1990          | -2475         |
| 66             | COM8            | 2125          | -2475         |
| 67             | COM9            | 2265          | -2475         |
| 68             | COM10           | 2410          | -2475         |
| 69             | COM11           | 2475          | -2290         |
| 70             | COM12           | 2475          | -2145         |
| 71             | COM13           | 2475          | -2005         |
| 72             | COM14           | 2475          | -1865         |
| 73             | COM15           | 2475          | -1730         |
| 74             | COM16           | 2475          | -1595         |
| —              | Dummy           | 2475          | -1465         |
| —              | Dummy           | 2475          | -1335         |
| —              | Dummy           | 2475          | -1205         |
| —              | Dummy           | 2475          | -1075         |
| —              | Dummy           | 2475          | -945          |
| —              | Dummy           | 2475          | -815          |
| —              | Dummy           | 2475          | -685          |
| —              | Dummy           | 2475          | -555          |
| —              | Dummy           | 2475          | -425          |
| —              | Dummy           | 2475          | -295          |
| —              | Dummy           | 2475          | -165          |
| —              | Dummy           | 2475          | -35           |

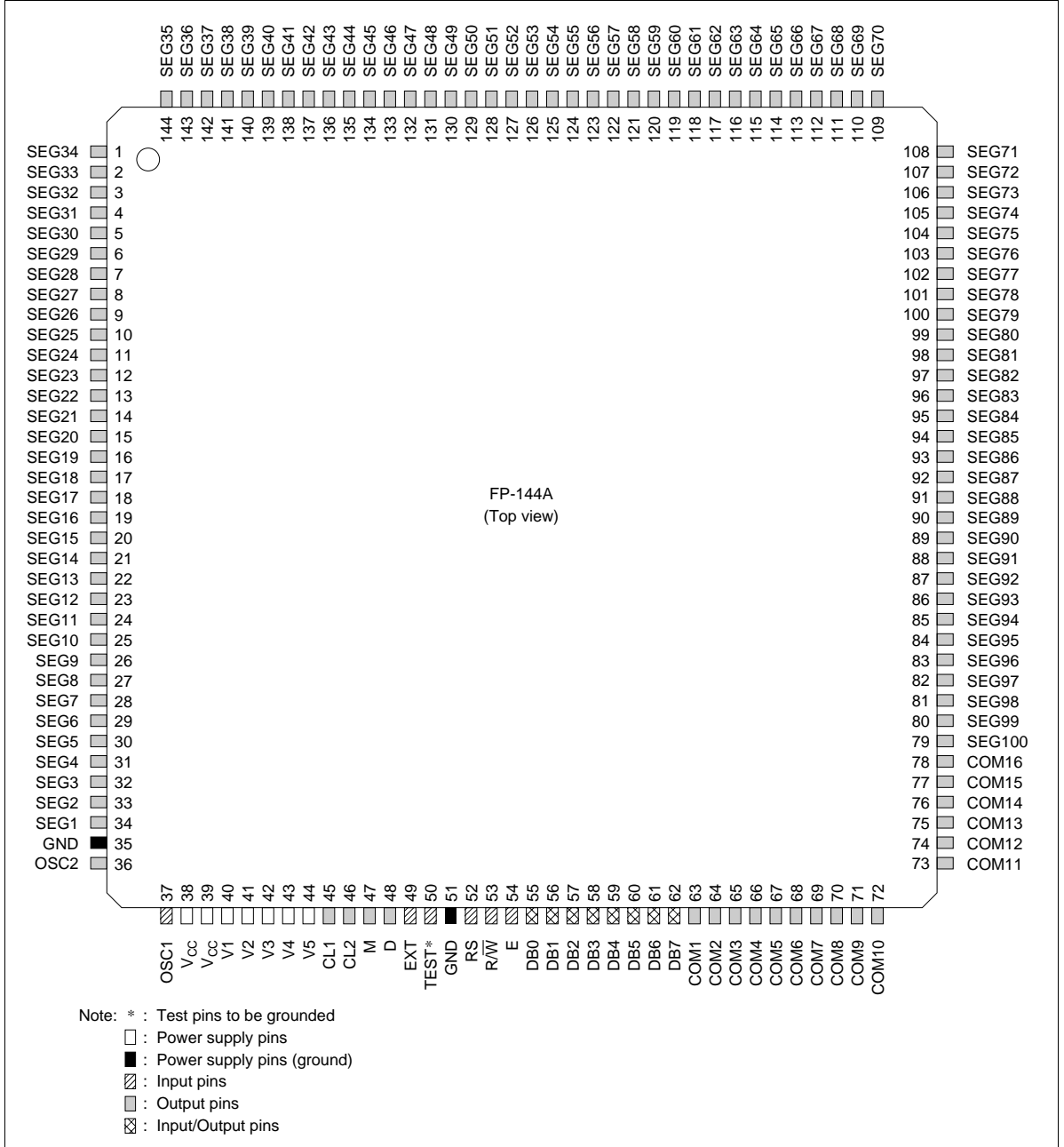
| <b>Pad No.</b> | <b>Pad Name</b> | <b>X (μm)</b> | <b>Y (μm)</b> |
|----------------|-----------------|---------------|---------------|
| —              | Dummy           | 2475          | 95            |
| —              | Dummy           | 2475          | 225           |
| —              | Dummy           | 2475          | 355           |
| —              | Dummy           | 2475          | 485           |
| 75             | SEG80           | 2475          | 615           |
| 76             | SEG79           | 2475          | 745           |
| 77             | SEG78           | 2475          | 875           |
| 78             | SEG77           | 2475          | 1005          |
| 79             | SEG76           | 2475          | 1135          |
| 80             | SEG75           | 2475          | 1265          |
| 81             | SEG74           | 2475          | 1395          |
| 82             | SEG73           | 2475          | 1525          |
| 83             | SEG72           | 2475          | 1655          |
| 84             | SEG71           | 2475          | 1790          |
| 85             | SEG70           | 2475          | 1925          |
| 86             | SEG69           | 2475          | 2065          |
| 87             | SEG68           | 2475          | 2205          |
| 88             | SEG67           | 2475          | 2350          |
| 89             | SEG66           | 2320          | 2475          |
| 90             | SEG65           | 2175          | 2475          |
| 91             | SEG64           | 2035          | 2475          |
| 92             | SEG63           | 1895          | 2475          |
| 93             | SEG62           | 1760          | 2475          |
| 94             | SEG61           | 1625          | 2475          |
| 95             | SEG60           | 1495          | 2475          |
| 96             | SEG59           | 1365          | 2475          |
| 97             | SEG58           | 1235          | 2475          |
| 98             | SEG57           | 1105          | 2475          |
| 99             | SEG56           | 975           | 2475          |
| 100            | SEG55           | 845           | 2475          |

| <b>Pad No.</b> | <b>Pad Name</b> | <b>X (μm)</b> | <b>Y (μm)</b> | <b>Pad No.</b> | <b>Pad Name</b> | <b>X (μm)</b> | <b>Y (μm)</b> |
|----------------|-----------------|---------------|---------------|----------------|-----------------|---------------|---------------|
| 101            | SEG54           | 195           | 2475          | 111            | SEG44           | -1105         | 2475          |
| 102            | SEG53           | 65            | 2475          | 112            | SEG43           | -1235         | 2475          |
| 103            | SEG52           | -65           | 2475          | 113            | SEG42           | -1365         | 2475          |
| 104            | SEG51           | -195          | 2475          | 114            | SEG41           | -1495         | 2475          |
| 105            | SEG50           | -325          | 2475          | 115            | SEG40           | -1625         | 2475          |
| 106            | SEG49           | -455          | 2475          | 116            | SEG39           | -1760         | 2475          |
| 107            | SEG48           | -585          | 2475          | 117            | SEG38           | -1895         | 2475          |
| 108            | SEG47           | -715          | 2475          | 118            | SEG37           | -2035         | 2475          |
| 109            | SEG46           | -845          | 2475          | 119            | SEG36           | -2175         | 2475          |
| 110            | SEG45           | -975          | 2475          | 120            | SEG35           | -2320         | 2475          |

Notes: 1. Coordinates originate from the chip center.

2. The above are preliminary specifications, and may be subject to change.

## HD66702 Pin Arrangement



## Pin Functions

**Table 1 Pin Functional Description**

| Signal  | I/O | Device Interfaced with | Function  |
|---|-----|------------------------|---|
| RS  | I   | MPU                    | Selects registers<br>0: Instruction register (for write)<br>Busy flag: address counter (for read)<br>1: Data register (for write and read)  |
| $\overline{R/W}$                                    | I   | MPU                    | Selects read or write<br>0: Write<br>1: Read  |
| E   | I   | MPU                    | Starts data read/write  |
| DB4 to DB7  | I/O | MPU                    | Four high order bidirectional tristate data bus pins. Used for data transfer between the MPU and the HD66701/2. DB7 can be used as a busy flag.   |
| DB0 to DB3  | I/O | MPU                    | Four low order bidirectional tristate data bus pins. Used for data transfer between the MPU and the HD66701/2. These pins are not used during 4-bit operation.  |
| CL1 (HD66702)                                       | O   | Extension driver       | Clock to latch serial data D sent to the extension driver   |
| CL2 (HD66702)                                       | O   | Extension driver       | Clock to shift serial data D  |
| M (HD66702)   | O   | Extension driver       | Switch signal for converting the liquid crystal drive waveform to AC  |
| D (HD66702)   | O   | Extension driver       | Character pattern data corresponding to each segment signal   |
| COM1 to COM16                                       | O   | LCD                    | Common signals that are not used are changed to non-selection waveforms. COM9 to COM16 are non-selection waveforms at 1/8 duty factor and COM12 to COM16 are non-selection waveforms at 1/11 duty factor. |
| SEG1 to SEG100 (HD66702)<br>SEG1 to SEG80 (HD66701) | O   | LCD                    | Segment signals   |
| V1 to V5  | —   | Power supply           | Power supply for LCD drive  |
| $V_{CC}$ , GND                                      | —   | Power supply           | $V_{CC}$ : +5V or +3V, GND: 0V  |
| TEST  | I   | —                      | Test pin, which must be grounded  |
| EXT   | I   | —                      | 0: Enables extension driver control signals CL1, CL2, M, and D to be output from its corresponding pins.<br>1: Drives CL1, CL2, M, and D as tristate, lowering power dissipation.                         |
| OSC1, OSC2  | —   | —                      | Pins for connecting the registers of the internal clock oscillation. When the pin input is an external clock, it must be input to OSC1.   |

## Function Description

### Registers

The HD66701/2 has two 8-bit registers, an instruction register (IR) and a data register (DR).

The IR stores instruction codes, such as display clear and cursor shift, and address information for display data RAM (DDRAM) and character generator RAM (CGRAM). The IR can only be written from the MPU.

The DR temporarily stores data to be written into DDRAM or CGRAM. Data written into the DR from the MPU is automatically written into DDRAM or CGRAM by an internal operation. The DR is also used for data storage when reading data from DDRAM or CGRAM. When address information is written into the IR, data is read and then stored into the DR from DDRAM or CGRAM by an internal operation. Data transfer between the MPU is then completed when the MPU reads the DR. After the read, data in DDRAM or CGRAM at the next address is sent to the DR for the next read from the MPU. By the register selector (RS) signal, these two registers can be selected (Table 2).

### Busy Flag (BF)

When the busy flag is 1, the HD66701/2 is in the internal operation mode, and the next instruction will not be accepted. When  $RS = 0$  and  $R/\overline{W} = 1$  (Table 2), the busy flag is output to DB7. The next instruction must be written after ensuring that the busy flag is 0.

### Address Counter (AC)

The address counter (AC) assigns addresses to both DDRAM and CGRAM. When an address of an instruction is written into the IR, the address information is sent from the IR to the AC. Selection of either DDRAM or CGRAM is also determined concurrently by the instruction.

After writing into (reading from) DDRAM or CGRAM, the AC is automatically incremented by 1 (decremented by 1). The AC contents are then output to DB0 to DB6 when  $RS = 0$  and  $R/\overline{W} = 1$  (Table 2).

**Table 2 Register Selection**

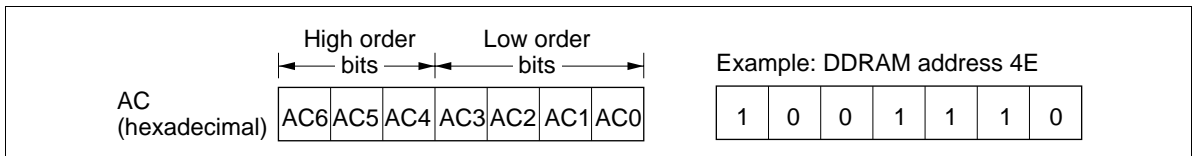
| <b>RS</b> | <b>R/<math>\overline{W}</math></b> | <b>Operation</b>   |
|-----------|------------------------------------|--|
| 0         | 0                                  | IR write as an internal operation (display clear, etc.)  |
| 0         | 1                                  | Read busy flag (DB7) and address counter (DB0 to DB6)    |
| 1         | 0                                  | DR write as an internal operation (DR to DDRAM or CGRAM) |
| 1         | 1                                  | DR read as an internal operation (DDRAM or CGRAM to DR)  |

**Display Data RAM (DDRAM)**

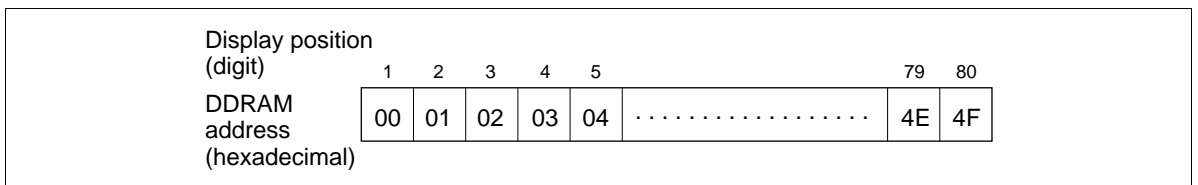
Display data RAM (DDRAM) stores display data represented in 8-bit character codes. Its extended capacity is  $80 \times 8$  bits, or 80 characters. The area in display data RAM (DDRAM) that is not used for display can be used as general data RAM. See Figure 1 for the relationships between DDRAM addresses and positions on the liquid crystal display.

The DDRAM address ( $A_{DD}$ ) is set in the address counter (AC) as hexadecimal.

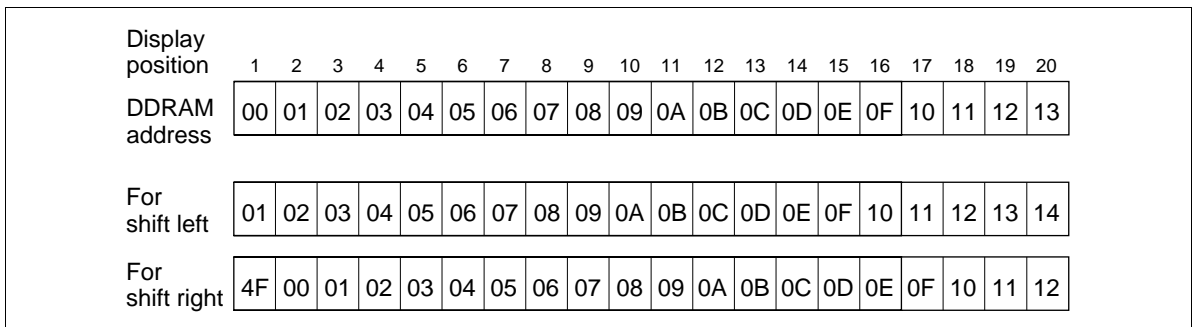
- 1-line display ( $N = 0$ ) (Figure 2)
  - When there are fewer than 80 display characters, the display begins at the head position. For example, if using only the HD66702, 20 characters are displayed. See Figure 3.
  - When the display shift operation is performed, the DDRAM address shifts. See Figure 3.



**Figure 1 DDRAM Address**



**Figure 2 1-Line Display**



**Figure 3 1-Line by 20-Character Display Example**

- 2-line display (N = 1) (Figure 4)
  - Case 1: When the number of display characters is less than  $40 \times 2$  lines, the two lines are displayed from the head. Note that the first line end address and the second line start address are not consecutive. For example, when just the HD66702 is used, 20 characters  $\times$  2 lines are displayed. See Figure 5.

When display shift operation is performed, the DDRAM address shifts. See Figure 5.

|                             |    |    |    |    |    |       |    |    |
|-----------------------------|----|----|----|----|----|-------|----|----|
| Display position            | 1  | 2  | 3  | 4  | 5  | ..... | 39 | 40 |
| DDRAM address (hexadecimal) | 00 | 01 | 02 | 03 | 04 | ..... | 26 | 27 |
|                             | 40 | 41 | 42 | 43 | 44 | ..... | 66 | 67 |

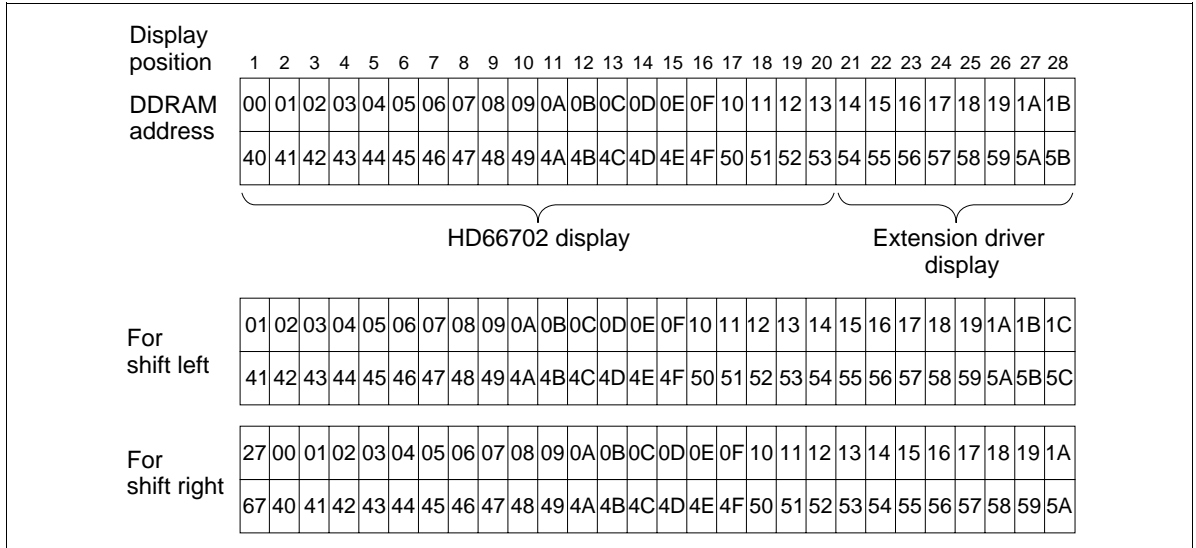
**Figure 4 2-Line Display**

|                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Display position | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 |
| DDRAM address    | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 0A | 0B | 0C | 0D | 0E | 0F | 10 | 11 | 12 | 13 |
|                  | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 | 49 | 4A | 4B | 4C | 4D | 4E | 4F | 50 | 51 | 52 | 53 |
| For shift left   | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 0A | 0B | 0C | 0D | 0E | 0F | 10 | 11 | 12 | 13 | 14 |
|                  | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 | 49 | 4A | 4B | 4C | 4D | 4E | 4F | 50 | 51 | 52 | 53 | 54 |
| For shift right  | 27 | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 0A | 0B | 0C | 0D | 0E | 0F | 10 | 11 | 12 |
|                  | 67 | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 | 49 | 4A | 4B | 4C | 4D | 4E | 4F | 50 | 51 | 52 |

**Figure 5 2-Line by 20-Character Display Example**

— Case 2: For a 28-character × 2-line display, the HD66702 can be extended using one 40-output extension driver. See Figure 6.

When display shift operation is performed, the DDRAM address shifts. See Figure 6.



**Figure 6 2-Line by 28-Character Display Example**

### **Character Generator ROM (CGROM)**

The character generator ROM generates  $5 \times 7$  dot or  $5 \times 10$  dot character patterns from 8-bit character codes (Table 5). It can generate 160  $5 \times 7$  dot character patterns and 32  $5 \times 10$  dot character patterns. User-defined character patterns are also available by mask-programmed ROM.

### **Character Generator RAM (CGRAM)**

In the character generator RAM, the user can rewrite character patterns by program. For  $5 \times 7$  dots, eight character patterns can be written, and for  $5 \times 10$  dots, four character patterns can be written.

Write the character codes at the addresses shown as the left column of Table 5 to show the character patterns stored in CGRAM.

See Table 6 for the relationship between CGRAM addresses and data and display patterns.

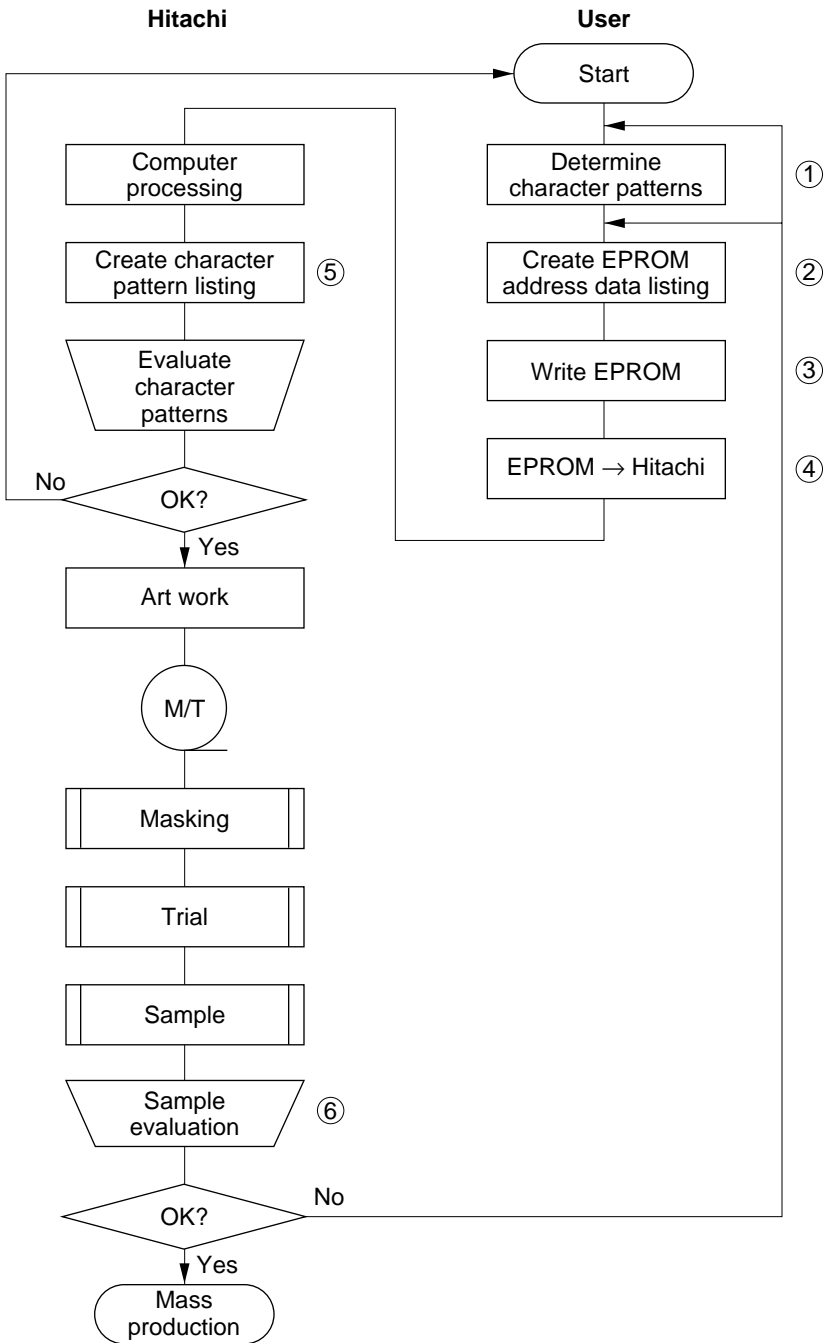
Areas that are not used for display can be used as general data RAM.

### **Modifying Character Patterns**

- Character pattern development procedure

The following operations correspond to the numbers listed in Figure 7:

1. Determine the correspondence between character codes and character patterns.
2. Create a listing indicating the correspondence between EPROM addresses and data.
3. Program the character patterns into the EPROM.
4. Send the EPROM to Hitachi.
5. Computer processing on the EPROM is performed at Hitachi to create a character pattern listing, which is sent to the user.
6. If there are no problems within the character pattern listing, a trial LSI is created at Hitachi and samples are sent to the user for evaluation. When it is confirmed by the user that the character patterns are correctly written, mass production of the LSI proceeds at Hitachi.



Note: For a description of the numbers used in this figure, refer to the preceding page.

Figure 7 Character Pattern Development Procedure

- Programming character patterns

This section explains the correspondence between addresses and data used to program character patterns in EPROM. The HD66702 character generator ROM can generate 160  $5 \times 7$  dot character patterns and 32  $5 \times 10$  dot character patterns for a total of 192 different character patterns.

—  $5 \times 7$  dot character pattern

EPROM address data and character pattern data correspond with each other to form a  $5 \times 7$  dot character pattern (Table 3).

**Table 3 Example of Correspondence between EPROM Address Data and Character Pattern ( $5 \times 7$  dots)**

| EPROM Address |    |    |    |    |    |    |    |    |    | Data |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|----|----|------|----|----|----|----|----|
| A10           | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0   | O4 | O3 | O2 | O1 | O0 |
| 0             | 1  | 0  | 1  | 0  | 0  | 1  | 0  | 0  | 0  | 0    | 1  | 1  | 1  | 1  | 0  |
|               |    |    |    |    |    |    |    | 0  | 0  | 1    | 1  | 0  | 0  | 0  | 1  |
|               |    |    |    |    |    |    |    | 0  | 1  | 0    | 1  | 0  | 0  | 0  | 1  |
|               |    |    |    |    |    |    |    | 0  | 1  | 1    | 1  | 1  | 1  | 1  | 0  |
|               |    |    |    |    |    |    |    | 1  | 0  | 0    | 1  | 0  | 1  | 0  | 0  |
|               |    |    |    |    |    |    |    | 1  | 0  | 1    | 1  | 0  | 0  | 1  | 0  |
|               |    |    |    |    |    |    |    | 1  | 1  | 0    | 1  | 0  | 0  | 0  | 1  |
|               |    |    |    |    |    |    |    | 1  | 1  | 1    | 0  | 0  | 0  | 0  | 0  |

Character code
Line position

← Fill line 8 (cursor position) with 0s

- Notes:
- EPROM addresses A10 to A3 correspond to a character code.
  - EPROM addresses A2 to A0 specify a line position of the character pattern.
  - EPROM data O4 to O0 correspond to character pattern data.
  - A lit display position (black) corresponds to a 1.
  - Line 8 (cursor position) of the character pattern must be blanked with 0s.
  - EPROM data O5 to O7 are not used.



Table 5 Correspondence between Character Codes and Character Patterns (ROM code: A00)

(HD66701/HD66702)

| Lower 4 Bits \ Upper 4 Bits | 0000       | 0010 | 0011 | 0100 | 0101 | 0110 | 0111 | 1010 | 1011 | 1100 | 1101 | 1110 | 1111  |
|-----------------------------|------------|------|------|------|------|------|------|------|------|------|------|------|---|
| xxxx0000                    | CG RAM (1) |      | 0    | a    | P    | `    | P    |      | -    | 9    | 3    | e    | p   |
| xxxx0001                    | (2)        | !    | 1    | A    | Q    | a    | q    | a    | 7    | 7    | 4    | ä    | q   |
| xxxx0010                    | (3)        | "    | 2    | B    | R    | b    | r    | r    | イ    | ツ    | ×    | ß    | ö   |
| xxxx0011                    | (4)        | #    | 3    | C    | S    | c    | s    | レ    | ウ    | テ    | エ    | z    | ø   |
| xxxx0100                    | (5)        | \$   | 4    | D    | T    | d    | t    | 、    | 工    | ト    | ト    | μ    | o   |
| xxxx0101                    | (6)        | %    | 5    | E    | U    | e    | u    | ・    | オ    | ナ    | ナ    | ö    | ü   |
| xxxx0110                    | (7)        | &    | 6    | F    | V    | f    | v    | ヲ    | カ    | ニ    | ヨ    | ρ    | Σ   |
| xxxx0111                    | (8)        | '    | 7    | G    | W    | g    | w    | ア    | †    | 又    | ウ    | g    | π   |
| xxxx1000                    | (1)        | (    | 8    | H    | X    | h    | x    | イ    | ウ    | ホ    | リ    | r    | ×   |
| xxxx1001                    | (2)        | )    | 9    | I    | Y    | i    | y    | ウ    | ウ    | ル    | ル    | ı    | y   |
| xxxx1010                    | (3)        | *    | :    | J    | Z    | j    | z    | 工    | コ    | ン    | ク    | j    | 7   |
| xxxx1011                    | (4)        | +    | ;    | K    | C    | k    | c    | レ    | オ    | サ    | ヒ    | ×    | π   |
| xxxx1100                    | (5)        | ,    | <    | L    | †    | l    | l    | レ    | シ    | フ    | ウ    | φ    | π   |
| xxxx1101                    | (6)        | -    | =    | M    | I    | m    | ı    | ユ    | ズ    | レ    | ウ    | ı    | ÷   |
| xxxx1110                    | (7)        | .    | >    | N    | ^    | n    | →    | ヨ    | セ    | ホ    | °    | ñ    |   |
| xxxx1111                    | (8)        | /    | ?    | O    | _    | o    | ←    | ウ    | リ    | マ    | °    | ö    |  |

Note: The user can specify any pattern for character-generator RAM.

Table 5 Correspondence between Character Codes and Character Patterns (ROM code: A01)

(HD66702)

| Lower 4 Bits \ Upper 4 Bits | 0000       | 0010 | 0011 | 0100 | 0101 | 0110 | 0111 | 1010 | 1011 | 1100 | 1101 | 1110 | 1111 |
|-----------------------------|------------|------|------|------|------|------|------|------|------|------|------|------|------|
| xxxx0000                    | CG RAM (1) |      | 0    | a    | P    | `    | F    | u    | -    | 夕    | 三    | 月    | 夕    |
| xxxx0001                    | (2)        | !    | 1    | A    | Q    | a    | q    | a    | フ    | チ    | 夕    | 日    | 夕    |
| xxxx0010                    | (3)        | "    | 2    | B    | R    | b    | r    | フ    | イ    | ツ    | 夕    | 夕    | 夕    |
| xxxx0011                    | (4)        | #    | 3    | C    | S    | c    | s    | フ    | ウ    | テ    | 夕    | 夕    | 夕    |
| xxxx0100                    | (5)        | \$   | 4    | D    | T    | d    | t    | フ    | エ    | ト    | 夕    | 夕    | 夕    |
| xxxx0101                    | (6)        | %    | 5    | E    | U    | e    | u    | フ    | オ    | ナ    | 夕    | 夕    | 夕    |
| xxxx0110                    | (7)        | &    | 6    | F    | V    | f    | v    | フ    | カ    | ニ    | 夕    | 夕    | 夕    |
| xxxx0111                    | (8)        | '    | 7    | G    | W    | g    | w    | フ    | ク    | 夕    | 夕    | 夕    | 夕    |
| xxxx1000                    | (1)        | (    | 8    | H    | X    | h    | x    | フ    | イ    | 夕    | 夕    | 夕    | 夕    |
| xxxx1001                    | (2)        | )    | 9    | I    | Y    | i    | y    | フ    | ウ    | 夕    | 夕    | 夕    | 夕    |
| xxxx1010                    | (3)        | *    | :    | J    | Z    | j    | z    | フ    | エ    | 夕    | 夕    | 夕    | 夕    |
| xxxx1011                    | (4)        | +    | ;    | K    | C    | k    | c    | フ    | オ    | 夕    | 夕    | 夕    | 夕    |
| xxxx1100                    | (5)        | ,    | <    | L    | #    | l    | l    | フ    | シ    | 夕    | 夕    | 夕    | 夕    |
| xxxx1101                    | (6)        | -    | =    | M    | I    | m    | >    | フ    | ス    | 夕    | 夕    | 夕    | 夕    |
| xxxx1110                    | (7)        | .    | >    | N    | ^    | n    | →    | フ    | セ    | 夕    | 夕    | 夕    | 夕    |
| xxxx1111                    | (8)        | /    | ?    | O    | _    | o    | ←    | フ    | ソ    | 夕    | 夕    | 夕    | 夕    |

Table 5 Correspondence between Character Codes and Character Patterns (ROM code: A02)

(HD66702)

| Lower 4 Bits \ Upper 4 Bits | 0000       | 0010 | 0011 | 0100 | 0101 | 0110 | 0111 | 1010 | 1011 | 1100 | 1101 | 1110 | 1111 |
|-----------------------------|------------|------|------|------|------|------|------|------|------|------|------|------|------|
| xxxx0000                    | CG RAM (1) |      | 0    | a    | P    | `    | P    | =    | “    | À    | Ð    | á    | ã    |
| xxxx0001                    | (2)        | !    | 1    | A    | Q    | a    | q    | !    | ”    | Á    | Ñ    | â    | ä    |
| xxxx0010                    | (3)        | "    | 2    | B    | R    | b    | r    | ¢    | Σ    | Â    | ó    | ã    | ó    |
| xxxx0011                    | (4)        | #    | 3    | C    | S    | c    | s    | £    | Ω    | Ã    | ô    | ä    | ô    |
| xxxx0100                    | (5)        | \$   | 4    | D    | T    | d    | t    | ¥    | ϖ    | Ä    | õ    | ä    | õ    |
| xxxx0101                    | (6)        | %    | 5    | E    | U    | e    | u    | ¥    | Π    | Å    | ö    | ä    | ö    |
| xxxx0110                    | (7)        | &    | 6    | F    | V    | f    | v    | !    | ∑    | Æ    | ö    | æ    | ö    |
| xxxx0111                    | (8)        | '    | 7    | G    | W    | g    | w    | 9    | Ω    | ×    | ø    | ÷    | ÷    |
| xxxx1000                    | (1)        | (    | B    | H    | X    | h    | x    | ∑    | ∑    | Æ    | ø    | ø    | ø    |
| xxxx1001                    | (2)        | )    | 9    | I    | Y    | i    | y    | →    | ö    | é    | ó    | é    | ó    |
| xxxx1010                    | (3)        | *    | #    | J    | Z    | j    | z    | ←    | é    | é    | ó    | é    | ó    |
| xxxx1011                    | (4)        | +    | ;    | K    | C    | k    | c    | ←    | Æ    | é    | ó    | é    | ó    |
| xxxx1100                    | (5)        | ,    | <    | L    | †    | l    | l    | ×    | ∑    | í    | ó    | í    | ó    |
| xxxx1101                    | (6)        | -    | =    | M    | I    | m    | )    | ↑    | z    | í    | í    | í    | í    |
| xxxx1110                    | (7)        | .    | >    | N    | ^    | n    | ~    | ↓    | ∑    | í    | í    | í    | í    |
| xxxx1111                    | (8)        | /    | ?    | O    | _    | o    | ±    | '    | z    | í    | í    | í    | í    |

**Table 6 Relationship between CGRAM Addresses, Character Codes (DDRAM) and Character Patterns (CGRAM Data)**

For 5 × 7 dot character patterns

| Character Codes (DDRAM data) |   |   |   |     |   |   |   | CGRAM Address |   |   |   | Character Patterns (CGRAM data) |   |   |   |      |   |   |   |     |   |   |   |   |   |  |  |  |  |  |  |  |  |
|------------------------------|---|---|---|-----|---|---|---|---------------|---|---|---|---------------------------------|---|---|---|------|---|---|---|-----|---|---|---|---|---|--|--|--|--|--|--|--|--|
| 7                            | 6 | 5 | 4 | 3   | 2 | 1 | 0 | 5             | 4 | 3 | 2 | 1                               | 0 | 7 | 6 | 5    | 4 | 3 | 2 | 1   | 0 |   |   |   |   |  |  |  |  |  |  |  |  |
| High                         |   |   |   | Low |   |   |   | High          |   |   |   | Low                             |   |   |   | High |   |   |   | Low |   |   |   |   |   |  |  |  |  |  |  |  |  |
| 0 0 0 0 * 0 0 0              |   |   |   |     |   |   |   | 0 0 0         |   |   |   | 0                               | 0 | 0 | 0 | ↑    | * | * | * | 1   | 1 | 1 | 1 | 0 | ↓ |  |  |  |  |  |  |  |  |
|                              |   |   |   |     |   |   |   |               |   |   |   | 0                               | 0 | 1 | 0 |      | 0 | 0 | 0 | 0   |   |   |   |   |   |  |  |  |  |  |  |  |  |
|                              |   |   |   |     |   |   |   |               |   |   |   | 0                               | 1 | 1 | 0 |      | 0 | 0 | 0 | 0   |   |   |   |   |   |  |  |  |  |  |  |  |  |
|                              |   |   |   |     |   |   |   |               |   |   |   | 1                               | 0 | 0 | 0 |      | 0 | 0 | 0 | 0   |   |   |   |   |   |  |  |  |  |  |  |  |  |
|                              |   |   |   |     |   |   |   |               |   |   |   | 1                               | 0 | 1 | 0 |      | 0 | 0 | 0 | 0   |   |   |   |   |   |  |  |  |  |  |  |  |  |
|                              |   |   |   |     |   |   |   |               |   |   |   | 1                               | 1 | 0 | 0 |      | 0 | 0 | 0 | 0   |   |   |   |   |   |  |  |  |  |  |  |  |  |
|                              |   |   |   |     |   |   |   |               |   |   |   | 1                               | 1 | 1 | 0 |      | 0 | 0 | 0 | 0   |   |   |   |   |   |  |  |  |  |  |  |  |  |
|                              |   |   |   |     |   |   |   |               |   |   |   | 1                               | 1 | 1 | 1 |      | 0 | 0 | 0 | 0   |   |   |   |   |   |  |  |  |  |  |  |  |  |
| 0 0 0 0 * 0 0 1              |   |   |   |     |   |   |   | 0 0 1         |   |   |   | 0                               | 0 | 0 | 0 | ↑    | * | * | * | 1   | 0 | 0 | 0 | 1 | ↓ |  |  |  |  |  |  |  |  |
|                              |   |   |   |     |   |   |   |               |   |   |   | 0                               | 1 | 0 | 0 |      | 0 | 0 | 1 | 0   | 0 |   |   |   |   |  |  |  |  |  |  |  |  |
|                              |   |   |   |     |   |   |   |               |   |   |   | 0                               | 1 | 1 | 0 |      | 0 | 0 | 1 | 0   | 0 |   |   |   |   |  |  |  |  |  |  |  |  |
|                              |   |   |   |     |   |   |   |               |   |   |   | 1                               | 0 | 0 | 0 |      | 0 | 0 | 1 | 0   | 0 |   |   |   |   |  |  |  |  |  |  |  |  |
|                              |   |   |   |     |   |   |   |               |   |   |   | 1                               | 0 | 1 | 0 |      | 0 | 0 | 1 | 0   | 0 |   |   |   |   |  |  |  |  |  |  |  |  |
|                              |   |   |   |     |   |   |   |               |   |   |   | 1                               | 1 | 0 | 0 |      | 0 | 0 | 1 | 0   | 0 |   |   |   |   |  |  |  |  |  |  |  |  |
|                              |   |   |   |     |   |   |   |               |   |   |   | 1                               | 1 | 1 | 0 |      | 0 | 0 | 1 | 0   | 0 |   |   |   |   |  |  |  |  |  |  |  |  |
|                              |   |   |   |     |   |   |   |               |   |   |   | 1                               | 1 | 1 | 1 |      | 0 | 0 | 0 | 0   | 0 |   |   |   |   |  |  |  |  |  |  |  |  |
| 0 0 0 0 * 1 1 1              |   |   |   |     |   |   |   | 1 1 1         |   |   |   | 0                               | 0 | 0 | 0 | ↑    | * | * | * |     |   |   |   | ↓ |   |  |  |  |  |  |  |  |  |
|                              |   |   |   |     |   |   |   |               |   |   |   | 0                               | 0 | 1 | 0 |      |   |   |   |     |   |   |   |   |   |  |  |  |  |  |  |  |  |
|                              |   |   |   |     |   |   |   |               |   |   |   | 1                               | 0 | 1 | 0 |      |   |   |   |     |   |   |   |   |   |  |  |  |  |  |  |  |  |
|                              |   |   |   |     |   |   |   |               |   |   |   | 1                               | 1 | 0 | 0 |      |   |   |   |     |   |   |   |   |   |  |  |  |  |  |  |  |  |
| 1                            | 1 | 1 | 0 |     |   |   |   |               |   |   |   |                                 |   |   |   |      |   |   |   |     |   |   |   |   |   |  |  |  |  |  |  |  |  |

- Notes:
- Character code bits 0 to 2 correspond to CGRAM address bits 3 to 5 (3 bits: 8 types).
  - CGRAM address bits 0 to 2 designate the character pattern line position. The 8th line is the cursor position and its display is formed by a logical OR with the cursor. Maintain the 8th line data, corresponding to the cursor display position, at 0 as the cursor display. If the 8th line data is 1, 1 bits will light up the 8th line regardless of the cursor presence.
  - Character pattern row positions correspond to CGRAM data bits 0 to 4 (bit 4 being at the left). Since CGRAM data bits 5 to 7 are not used for display, they can be used for general data RAM.
  - As shown Tables 5 and 6, CGRAM character patterns are selected when character code bits 4 to 7 are all 0. However, since character code bit 3 has no effect, the R display example above can be selected by either character code 00H or 08H.
  - 1 for CGRAM data corresponds to display selection and 0 to non-selection.
- \* Indicates no effect.

Table 6 Relationship between CGRAM Addresses, Character Codes (DDRAM) and Character Patterns (CGRAM Data) (cont)

For 5 × 10 dot character patterns

| Character Codes (DDRAM data) |  | CGRAM Address |           | Character Patterns (CGRAM data) |           |                     |
|------------------------------|--|---------------|-----------|---------------------------------|-----------|---------------------|
| 7 6 5 4 3 2 1 0              |  | 5 4 3 2 1 0   |           | 7 6 5 4 3 2 1 0                 |           |                     |
| High Low                     |  | High Low      |           | High Low                        |           |                     |
| 0 0 0 0 * 0 0 *              |  | 0 0           | 0 0 0 0   | * * *                           | 0 0 0 0 0 | } Character pattern |
|                              |  |               | 0 0 0 1   | ↑                               | 0 0 0 0 0 |                     |
|                              |  |               | 0 0 1 0   |                                 | 1 0 1 1 0 |                     |
|                              |  |               | 0 0 1 1   |                                 | 1 1 0 0 1 |                     |
|                              |  |               | 0 1 0 0   |                                 | 1 0 0 0 1 |                     |
|                              |  |               | 0 1 0 1   |                                 | 1 0 0 0 1 |                     |
|                              |  |               | 0 1 1 0   |                                 | 1 1 1 1 0 |                     |
|                              |  |               | 0 1 1 1   |                                 | 1 0 0 0 0 |                     |
|                              |  |               | 1 0 0 0   |                                 | 1 0 0 0 0 |                     |
|                              |  |               | 1 0 0 1   |                                 | 1 0 0 0 0 |                     |
| 1 0 1 0                      |  | * * *         | 0 0 0 0 0 | } Cursor position               |           |                     |
| 1 0 1 1                      |  | * * *         | * * * * * |                                 |           |                     |
| 0 0 0 0 * 1 1 *              |  | 1 1           | 1 1 0 0   | ↑                               | * * *     |                     |
|                              |  |               | 1 0 1 0   | ↓                               | * * *     |                     |
|                              |  |               | 1 0 1 1   |                                 | * * * * * |                     |
|                              |  |               | 1 1 0 0   | ↑                               | * * * * * |                     |
|                              |  |               | 1 1 0 1   | ↓                               | * * * * * |                     |
| 1 1 1 0                      |  | * * * * *     |           |                                 |           |                     |
| 1 1 1 1                      |  | * * * * *     |           |                                 |           |                     |

- Notes:
- Character code bits 1 and 2 correspond to CGRAM address bits 4 and 5 (2 bits: 4 types).
  - CGRAM address bits 0 to 3 designate the character pattern line position. The 11th line is the cursor position and its display is formed by a logical OR with the cursor. Maintain the 11th line data corresponding to the cursor display position at 0 as the cursor display. If the 11th line data is 1, 1 bits will light up the 11th line regardless of the cursor presence. Since lines 12 to 16 are not used for display, they can be used for general data RAM.
  - Character pattern row positions are the same as 5 × 7 dot character pattern positions.
  - CGRAM character patterns are selected when character code bits 4 to 7 are all 0. However, since character code bits 0 and 3 have no effect, the P display example above can be selected by character codes 00H, 01H, 08H, and 09H.
  - 1 for CGRAM data corresponds to display selection and 0 to non-selection.
- \* Indicates no effect.

**Timing Generation Circuit**

The timing generation circuit generates timing signals for the operation of internal circuits such as DDRAM, CGROM and CGRAM. RAM read timing for display and internal operation timing by MPU access are generated separately to avoid interfering with each other. Therefore, when writing data to DDRAM, for example, there will be no undesirable interferences, such as flickering, in areas other than the display area.

**Liquid Crystal Display Driver Circuit**

The liquid crystal display driver circuit consists of 16 common signal drivers and 100 segment (HD66702) or 80 segment (HD66701) signal drivers. When the character font and number of lines are selected by a program, the required common signal drivers automatically output drive waveforms, while the other common signal drivers continue to output non-selection waveforms.

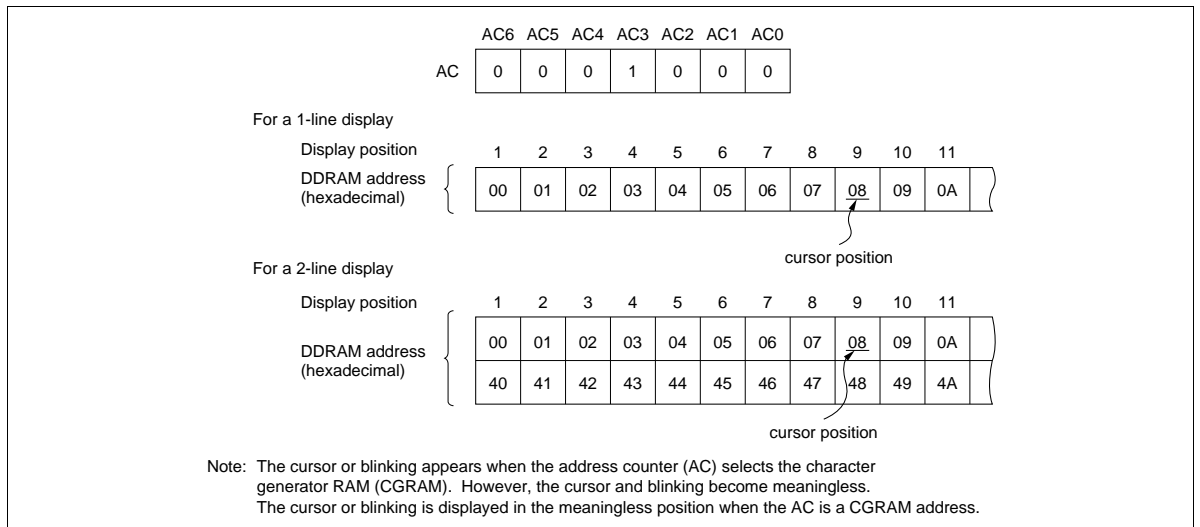
Sending serial data always starts at the display data character pattern corresponding to the last address of the display data RAM (DDRAM).

Since serial data is latched when the display data character pattern corresponding to the starting address enters the internal shift register, the HD66701/2 drives from the head display.

**Cursor/Blink Control Circuit**

The cursor/blink control circuit generates the cursor or character blinking. The cursor or the blinking will appear with the digit located at the display data RAM (DDRAM) address set in the address counter (AC).

For example (Figure 8), when the address counter is 08H, the cursor position is displayed at DDRAM address 08H.

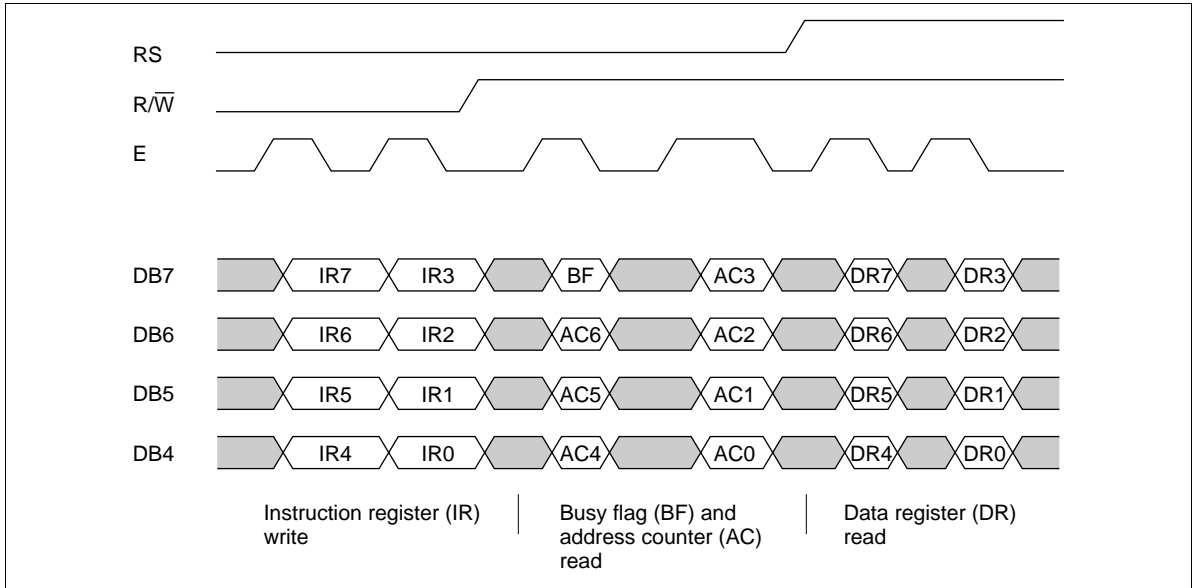


**Figure 8 Cursor/Blink Display Example**

## Interfacing to the MPU

The HD66701/2 can send data in either two 4-bit operations or one 8-bit operation, thus allowing interfacing with 4- or 8-bit MPUs.

- For 4-bit interface data, only four bus lines (DB4 to DB7) are used for transfer. Bus lines DB0 to DB3 are disabled. The data transfer between the HD66701/2 and the MPU is completed after the 4-bit data has been transferred twice. As for the order of data transfer, the four high order bits (for 8-bit operation, DB4 to DB7) are transferred before the four low order bits (for 8-bit operation, DB0 to DB3). The busy flag must be checked (one instruction) after the 4-bit data has been transferred twice. Two more 4-bit operations then transfer the busy flag and address counter data.
- For 8-bit interface data, all eight bus lines (DB0 to DB7) are used.



**Figure 9 4-Bit Transfer Example**

## **Reset Function**

### **Initializing by Internal Reset Circuit**

An internal reset circuit automatically initializes the HD66701/2 when the power is turned on. The following instructions are executed during the initialization. The busy flag (BF) is kept in the busy state until the initialization ends (BF = 1). The busy state lasts for 15 ms after  $V_{CC}$  rises to 4.5V, or 40 ms after  $V_{CC}$  rises to 2.7V.

1. Display clear
2. Function set:
  - DL = 1; 8-bit interface data
  - N = 0; 1-line display
  - F = 0; 5 × 7 dot character font
3. Display on/off control:
  - D = 0; Display off
  - C = 0; Cursor off
  - B = 0; Blinking off
4. Entry mode set:
  - I/D = 1; Increment by 1
  - S = 0; No shift

**Note:** If the electrical characteristics conditions listed under the Table Power Supply Conditions Using Internal Reset Circuit are not met, the internal reset circuit will not operate normally and will fail to initialize the HD66701/2. For such a case, initial-ization must be performed by the MPU as explained in the section, Initializing by Instruction.

## Instructions

### Outline

Only the instruction register (IR) and the data register (DR) of the HD66701/2 can be controlled by the MPU. Before starting the internal operation of the HD66701/2, control information is temporarily stored into these registers to allow interfacing with various MPUs, which operate at different speeds, or various peripheral control devices. The internal operation of the HD66702 is determined by signals sent from the MPU. These signals, which include register selection (RS), read/write ( $R/\overline{W}$ ), and the data bus (DB0 to DB7), make up the HD66701/2 instructions (Table 7). There are four categories of instructions that:

- Designate HD66701/2 functions, such as display format, data length, etc.
- Set internal RAM addresses
- Perform data transfer with internal RAM
- Perform miscellaneous functions

Normally, instructions that perform data transfer with internal RAM are used the most. However, auto-incrementation by 1 (or auto-decrementation by 1) of internal HD66701/2 RAM addresses after each data write can lighten the program load of the MPU. Since the display shift instruction (Table 12) can perform concurrently with display data write, the user can minimize system development time with maximum programming efficiency.

When an instruction is being executed for internal operation, no instruction other than the busy flag/address read instruction can be executed.

Because the busy flag is set to 1 while an instruction is being executed, check it to make sure it is 0 before sending another instruction from the MPU.

Note: Be sure the HD66701/2 is not in the busy state (BF = 0) before sending an instruction from the MPU to the HD66701/2. If an instruction is sent without checking the busy flag, the time between the first instruction and next instruction will take much longer than the instruction time itself. Refer to Table 7 for the list of each instruction execution time.

**Table 7 Instructions**

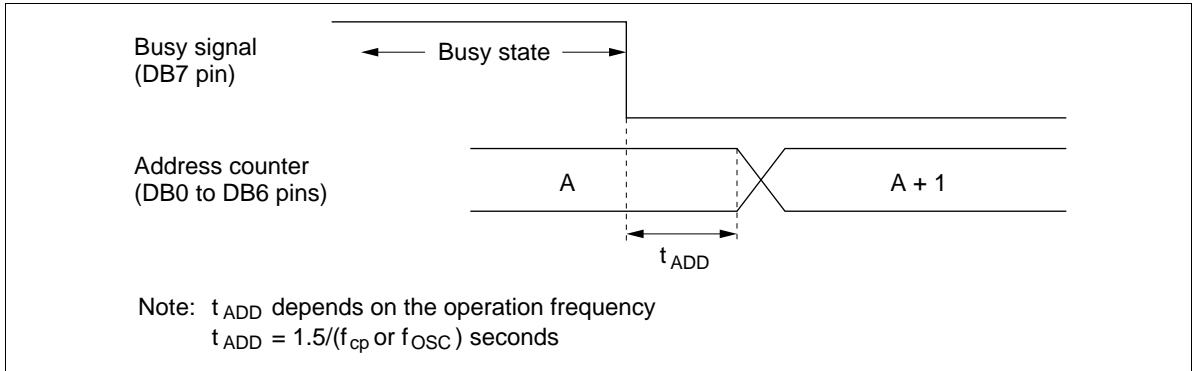
| Instruction              | Code |     |     |     |     |     |     |     |     |     | Description  | Execution Time<br>(max) (when $f_{op}$ or<br>$f_{osc}$ is 320 kHz)  |         |
|--------------------------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|--|---|---------|
|                          | RS   | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |  |   |         |
| Clear display            | 0    | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 1   | Clears entire display and sets DDRAM address 0 in address counter.   | 1.28 ms   |         |
| Return home              | 0    | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 1   | —  | Sets DDRAM address 0 in address counter. Also returns display from being shifted to original position. DDRAM contents remain unchanged. | 1.28 ms |
| Entry mode set           | 0    | 0   | 0   | 0   | 0   | 0   | 0   | 1   | I/D | S   | Sets cursor move direction and specifies display shift. These operations are performed during data write and read. | 31 $\mu$ s  |         |
| Display on/off control   | 0    | 0   | 0   | 0   | 0   | 0   | 1   | D   | C   | B   | Sets entire display (D) on/off, cursor on/off (C), and blinking of cursor position character (B).                  | 31 $\mu$ s  |         |
| Cursor or display shift  | 0    | 0   | 0   | 0   | 0   | 1   | S/C | R/L | —   | —   | Moves cursor and shifts display without changing DDRAM contents.   | 31 $\mu$ s  |         |
| Function set             | 0    | 0   | 0   | 0   | 1   | DL  | N   | F   | —   | —   | Sets interface data length (DL), number of display lines (L), and character font (F).                              | 31 $\mu$ s  |         |
| Set CGRAM address        | 0    | 0   | 0   | 1   | ACG | ACG | ACG | ACG | ACG | ACG | Sets CGRAM address. CGRAM data is sent and received after this setting.  | 31 $\mu$ s  |         |
| Set DDRAM address        | 0    | 0   | 1   | ADD | ADD | ADD | ADD | ADD | ADD | ADD | Sets DDRAM address. DDRAM data is sent and received after this setting.  | 31 $\mu$ s  |         |
| Read busy flag & address | 0    | 1   | BF  | AC  | AC  | AC  | AC  | AC  | AC  | AC  | Reads busy flag (BF) indicating internal operation is being performed and reads address counter contents.          | 0 $\mu$ s   |         |

**Table 7 Instructions (cont)**

| Instruction                | Code  |     |            |     |     |     |     |     |     |     | Description  | Execution Time (max) (when $f_{cp}$ or $f_{osc}$ is 320 kHz)  |                                  |   |
|----------------------------|---|-----|------------|-----|-----|-----|-----|-----|-----|-----|--|---|----------------------------------|---|
|                            | RS  | R/W | DB7        | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |  |   |                                  |   |
| Write data to CG or DDRAM  | 1   | 0   | Write data |     |     |     |     |     |     |     |  |   | Writes data into DDRAM or CGRAM. | 31 $\mu$ s<br>$t_{ADD} = 4.7 \mu\text{s}^*$ |
| Read data from CG or DDRAM | 1   | 1   | Read data  |     |     |     |     |     |     |     |  |   | Reads data from DDRAM or CGRAM.  | 31 $\mu$ s<br>$t_{ADD} = 4.7 \mu\text{s}^*$ |
|                            | I/D = 1: Increment<br>I/D = 0: Decrement                        |     |            |     |     |     |     |     |     |     | DDRAM: Display data RAM                                  | Execution time changes when frequency changes<br>Example:<br>When $f_{cp}$ or $f_{osc}$ is 270 kHz,<br>$31 \mu\text{s} \times \frac{320}{270} = 37 \mu\text{s}$ |                                  |   |
|                            | S = 1: Accompanies display shift                                |     |            |     |     |     |     |     |     |     | CGRAM: Character generator RAM                           |   |                                  |   |
|                            | S/C = 1: Display shift  |     |            |     |     |     |     |     |     |     | ACG: CGRAM address                                       |   |                                  |   |
|                            | S/C = 0: Cursor move  |     |            |     |     |     |     |     |     |     | ADD: DDRAM address (corresponds to cursor address)       |   |                                  |   |
|                            | R/L = 1: Shift to the right                                     |     |            |     |     |     |     |     |     |     | AC: Address counter used for both DD and CGRAM addresses |   |                                  |   |
|                            | R/L = 0: Shift to the left                                      |     |            |     |     |     |     |     |     |     |  |   |                                  |   |
|                            | DL = 1: 8 bits, DL = 0: 4 bits                                  |     |            |     |     |     |     |     |     |     |  |   |                                  |   |
|                            | N = 1: 2 lines, N = 0: 1 line                                   |     |            |     |     |     |     |     |     |     |  |   |                                  |   |
|                            | F = 1: 5 $\times$ 10 dots, F = 0: 5 $\times$ 7 dots             |     |            |     |     |     |     |     |     |     |  |   |                                  |   |
|                            | BF = 1: Internally operating<br>BF = 0: Instructions acceptable |     |            |     |     |     |     |     |     |     |  |   |                                  |   |

Note: — indicates no effect.

\* After execution of the CGRAM/DDRAM data write or read instruction, the RAM address counter is incremented or decremented by 1. The RAM address counter is updated after the busy flag turns off. In Figure 10,  $t_{ADD}$  is the time elapsed after the busy flag turns off until the address counter is updated.



**Figure 10 Address Counter Update**

## Instruction Description

### Clear Display

Clear display writes space code 20H (character pattern for character code 20H must be a blank pattern) into all DDRAM addresses. It then sets DDRAM address 0 into the address counter, and returns the display to its original status if it was shifted. In other words, the display disappears and the cursor or blinking goes to the left edge of the display (in the first line if 2 lines are displayed). It also sets I/D to 1 (increment mode) in entry mode. S of entry mode does not change.

### Return Home

Return home sets DDRAM address 0 into the address counter, and returns the display to its original status if it was shifted. The DDRAM contents do not change.

The cursor or blinking go to the left edge of the display (in the first line if 2 lines are displayed).

### Entry Mode Set

**I/D:** Increments ( $I/D = 1$ ) or decrements ( $I/D = 0$ ) the DDRAM address by 1 when a character code is written into or read from DDRAM.

The cursor or blinking moves to the right when incremented by 1 and to the left when decremented by 1. The same applies to writing and reading of CGRAM.

**S:** Shifts the entire display either to the right ( $I/D = 0$ ) or to the left ( $I/D = 1$ ) when S is 1. The display does not shift if S is 0.

If S is 1, it will seem as if the cursor does not move but the display does. The display does not shift when reading from DDRAM. Also, writing into or reading out from CGRAM does not shift the display.

### Display On/Off Control

**D:** The display is on when D is 1 and off when D is 0. When off, the display data remains in DDRAM, but can be displayed instantly by setting D to 1.

**C:** The cursor is displayed when C is 1 and not displayed when C is 0. Even if the cursor disappears, the function of I/D or other specifications will not change during display data write. The cursor is displayed using 5 dots in the 8th line for  $5 \times 7$  dot character font selection and in the 11th line for the  $5 \times 10$  dot character font selection (Figure 13).

**B:** The character indicated by the cursor blinks when B is 1 (Figure 13). The blinking is displayed as switching between all blank dots and displayed characters at a speed of 320-ms intervals when  $f_{cp}$  or  $f_{osc}$  is 320 kHz. The cursor and blinking can be set to display simultaneously. (The blinking frequency changes according to  $f_{osc}$  or the reciprocal of  $f_{cp}$ . For example, when  $f_{cp}$  is 270 kHz,  $320 \times 320/270 = 379.2$  ms.)

### **Cursor or Display Shift**

Cursor or display shift shifts the cursor position or display to the right or left without writing or reading display data (Table 8). This function is used to correct or search the display. In a 2-line display, the cursor moves to the second line when it passes the 40th digit of the first line. Note that the first and second line displays will shift at the same time.

When the displayed data is shifted repeatedly each line moves only horizontally. The second line display does not shift into the first line position.

The address counter (AC) contents will not change if the only action performed is a display shift.

### **Function Set**

**DL:** Sets the interface data length. Data is sent or received in 8-bit lengths (DB7 to DB0) when DL is 1, and in 4-bit lengths (DB7 to DB4) when DL is 0.

When 4-bit length is selected, data must be sent or received twice.

**N:** Sets the number of display lines (Table 9).

**F:** Sets the character font (Table 9).

Note: Perform the function at the head of the program before executing any instructions (except for the read busy flag and address instruction). From this point, the function set instruction cannot be executed unless the interface data length is changed.

### **Set CGRAM Address**

Set CGRAM address sets the CGRAM address binary AAAAAA into the address counter.

Data is then written to or read from the MPU for CGRAM.

|                         |      | RS | R $\bar{W}$ | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |                     |
|-------------------------|------|----|-------------|-----|-----|-----|-----|-----|-----|-----|-----|---------------------|
| Clear display           | Code | 0  | 0           | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 1   |                     |
|                         |      |    |             |     |     |     |     |     |     |     |     |                     |
| Return home             | Code | 0  | 0           | 0   | 0   | 0   | 0   | 0   | 0   | 1   | *   | Note: * Don't care. |
|                         |      |    |             |     |     |     |     |     |     |     |     |                     |
| Entry mode set          | Code | 0  | 0           | 0   | 0   | 0   | 0   | 0   | 1   | I/D | S   |                     |
|                         |      |    |             |     |     |     |     |     |     |     |     |                     |
| Display on/off control  | Code | 0  | 0           | 0   | 0   | 0   | 0   | 1   | D   | C   | B   |                     |
|                         |      |    |             |     |     |     |     |     |     |     |     |                     |
| Cursor or display shift | Code | 0  | 0           | 0   | 0   | 0   | 1   | S/C | R/L | *   | *   | Note: * Don't care. |
|                         |      |    |             |     |     |     |     |     |     |     |     |                     |
| Function set            | Code | 0  | 0           | 0   | 0   | 1   | DL  | N   | F   | *   | *   | Note: * Don't care. |
|                         |      |    |             |     |     |     |     |     |     |     |     |                     |
| Set CGRAM address       | Code | 0  | 0           | 0   | 1   | A   | A   | A   | A   | A   | A   |                     |
|                         |      |    |             |     |     |     |     |     |     |     |     |                     |
|                         |      |    |             |     |     |     |     |     |     |     |     | Highest order bit   |
|                         |      |    |             |     |     |     |     |     |     |     |     | Lowest order bit    |

Figure 11 Instruction (1)

**Set DDRAM Address**

Set DDRAM address sets the DDRAM address binary AAAAAAA into the address counter.

Data is then written to or read from the MPU for DDRAM.

However, when N is 0 (1-line display), AAAAAAA can be 00H to 4FH. When N is 1 (2-line display), AAAAAAA can be 00H to 27H for the first line, and 40H to 67H for the second line.

**Read Busy Flag and Address**

Read busy flag and address reads the busy flag (BF) indicating that the system is now internally operating on a previously received instruction. If BF is 1, the internal operation is in progress. The next instruction will not be accepted until BF is reset to 0. Check the BF status before the next write operation. At the same time, the value of the address counter in binary AAAAAAA is read out. This address counter is used by both CG and DDRAM addresses, and its value is determined by the previous instruction. The address contents are the same as for instructions set CGRAM address and set DDRAM address.

**Table 8 Shift Function**

| <b>S/C</b> | <b>R/L</b> |   |
|------------|------------|---|
| 0          | 0          | Shifts the cursor position to the left. (AC is decremented by one.)           |
| 0          | 1          | Shifts the cursor position to the right. (AC is incremented by one.)          |
| 1          | 0          | Shifts the entire display to the left. The cursor follows the display shift.  |
| 1          | 1          | Shifts the entire display to the right. The cursor follows the display shift. |

**Table 9 Function Set**

| <b>N</b> | <b>F</b> | <b>No. of Display Lines</b> | <b>Character Font</b> | <b>Duty Factor</b> | <b>Remarks</b>  |
|----------|----------|-----------------------------|-----------------------|--------------------|---|
| 0        | 0        | 1                           | 5 × 7 dots            | 1/8                |   |
| 0        | 1        | 1                           | 5 × 10 dots           | 1/11               |   |
| 1        | *        | 2                           | 5 × 7 dots            | 1/16               | Cannot display two lines for 5 × 10 dot character font. |

Note: \* Indicates don't care.

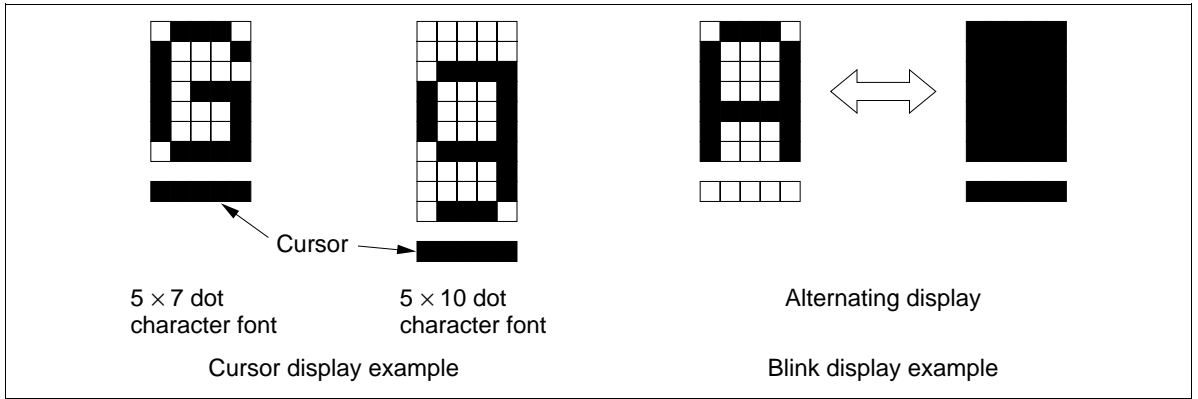


Figure 12 Cursor and Blinking

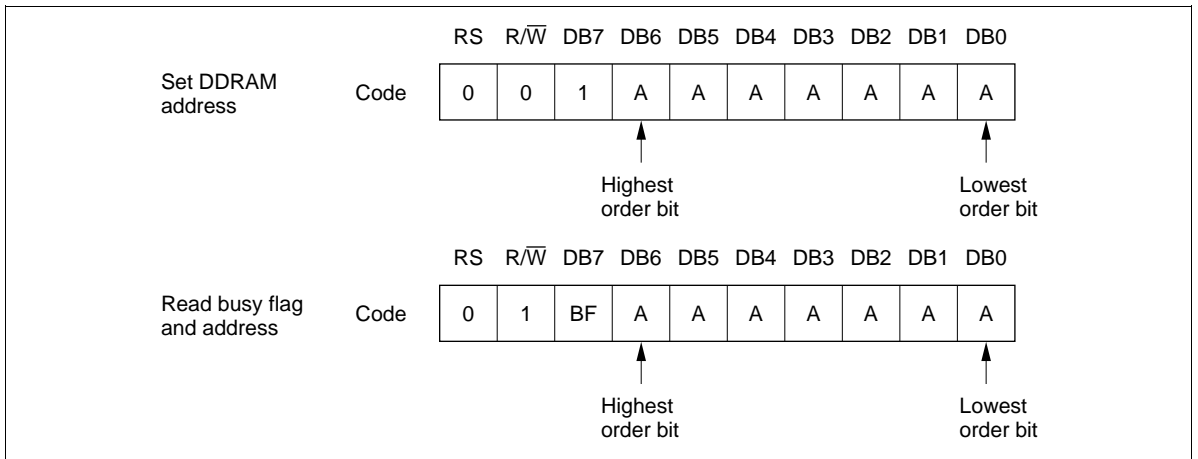


Figure 13 Instruction (2)

## Write Data to CG or DDRAM

Write data to CG or DDRAM writes 8-bit binary data DDDDDDDD to CG or DDRAM.

To write into CG or DDRAM is determined by the previous specification of the CGRAM or DDRAM address setting. After a write, the address is automatically incremented or decremented by 1 according to the entry mode. The entry mode also determines the display shift.

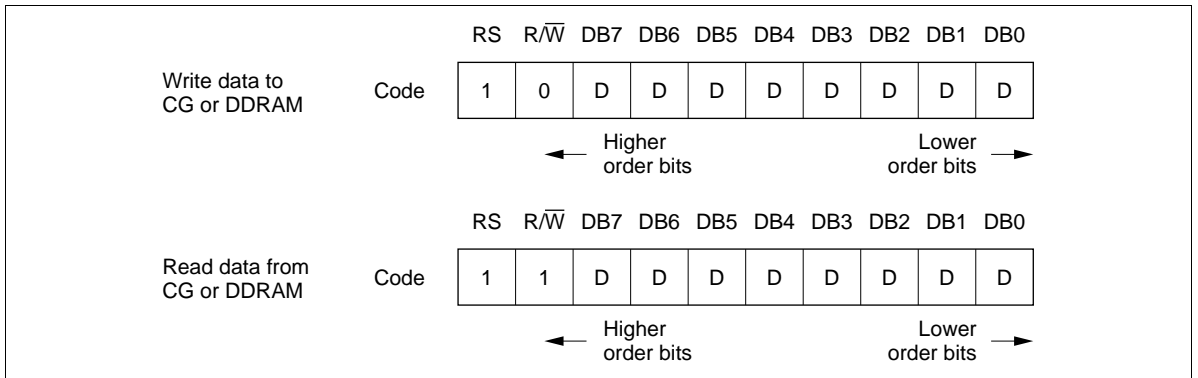
## Read Data from CG or DDRAM

Read data from CG or DDRAM reads 8-bit binary data DDDDDDDD from CG or DDRAM.

The previous designation determines whether CG or DDRAM is to be read. Before entering this read instruction, either CGRAM or DDRAM address set instruction must be executed. If not executed, the first read data will be invalid. When serially executing read instructions, the next address data is normally read from the second read. The address set instructions need not be executed just before this read instruction when shifting the cursor by the cursor shift instruction (when reading out DDRAM). The operation of the cursor shift instruction is the same as the set DDRAM address instruction.

After a read, the entry mode automatically increases or decreases the address by 1. However, display shift is not executed regardless of the entry mode.

Note: The address counter (AC) is automatically incremented or decremented by 1 after the write instructions to CGRAM or DDRAM are executed. The RAM data selected by the AC cannot be read out at this time even if read instructions are executed. Therefore, to correctly read data, execute either the address set instruction or cursor shift instruction (only with DDRAM), then just before reading the desired data, execute the read instruction from the second time the read instruction is sent.



**Figure 14 Instruction (3)**

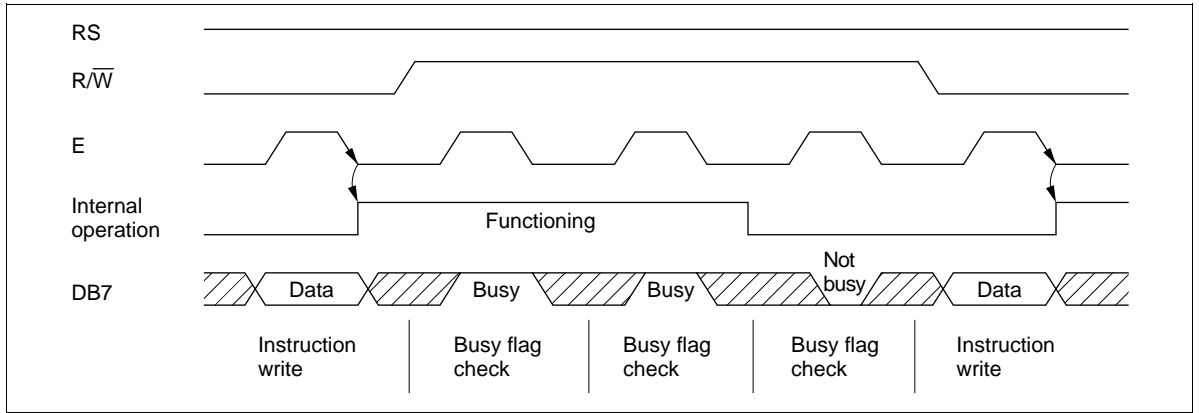
## Interfacing the HD66702

### Interface to MPUs

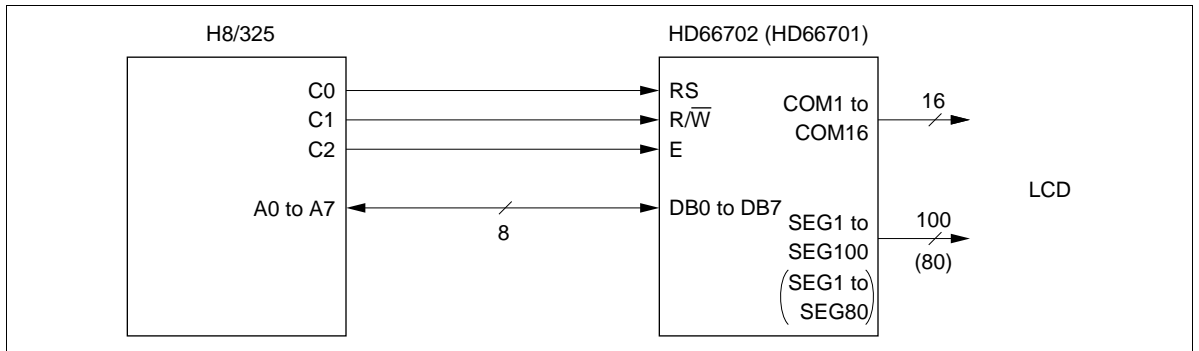
- Interfacing to an 8-bit MPU

See Figure 16 for an example of using a I/O port (for a single-chip microcomputer) as an interface device.

In this example, A0 to A7 are connected to the data bus DB0 to DB7, and C0 to C2 are connected to E, R/W, and RS, respectively.



**Figure 15 Example of Busy Flag Check Timing Sequence**



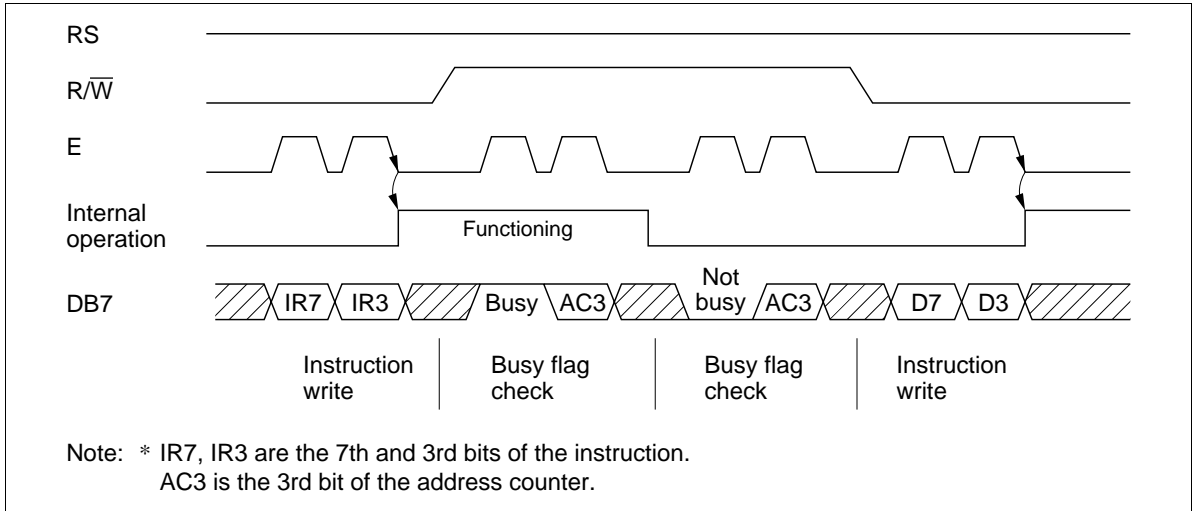
**Figure 16 8-bit MPU Interface**

- Interfacing to a 4-bit MPU

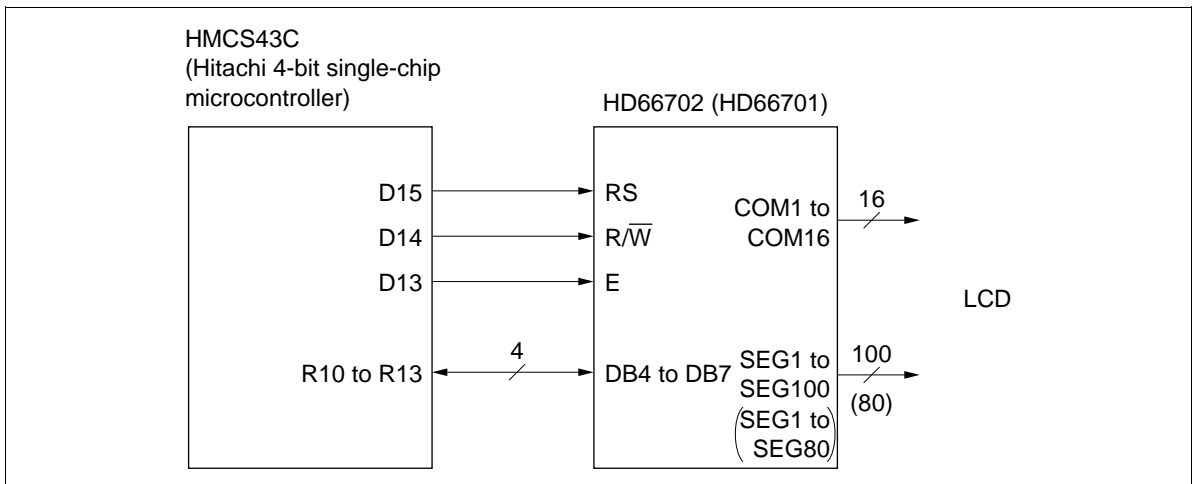
The HD66701/2 can be connected to the I/O port of a 4-bit MPU. If the I/O port has enough bits, 8-bit data can be transferred. Otherwise, one data transfer must be made in two operations for 4-bit data. In this case, the timing sequence becomes somewhat complex. (See Figure 17.)

See Figure 18 for an interface example to the HMCS43C.

Note that two cycles are needed for the busy flag check as well as for the data transfer. The 4-bit operation is selected by the program.



**Figure 17 Example of 4-Bit Data Transfer Timing Sequence**



**Figure 18 Example of Interface to HMCS43C**

**Interface to Liquid Crystal Display**

**Character Font and Number of Lines:** The HD66702 can perform two types of displays, 5 × 7 dot and 5 × 10 dot character fonts, each with a cursor.

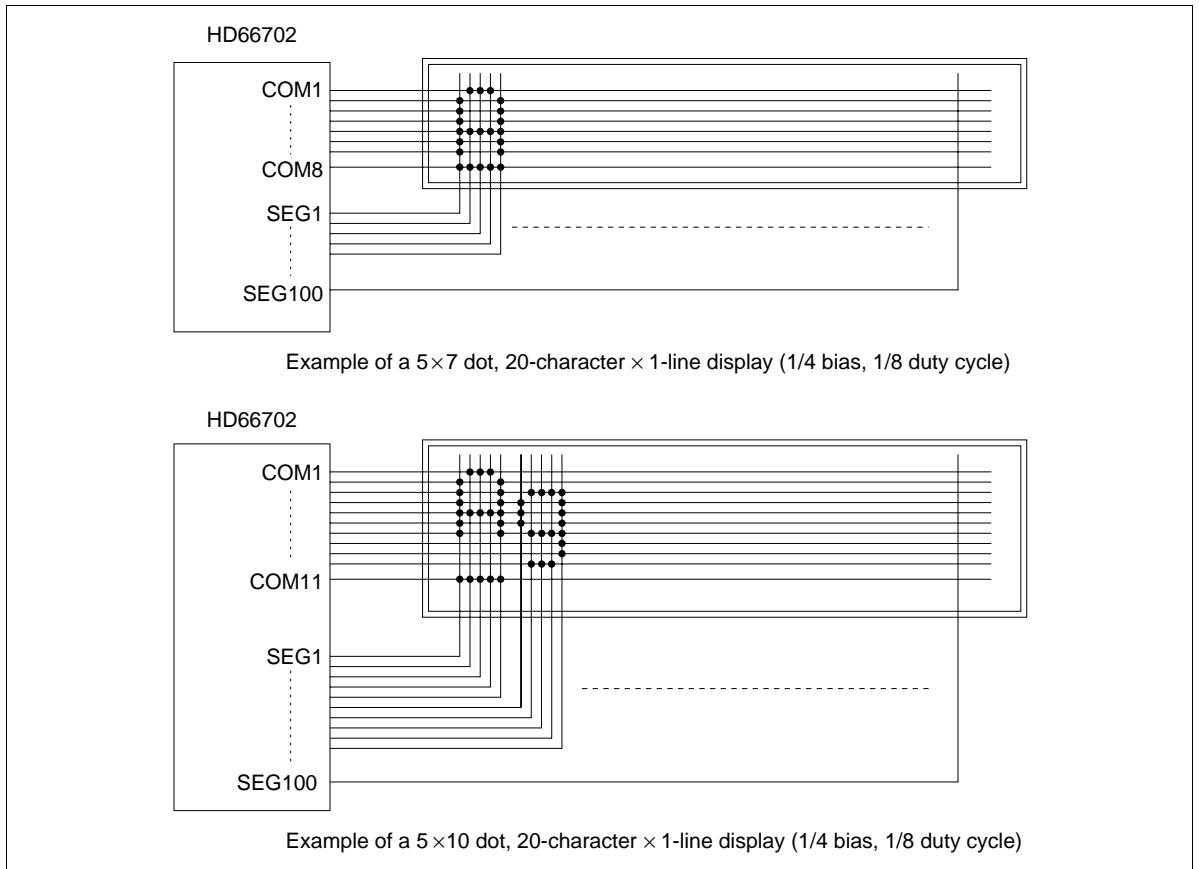
Up to two lines are displayed for 5 × 7 dots and one line for 5 × 10 dots. Therefore, a total of three types of common signals are available (Table 10).

The number of lines and font types can be selected by the program. (See Table 7, Instructions.)

**Connection to HD66702 and Liquid Crystal Display:** See Figure 19 for the connection examples.

**Table 10 Common Signals**

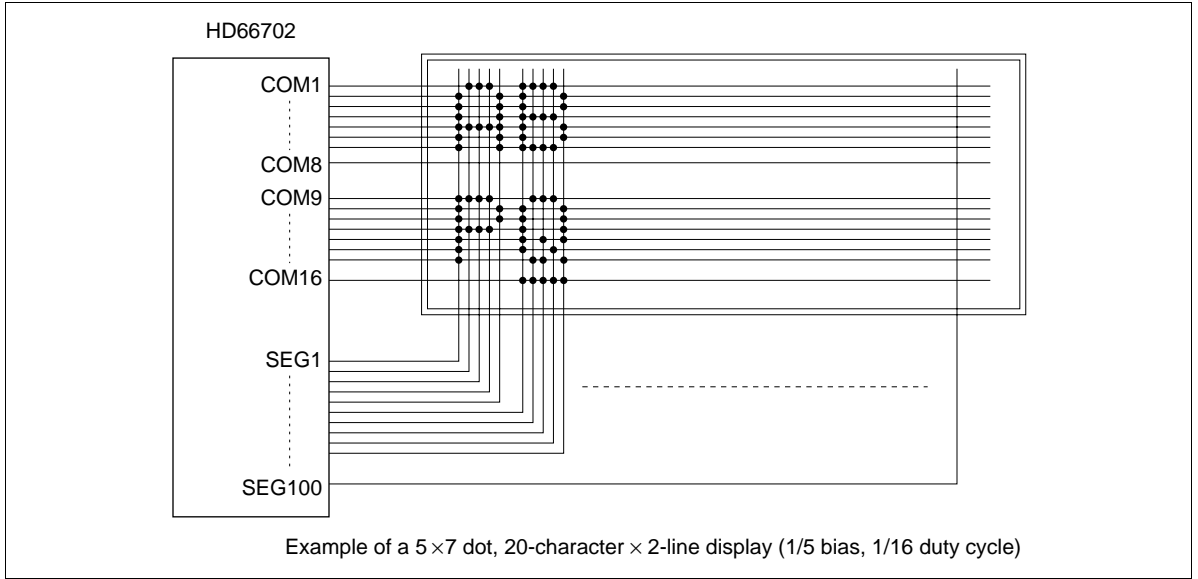
| Number of Lines | Character Font       | Number of Common Signals | Duty Factor |
|-----------------|----------------------|--------------------------|-------------|
| 1               | 5 × 7 dots + cursor  | 8                        | 1/8         |
| 1               | 5 × 10 dots + cursor | 11                       | 1/11        |
| 2               | 5 × 7 dots + cursor  | 16                       | 1/16        |



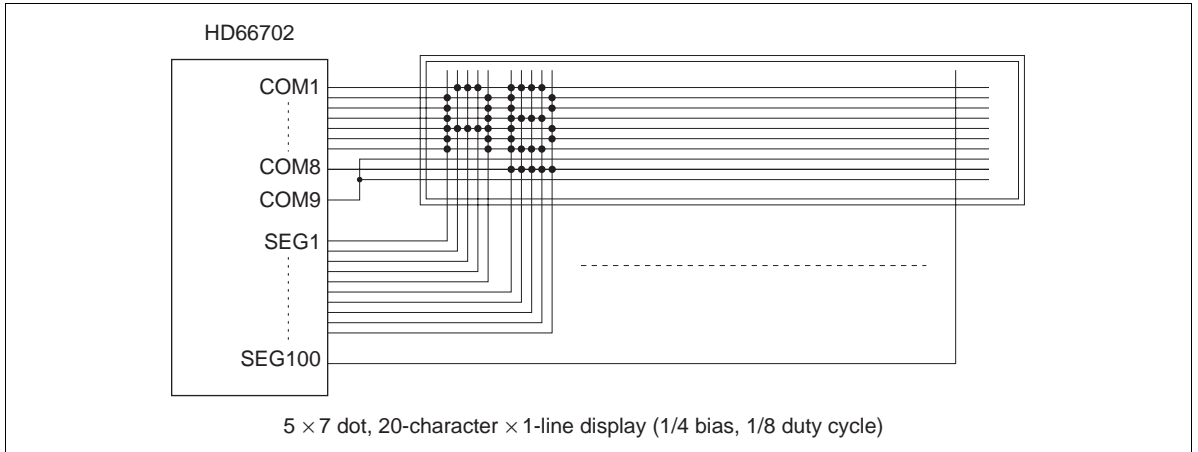
**Figure 19 Liquid Crystal Display and HD66702 Connections**

Since five segment signal lines can display one digit, one HD66702 can display up to 20 digits for a 1-line display and 40 digits for a 2-line display.

The examples in Figure 19 have unused common signal pins, which always output non-selection waveforms. When the liquid crystal display panel has unused extra scanning lines, connect the extra scanning lines to these common signal pins to avoid any undesirable effects due to crosstalk during the floating state (Figure 20).

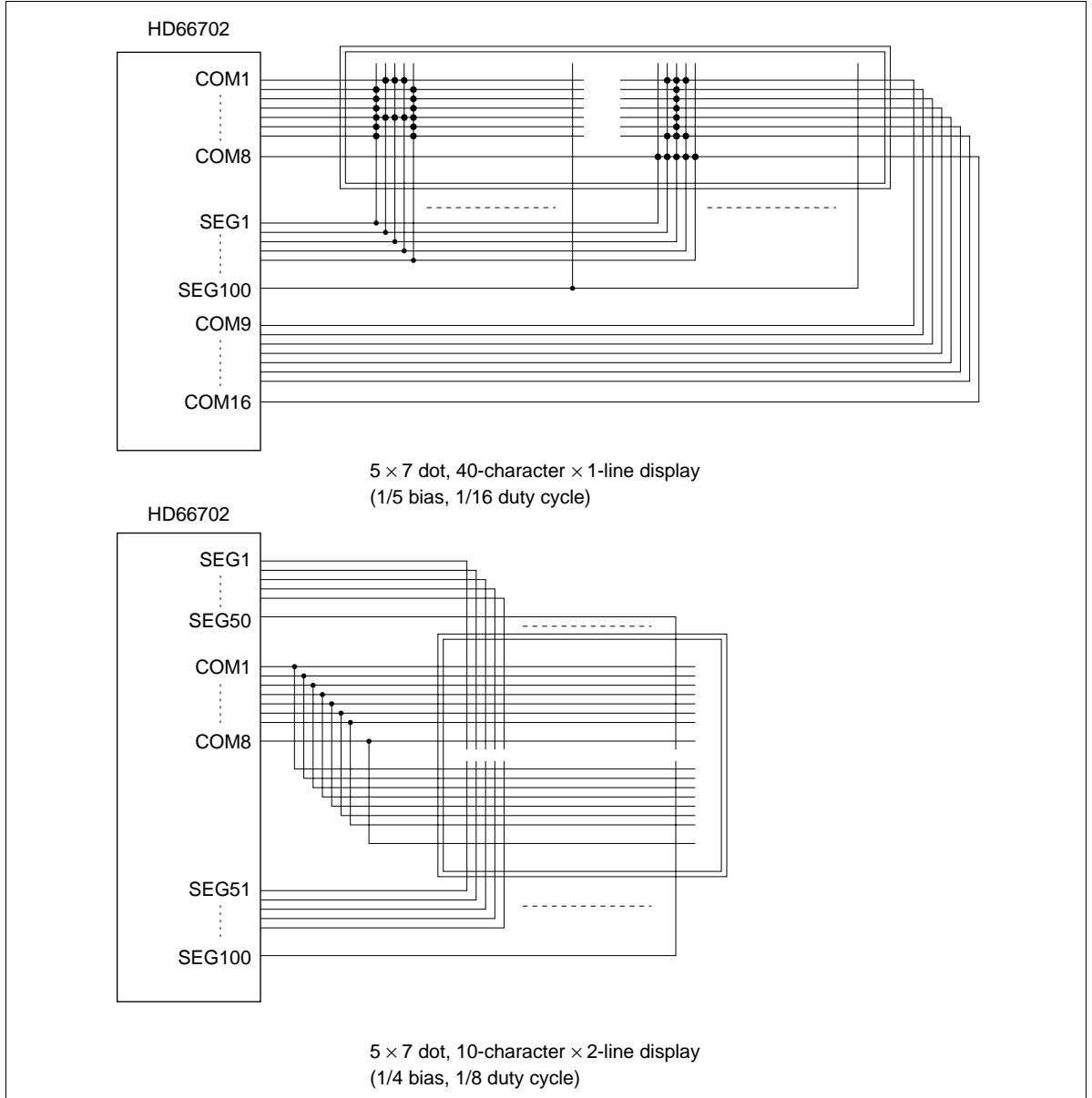


**Figure 19 Liquid Crystal Display and HD66702 Connections (cont)**



**Figure 20 Using COM9 to Avoid Crosstalk on Unneeded Scanning Line**

**Connection of Changed Matrix Layout:** In the preceding examples, the number of lines correspond to the scanning lines. However, the following display examples (Figure 21) are made possible by altering the matrix layout of the liquid crystal display panel. In either case, the only change is the layout. The display characteristics and the number of liquid crystal display characters depend on the number of common signals or on duty factor. Note that the display data RAM (DDRAM) addresses for 10 characters  $\times$  2 lines and for 40 characters  $\times$  1 line are the same as in Figure 19.



**Figure 21 Changed Matrix Layout Displays**

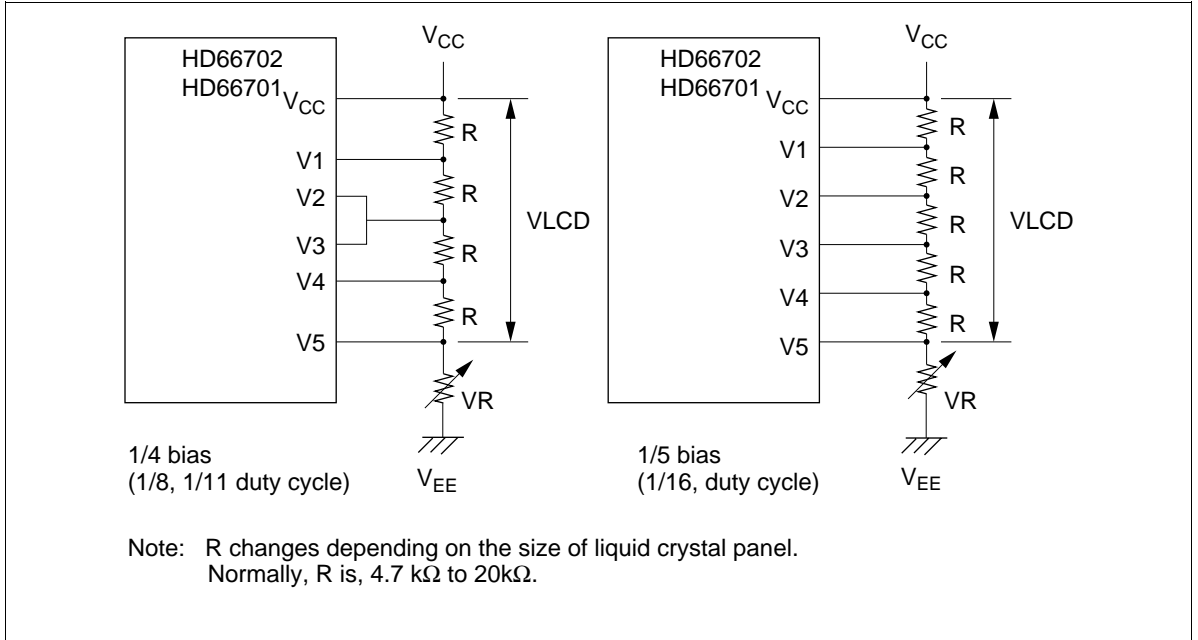
**Power Supply for Liquid Crystal Display Drive**

Various voltage levels must be applied to pins V1 to V5 of the HD66701/2 to obtain the liquid crystal display drive waveforms. The voltages must be changed according to the duty factor (Table 11).

VLCD is the peak value for the liquid crystal display drive waveforms, and resistance dividing provides voltages V1 to V5 (Figure 22).

**Table 11 Duty Factor and Power Supply for Liquid Crystal Display Drive**

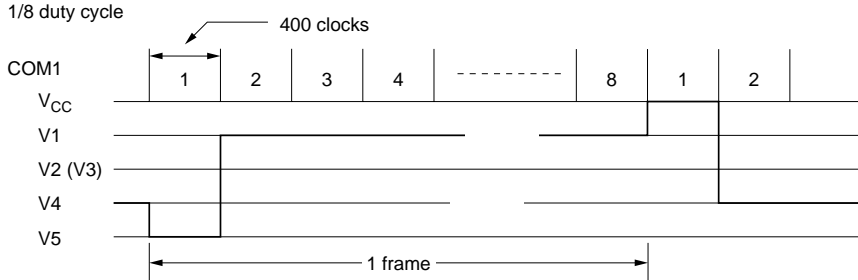
| Power Supply | Duty Factor               |                           |
|--------------|---------------------------|---------------------------|
|              | 1/8, 1/11                 | 1/16                      |
|              | Bias                      |                           |
|              | 1/4                       | 1/5                       |
| V1           | $V_{cc}-1/4 \text{ VLCD}$ | $V_{cc}-1/5 \text{ VLCD}$ |
| V2           | $V_{cc}-1/2 \text{ VLCD}$ | $V_{cc}-2/5 \text{ VLCD}$ |
| V3           | $V_{cc}-1/2 \text{ VLCD}$ | $V_{cc}-3/5 \text{ VLCD}$ |
| V4           | $V_{cc}-3/4 \text{ VLCD}$ | $V_{cc}-4/5 \text{ VLCD}$ |
| V5           | $V_{cc}-\text{VLCD}$      | $V_{cc}-\text{VLCD}$      |



**Figure 22 Drive Voltage Supply Example**

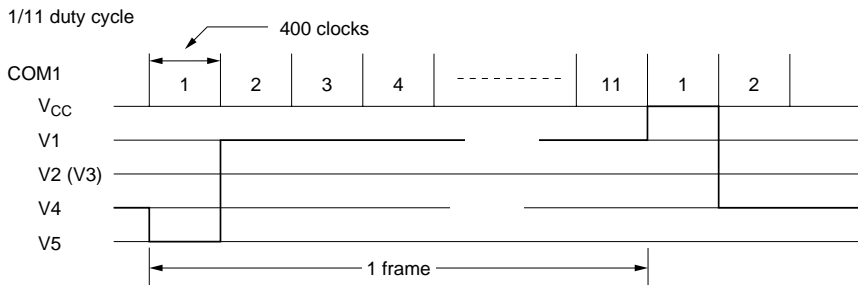
## Relationship between Oscillation Frequency and Liquid Crystal Display Frame Frequency

The liquid crystal display frame frequencies of Figure 23 apply only when the oscillation frequency is 320 kHz (one clock pulse of 3.125 μs).



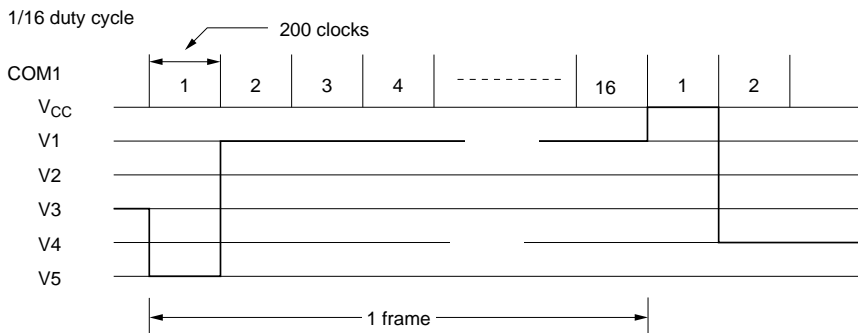
$$1 \text{ frame} = 3.125 \mu\text{s} \times 400 \times 8 = 10000 \mu\text{s} = 10 \text{ ms}$$

$$\text{Frame frequency} = \frac{1}{10 \text{ ms}} = 100 \text{ Hz}$$



$$1 \text{ frame} = 3.125 \mu\text{s} \times 400 \times 11 = 13750 \mu\text{s} = 13.75 \text{ ms}$$

$$\text{Frame frequency} = \frac{1}{13.75 \text{ ms}} = 72.7 \text{ Hz}$$



$$1 \text{ frame} = 3.125 \mu\text{s} \times 200 \times 16 = 10000 \mu\text{s} = 10 \text{ ms}$$

$$\text{Frame frequency} = \frac{1}{10 \text{ ms}} = 100 \text{ Hz}$$

Figure 23 Frame Frequency

## Instruction and Display Correspondence

- 8-bit operation, 20-digit × 1-line display with internal reset

Refer to Table 12 for an example of an 8-bit × 1-line display in 8-bit operation. The HD66702 functions must be set by the function set instruction prior to the display. Since the display data RAM can store data for 80 characters, as explained before, the RAM can be used for displays such as for advertising when combined with the display shift operation.

Since the display shift operation changes only the display position with DDRAM contents unchanged, the first display data entered into DDRAM can be output when the return home operation is performed.

- 4-bit operation, 20-digit × 1-line display with internal reset

The program must set all functions prior to the 4-bit operation (Table 13). When the power is turned on, 8-bit operation is automatically selected and the first write is performed as an 8-bit operation. Since DB0 to DB3 are not connected, a rewrite is then required. However, since one operation is completed in two accesses for 4-bit operation, a rewrite is needed to set the functions (see Table 13). Thus, DB4 to DB7 of the function set instruction is written twice.

- 8-bit operation, 20-digit × 2-line display

For a 2-line display, the cursor automatically moves from the first to the second line after the 40th digit of the first line has been written. Thus, if there are only 20 characters in the first line, the DDRAM address must be again set after the 20th character is completed. (See Table 14.) Note that the display shift operation is performed for the first and second lines. In the example of Table 14, the display shift is performed when the cursor is on the second line. However, if the shift operation is performed when the cursor is on the first line, both the first and second lines move together. If the shift is repeated, the display of the second line will not move to the first line. The same display will only shift within its own line for the number of times the shift is repeated.

Note: When using the internal reset, the electrical characteristics in the Power Supply Conditions Using Internal Reset Circuit table must be satisfied. If not, the HD66702 must be initialized by instructions. (Because the internal reset does not function correctly when  $V_{CC}$  is 3V, it must always be initialized by software.) See the section, Initializing by Instruction.

**Table 12 8-Bit Operation, 20-Digit × 1-Line Display Example with Internal Reset**

| Step | Instruction  |     |     |     |     |     |     |     |     |     | Display                               | Operation   |
|------|--|-----|-----|-----|-----|-----|-----|-----|-----|-----|---------------------------------------|---|
| No.  | RS   | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |                                       |   |
| 1    | Power supply on (the HD66702 is initialized by the internal reset circuit) |     |     |     |     |     |     |     |     |     | <input type="text"/>                  | Initialized. No display.  |
| 2    | Function set<br>0 0 0 0 1 1 0 0 * *  |     |     |     |     |     |     |     |     |     | <input type="text"/>                  | Sets to 8-bit operation and selects 1-line display and character font. (Number of display lines and character fonts cannot be changed after step #2.) |
| 3    | Display on/off control<br>0 0 0 0 0 0 1 1 1 0                              |     |     |     |     |     |     |     |     |     | <input type="text" value="-"/>        | Turns on display and cursor. Entire display is in space mode because of initialization.   |
| 4    | Entry mode set<br>0 0 0 0 0 0 0 1 1 0                                      |     |     |     |     |     |     |     |     |     | <input type="text" value="-"/>        | Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the DD/CGRAM. Display is not shifted.          |
| 5    | Write data to CGRAM/DDRAM<br>1 0 0 1 0 0 1 0 0 0                           |     |     |     |     |     |     |     |     |     | <input type="text" value="H_"/>       | Writes H. DDRAM already been selected by initialization when the power was turned on. The cursor is incremented by one and shifted to the right.      |
| 6    | Write data to CGRAM/DDRAM<br>1 0 0 1 0 0 1 0 0 1                           |     |     |     |     |     |     |     |     |     | <input type="text" value="HI_"/>      | Writes I.   |
| 7    |  |     |     |     |     |     |     |     |     |     |                                       | .   |
|      |  |     |     |     |     |     |     |     |     |     |                                       | .   |
|      |  |     |     |     |     |     |     |     |     |     |                                       | .   |
|      |  |     |     |     |     |     |     |     |     |     |                                       | .   |
|      |  |     |     |     |     |     |     |     |     |     |                                       | .   |
| 8    | Write data to CGRAM/DDRAM<br>1 0 0 1 0 0 1 0 0 1                           |     |     |     |     |     |     |     |     |     | <input type="text" value="HITACHI_"/> | Writes I.   |
| 9    | Entry mode set<br>0 0 0 0 0 0 0 1 1 1                                      |     |     |     |     |     |     |     |     |     | <input type="text" value="HITACHI_"/> | Sets mode to shift display at the time of write.  |
| 10   | Write data to CGRAM/DDRAM<br>1 0 0 0 1 0 0 0 0 0                           |     |     |     |     |     |     |     |     |     | <input type="text" value="ITACHI _"/> | Writes a space.   |

**Table 12 8-Bit Operation, 20-Digit × 1-Line Display Example with Internal Reset (cont)**

| Step | Instruction               |     |     |     |     |     |     |     |     |     | Display           | Operation  |
|------|---------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-------------------|--|
| No.  | RS                        | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |                   |  |
| 11   | Write data to CGRAM/DDRAM |     |     |     |     |     |     |     |     |     | TACHI M_          | Writes M.  |
|      | 1                         | 0   | 0   | 1   | 0   | 0   | 1   | 1   | 0   | 1   |                   |  |
| 12   |                           |     |     |     |     |     |     |     |     |     |                   | .  |
|      |                           |     |     |     |     |     |     |     |     |     |                   | .  |
|      |                           |     |     |     |     |     |     |     |     |     |                   | .  |
|      |                           |     |     |     |     |     |     |     |     |     |                   | .  |
|      |                           |     |     |     |     |     |     |     |     |     |                   | .  |
| 13   | Write data to CGRAM/DDRAM |     |     |     |     |     |     |     |     |     | MICROKO_          | Writes O.  |
|      | 1                         | 0   | 0   | 1   | 0   | 0   | 1   | 1   | 1   | 1   |                   |  |
| 14   | Cursor or display shift   |     |     |     |     |     |     |     |     |     | MICROK <u>O</u>   | Shifts only the cursor position to the left.                         |
|      | 0                         | 0   | 0   | 0   | 0   | 1   | 0   | 0   | *   | *   |                   |  |
| 15   | Cursor or display shift   |     |     |     |     |     |     |     |     |     | MICROK <u>O</u>   | Shifts only the cursor position to the left.                         |
|      | 0                         | 0   | 0   | 0   | 0   | 1   | 0   | 0   | *   | *   |                   |  |
| 16   | Write data to CGRAM/DDRAM |     |     |     |     |     |     |     |     |     | ICRO <u>C</u> O   | Writes C over K.<br>The display moves to the left.                   |
|      | 1                         | 0   | 0   | 1   | 0   | 0   | 0   | 0   | 1   | 1   |                   |  |
| 17   | Cursor or display shift   |     |     |     |     |     |     |     |     |     | MICRO <u>C</u> O  | Shifts the display and cursor position to the right.                 |
|      | 0                         | 0   | 0   | 0   | 0   | 1   | 1   | 1   | *   | *   |                   |  |
| 18   | Cursor or display shift   |     |     |     |     |     |     |     |     |     | MICRO <u>C</u> O_ | Shifts the display and cursor position to the right.                 |
|      | 0                         | 0   | 0   | 0   | 0   | 1   | 0   | 1   | *   | *   |                   |  |
| 19   | Write data to CGRAM/DDRAM |     |     |     |     |     |     |     |     |     | ICRO <u>C</u> OM_ | Writes M.  |
|      | 1                         | 0   | 0   | 1   | 0   | 0   | 1   | 1   | 0   | 1   |                   |  |
| 20   |                           |     |     |     |     |     |     |     |     |     |                   | .  |
|      |                           |     |     |     |     |     |     |     |     |     |                   | .  |
|      |                           |     |     |     |     |     |     |     |     |     |                   | .  |
|      |                           |     |     |     |     |     |     |     |     |     |                   | .  |
|      |                           |     |     |     |     |     |     |     |     |     |                   | .  |
| 21   | Return home               |     |     |     |     |     |     |     |     |     | HITACHI           | Returns both display and cursor to the original position(address 0). |
|      | 0                         | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 1   | 0   |                   |  |

**Table 13 4-Bit Operation, 20-Digit × 1-Line Display Example with Internal Reset**

| Step |  | Instruction |     |     |     |     | Display | Operation  |
|------|--|-------------|-----|-----|-----|-----|---------|--|
| No.  | RS   | R/W         | DB7 | DB6 | DB5 | DB4 |         |  |
| 1    | Power supply on (the HD66702 is initialized by the internal reset circuit) |             |     |     |     |     |         | Initialized. No display.   |
| 2    | Function set   |             |     |     |     |     |         | Sets to 4-bit operation. In this case, operation is handled as 8 bits by initialization, and only this instruction completes with one write.   |
|      | 0  | 0           | 0   | 0   | 1   | 0   |         |  |
| 3    | Function set   |             |     |     |     |     |         | Sets 4-bit operation and selects 1-line display and 5 × 7 dot character font. 4-bit operation starts from this step and resetting is necessary. (Number of display lines and character fonts cannot be changed after step #3.) |
|      | 0  | 0           | 0   | 0   | 1   | 0   |         |  |
|      | 0  | 0           | 0   | 0   | *   | *   |         |  |
| 4    | Display on/off control   |             |     |     |     |     |         | Turns on display and cursor. Entire display is in space mode because of initialization.  |
|      | 0  | 0           | 0   | 0   | 0   | 0   |         |  |
|      | 0  | 0           | 1   | 1   | 1   | 0   |         |  |
| 5    | Entry mode set   |             |     |     |     |     |         | Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the DD/CGRAM. Display is not shifted.   |
|      | 0  | 0           | 0   | 0   | 0   | 0   |         |  |
|      | 0  | 0           | 0   | 1   | 1   | 0   |         |  |
| 6    | Write data to CGRAM/DDRAM  |             |     |     |     |     |         | Writes H. The cursor is incremented by one and shifts to the right.  |
|      | 1  | 0           | 0   | 1   | 0   | 0   |         |  |
|      | 1  | 0           | 1   | 0   | 0   | 0   |         |  |

Note: The control is the same as for 8-bit operation beyond step #6.

**Table 14 8-Bit Operation, 20-Digit × 2-Line Display Example with Internal Reset**

| Step No. | RS   | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Display   | Operation  |
|----------|--|-----|-----|-----|-----|-----|-----|-----|-----|-----|---|--|
| 1        | Power supply on (the HD66702 is initialized by the internal reset circuit) |     |     |     |     |     |     |     |     |     | <div style="border: 1px solid black; width: 100px; height: 20px; margin-bottom: 2px;"></div> <div style="border: 1px solid black; width: 100px; height: 20px;"></div>   | Initialized. No display.   |
| 2        | 0  | 0   | 0   | 0   | 1   | 1   | 1   | 0   | *   | *   | <div style="border: 1px solid black; width: 100px; height: 20px; margin-bottom: 2px;"></div> <div style="border: 1px solid black; width: 100px; height: 20px;"></div>   | Sets to 8-bit operation and selects 2-line display and 5 × 7 dot character font.   |
| 3        | 0  | 0   | 0   | 0   | 0   | 0   | 1   | 1   | 1   | 0   | <div style="border: 1px solid black; width: 100px; height: 20px; margin-bottom: 2px; text-align: center;">_</div> <div style="border: 1px solid black; width: 100px; height: 20px;"></div>                            | Turns on display and cursor. All display is in space mode because of initialization.   |
| 4        | 0  | 0   | 0   | 0   | 0   | 0   | 0   | 1   | 1   | 0   | <div style="border: 1px solid black; width: 100px; height: 20px; margin-bottom: 2px; text-align: center;">_</div> <div style="border: 1px solid black; width: 100px; height: 20px;"></div>                            | Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the DD/CGRAM. Display is not shifted.         |
| 5        | 1  | 0   | 0   | 1   | 0   | 0   | 1   | 0   | 0   | 0   | <div style="border: 1px solid black; width: 100px; height: 20px; margin-bottom: 2px; text-align: center;">H_</div> <div style="border: 1px solid black; width: 100px; height: 20px;"></div>                           | Writes H. DDRAM has already been selected by initialization when the power was turned on. The cursor is incremented by one and shifted to the right. |
| 6        |  |     |     |     | .   | .   | .   | .   | .   | .   | <div style="border: 1px solid black; width: 100px; height: 20px; margin-bottom: 2px;"></div> <div style="border: 1px solid black; width: 100px; height: 20px;"></div>   |  |
| 7        | 1  | 0   | 0   | 1   | 0   | 0   | 1   | 0   | 0   | 1   | <div style="border: 1px solid black; width: 100px; height: 20px; margin-bottom: 2px; text-align: center;">HITACHI_</div> <div style="border: 1px solid black; width: 100px; height: 20px;"></div>                     | Writes I.  |
| 8        | 0  | 0   | 1   | 1   | 0   | 0   | 0   | 0   | 0   | 0   | <div style="border: 1px solid black; width: 100px; height: 20px; margin-bottom: 2px; text-align: center;">HITACHI</div> <div style="border: 1px solid black; width: 100px; height: 20px; text-align: center;">_</div> | Sets RAM address so that the cursor is positioned at the head of the second line.  |

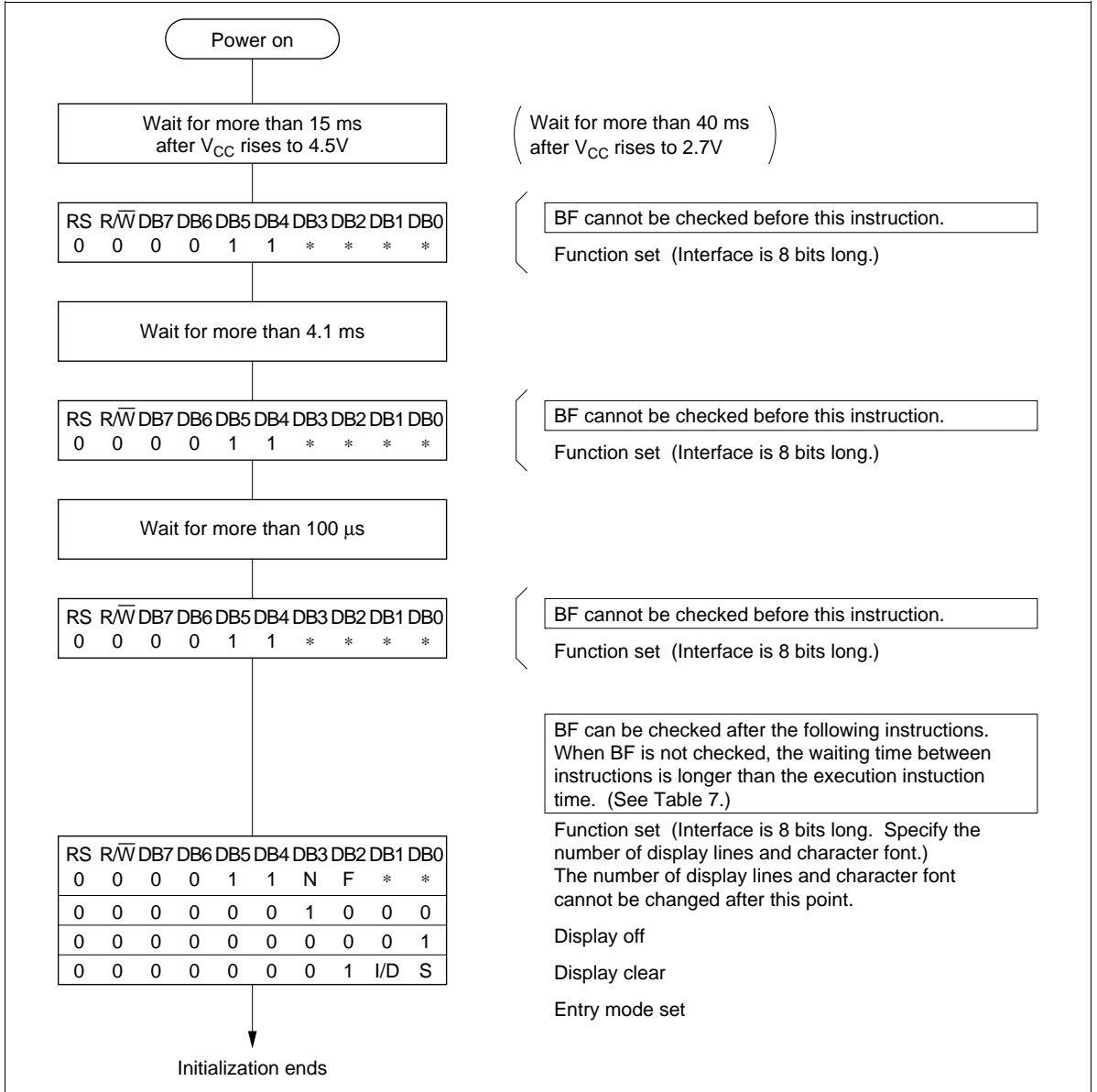
**Table 14 8-Bit Operation, 20-Digit × 2-Line Display Example with Internal Reset (cont)**

| Step |                           | Instruction |     |     |     |     |     |     |     |     |   | Display             | Operation  |
|------|---------------------------|-------------|-----|-----|-----|-----|-----|-----|-----|-----|---|---------------------|--|
| No.  | RS                        | R/W         | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |   |                     |  |
| 9    | Write data to CGRAM/DDRAM | 1           | 0   | 0   | 1   | 0   | 0   | 1   | 1   | 0   | 1 | HITACHI<br>M_       | Writes M.  |
| 10   |                           |             |     |     |     |     |     |     |     |     |   | .                   | .  |
| 11   | Write data to CGRAM/DDRAM | 1           | 0   | 0   | 1   | 0   | 0   | 1   | 1   | 1   | 1 | HITACHI<br>MICROCO_ | Writes O.  |
| 12   | Entry mode set            | 0           | 0   | 0   | 0   | 0   | 0   | 0   | 1   | 1   | 1 | HITACHI<br>MICROCO_ | Sets mode to shift display at the time of write.   |
| 13   | Write data to CGRAM/DDRAM | 1           | 0   | 0   | 1   | 0   | 0   | 1   | 1   | 0   | 1 | ITACHI<br>ICROCOM_  | Writes M. Display is shifted to the right. The first and second lines both shift at the same time. |
| 14   |                           |             |     |     |     |     |     |     |     |     |   | .                   | .  |
| 15   | Return home               | 0           | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 1   | 0 | HITACHI<br>MICROCOM | Returns both display and cursor to the original position (address 0).                              |

**Initializing by Instruction**

If the power supply conditions for correctly operating the internal reset circuit are not met, initialization by instructions becomes necessary.

Refer to Figures 24 and 25 for the procedures on 8-bit and 4-bit initializations, respectively.



**Figure 24 8-Bit Interface**

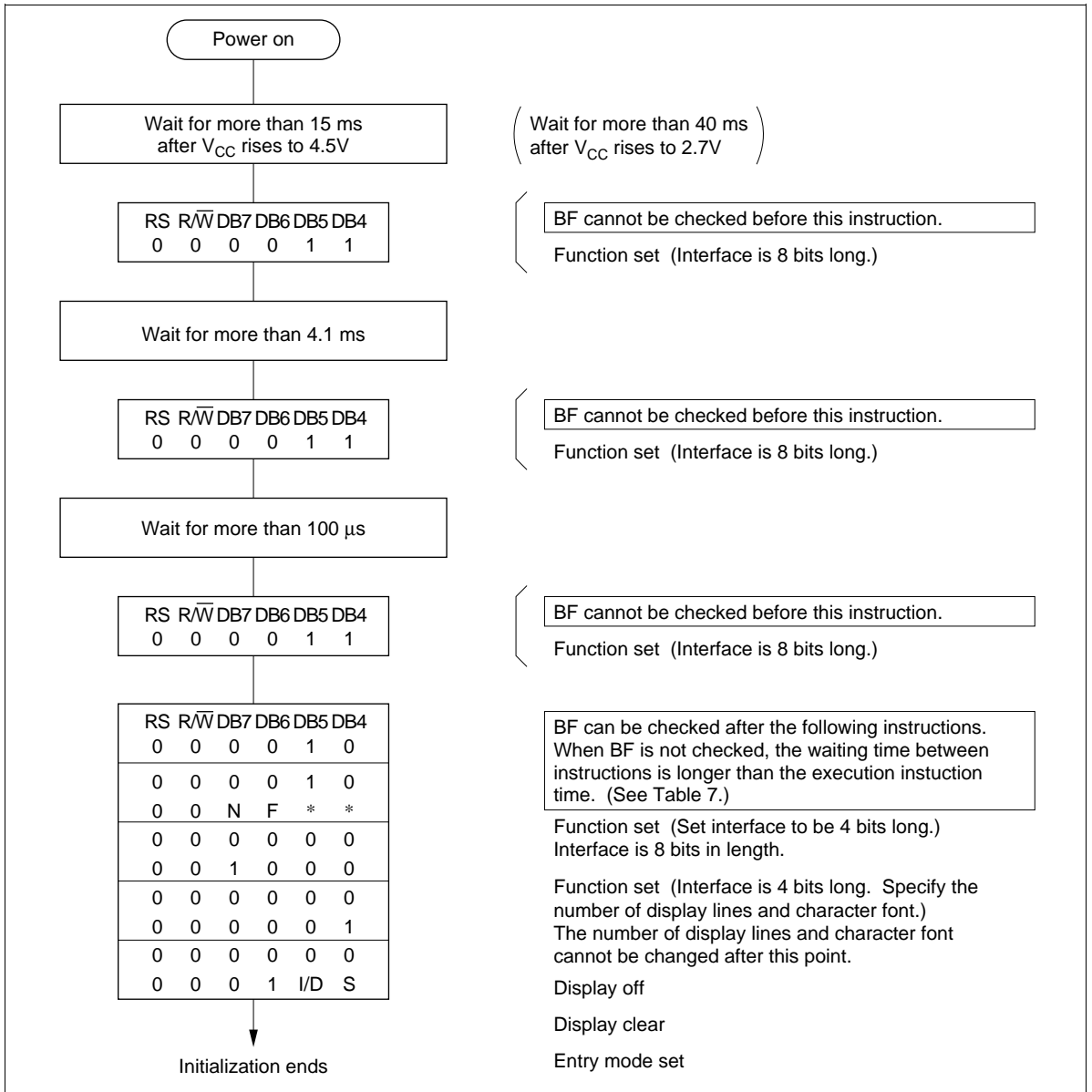


Figure 25 4-Bit Interface

**[Low voltage version]****Absolute Maximum Ratings\***

| <b>Item</b>              | <b>Symbol</b> | <b>Unit</b> | <b>Value</b>           | <b>Notes</b> |
|--------------------------|---------------|-------------|------------------------|--------------|
| Power supply voltage (1) | $V_{CC}$      | V           | -0.3 to +7.0           | 1            |
| Power supply voltage (2) | $V_{CC}-V_5$  | V           | -0.3 to +8.5           | 2            |
| Input voltage            | $V_t$         | V           | -0.3 to $V_{CC} + 0.3$ | 1            |
| Operating temperature    | $T_{opr}$     | °C          | -30 to +75             |              |
| Storage temperature      | $T_{stg}$     | °C          | -55 to +125            | 4            |

Note: 1. The operating temperature is 75°C.

If the LSI is used above these absolute maximum ratings, it may become permanently damaged. Using the LSI within the following electrical characteristic limits is strongly recommended for normal operation. If these electrical characteristic conditions are also exceeded, the LSI will malfunction and cause poor reliability. Refer to the Electrical Characteristics Notes section following these tables.

**DC Characteristics ( $V_{CC} = 2.7$  to  $5.5V$ ,  $T_a = -30$  to  $+75^{\circ}C^{*3}$ )**

| Item  | Symbol    | Min          | Typ | Max         | Unit       | Test Condition  | Notes* |
|---|-----------|--------------|-----|-------------|------------|---|--------|
| Input high voltage (1)<br>(except OSC1)     | VIH1      | $0.7V_{CC}$  | —   | $V_{CC}$    | V          |   | 6, 17  |
| Input low voltage (1)<br>(except OSC1)      | VIL1      | -0.3         | —   | 0.55        | V          |   | 6, 17  |
| Input high voltage (2)<br>(OSC1)            | VIH2      | $0.7V_{CC}$  | —   | $V_{CC}$    | V          |   | 15     |
| Input low voltage (2)<br>(OSC1)             | VIL2      | —            | —   | $0.2V_{CC}$ | V          |   | 15     |
| Output high voltage (1)<br>(D0–D7)          | VOH1      | $0.75V_{CC}$ | —   | —           | V          | $-I_{OH} = 0.1$ mA  | 7      |
| Output low voltage (1)<br>(DB0–DB7)         | VOL1      | —            | —   | $0.2V_{CC}$ | V          | $I_{OL} = 0.1$ mA   | 7      |
| Output high voltage (2)<br>(except DB0–DB7) | VOH2      | $0.8V_{CC}$  | —   | —           | V          | $-I_{OH} = 0.04$ mA   | 8      |
| Output low voltage (2)<br>(except D0–D7)    | VOL2      | —            | —   | $0.2V_{CC}$ | V          | $I_{OL} = 0.04$ mA  | 8      |
| Driver on resistance<br>(COM)               | $R_{COM}$ | —            | 2   | 20          | k $\Omega$ | $\pm I_d = 0.05$ mA (COM)   | 13     |
| Driver on resistance<br>(SEG)               | $R_{SEG}$ | —            | 2   | 30          | k $\Omega$ | $\pm I_d = 0.05$ mA (SEG)   | 13     |
| Input leakage current                       | $I_{LI}$  | -1           | —   | 1           | $\mu$ A    | $V_{IN} = 0$ to $V_{CC}$  | 9      |
| Pull-up MOS current<br>(RS, R/W, D0–D7)     | $-I_p$    | 10           | 50  | 120         | $\mu$ A    | $V_{CC} = 3V$   |        |
| Power supply current                        | $I_{CC}$  | —            | 150 | 300         | $\mu$ A    | $R_f$ oscillation,<br>external clock<br>$V_{CC} = 3V$ , $f_{OSC} = 320$ kHz | 10, 14 |
| LCD voltage                                 | VLCD1     | 3.0          | —   | 8.3         | V          | $V_{CC}-V_5$ , 1/5 bias   | 16     |
|   | VLCD2     | 3.0          | —   | 8.3         | V          | $V_{CC}-V_5$ , 1/4 bias   | 16     |

Note: \* Refer to the Electrical Characteristics Notes section following these tables.

**AC Characteristics ( $V_{CC} = 2.7$  to  $5.5V$ ,  $T_a = -30$  to  $+75^{\circ}C^{*3}$ )**
**Clock Characteristics**

| Item                     |                             | Symbol    | Min | Typ | Max | Unit    | Test Condition                             | Notes* |
|--------------------------|-----------------------------|-----------|-----|-----|-----|---------|--|--------|
| External clock operation | External clock frequency    | $f_{cp}$  | 125 | 270 | 410 | kHz     |  | 11     |
|                          | External clock duty         | Duty      | 45  | 50  | 55  | %       |  |        |
|                          | External clock rise time    | $t_{rcp}$ | —   | —   | 0.2 | $\mu s$ |  |        |
|                          | External clock fall time    | $t_{fcp}$ | —   | —   | 0.2 | $\mu s$ |  |        |
| $R_f$ oscillation        | Clock oscillation frequency | $f_{OSC}$ | 240 | 320 | 390 | kHz     | $R_f = 56\text{ k}\Omega$<br>$V_{CC} = 3V$ | 12     |

Note: \* Refer to the Electrical Characteristics Notes section following these tables.

**Bus Timing Characteristics**
**Write Operation**

| Item  | Symbol           | Min  | Typ | Max | Unit | Test Condition |
|---|------------------|------|-----|-----|------|----------------|
| Enable cycle time                               | $t_{cycE}$       | 1000 | —   | —   | ns   | Figure 27      |
| Enable pulse width (high level)                 | $PW_{EH}$        | 450  | —   | —   |      |                |
| Enable rise/fall time                           | $t_{Er}, t_{Ef}$ | —    | —   | 25  |      |                |
| Address set-up time (RS, $R/\overline{W}$ to E) | $t_{AS}$         | 40   | —   | —   |      |                |
| Address hold time                               | $t_{AH}$         | 20   | —   | —   |      |                |
| Data set-up time                                | $t_{DSW}$        | 195  | —   | —   |      |                |
| Data hold time                                  | $t_H$            | 10   | —   | —   |      |                |

**Read Operation**

| Item  | Symbol           | Min  | Typ | Max | Unit | Test Condition |
|---|------------------|------|-----|-----|------|----------------|
| Enable cycle time                               | $t_{cycE}$       | 1000 | —   | —   | ns   | Figure 28      |
| Enable pulse width (high level)                 | $PW_{EH}$        | 450  | —   | —   |      |                |
| Enable rise/fall time                           | $t_{Er}, t_{Ef}$ | —    | —   | 25  |      |                |
| Address set-up time (RS, $R/\overline{W}$ to E) | $t_{AS}$         | 40   | —   | —   |      |                |
| Address hold time                               | $t_{AH}$         | 20   | —   | —   |      |                |
| Data delay time                                 | $t_{DDR}$        | —    | —   | 350 |      |                |
| Data hold time                                  | $t_{DHR}$        | 10   | —   | —   |      |                |

## Interface Timing Characteristics with External Driver (HD66702)

| Item                 |            | Symbol    | Min   | Typ | Max  | Unit | Test Condition |
|----------------------|------------|-----------|-------|-----|------|------|----------------|
| Clock pulse width    | High level | $t_{CWH}$ | 800   | —   | —    | ns   | Figure 28      |
|                      | Low level  | $t_{CWL}$ | 800   | —   | —    |      |                |
| Clock set-up time    |            | $t_{CSU}$ | 500   | —   | —    |      |                |
| Data set-up time     |            | $t_{SU}$  | 300   | —   | —    |      |                |
| Data hold time       |            | $t_{DH}$  | 300   | —   | —    |      |                |
| M delay time         |            | $t_{DM}$  | -1000 | —   | 1000 |      |                |
| Clock rise/fall time |            | $t_{ct}$  | —     | —   | 200  |      |                |

## Power Supply Conditions Using Internal Reset Circuit

| Item                   |  | Symbol    | Min | Typ | Max | Unit | Test Condition |
|------------------------|--|-----------|-----|-----|-----|------|----------------|
| Power supply rise time |  | $t_{rCC}$ | 0.1 | —   | 10  | ms   | Figure 29      |
| Power supply off time  |  | $t_{OFF}$ | 1   | —   | —   |      |                |

## [Standard Voltage Version]

### Absolute Maximum Ratings\*

| Item                     | Symbol       | Unit | Value                | Notes |
|--------------------------|--------------|------|----------------------|-------|
| Power supply voltage (1) | $V_{CC}$     | V    | -0.3 to +7.0         | 1     |
| Power supply voltage (2) | $V_{CC}-V_5$ | V    | -0.3 to +8.5         | 2     |
| Input voltage            | $V_t$        | V    | -0.3 to $V_{CC}+0.3$ | 1     |
| Operating temperature    | $T_{opr}$    | °C   | -30 to +75           |       |
| Storage temperature      | $T_{stg}$    | °C   | -55 to +125          | 4     |

Note: \* If the LSI is used above these absolute maximum ratings, it may become permanently damaged. Using the LSI within the following electrical characteristic limits is strongly recommended for normal operation. If these electrical characteristic conditions are also exceeded, the LSI will malfunction and cause poor reliability. Refer to the Electrical Characteristics Notes section following these tables.

**DC Characteristics ( $V_{CC} = 5V \pm 10\%$ ,  $T_a = -30$  to  $+75^\circ C^{*3}$ )**

| Item                                      | Symbol    | Min          | Typ | Max          | Unit       | Test Condition  | Notes* |
|---|-----------|--------------|-----|--------------|------------|---|--------|
| Input high voltage (1)<br>(except OSC1)   | VIH1      | 2.2          | —   | $V_{CC}$     | V          |   | 6, 17  |
| Input low voltage (1)<br>(except OSC1)    | VIL1      | -0.3         | —   | 0.6          | V          |   | 6, 17  |
| Input high voltage (2)<br>(OSC1)          | VIH2      | $V_{CC}-1.0$ | —   | $V_{CC}$     | V          |   | 15     |
| Input low voltage (2)<br>(OSC1)           | VIL2      | —            | —   | 1.0          | V          |   | 15     |
| Output high voltage (1)<br>(DB0-DB7)      | VOH1      | 2.4          | —   | —            | V          | $-I_{OH} = 0.205$ mA  | 7      |
| Output low voltage (1)<br>(DB0-DB7)       | VOL1      | —            | —   | 0.4          | V          | $I_{OL} = 1.6$ mA   | 7      |
| Output high voltage (2)<br>(except D0-D7) | VOH2      | $0.9 V_{CC}$ | —   | —            | V          | $-I_{OH} = 0.04$ mA   | 8      |
| Output low voltage (2)<br>(except D0-D7)  | VOL2      | —            | —   | $0.1 V_{CC}$ | V          | $I_{OL} = 0.04$ mA  | 8      |
| Driver on resistance<br>(COM)             | $R_{COM}$ | —            | 2   | 20           | k $\Omega$ | $\pm I_d = 0.05$ mA (COM)   | 13     |
| Driver on resistance<br>(SEG)             | $R_{SEG}$ | —            | 2   | 30           | k $\Omega$ | $\pm I_d = 0.05$ mA (SEG)   | 13     |
| Input leakage current                     | $I_{LI}$  | -1           | —   | 1            | $\mu A$    | $V_{IN} = 0$ to $V_{CC}$  | 9      |
| Pull-up MOS current<br>(RS, R/W, D0-D7)   | $-I_p$    | 50           | 125 | 250          | $\mu A$    | $V_{CC} = 5V$   |        |
| Power supply current                      | $I_{CC}$  | —            | 350 | 600          | $\mu A$    | $R_f$ oscillation,<br>external clock<br>$V_{CC} = 5V$ , $f_{osc} = 320$ kHz | 10, 14 |
| LCD voltage                               | VLCD1     | 3.0          | —   | 8.3          | V          | $V_{CC}-V_5$ , 1/5 bias   | 16     |
|   | VLCD2     | 3.0          | —   | 8.3          | V          | $V_{CC}-V_5$ , 1/4 bias   | 16     |

Note: \* Refer to the Electrical Characteristics Notes section following these tables.

**AC Characteristics ( $V_{CC} = 5V \pm 10\%$ ,  $T_a = -30$  to  $+75^\circ C^{*3}$ )**

**Clock Characteristics**

| Item                     |                             | Symbol    | Min | Typ | Max | Unit    | Test Condition                             | Notes* |
|--------------------------|-----------------------------|-----------|-----|-----|-----|---------|--|--------|
| External clock operation | External clock frequency    | $f_{cp}$  | 125 | 270 | 410 | kHz     |  | 11     |
|                          | External clock duty         | Duty      | 45  | 50  | 55  | %       |  | 11     |
|                          | External clock rise time    | $t_{rcp}$ | —   | —   | 0.2 | $\mu s$ |  | 11     |
|                          | External clock fall time    | $t_{fcp}$ | —   | —   | 0.2 | $\mu s$ |  | 11     |
| $R_f$ oscillation        | Clock oscillation frequency | $f_{OSC}$ | 220 | 320 | 420 | kHz     | $R_f = 68\text{ k}\Omega$<br>$V_{CC} = 5V$ | 12     |

Note: \* Refer to the Electrical Characteristics Notes section following these tables.

**Bus Timing Characteristics**

**Write Operation**

| Item  | Symbol           | Min  | Typ | Max | Unit | Test Condition |
|---|------------------|------|-----|-----|------|----------------|
| Enable cycle time                               | $t_{cycE}$       | 1000 | —   | —   | ns   | Figure 26      |
| Enable pulse width (high level)                 | $PW_{EH}$        | 450  | —   | —   |      |                |
| Enable rise/fall time                           | $t_{Er}, t_{Ef}$ | —    | —   | 25  |      |                |
| Address set-up time (RS, $R/\overline{W}$ to E) | $t_{AS}$         | 40   | —   | —   |      |                |
| Address hold time                               | $t_{AH}$         | 10   | —   | —   |      |                |
| Data set-up time                                | $t_{DSW}$        | 195  | —   | —   |      |                |
| Data hold time                                  | $t_H$            | 10   | —   | —   |      |                |

**Read Operation**

| Item  | Symbol           | Min  | Typ | Max | Unit | Test Condition |
|---|------------------|------|-----|-----|------|----------------|
| Enable cycle time                               | $t_{cycE}$       | 1000 | —   | —   | ns   | Figure 27      |
| Enable pulse width (high level)                 | $PW_{EH}$        | 450  | —   | —   |      |                |
| Enable rise/fall time                           | $t_{Er}, t_{Ef}$ | —    | —   | 25  |      |                |
| Address set-up time (RS, $R/\overline{W}$ to E) | $t_{AS}$         | 40   | —   | —   |      |                |
| Address hold time                               | $t_{AH}$         | 10   | —   | —   |      |                |
| Data delay time                                 | $t_{DDR}$        | —    | —   | 320 |      |                |
| Data hold time                                  | $t_{DHR}$        | 20   | —   | —   |      |                |

**Interface Timing Characteristics with External Driver (HD66702)**

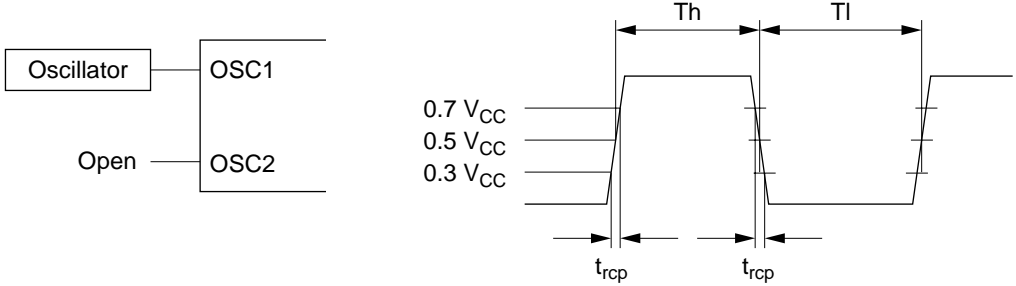
| <b>Item</b>          |            | <b>Symbol</b> | <b>Min</b> | <b>Typ</b> | <b>Max</b> | <b>Unit</b> | <b>Test Condition</b> |
|----------------------|------------|---------------|------------|------------|------------|-------------|-----------------------|
| Clock pulse width    | High level | $t_{CWH}$     | 800        | —          | —          | ns          | Figure 28             |
|                      | Low level  | $t_{CWL}$     | 800        | —          | —          |             |                       |
| Clock set-up time    |            | $t_{CSU}$     | 500        | —          | —          |             |                       |
| Data set-up time     |            | $t_{SU}$      | 300        | —          | —          |             |                       |
| Data hold time       |            | $t_{DH}$      | 300        | —          | —          |             |                       |
| M delay time         |            | $t_{DM}$      | -1000      | —          | 1000       |             |                       |
| Clock rise/fall time |            | $t_{ct}$      | —          | —          | 100        |             |                       |

**Power Supply Conditions Using Internal Reset Circuit**

| <b>Item</b>            |  | <b>Symbol</b> | <b>Min</b> | <b>Typ</b> | <b>Max</b> | <b>Unit</b> | <b>Test Condition</b> |
|------------------------|--|---------------|------------|------------|------------|-------------|-----------------------|
| Power supply rise time |  | $t_{ICC}$     | 0.1        | —          | 10         | ms          | Figure 29             |
| Power supply off time  |  | $t_{OFF}$     | 1          | —          | —          |             |                       |

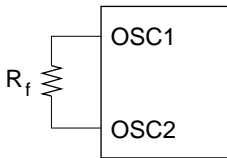


6. Applies to input pins and I/O pins, excluding the OSC1 pin.
7. Applies to I/O pins.
8. Applies to output pins.
9. Current flowing through pull-up MOSs, excluding output drive MOSs.
10. Input/output current is excluded. When input is at an intermediate level with CMOS, the excessive current flows through the input circuit to the power supply. To avoid this from happening, the input level must be fixed high or low.
11. Applies only to external clock operation.



$$\text{Duty} = \frac{T_h}{T_h + T_l} \times 100\%$$

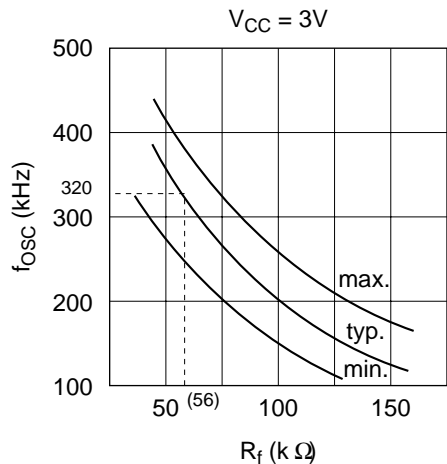
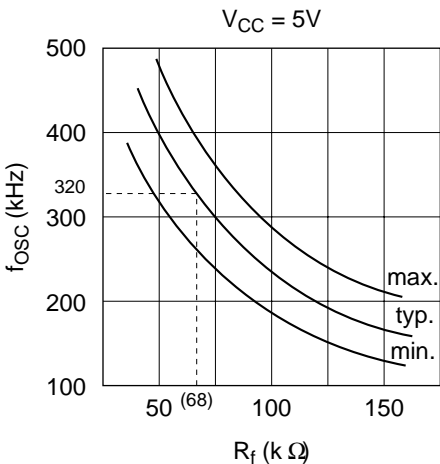
12. Applies only to the internal oscillator operation using oscillation resistor  $R_f$ .



$R_f$ : 56 k $\Omega$   $\pm$  2% (when  $V_{CC} = 3V$ )

$R_f$ : 68 k $\Omega$   $\pm$  2% (when  $V_{CC} = 5V$ )

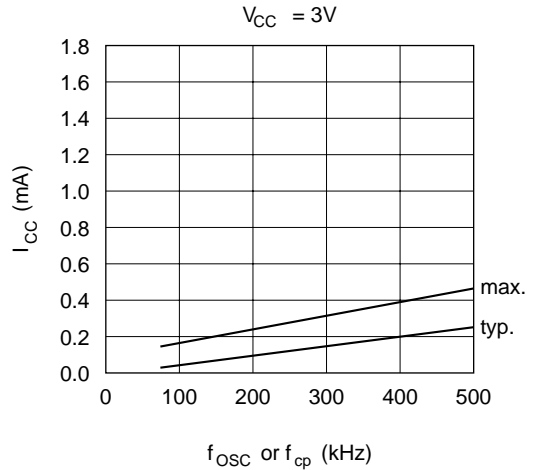
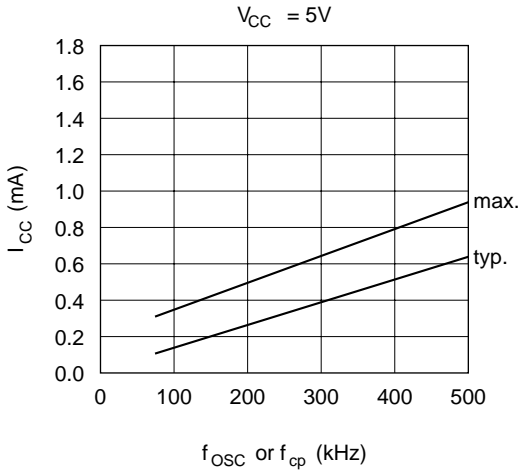
Since the oscillation frequency varies depending on the OSC1 and OSC2 pin capacitance, the wiring length to these pins should be minimized.



13.  $R_{COM}$  is the resistance between the power supply pins ( $V_{CC}$ , V1, V4, V5) and each common signal pin (COM1 to COM16).

$R_{SEG}$  is the resistance between the power supply pins ( $V_{CC}$ , V2, V3, V5) and each segment signal pin (SEG1 to SEG100).

14. The following graphs show the relationship between operation frequency and current consumption.



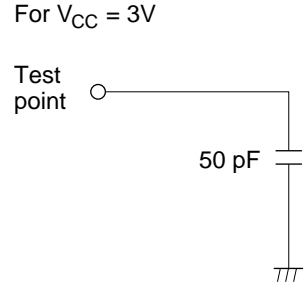
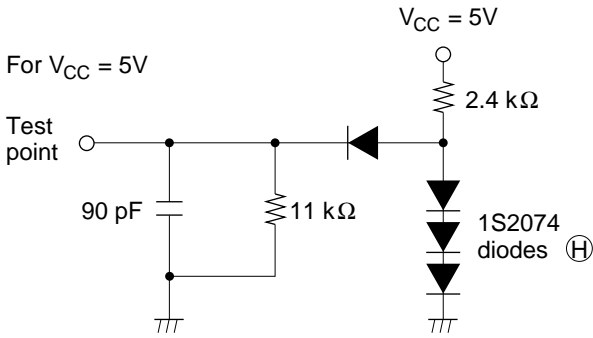
15. Applies to the OSC1 pin.

16. Each COM and SEG output voltage is within  $\pm 0.15V$  of the LCD voltage ( $V_{CC}$ , V1, V2, V3, V4, V5) when there is no load.

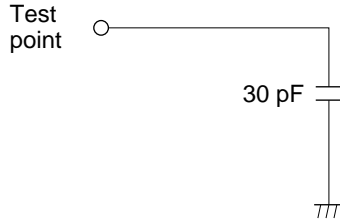
17. The TEST pin should be fixed to GND and the EXT pin should be fixed to  $V_{CC}$  or GND.

Load Circuits

Data Bus DB0 to DB7



External Driver Control Signal: CL1, CL2, D, M (HD66702)



Timing Characteristics

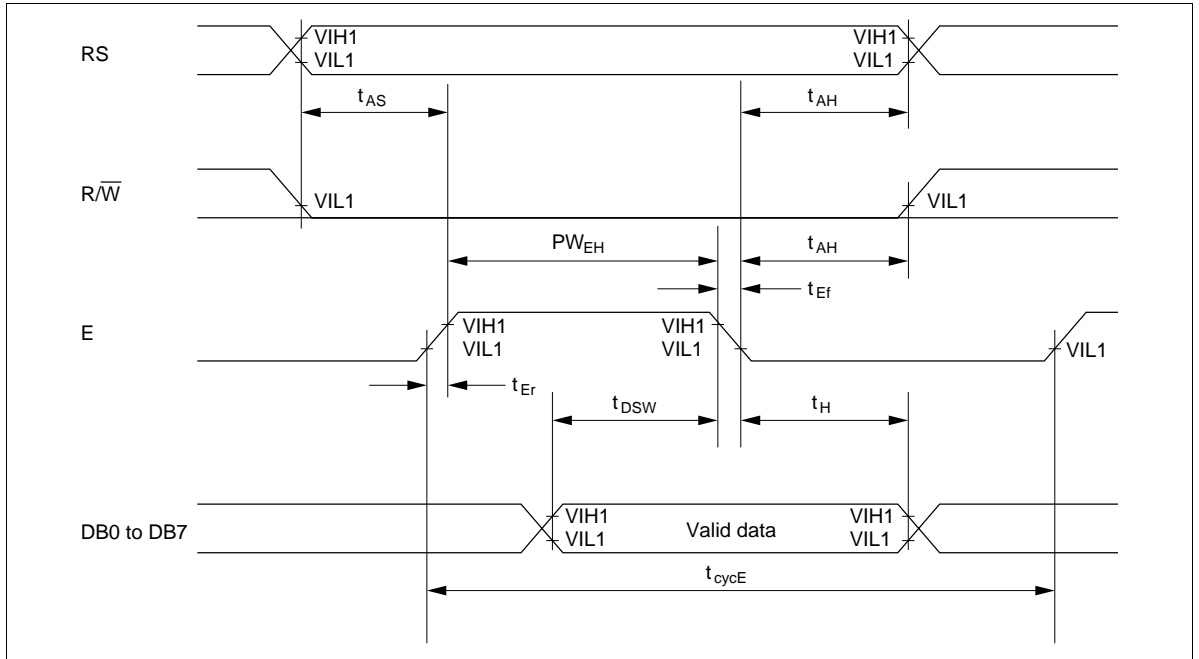


Figure 26 Write Operation

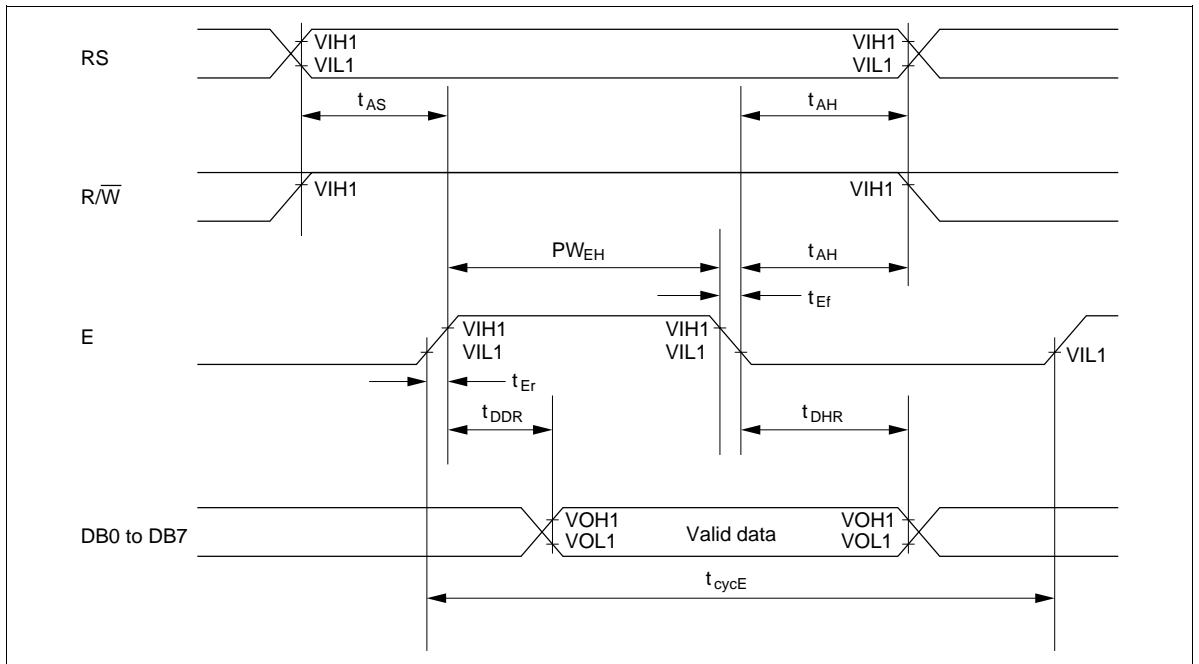


Figure 27 Read Operation

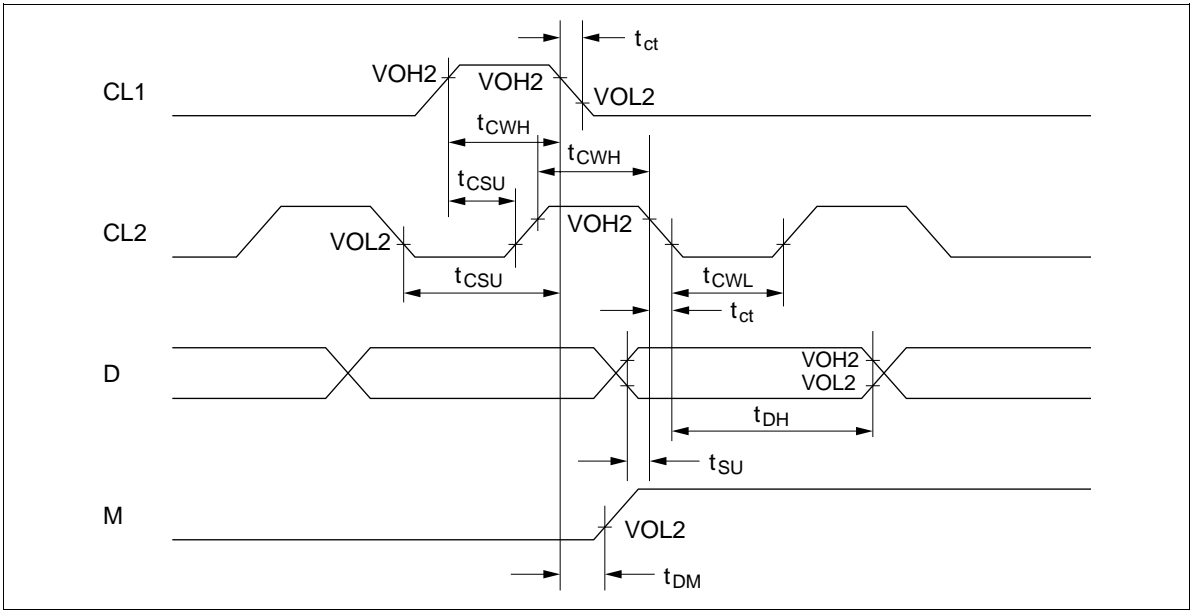
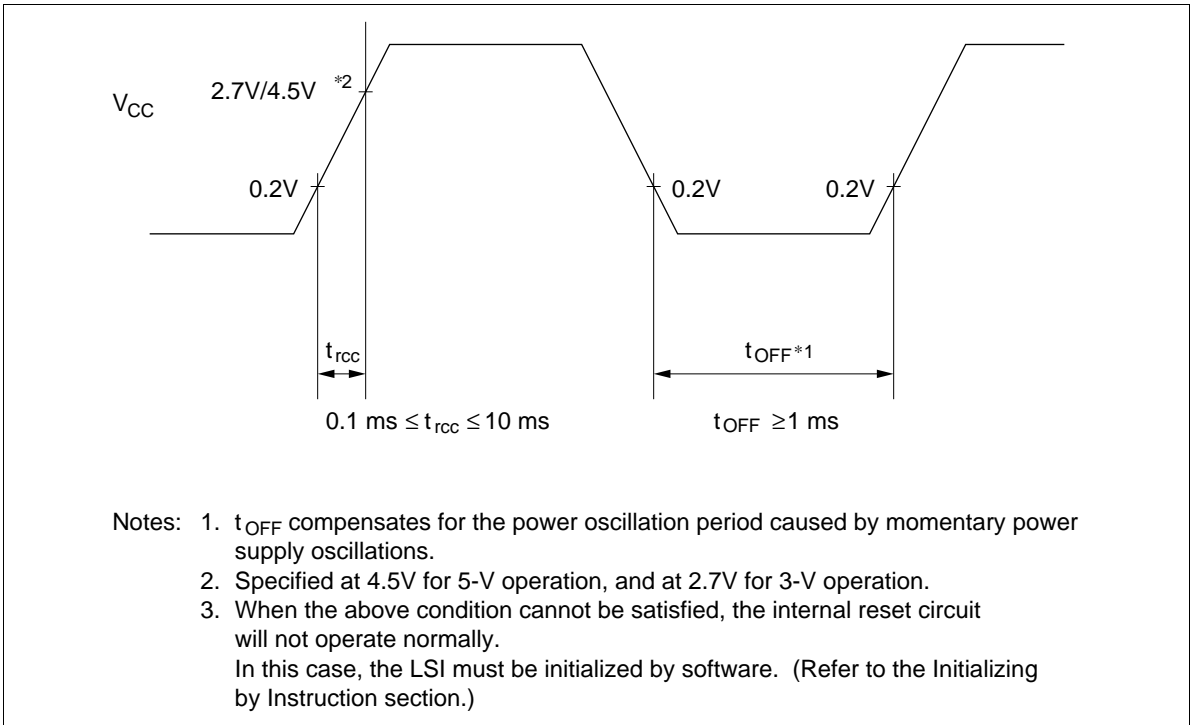


Figure 28 Interface Timing with External Driver (HD66702)



- Notes:
1.  $t_{OFF}$  compensates for the power oscillation period caused by momentary power supply oscillations.
  2. Specified at 4.5V for 5-V operation, and at 2.7V for 3-V operation.
  3. When the above condition cannot be satisfied, the internal reset circuit will not operate normally.  
In this case, the LSI must be initialized by software. (Refer to the Initializing by Instruction section.)

Figure 29 Internal Power Supply Reset

## Cautions

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