

NEC

NEC Electronics Inc.

μPD42S64800, 42S65800**8,388,608 x 8-Bit****Dynamic CMOS RAM****Preliminary****September 1993****Description**

The μPD42S64800 and μPD42S65800 are 64M-bit dynamic RAMs organized as 8,388,608 words by 8 bits. They are designed to operate from a single +3.3-volt power supply and have an optional fast-page mode.

Advanced polycide technology minimizes silicon areas and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and advanced CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative voltage substrate bias—automatically and transparently.

The three-state outputs are controlled by $\overline{\text{CAS}}$ independent of $\overline{\text{RAS}}$. After a valid read or read-modify-write cycle, data is held on the outputs by maintaining $\overline{\text{CAS}}$ low. Data outputs return to high impedance when $\overline{\text{CAS}}$ goes high. Fast-page read and write cycles can be executed by cycling $\overline{\text{CAS}}$.

Refreshing may be accomplished by a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycle that internally generates the refresh address. Refreshing can also be accomplished by $\overline{\text{RAS}}$ -only refresh cycles or by normal read or write cycles during a 256-ms refresh period.

Two versions of the 8M x 8-bit DRAM are available. The μPD42S64800 uses 8192 combinations of $A_0 - A_{12}$ for

$\overline{\text{RAS}}$ -only refreshing and 4096 address combinations of $A_0 - A_{11}$ to perform $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ and hidden refreshing of the memory during a 256-ms period. The μPD42S65800 uses 4096 address combinations of $A_0 - A_{11}$ during a 256-ms period for all refresh modes.

The μPD42S64800 and μPD42S65800 are available in a 34-pin plastic SOJ and 34-pin plastic TSOP.

Features

- 8,388,608 x 8-bit organization
- Single +3.3-volt power supply
- Fast-page option
- Low power dissipation: 0.72 mW (max) standby
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh or self-refresh cycles
- Multiplexed address inputs
- On-chip substrate bias generator
- TTL-compatible inputs and outputs
- Nonlatched, three-state outputs
- Low input capacitance
- 34-pin plastic SOJ and TSOP packaging

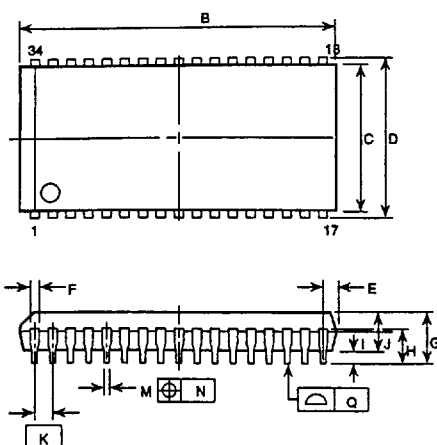
Ordering Information

Part Number	Access Time (max)	R/W Cycle (max)	Fast-Page Cycle (max)	Active Power (max)	Package
μPD42S64800LG-A50	50 ns	90 ns	35 ns	378 mW	34-pin plastic SOJ
-A60	60 ns	110 ns	40 ns	342 mW	
-A70	70 ns	130 ns	45 ns	306 mW	
-A80	80 ns	150 ns	50 ns	270 mW	
μPD42S64800G7-A50	50 ns	90 ns	35 ns	378 mW	34-pin plastic TSOP
-A60	60 ns	110 ns	40 ns	342 mW	
-A70	70 ns	130 ns	45 ns	306 mW	
-A80	80 ns	150 ns	50 ns	270 mW	
μPD42S65800LG-A50	50 ns	90 ns	35 ns	486 mW	34-pin plastic SOJ
-A60	60 ns	110 ns	40 ns	414 mW	
-A70	70 ns	130 ns	45 ns	378 mW	
-A80	80 ns	150 ns	50 ns	342 mW	
μPD42S65800G7-A50	50 ns	90 ns	35 ns	486 mW	34-pin plastic TSOP
-A60	60 ns	110 ns	40 ns	414 mW	
-A70	70 ns	130 ns	45 ns	378 mW	
-A80	80 ns	150 ns	50 ns	342 mW	

μPD42S64800, 42S65800**34-Pin Plastic SOJ (500-mil)**

Item	Millimeters	Inches
B	22.42 ± 0.2	.883 ± 0.008
C	12.7	.500
D	13.72 ± 0.2	.540 ± 0.008
E	1.05 ± 0.15	.041 ± .007
F	0.74	.029
G	3.5 ± 0.2	.138 ± .008
H	2.545 ± 0.2	.100 ± .008
I	0.8 min	.031 min
J	2.6	.102
K	1.27 (TP)	.050 (TP)
M	0.40 ± 0.10	.016 ± .004
N	0.12	.005
P*	11.94 ± 0.2	.470 ± .008
Q	0.10	.004
T	0.85 rad	.033 rad
U	0.20 ± 0.10	.008 ± .004
	-0.05	-.002

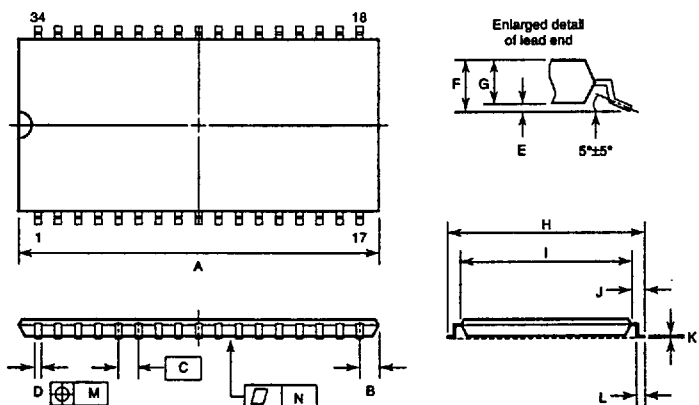
* Item P to center of leads.

**SOJ or TSOP**

V _{CC}	1	34	V _{SS}
I/O ₁	2	33	I/O ₈
I/O ₂	3	32	I/O ₇
I/O ₃	4	31	I/O ₆
I/O ₄	5	30	I/O ₅
NC	6	29	V _{SS}
V _{CC}	7	28	CAS
WE	8	27	OE
RAS	9	26	NC
NC	10	25	A ₁₂
A ₀	11	24	A ₁₁
A ₁	12	23	A ₁₀
A ₂	13	22	A ₉
A ₃	14	21	A ₈
A ₄	15	20	A ₇
A ₅	16	19	A ₆
V _{CC}	17	18	V _{SS}

34-Pin Plastic TSOP (500 mil)

Item	Millimeters	Inches
A	22.66 max	.893 max
B	1.20 max	.048 max
C	1.27 (TP)	.050 (TP)
D	0.40 ± 0.10	.016 ± .004
E	0.05 ± 0.05	.002 ± .002
F	1.10 max	.044 max
G	0.97	.038
H	14.3 ± 0.2	.563 ± 0.008
I	12.7 ± 0.1	.500 ± 0.004
J	0.8 ± 0.2	.031 ± .008
K	0.125 ± 0.10	.005 ± .004
	-0.05	-.002
L	0.5 ± 0.1	.020 ± .004
	-0.05	-.002
M	0.21	.009
N	0.10	.004



A ₀ to A ₁₁ (A ₁₂)	Address inputs
I/O ₁ to I/O ₈	Data inputs/outputs
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
OE	Output enable
V _{CC}	Supply voltage
V _{SS}	Ground
NC	No connection

NEC**NEC Electronics Inc.**

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