Advance Data Sheet

T7210A Manchester Decoder and Interface Chip (MDIC)

Features

- Compatible with IEEE 802.3 10BASE-T proposed standards
- Contains precision timing elements controlled by a delay-locked loop
- Detects end-of-packet delimiter (IDL)
- Detects Manchester code violations
- Recovers data and clock signals from incoming 10 Mbits/s Manchester data
- Decodes the recovered Manchester data into NRZ form
- Interface to a T7300 LAN Controller
- Designed for 10BASE-T station or repeater

Description

The T7210A Manchester Decoder and Interface Chip (MDIC) is a general-purpose VLSI device that provides 10 Mbits/s Manchester decoding and interfacing functions. The device recovers and decodes 10 Mbits/s serial Manchester data from a line receiver and produces NRZ data and clock signals for the controller chip. The T7210A MDIC detects Manchester code violations and reports these to the controller. To prevent line over-charge, the transmitter control section of the MDIC provides a predistortion signal. The device provides essential timing recovery functions for the 10BASE-T stations, repeaters, and any LAN applications based to 10 Mbits/s Manchester-coded data format. The T7210A MDIC is fabricated by using linear CMOS technology and is available in a 24-pin, plastic DIP or a 28-pin, plastic SOJ package.

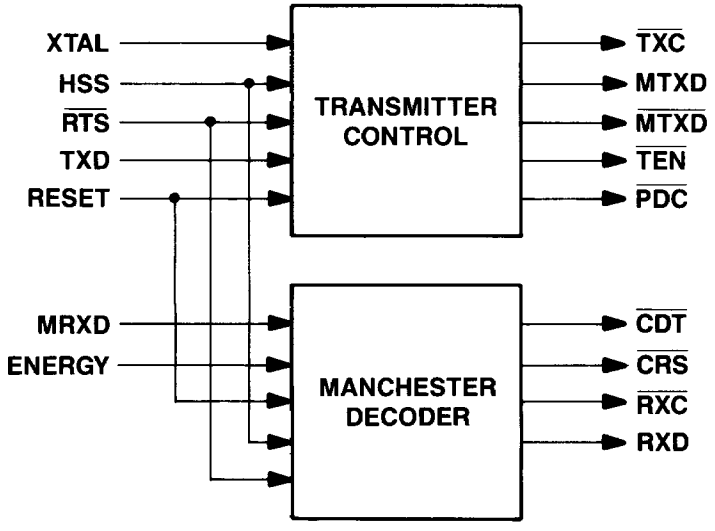


Figure 1. Block Diagram

User Information

Pin Descriptions

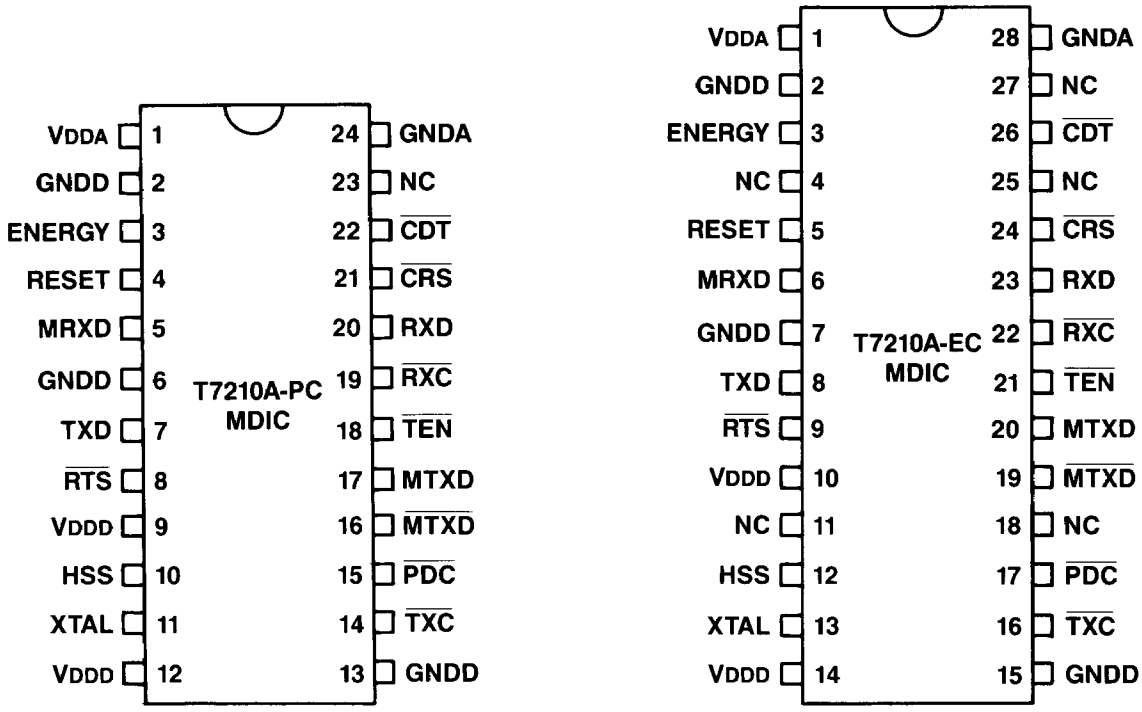


Figure 2. 24-Pin, Plastic DIP and 28-Pin, Plastic SOJ Pin Function Diagrams

Table 1. Pin Descriptions

Symbol	Type	Name/Function
VDDA	—	**+5 V Supply.**
GNDD	—	**Ground.** 0.0 V.
ENERGY	I	**Carrier Energy.** This pin is asserted at the beginning of a packet, indicating that carrier energy on the line receiver has exceeded the noise threshold and that data packets are following. Data is assumed to be stabilized and valid after two bit-times. This pin must remain high until the packet has been completely received. It must be de-asserted within the inter-frame spacing (IFS).
RESET	I	**Reset.** This pin is active-high. Reset must be low for normal MDIC operations. The XTAL must be running; reset takes 1 ms to complete. Reset is an optional feature not required for most applications.
MRXD	I	**Manchester-Coded Receive Data.** This pin carries the received Manchester-coded data, collision presence (CP), or IDL. The T7210A device can lock onto and track Manchester data with $\leq \pm$ 18 ns of jitter, as defined in IEEE 802.3 standards.
GNDD	—	**Ground.** 0.0 V.

Table 1. Pin Descriptions (Continued)

Symbol	Type	Name/Function
TXD	I	**Transmit Data.** A signal on this pin carries a Manchester data stream from the controller. The rise and fall times should be less than 10 ns. When in the station mode, the transition time of TXD from TXC low or high should be less than 40 ns.
$\overline{\text{RTS}}$	I	**Request To Send (Active-Low).** This signal indicates the data from the controller is valid on the TXD input. It is used as a transmitter-enable signal by MDIC. If HSS is high (station), the RTS signal will be internally delayed by 2.5 bit-times so that the MDIC does not transmit extra bits ahead of preamble. If HSS is low (Hub), the RTS signal is delayed 0.5 bit-times.
VDDD	—	**+5 V Supply.**
HSS	I	**Hub or Station Select.** If Hub is selected (HSS = low), the RTS signal is delayed 0.5 bit-times. If station is selected (HSS = high), the RTS signal will be delayed 2.5 bit-times.
XTAL	I	**Crystal Oscillator Input.** This pin is a 20 MHz ± 0.01% (50% ± 10% duty cycle) frequency reference input for internal chip timing and data transmission synchronization.
VDDD	—	**+5 V Supply.**
GNDD	—	**Ground.** 0.0 V.
$\overline{\text{TXC}}$	O	**Transmit Clock (Active-Low).** This pin outputs a 10 MHz clock signal with a maximum rise and fall time of 5 ns to the controller. The high or low time should be > 40 ns.
$\overline{\text{PDC}}$	O	**Predistortion Control (Active-Low).** A predistortion control signal reduces the amount of jitter by preventing overcharge. This pin should be high during the second half of a wide data pulse, which is either high or low. For IDL, it should go high after a half bit-time from the start of IDL. $\overline{\text{PDC}}$ is edge-synchronous ± 1.5 ns with MTXD and $\overline{\text{MTXD}}$. While in a low state, $\overline{\text{PDC}}$ should not produce any glitches. A high on this pin sets $\overline{\text{PDC}}$ in an inactive state.
$\overline{\text{MTXD}}$	O	**Manchester-Coded Transmit Data Complement (Active-Low).** A signal on this pin is used to drive a line transmitter without a signal skew. MTXD and $\overline{\text{MTXD}}$ should be edge-synchronous within 1.5 ns.
MTXD	O	**Manchester-Coded Transmit Data.** This pin receives the transmit data from MDIC. The MTXD output follows TXD, which must be in a Manchester-coded format.

Table 1. Pin Descriptions (Continued)

Symbol	Type	Name/Function
$\overline{\text{TEN}}$	O	**Transmitter Enable (Active-Low).** An active-low from this pin enables the line transmitter. This pin must go low with the front bit boundary of the first valid bit of MTXD within ± 1.5 ns and remains low until the end of the IDL signal.
$\overline{\text{RXC}}$	O	**Receive Clock (Active-Low).** This clock signal is derived from the Manchester data. The nominal period is 100 ns. Synchronization with the incoming data occurs before $\overline{\text{CRS}}$ is asserted. When MRXD is idle, the clock is self-running at a frequency of 10 MHz ± 0.01%.
RXD	O	**Receive Data (NRZ).** This pin is tied directly to the RXD input of the T7300 device (or Hub controller) and is sampled by the T7300 at the negative edge of $\overline{\text{RXC}}$. The bit-stream received from the line receiver is recovered and Manchester-decoded into NRZ format prior to being transferred to the controller through this pin. RXD data is assumed to be valid as long as $\overline{\text{CRS}}$ is asserted. Internally, RXD transitions are on the rising edge of $\overline{\text{RXC}}$. RXD is high during an idle state and is clamped low during collision.
$\overline{\text{CRS}}$	O	**Carrier Sensed (Active-Low).** An active-low output from this pin signals to the controller that there is valid data available on the RXD output to be taken on the next falling edge of $\overline{\text{RXC}}$.
$\overline{\text{CDT}}$	O	**Collision Detected (Active-Low).** This pin is asserted if a Manchester-code violation (except IDL) is detected on the incoming data. A collision by code violation should be asserted if a missing midbit transition is detected once the T7210A is synchronized to the incoming data. When $\overline{\text{CDT}}$ is asserted, RXD is low.
NC	—	**No Connection.**
GNDA	—	**Analog Ground.** 0.0 V.

Overview

The T7210A MDIC is used in station interfaces (see Figure 3) and Hub interfaces (see Figure 4) for twisted-pair (TP) and AUI applications.

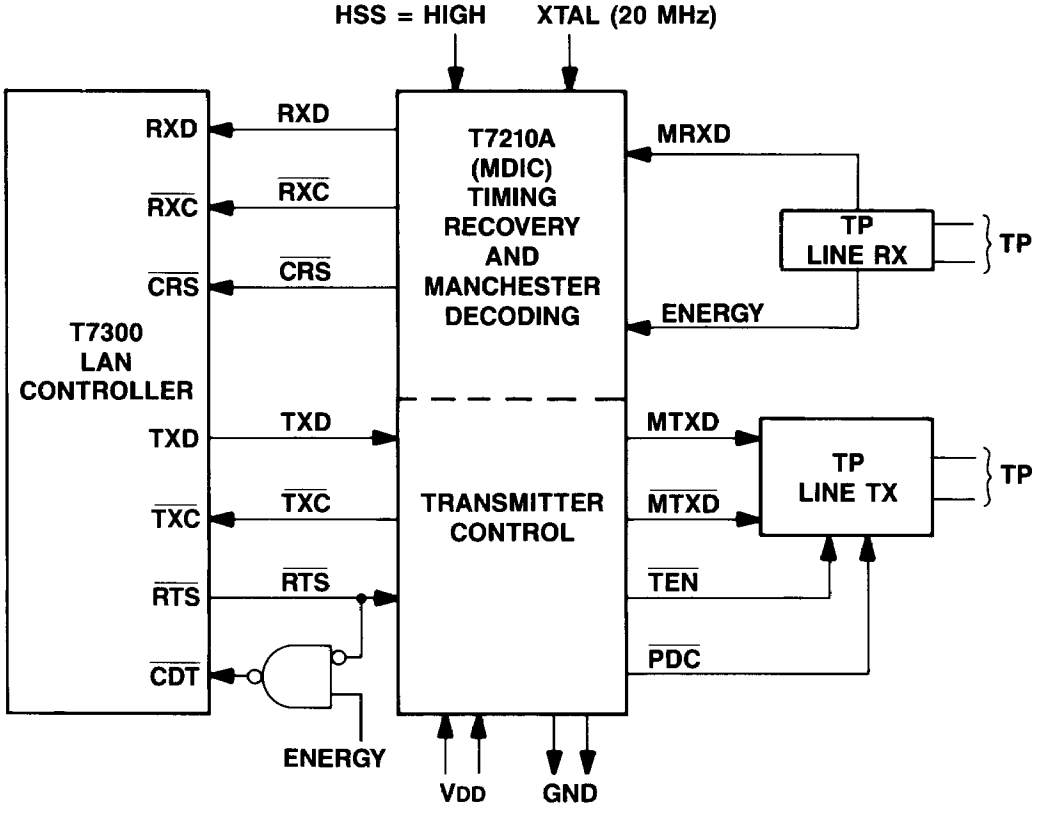


Figure 3. Station Interface Application Diagram

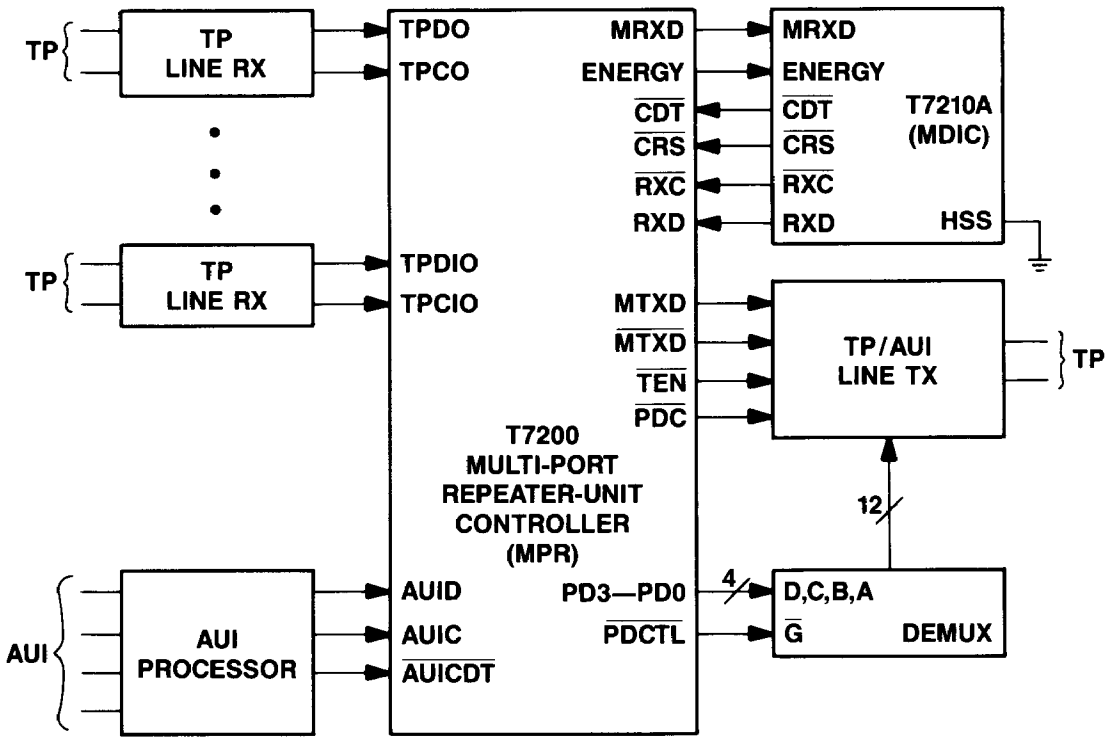


Figure 4. Hub Interface Application Diagram

Characteristics

Electrical Characteristics

T_A = 0 °C to 70 °C, V_{DD} = 5 V ±10%, V_{SS} = 0.0 V

Parameter	Symbol	Test Conditions	Min	Max	Unit
Input Voltage:					
Low	V_{IL}	—	−0.5	0.6	V
High	V_{IH}	—	2.0	V_{DD} + 0.5	V
Output Voltage:					
Low	V_{OL}	I_{OL} = 25 mA	—	0.5	V
High	V_{OH}	I_{OH} = −25 mA	2.4	—	V
Power Supply Current:*					
No traffic load	I_{DD}	V_{DD} = 5.0 V	—	40	mA
With traffic load	I_{DD}	V_{DD} = 5.0 V	—	80	mA
Input Leakage Current:					
TTL inputs	I_{ILH}, I_{ILL}	V_{IH} = 5.5 V	—	10	μA
Power Dissipation:*					
No traffic load	PD	V_{DD} = 5.0 V	—	0.20	W
With traffic load	PD	V_{DD} = 5.0 V	—	0.4	W
Output Rise and Fall Time	tr	C_{LOAD} = 20 pF	—	5	ns
	tf	C_{LOAD} = 20 pF	—	5	ns

* Not including excessive output buffer loads.

Absolute Maximum Ratings

Ambient Operating Temperature (T_A) Range ..... 0 °C to 70 °C
Storage Temperature (T_{stg}) Range ..... −40 °C to +125 °C
Power Dissipation (PD) ..... 400 mW
Voltage on Any Pin with Respect to Ground ..... − 0.5 V to V_{DD} + 0.5 V

Absolute maximum ratings are the limiting conditions that can be applied under all variations of circuit and environmental conditions without the occurrence of permanent damage. External leads can be bonded or soldered safely at temperatures up to 300 °C.

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. AT&T employs a human-body model (HBM) and a charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used to define the model. No industry-wide standard has been adopted for the CDM. However, a standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and therefore can be used for comparison purposes. The HBM ESD threshold presented here was obtained by using these circuit parameters.

Human-Body Model ESD Threshold	
Device	**Voltage**
T7210A-PC	> ± 500 V, < ± 2500 V
T7210A-EC	> ± 500 V, < ± 2500 V

Decoder Timing Characteristics

Measurements are from 50% points, unless otherwise noted.

Symbol	Parameter	Min	Max	Unit	Figure
tRCHCRL	$\overline{RXC}$ High to $\overline{CRS}$ Asserted	3	19	ns	5
tCRLRCL	$\overline{CRS}$ Asserted to $\overline{RXC}$ Low	30	50	ns	5
tRCHCRH	$\overline{RXC}$ High to $\overline{CRS}$ De-asserted	3	19	ns	6
tCRHRCL	$\overline{CRS}$ De-asserted to $\overline{RXC}$ Low	30	50	ns	6
tCRHRCH	$\overline{CRS}$ De-asserted to $\overline{RXC}$ High	80	110	ns	6
tRCHRCL	$\overline{RXC}$ High Pulse Width as Captured Data Clock	40	60	ns	7
tRCLRCH	$\overline{RXC}$ Low Pulse Width as Captured Data Clock	40	60	ns	7
tRCHRCH	$\overline{RXC}$ Period as Captured Data Clock	94	106	ns	7
tRCHRDX	$\overline{RXC}$ High to RXD Transition	3	20	ns	8
tRCLRDX	$\overline{RXC}$ Low to RXD Transition	50	65	ns	8
tRDXRCL	RXD Transition to $\overline{RXC}$ Low	30	50	ns	8
tMRXRCL	MRXD Midbit Transition to $\overline{RXC}$ Low	310	360	ns	9
tENHCRL	ENERGY High to $\overline{CRS}$ Low	600	1000	ns	10
tMRHCRH	Beginning of IDL to $\overline{CRS}$ De-asserted (last bit = 0) Beginning of IDL to $\overline{CRS}$ De-asserted (last bit = 1)	360 410	410 460	ns ns	11

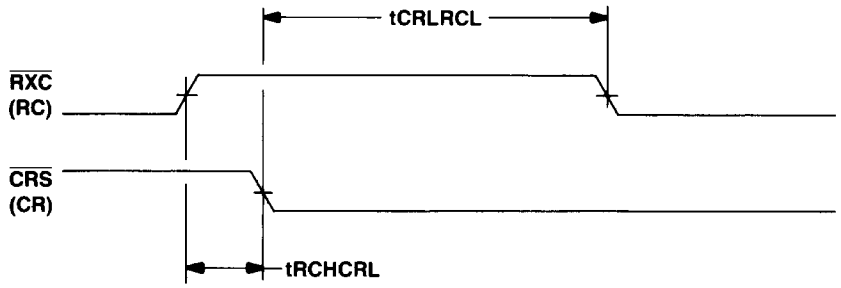


Figure 5. Negative-Transition $\overline{\text{CRS}}$ Timing Relative to $\overline{\text{RXC}}$

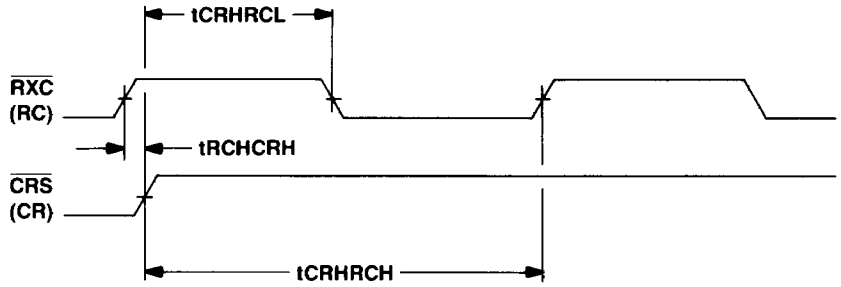


Figure 6. Positive-Transition $\overline{\text{CRS}}$ Timing Relative to $\overline{\text{RXC}}$

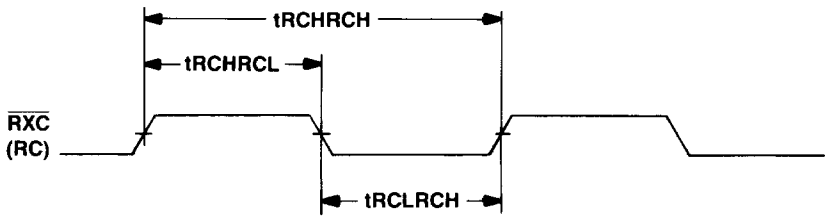


Figure 7. $\overline{\text{RXC}}$ Timing Measurements

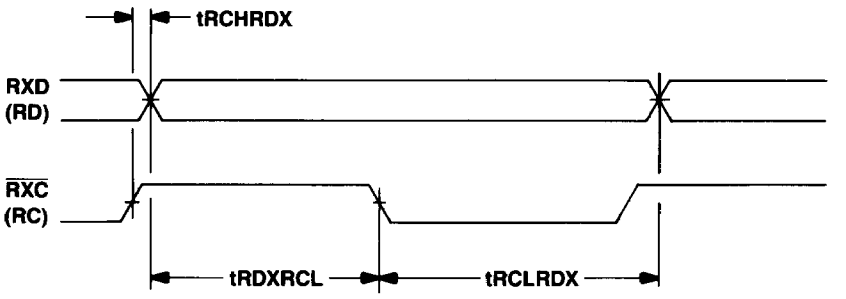


Figure 8. RXD Timing Relative to RXC

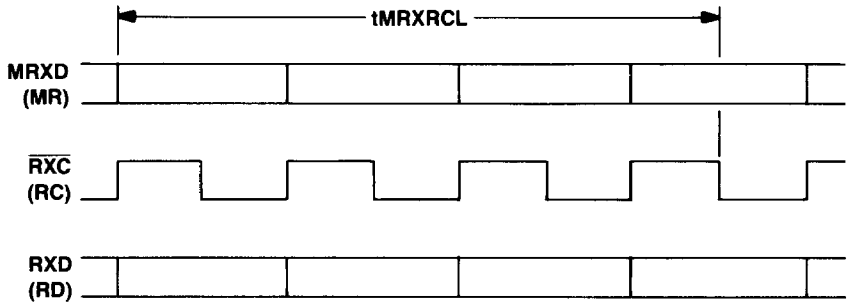


Figure 9. Latency-Definition Timing Measurements

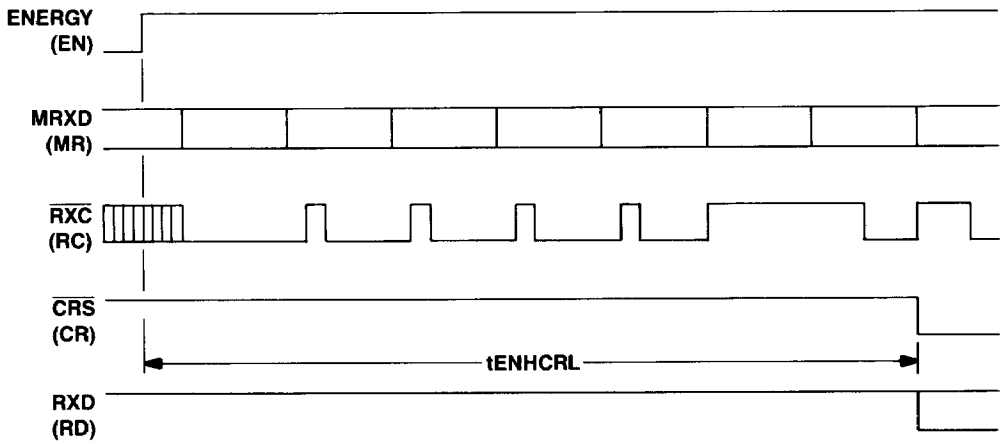


Figure 10. Start-of-Packet Timing Measurements

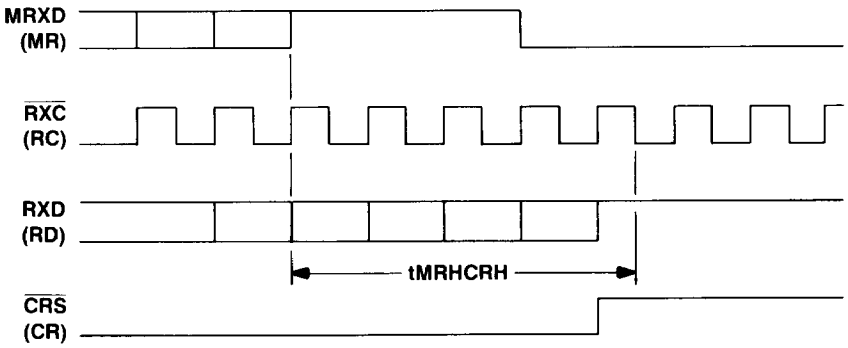


Figure 11. End-of-Normal-Packet Timing Measurements

Transmitter Timing Characteristics

Measurements are from 50% points, unless otherwise noted. The input duty-cycle requirement for XTAL is 50% ± 10%.

Table 2. Station Timing Characteristics

Symbol	Parameter	Min	Max	Unit	Figure
tTCHMDV	Data Clocked to TXD to Data at Output MTXD (latency)	100	190	ns	12
tTCLTNL	$\overline{RTS}$ Assertion Clocked to $\overline{TEN}$ Assertion*	340	440	ns	12
tTDVTCX, tRSVTCX	TXD and $\overline{RTS}$ Setup Time With Respect to TXC Transition	10	—	ns	13
tRSHTCX, tTDHTCX	TXD and $\overline{RTS}$ Hold Time With Respect to TXC Transition	0	—	ns	13
tTCLTNH	$\overline{RTS}$ De-assertion Clocked to $\overline{TEN}$ De-assertion†	340	440	ns	14

* Station start-of-packet delay — 2.5 bit-times of data are masked after $\overline{RTS}$ is asserted by delaying $\overline{TEN}$ assertion.
† Station/Hub end-of-packet delay — 2.5 bit-times of data are transmitted beyond $\overline{RTS}$ de-assertion by allowing $\overline{TEN}$ to remain asserted.

Table 3. Hub Timing Characteristics

Symbol	Parameter	Min	Max	Unit	Figure
tXTHMDV	Data Clocked to TXD to Data at Output MTXD (latency)	100	210	ns	15
tXTHTNL	$\overline{RTS}$ Assertion Clocked to $\overline{TEN}$ Assertion*	140	260	ns	15
tTDVXTH, tRSVXTH	TXD and $\overline{RTS}$ Setup Time with Respect to XTAL High	20	—	ns	16
tRSHXTH, tTDHXTH	TXD and $\overline{RTS}$ Hold Time with Respect to XTAL High	0	−5	ns	16
tXTHTNH	$\overline{RTS}$ De-assertion Clocked to $\overline{TEN}$ De-assertion†	340	460	ns	17

* Hub start-of-packet delay — .5 bit-times of data are masked after $\overline{RTS}$ is asserted by delaying $\overline{TEN}$ assertion.
† Station/Hub end-of-packet delay — 2.5 bit-times of data are transmitted beyond $\overline{RTS}$ de-assertion by allowing $\overline{TEN}$ to remain asserted.

Table 4. Output Timing Characteristics

Symbol	Parameter	Min	Max	Unit	Figure
tSTROBE	Maximum Deviation from the Ideal 50 ns Strobe Point for $\overline{TEN}$, MTXD, $\overline{MTXD}$, and $\overline{PDC}$	—	1.5	ns	18
tMXHMXL − tMXLMXH	MTXD/$\overline{MTXD}$ Worst-case Duty-cycle Mismatch, 10 pf Load	−3	3	ns	19
tTCHTCL	$\overline{TXC}$ High Pulse Width	40	60	ns	20
tTCLTCH	$\overline{TXC}$ Low Pulse Width	40	60	ns	20

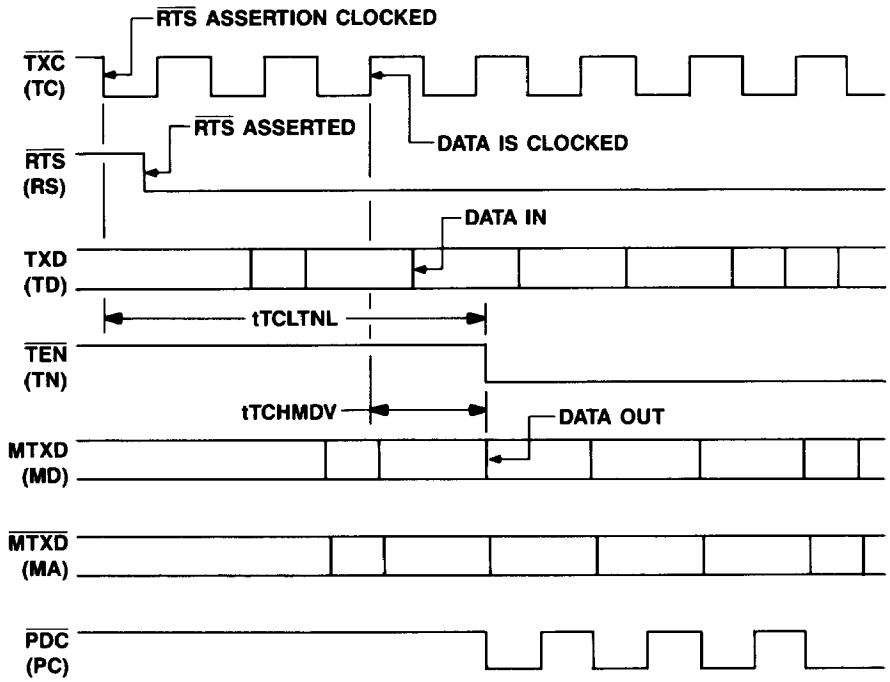


Figure 12. Station — Start-of-Packet

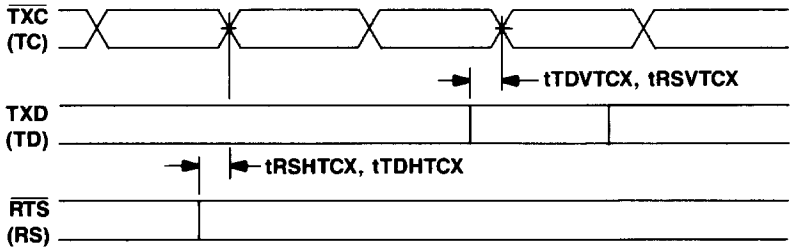


Figure 13. Station — TXD and RTS Setup Time

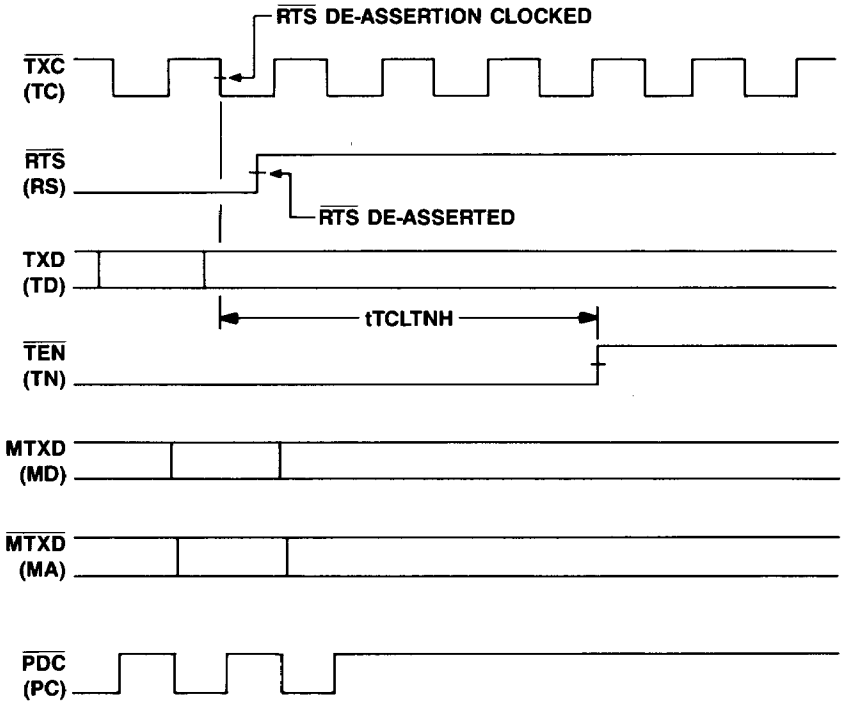


Figure 14. Station — End-of-Packet

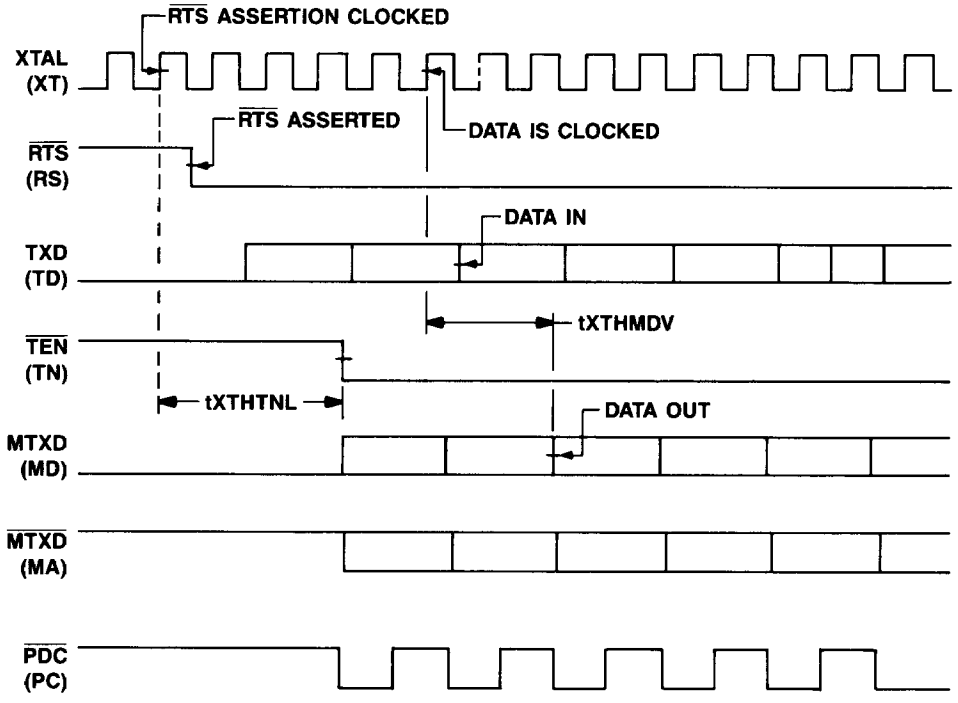


Figure 15. Hub — Start-of-Packet

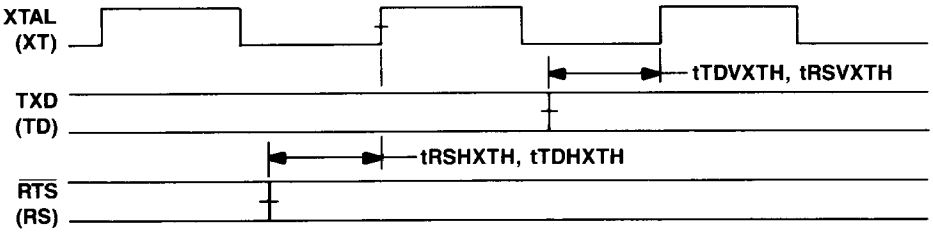


Figure 16. Hub — TXD and $\overline{\text{RTS}}$ Setup Time

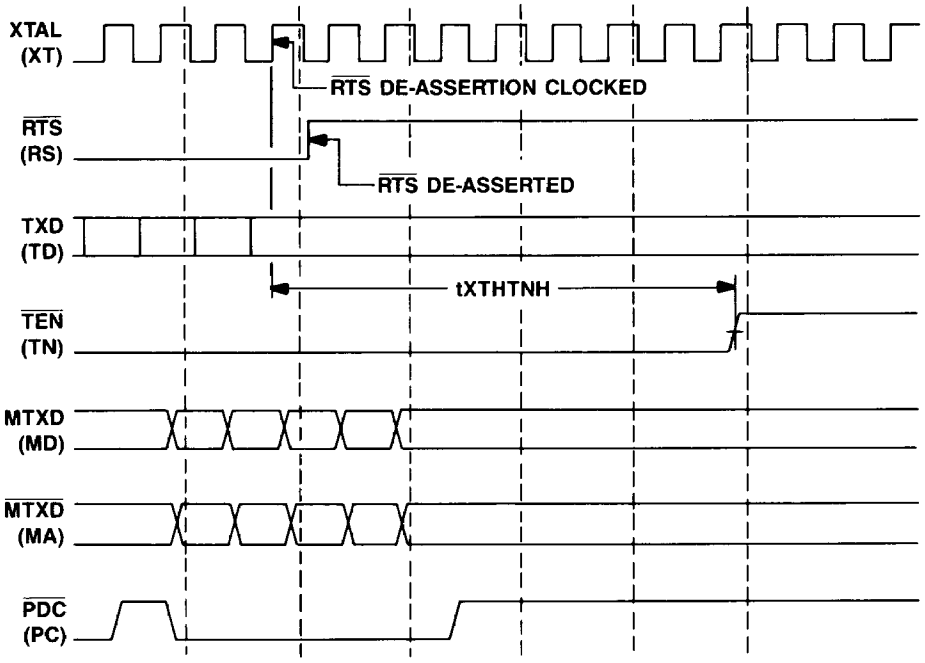


Figure 17. Hub — End-of-Packet

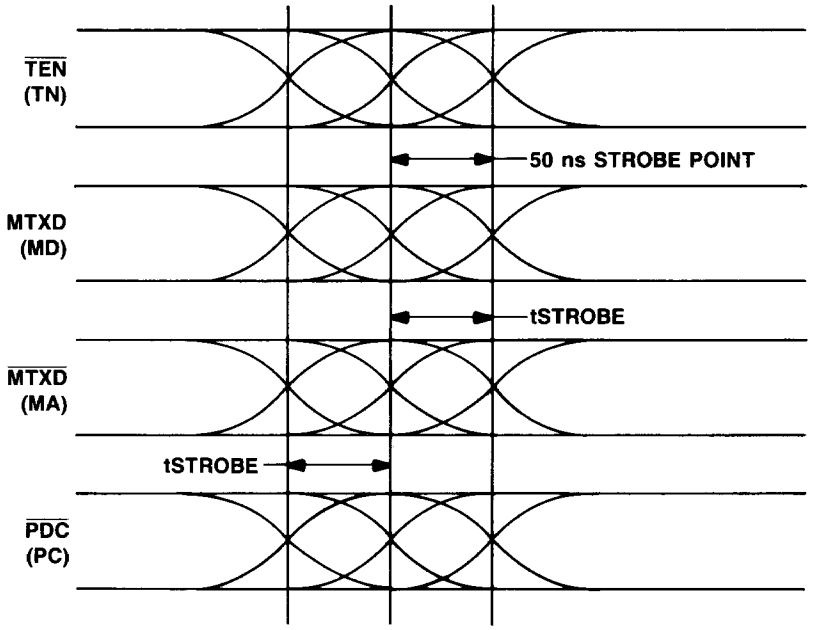


Figure 18. Maximum Deviation From Ideal 50 ns Strobe Point

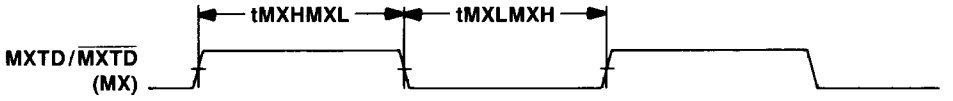


Figure 19. Worst-Case Duty-Cycle Mismatch

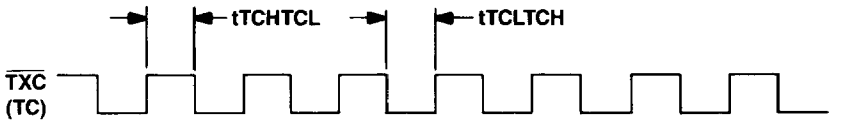
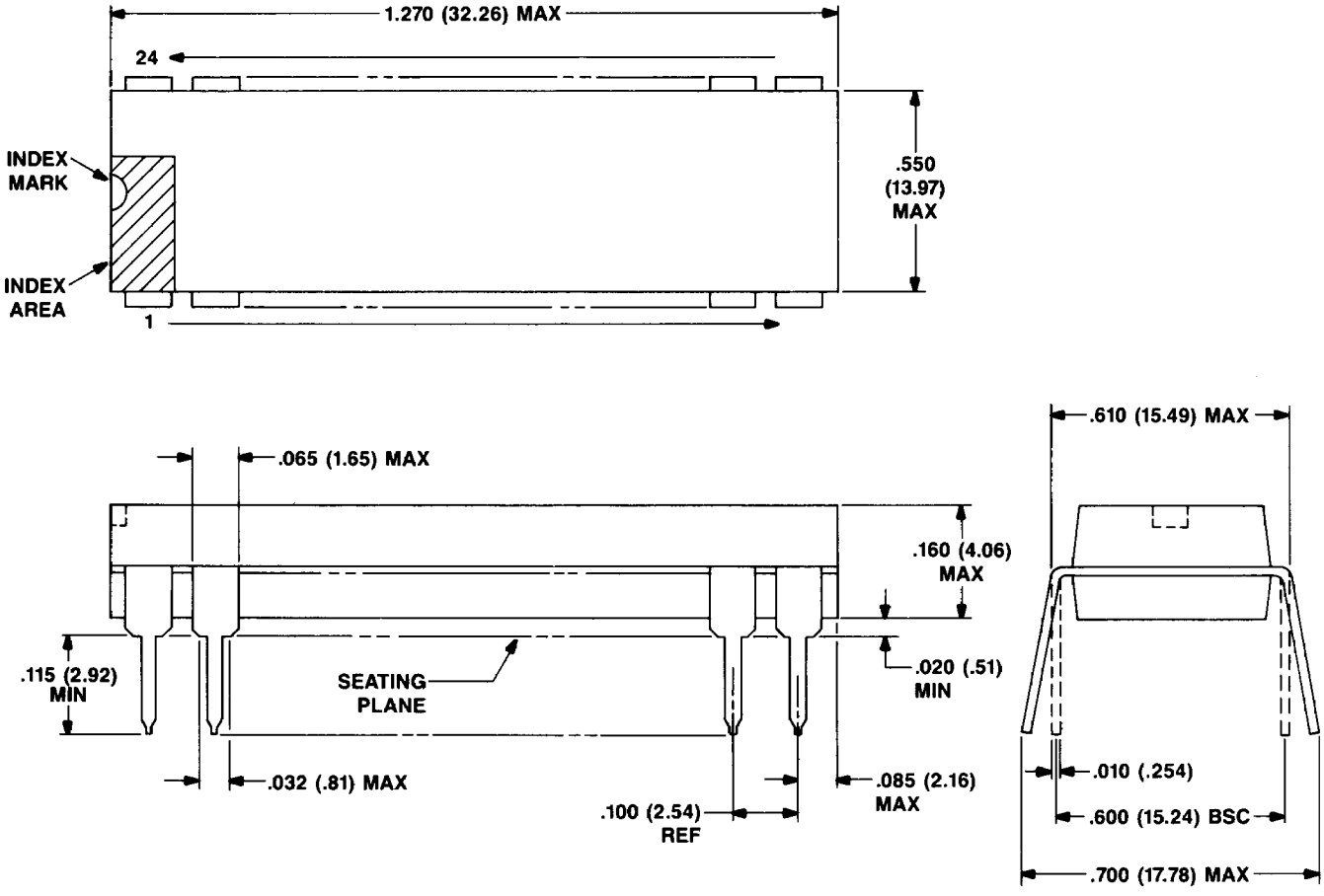


Figure 20. TXC Pulse Width

Outline Diagram

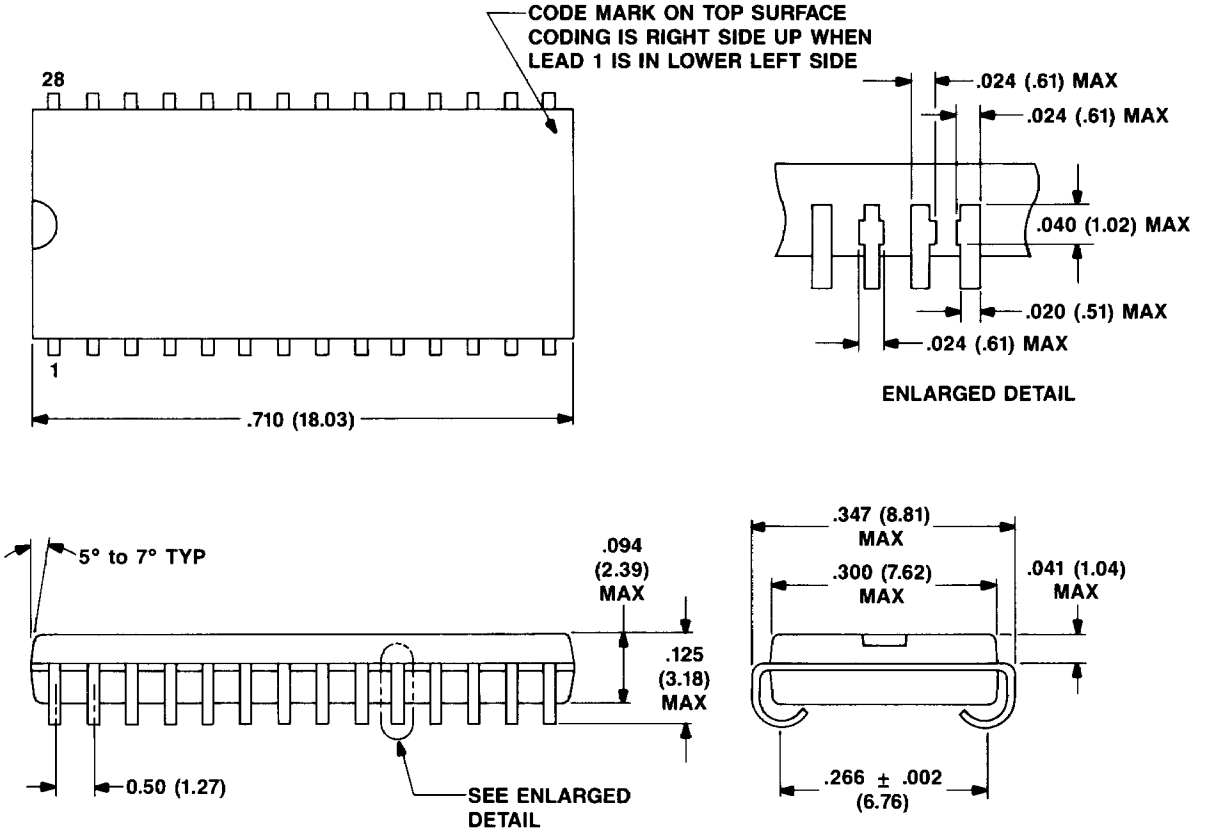
24-Pin, Plastic DIP

Dimensions are in inches and (millimeters).



28-Pin, Plastic SOJ

Dimensions are in inches and (millimeters).



Ordering Information

Device Code	Package	Temperature
T7210A - PC	24-Pin, Plastic DIP	0 °C to 70 °C
T7210A - EC	28-Pin, Plastic SOJ	0 °C to 70 °C

For additional information, contact your AT&T Account Manager, or call:

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