TOSHIBA MOS MEMORY PRODUCTS

TC514268AP/AJ/AZ-70, TC514268AP/AJ/AZ-80
TC514268AP/AJ/AZ-10

DESCRIPTION

The TC514268AP/AJ/AZ is the new generation dynamic RAM organized 262,144 words by 4 bits. The TC514268AP/AJ/AZ utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514268AP/AJ/AZ to be packaged in a standard 20 pin plastic DIP and 26/20 pin plastic SOJ and 20/19 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

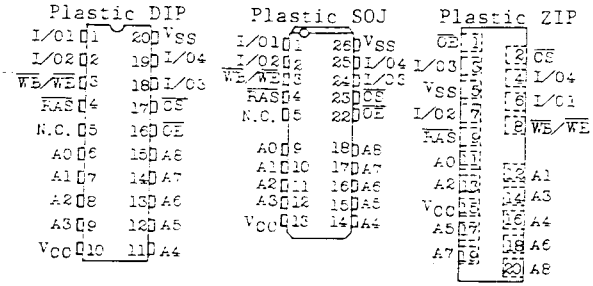
FEATURES

- 262,144 word by 4 bit organization
- Fast access time and cycle time

		TC514268AP/AJ/AZ -70/-80/-10		
t_{RAC}	$\overline{RAS}$ Access Time	70ns	80ns	100ns
t_{AA}	Column Address Access Time	35ns	40ns	50ns
t_{CAC}	$\overline{CS}$ Access Time	25ns	25ns	30ns
t_{RC}	Cycle Time	130ns	150ns	180ns
t_{SC}	Static Column Mode Cycle Time	40ns	45ns	55ns

- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low power
  440mW MAX. Operating(TC514268AP/AJ/AZ-70)
  385mW MAX. Operating(TC514268AP/AJ/AZ-80)
  330mW MAX. Operating(TC514268AP/AJ/AZ-10)
  5.5mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh Write Per Bit, and Static Column Mode capability
- All inputs and outputs TTL compatible
- 512 refresh cycles/8ms
- Package Plastic DIP: TC514268AP
  Plastic SOJ: TC514268AJ
  Plastic ZIP: TC514268AZ

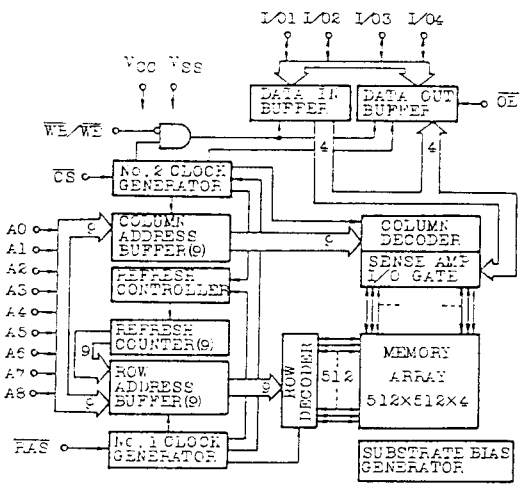
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0 ∿ A8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select
$\overline{WE}/\overline{WE}$	Write Per Bit/Read/Write Input
$\overline{OE}$	Output Enable
I/O1 ∿ I/O4	Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	-1 ~ 7	V	1
Output Voltage	V_{OUT}	-1 ~ 7	V	1
Power Supply Voltage	V_{CC}	-1 ~ 7	V	1
Operating Temperature	T_{OPR}	0 ~ 70	°C	1
Storage Temperature	T_{STG}	-55 ~ 150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta=0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 ~ 70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	UNIT
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CS}$, Address Cycleing: t_{RC}=t_{RC} MIN.)	TC514268AP/AJ/AZ-70	-	80	mA	3, 4
		TC514268AP/AJ/AZ-80	-	70		
		TC514268AP/AJ/AZ-10	-	60		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CS}$=V_{IH})		-	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	TC514268AP/AJ/AZ-70	-	80	mA	3
		TC514268AP/AJ/AZ-80	-	70		
		TC514268AP/AJ/AZ-10	-	60		
I_{CC4}	STATIC COLUMN MODE CURRENT Average Power Supply Current, Static Column Mode ($\overline{RAS}$=$\overline{CS}$=V_{IL}, Address Cycling: t_{SC}=t_{SC} MIN.)	TC514268AP/AJ/AZ-70	-	60	mA	3, 4
		TC514268AP/AJ/AZ-80	-	50		
		TC514268AP/AJ/AZ-10	-	40		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CS}$=V_{CC}-0.2V)		-	1	mA	
I_{CC6}	$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CS}$ Cycling: t_{RC}=t_{RC} MIN.)	TC514268AP/AJ/AZ-70	-	80	mA	3
		TC514268AP/AJ/AZ-80	-	70		
		TC514268AP/AJ/AZ-10	-	60		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≦ V_{IN} ≦ 6.5V, All Other Pins Not Under Test=0V)		-10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disable, 0V ≦ V_{OUT} ≦ 5.5V)		-10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0 ~ 70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	TC514268AP/AJ/AZ-70		TC514268AP/AJ/AZ-80		TC514268AP/AJ/AZ-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	130	-	150	-	180	-	ns	
t_{RMW}	Read-Modify-Write Cycle Time	185	-	205	-	245	-	ns	
t_{SC}	Static Column Mode Cycle Time	40	-	45	-	55	-	ns	
t_{SRMW}	Static Column Mode Read-Modify-Write Cycle Time	100	-	110	-	135	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	70	-	80	-	100	ns	8, 13
t_{CAC}	Access Time from $\overline{CS}$	-	25	-	25	-	30	ns	8, 13
t_{AA}	Access Time from Column Address	-	35	-	40	-	50	ns	8, 14
t_{ALW}	Access Time from Last Write	-	65	-	75	-	95	ns	8, 15
t_{CLZ}	$\overline{CS}$ to Output in Low-Z	0	-	0	-	0	-	ns	8
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	9
t_{AOH}	Output Data Hold Time from Column Address	5	-	5	-	5	-	ns	
t_{OW}	Output Data Enable Time from $\overline{WE}$	-	25	-	25	-	30	ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	50	-	60	-	70	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10,000	80	10,000	100	10,000	ns	
t_{RASC}	$\overline{RAS}$ Pulse Width (Static Column Mode)	70	100,000	80	100,000	100	100,000	ns	
t_{RSH}	$\overline{CS}$ to $\overline{RAS}$ Hold Time	25	-	25	-	30	-	ns	
t_{CSH}	$\overline{RAS}$ to $\overline{CS}$ Hold Time	70	-	80	-	100	-	ns	
t_{CS}	$\overline{CS}$ Pulse Width	25	10,000	25	10,000	30	10,000	ns	
t_{CSC}	$\overline{CS}$ Pulse Width(Static Column Mode)	25	100,000	25	100,000	30	100,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CS}$ Delay Time	20	45	20	55	25	70	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	20	50	ns	14
t_{CRP}	$\overline{CS}$ to $\overline{RAS}$ Precharge Time	5	-	5	-	5	-	ns	
t_{CPN}	$\overline{CS}$ Precharge Time	10	-	10	-	15	-	ns	
t_{CP}	$\overline{CS}$ Precharge Time (Static Column Mode)	10	-	10	-	10	-	ns	
t_{ASR}	Row Address Set-up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	15	-	ns	
t_{ASC}	Column Address Set-up Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	15	-	15	-	20	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	TC514268AP/AJ/AZ-70		TC514268AP/AJ/AZ-80		TC514268AP/AJ/AZ-10		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{AWR}	Write Address Hold Time Referenced to $\overline{RAS}$	55	-	60	-	75	-	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	80	-	90	-	115	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	-	40	-	50	-	ns	
t_{AH}	Column Address Hold Time Referenced to $\overline{RAS}$ Rise	5	-	5	-	10	-	ns	16
t_{LWAD}	Last Write to Column Address Delay Time	20	30	20	35	25	45	ns	17
t_{AHLW}	Last Write to Column Address Hold Time	65	-	75	-	95	-	ns	
t_{RCS}	Read Command Set-up Time Referenced to $\overline{CS}$	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time Referenced to $\overline{CS}$	0	-	0	-	0	-	ns	10
t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	10
t_{WCH}	Write Command Hold Time (Output Data Disable)	15	-	15	-	20	-	ns	12
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	55	-	60	-	75	-	ns	
t_{WP}	$\overline{WE}$ Pulse Width	15	-	15	-	20	-	ns	
t_{WI}	$\overline{WE}$ Inactive Time	10	-	10	-	10	-	ns	
t_{RWL}	$\overline{WE}$ Command to $\overline{RAS}$ Lead Time	20	-	20	-	25	-	ns	
t_{CWL}	$\overline{WE}$ Command to $\overline{CS}$ Lead Time	20	-	20	-	25	-	ns	
t_{DS}	Data-In Set-Up Time	0	-	0	-	0	-	ns	11
t_{DH}	Data-In Hold Time	15	-	15	-	20	-	ns	11
t_{DHR}	Data-In Hold Time Referenced to $\overline{RAS}$	55	-	60	-	75	-	ns	
t_{REF}	Refresh Period	-	8	-	8	-	8	ms	
t_{WCS}	$\overline{WE}$ Command Set-Up Time (Output Data Disable)	0	-	0	-	0	-	ns	12
t_{CWD}	$\overline{CS}$ to $\overline{WE}$ Delay Time (READ-MODIFY-WRITE CYCLE)	55	-	55	-	65	-	ns	12
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time (READ-MODIFY-WRITE CYCLE)	100	-	110	-	135	-	ns	12
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	65	-	70	-	85	-	ns	12

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

SYMBOL	PARAMETER	TC514268AP/AJ/AZ-70		TC514268AP/AJ/AZ-80		TC514268AP/AJ/AZ-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{CSR}	$\overline{CS}$ Set-Up Time ($\overline{CS}$ before $\overline{RAS}$)	10	-	10	-	10	-	ns	
t_{CHR}	$\overline{CS}$ Hold Time ($\overline{CS}$ before $\overline{RAS}$)	30	-	30	-	30	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CS}$ Precharge Time	0	-	0	-	0	-	ns	
t_{CPT}	$\overline{CS}$ Precharge Time ($\overline{CS}$ before $\overline{RAS}$ Counter Test Cycle)	40	-	40	-	50	-	ns	
t_{ROH}	$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	10	-	10	-	20	-	ns	
t_{OEA}	$\overline{OE}$ Access Time	-	25	-	25	-	30	ns	
t_{OED}	$\overline{OE}$ to Data Delay	20	-	20	-	25	-	ns	
t_{OEZ}	Output Buffer turn off Delay Time from $\overline{OE}$	0	20	0	20	0	25	ns	9
t_{OEH}	$\overline{OE}$ Command Hold Time	20	-	20	-	25	-	ns	
t_{WBS}	Write Per Bit Set-Up Time	0	-	0	-	0	-	ns	
t_{WBH}	Write Per Bit Hold Time	10	-	10	-	10	-	ns	
t_{WDS}	Write Per Bit Selection Set-Up Time	0	-	0	-	0	-	ns	
t_{WDH}	Write Per Bit Selection Hold Time	10	-	10	-	10	-	ns	

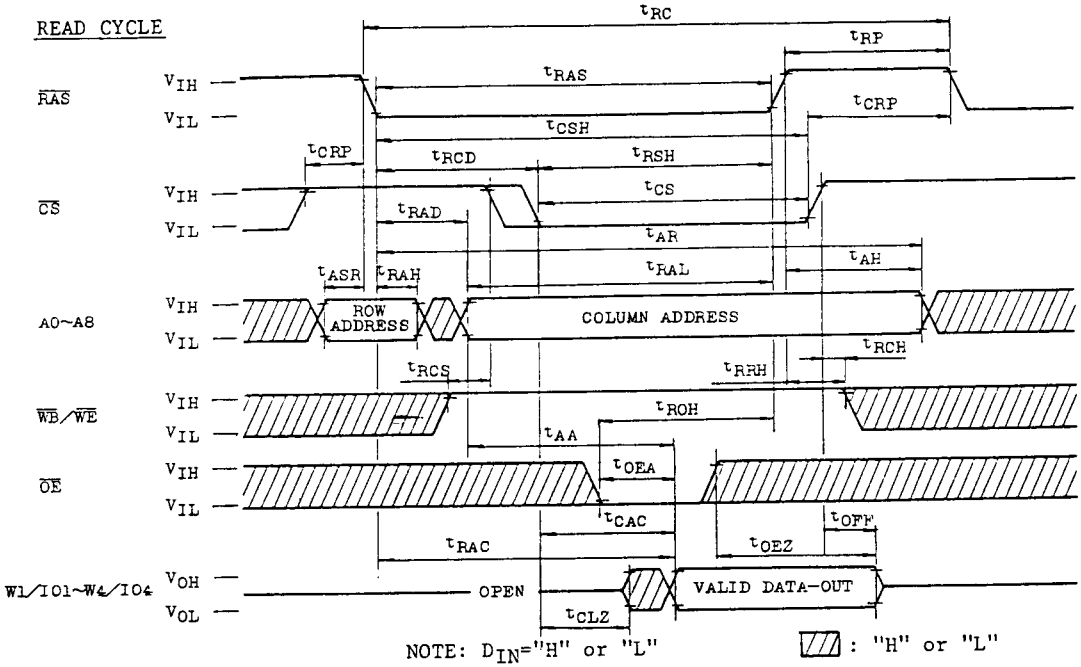
CAPACITANCE (V_{CC}=5V±10%, f=1MHz, Ta=0∿70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0∿A8)	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{WB}/\overline{WE}$, $\overline{OE}$)	-	7	
C_O	Input/Output Capacitance (I/O1∿I/O4)	-	7	

NOTES:

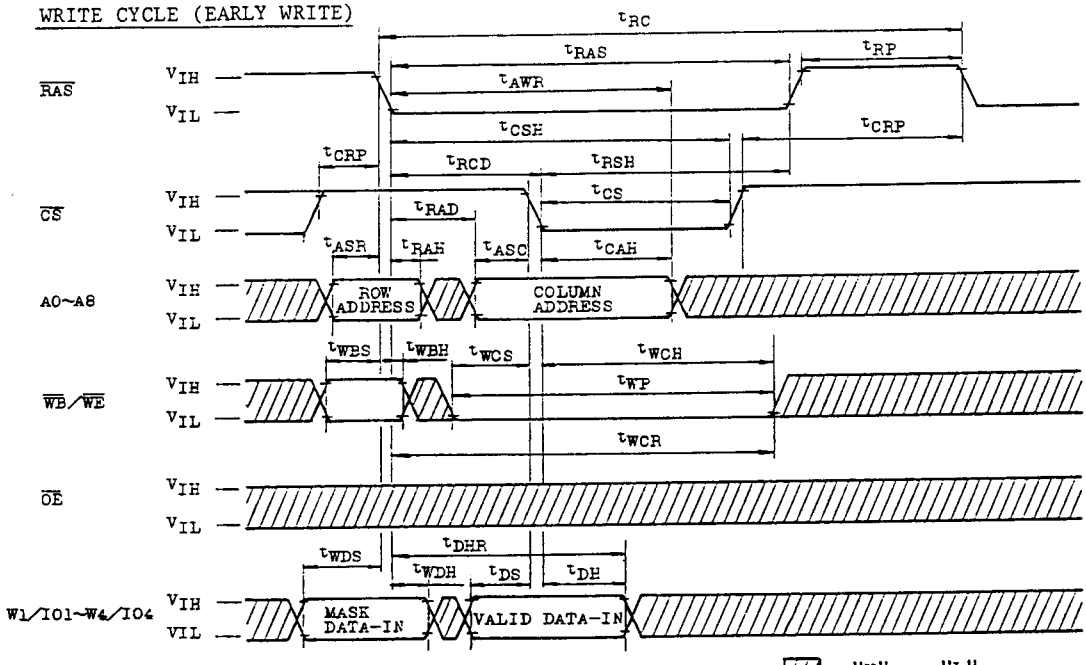
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CS}$ Before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume t_T=5ns.
7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals.
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9. t_{OFF}(max.) and t_{OEZ}(max.) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CS}$ leading edge in early write cycles and to $\overline{WE}$/$\overline{WE}$ leading edge in Read-Modify-Write cycles.
12. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.) and $t_{AWD} \geq t_{AWD}$(min.), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
14. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.
15. Operation within the t_{LWAD}(max.) limit insures that t_{ALW}(max.) can be met. t_{LWAD}(max.) is specified as a reference point only: If t_{LWAD} is greater than the specified t_{LWAD}(max.) limit, then access time is controlled exclusively by t_{AA}.
16. t_{AH} is the condition to latch column address when $\overline{RAS}$ has rised up.

READ CYCLE



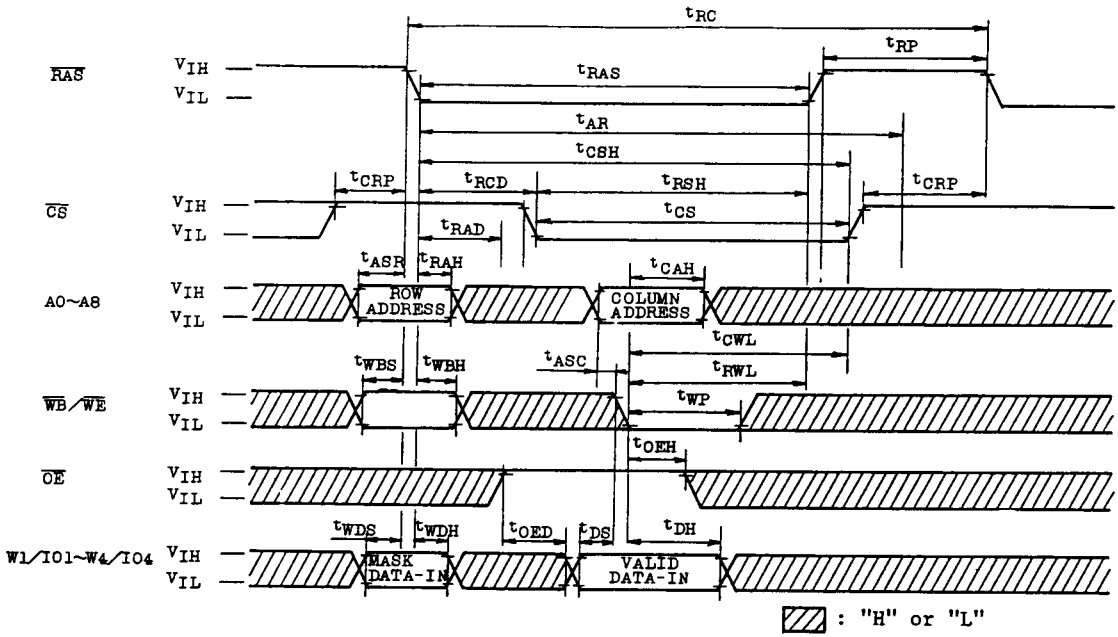
NOTE: D_{IN}="H" or "L" ▨: "H" or "L"

WRITE CYCLE (EARLY WRITE)

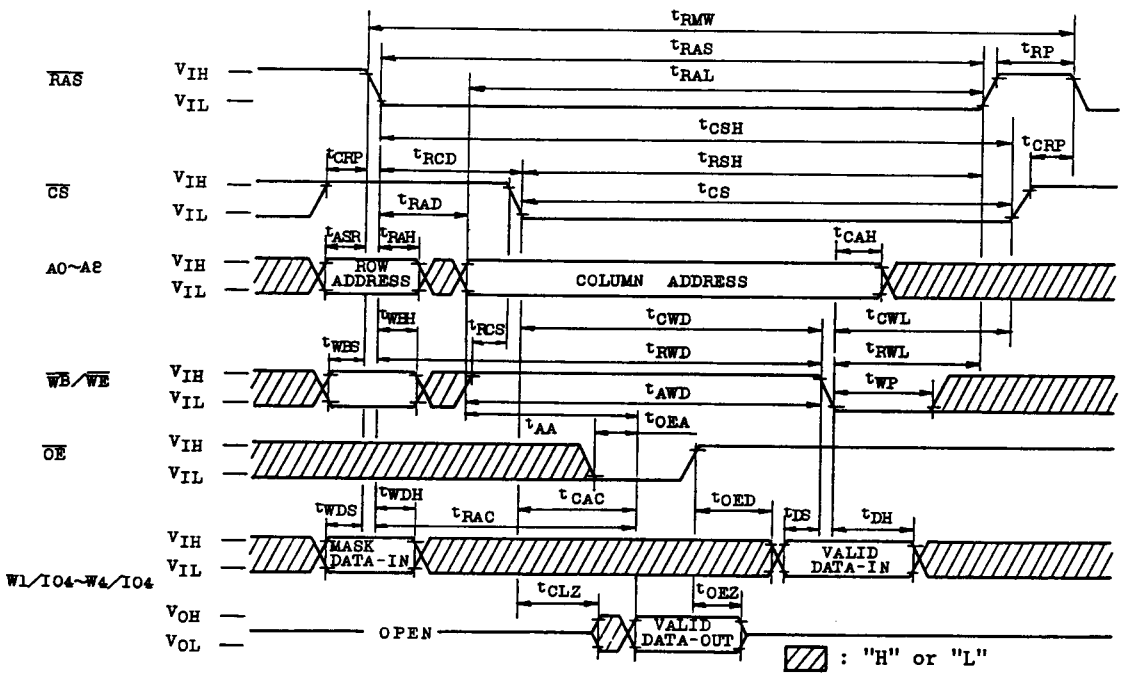


NOTE: D_{OUT}=OPEN ▨: "H" or "L"

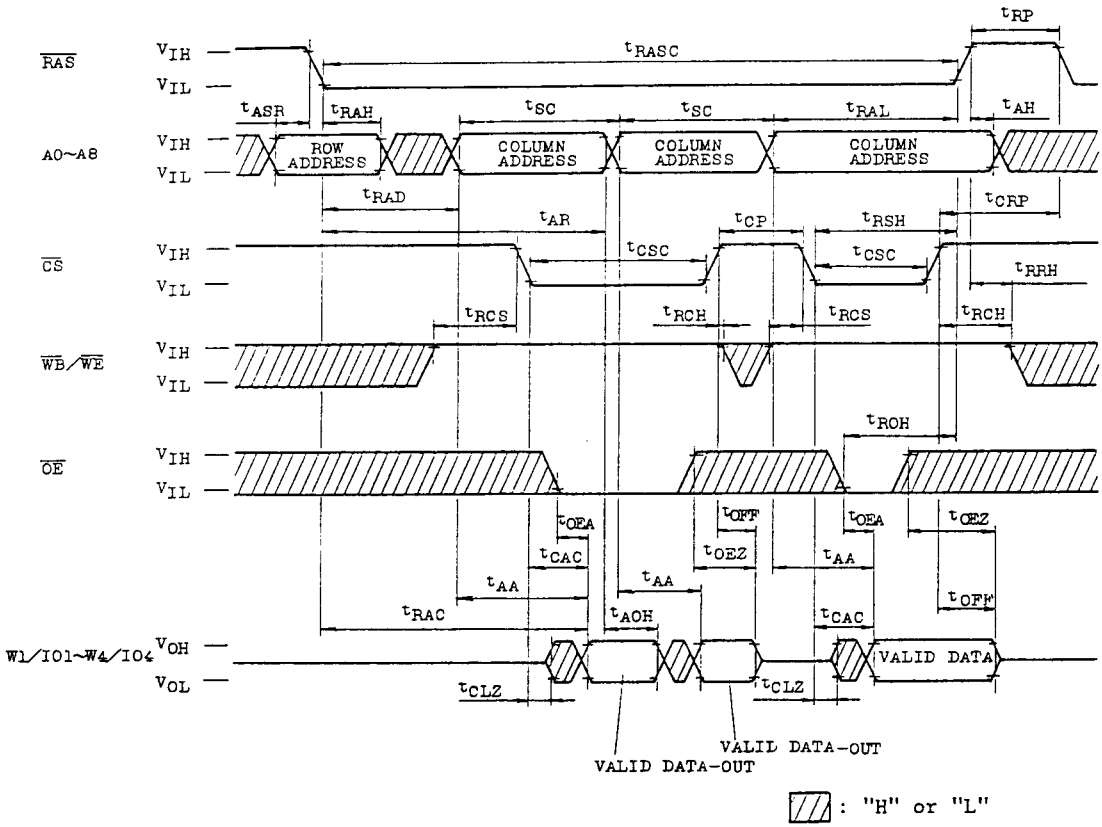
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



READ-MODIFY-WRITE CYCLE

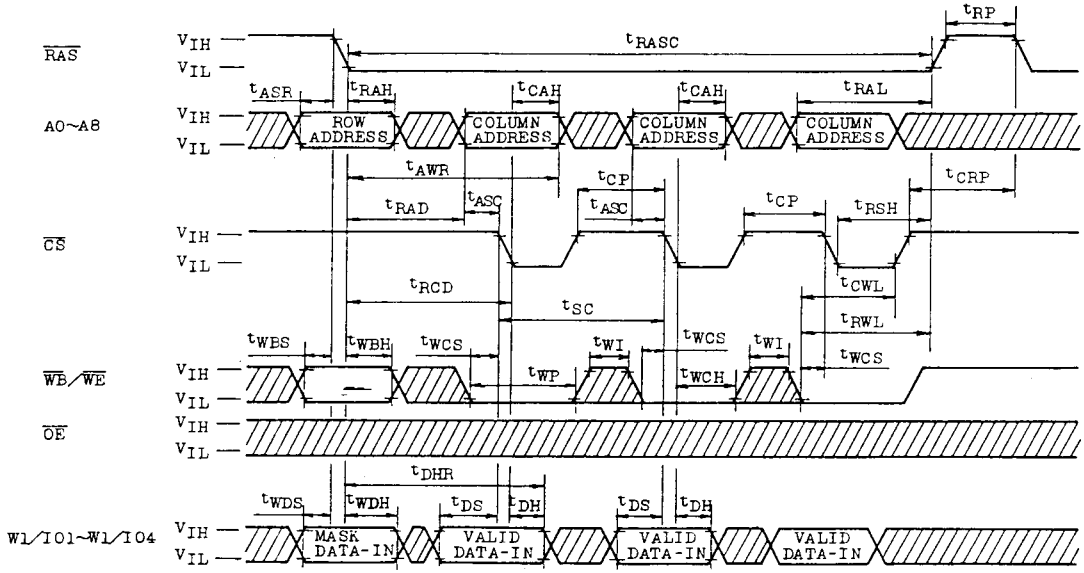


STATIC COLUMN MODE READ CYCLE

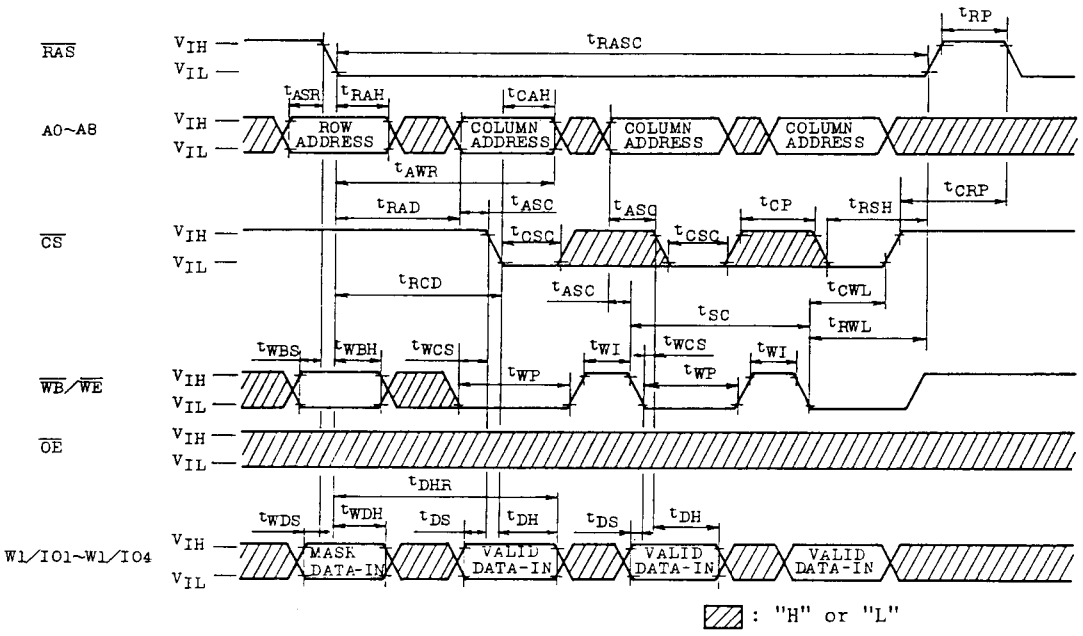


NOTE: D_{IN}="H" or "L"

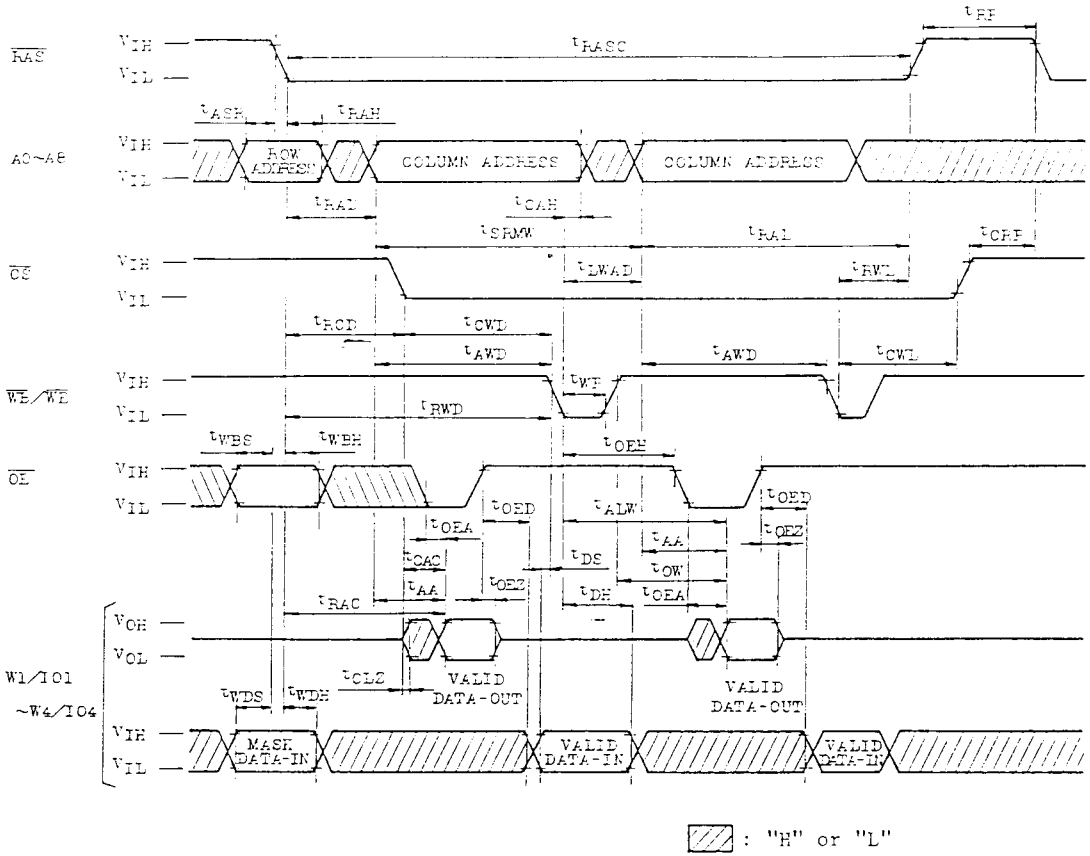
STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)



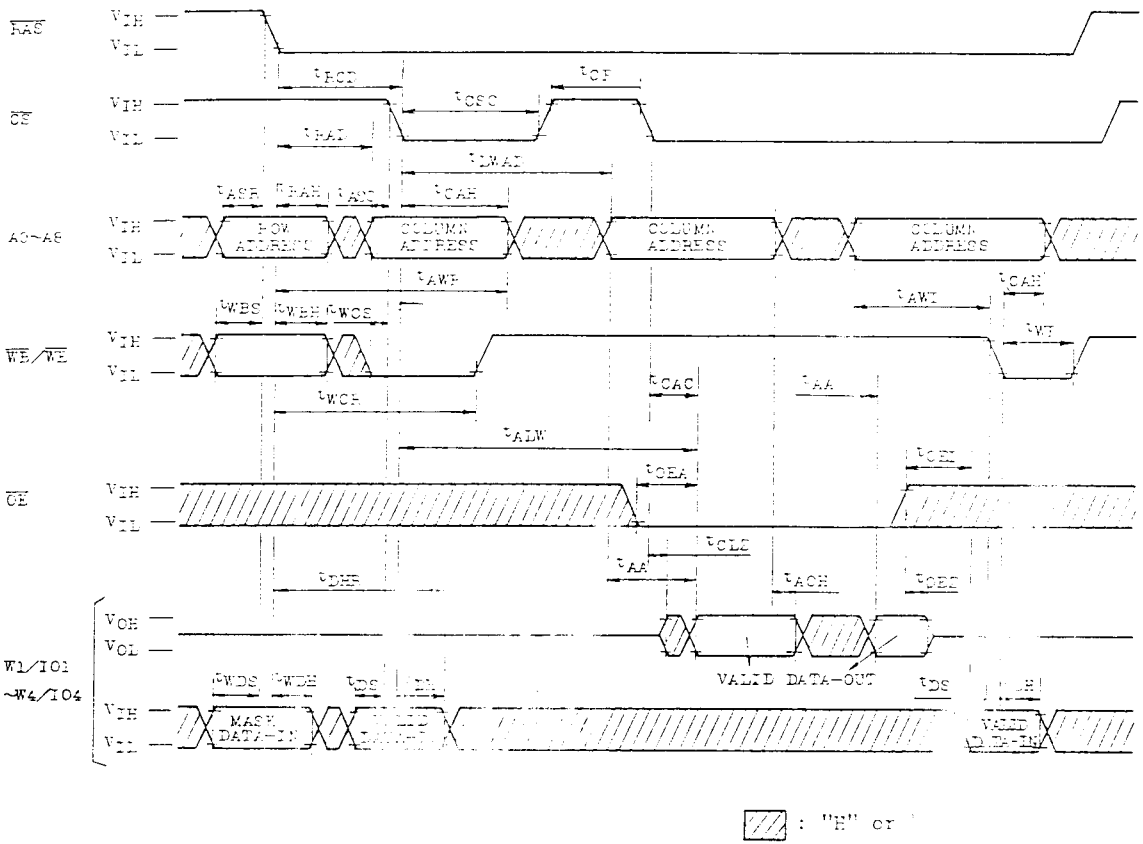
STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)



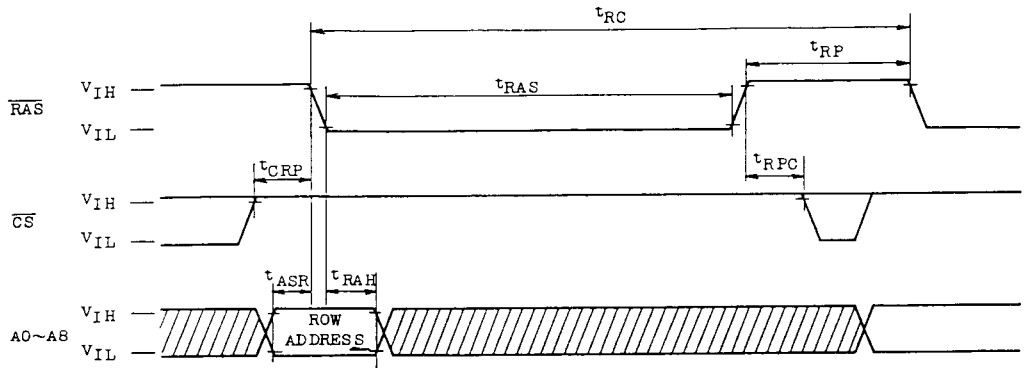
STATIC COLUMN MODE READ-MODIFY-WRITE CYCLE



STATIC COLUMN MODE MIXED CYCLE

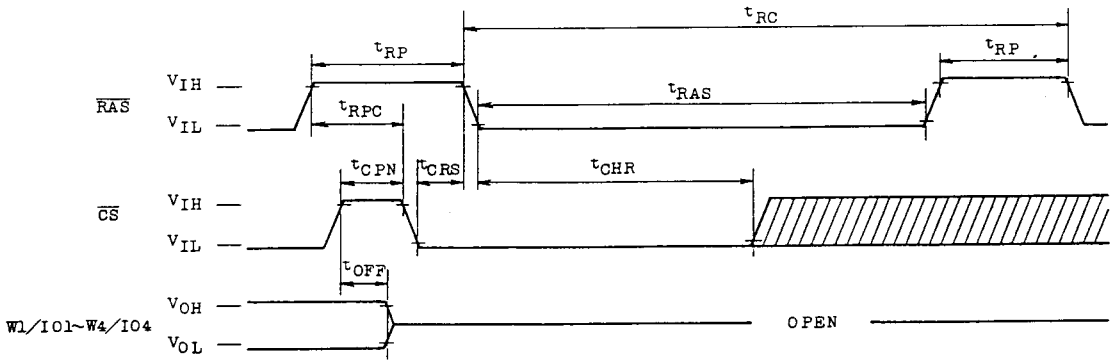


$\overline{RAS}$ ONLY REFRESH CYCLE



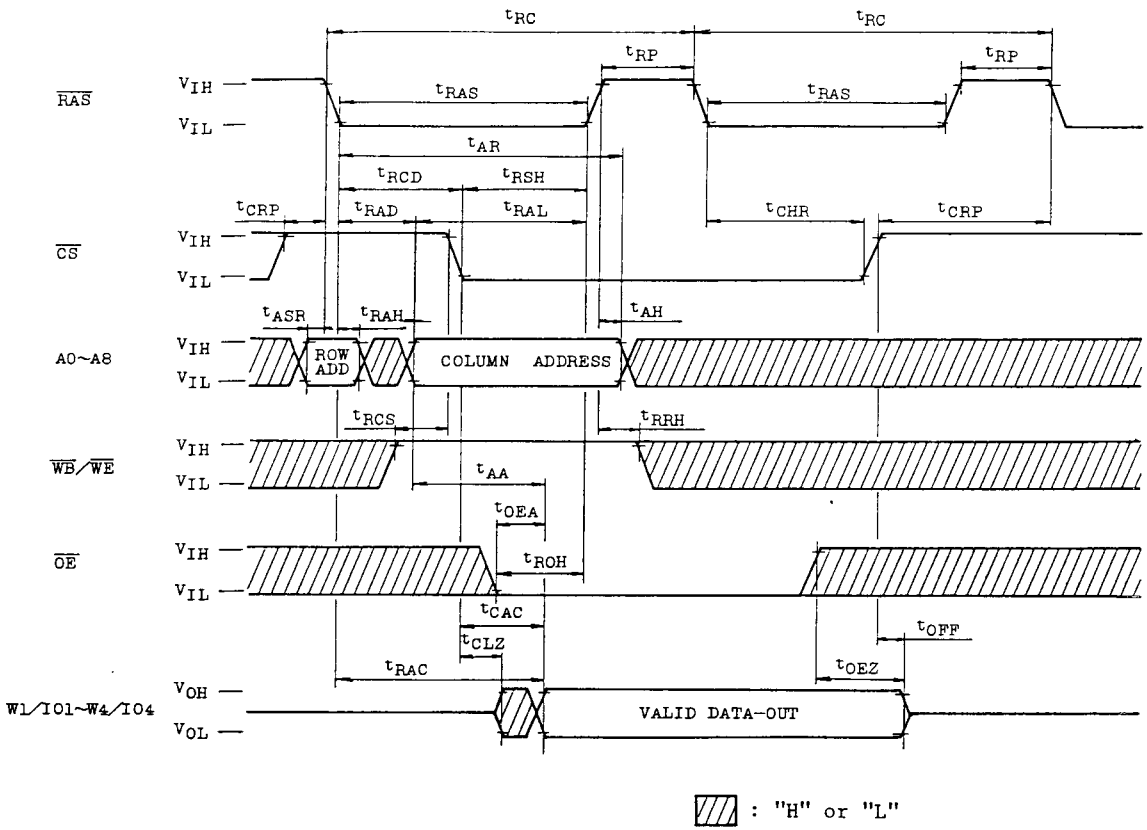
Note: $\overline{WB}/\overline{WE}$, $\overline{OE}$=Don't Care ▨: "H" or "L"

$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

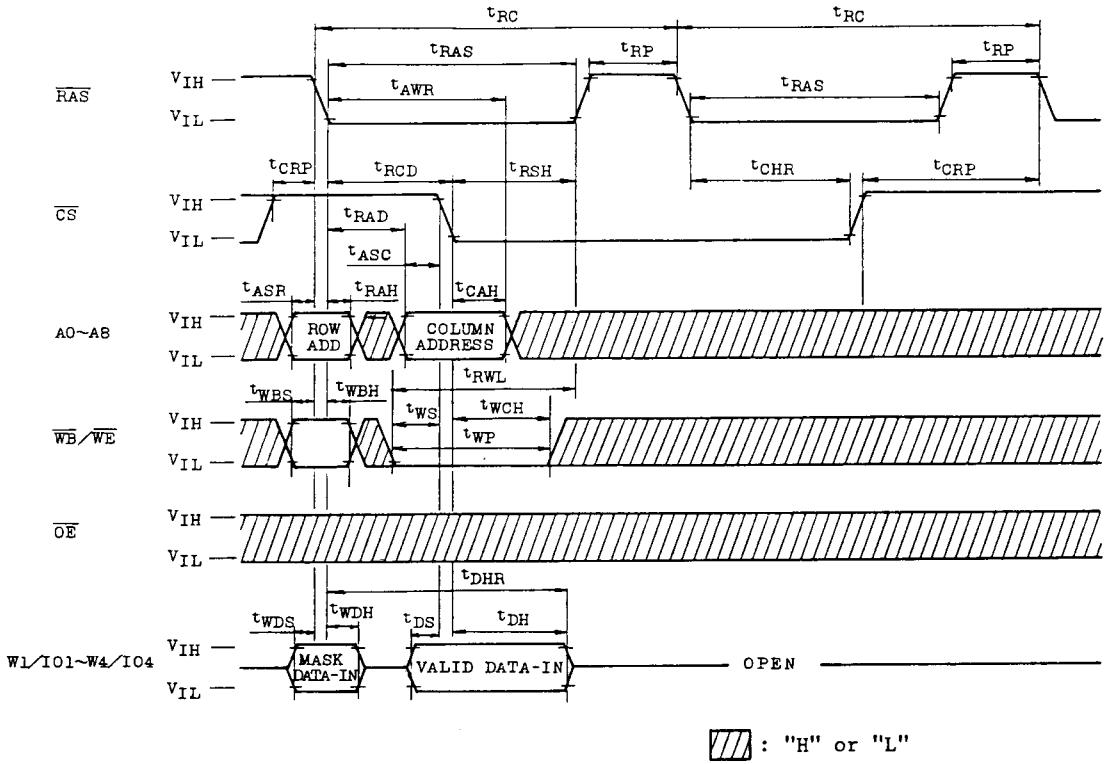


Note: $\overline{WB}/\overline{WE}$, $\overline{OE}$, A0 ∿ A8="H" or "L" ▨: "H" or "L"

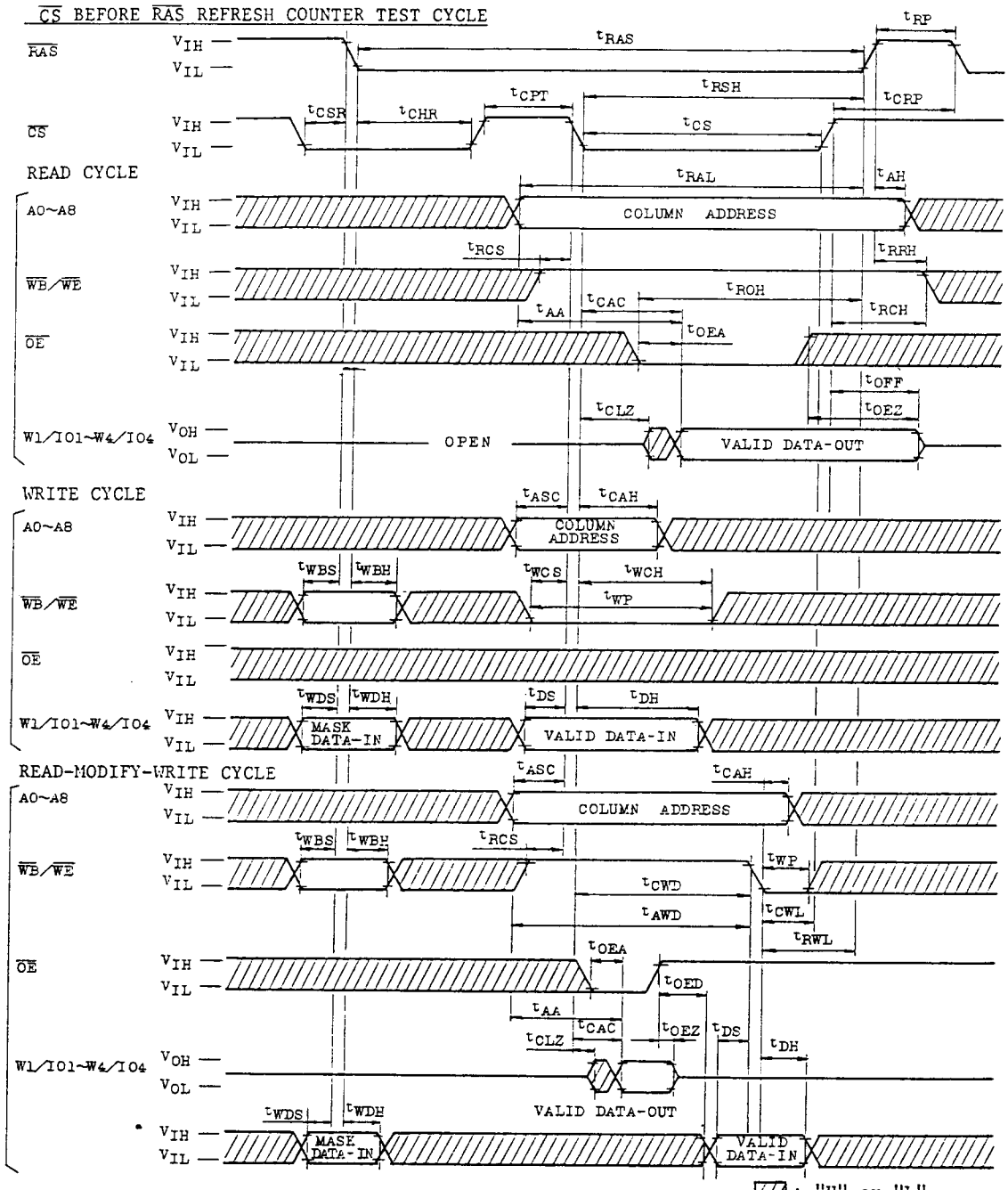
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



NOTE: D_{OUT}=OPEN


CS BEFORE RAS REFRESH COUNTER TEST CYCLE
RAS
CS
READ CYCLE
A0~A8
WB/WE
OE
W1/IO1~W4/IO4
WRITE CYCLE
READ-MODIFY-WRITE CYCLE
VIH
VIL
VOH
VOL
tRAS
tRP
tRSH
tCRP
tCSR
tCHR
tCPT
tCS
tRAL
tAH
COLUMN ADDRESS
tRCS
tRRH
tROH
tAA
tCAC
tRCH
tOEA
tOFF
tOEZ
tCLZ
OPEN
VALID DATA-OUT
tASC
tCAH
COLUMN ADDRESS
tWBS
tWBH
tWCS
tWCH
tWP
tWDS
tWDH
tDS
tDH
MASK DATA-IN
VALID DATA-IN
tCWD
tAWD
tCWL
tRWL
tOED
: "H" or "L"

APPLICATION INFORMATION

ADDRESSING

The 18 address bits required to decode 1 of the 262,144 cell locations within the TC514268AP/AJ/AZ are multiplexed onto the 9 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row address Strobe ($\overline{RAS}$), latches the 9 row address bits into the chip. The second clock, in a read cycle column-address must be held stable until the access time. In a write cycle column-address are latched at the last falling of edge of $\overline{WE}$ or $\overline{CS}$.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. The "gated $\overline{CS}$" feature allows the $\overline{CS}$ clock to be externally activated as soon as the Row Address Hole Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

Data Inputs

Write Cycle. A write cycle is performed by bringing ($\overline{WB}$/)$\overline{WE}$ low during the $\overline{RAS}$/$\overline{CS}$ operation. The falling edge of $\overline{CS}$ or ($\overline{WB}$/)$\overline{WE}$ strobes data on (Wi)IOi into the on-chip data latch. To make use of the write-per-bit capability $\overline{WB}$(/$\overline{WE}$) must be low as $\overline{RAS}$ falls. In this case data bits to which the write operation is applied can be specified by keeping Wi(/IOi) high with set-up and hold times referenced to the $\overline{RAS}$ negative transition.
For those data bits of Wi(/IOi) that are kept low as $\overline{RAS}$ talls the write operation is inhibited on the chip if $\overline{WB}$(/$\overline{WE}$) is high as $\overline{RAS}$ falls, the write-per-bit capability does not work and the write operation is performed for all four data bits.

Data Outputs

The three-state output buffers provide direct TTL compatibility with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The outputs are in the high-impedance state until $\overline{CS}$ is brought low. In a read cycle the outputs go active after the access time interval t_{RAC} and t_{OEA} are satisfied.

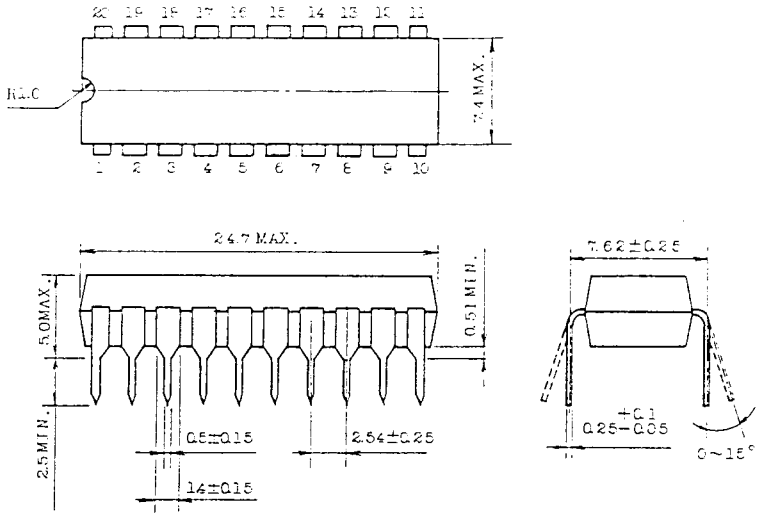
The outputs become valid after the access time has elapsed and remains valid while $\overline{CS}$ and $\overline{OE}$ are low. $\overline{CS}$ or $\overline{OE}$ going high returns it to a high impedance state. In an early-write cycle, the outputs are always in the high-impedance state. In a delayed-write or read-modify-write cycle, the outputs will follow the sequence for the read cycle.

When the $\overline{OE}$ input is brought to a logical low level, the output buffer are enabled. Both $\overline{CS}$ and $\overline{OE}$ can control the output. Thus in a read operation, either $\overline{OE}$ or $\overline{CS}$ returning high forces the outputs into the high impedance state.

OUTLINE DRAWINGS

· Plastic DIP

Unit in mm



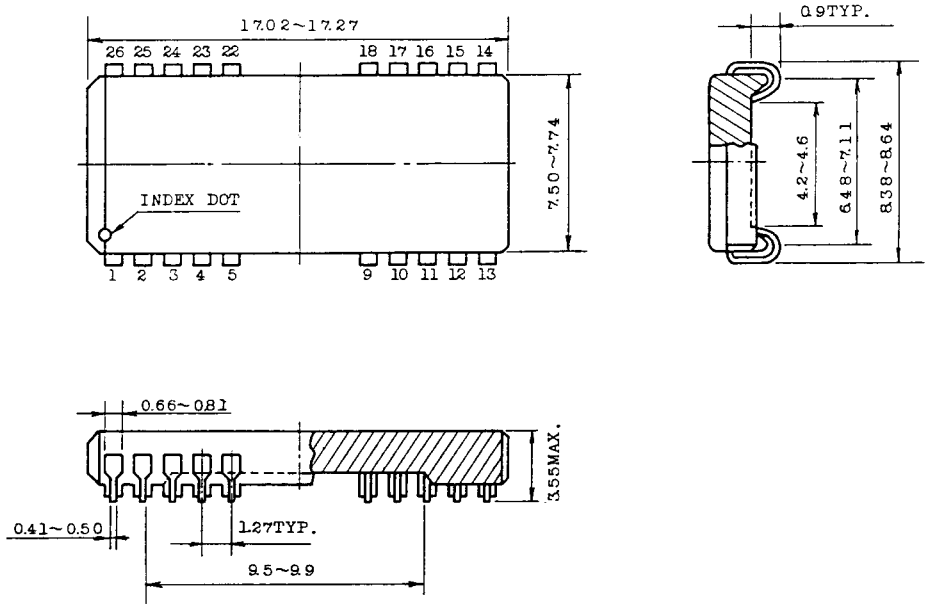
Note: Each lead pitch is 2.54mm.

All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.20 leads.

All dimensions are in millimeters.

• Plastic SOJ

Unit in mm



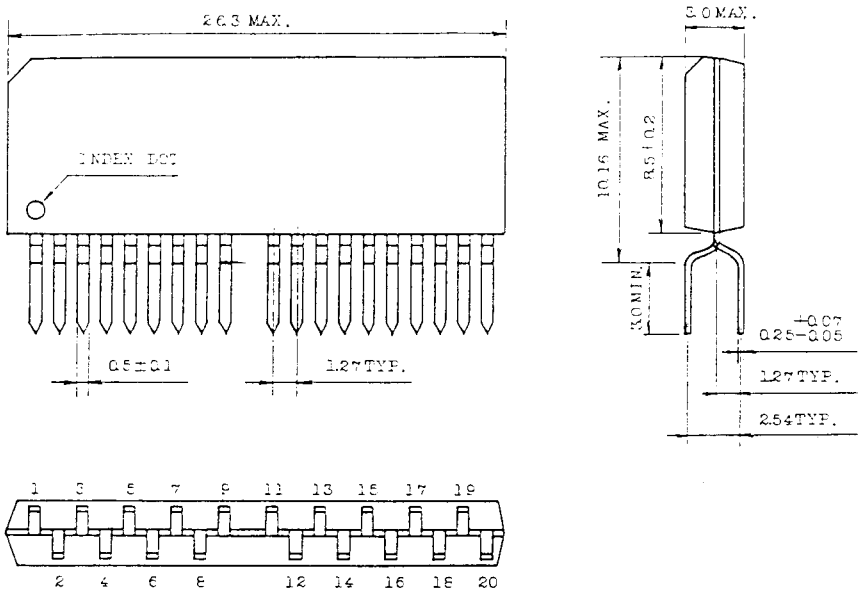
Note: Each lead pitch 1.27mm.

All dimensions are in millimeters.

Toshiba does not assume any responsibility ofr use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

• Plastic ZIP

Unit in mm



Note: Each lead pitch is 1.27mm.

All dimensions are in millimeters.

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