

AGP MEMORY MODULE

MT2LSDT132AGP

For the latest data sheet, please refer to the Micron
Web site: www.micron.com/mtl/msp/html/datasheet.html

FEATURES

- AGP Inline Memory Module (AIMM)
- 4MB (1 Meg x 32)
- Single +3.3V $\pm 0.3V$ power supply
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8, or full page
- Auto Precharge and Auto Refresh Modes
- 64ms, 4,096-cycle refresh
- LVTTTL-compatible inputs and outputs
- Fits in AGP port slot

OPTIONS

- Timing (Cycle Time)
6ns

MARKING

-6

KEY SDRAM COMPONENT TIMING PARAMETERS

SPEED GRADE	CLOCK FREQUENCY	ACCESSTIME		SETUP TIME	HOLD TIME
		CL = 2*	CL = 3*		
-6	166MHz	8ns	5.5ns	2ns	1ns

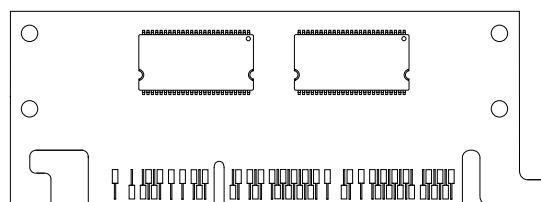
*CL = CAS (READ) latency

PART NUMBERS

PART NUMBER	CONFIGURATION	DEVICE PACKAGE
MT2LSDT132AGP-6_	1 Meg x 32	TSOP

NOTE: All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT2LSDT132AGP-6E1.

66-Pin AIMM (Front View)



PIN ASSIGNMENT

PIN	B	A	PIN	B	A
1	NC	NC	34	V _{DDQ}	V _{DDQ}
2	NC	TYPEDET	35	DQ16	A0
3	NC	NC	36	DQ15	A9
4	NC	NC	37	GND	GND
5	GND	GND	38	DQ14	A11/BA
6	NC	NC	39	DQ13	A8
7	NC	NC	40	V _{DDQ}	V _{DDQ}
8	DQ27	NC	41	DQ12	A10
9	V _{CC}	V _{CC}	42	NC	NC
10	DQ28	DQM3	43	GND	GND
11	DQ29	NC	44	NC	NC
12	DQ30	DQ24	45	V _{CC}	V _{CC}
13	GND	GND	46	DQ11	A7
14	NC	NC	47	V _{DDQ}	CS#
15	DQ31	DQ25	48	NC	NC
16	V _{CC}	V _{CC}	49	GND	GND
17	DQM2	DQ26	50	NC	A6
18	NC	NC	51	DQ10	A1
19	GND	GND	52	V _{DDQ}	CQ#
20	DQ23	WE#	53	DQ9	A5
21	DQ22	FSEL	54	DQ8	A2
22	Keyway	Keyway	55	GND	GND
23	Keyway	Keyway	56	DQM1	A4
24	Keyway	Keyway	57	DQ0	A3
25	Keyway	Keyway	58	V _{DDQ}	V _{DDQ}
26	DQ21	TCLK0	59	NC	NC
27	DQ20	TCLK1	60	DQ1	DQ5
28	V _{CC}	V _{CC}	61	GND	GND
29	DQ19	CAS#	62	DQ2	DQ6
30	DQ18	NC	63	DQ3	DQ7
31	GND	GND	64	V _{DDQ}	V _{DDQ}
32	NC	NC	65	DQ4	DQM0
33	DQ17	RAS#	66	NC	NC

NOTE: Pins A(B)22 through A(B)25 are keyway pins.

INTRODUCTION

Accelerated Graphics Port (AGP) technology provides a dedicated, high-speed port for the movement of large blocks of 3D texture data between the PC's graphics controller and system memory. AGP is based on a set of performance extensions or enhancements to the PCI bus. However, AGP neither replaces nor diminishes the necessity of PCI in the system. This high speed port is physically, logically, and electrically independent of the PCI bus. It is intended for the exclusive use of visual display devices; all other I/O devices will remain on the PCI bus.

GENERAL DESCRIPTION

The MT2LSDT132AGP is a high-speed CMOS, dynamic random-access, 4MB solid-state memory organized in a x32 configuration. This module is configured as a single bank with a synchronous interface (all signals are registered on the positive edge of the clock signals TCLK0 and TCLK1). Read and write accesses to the SDRAM module are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with

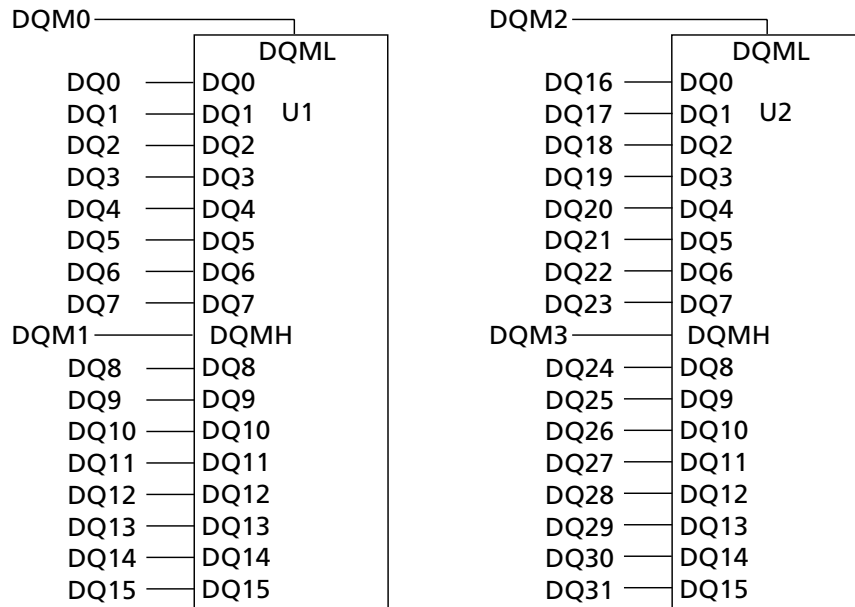
the ACTIVE command are used to select the bank and row to be accessed (BA0 selects the bank; A0-A11 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

This module is designed to be used in the AGP port in PC motherboards and is intended to be a mid-level cost between no added graphics memory and more expensive AGP card solutions.

This module provides for a programmable READ or WRITE burst terminate option. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence. This module uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the $2n$ rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing the alternate bank will hide the PRECHARGE cycles and provide seamless, high-speed, random-access operation.

For more information regarding SDRAM operation, refer to the 16 Meg x 16 SDRAM data sheet.

**FUNCTIONAL BLOCK DIAGRAM
MT2LSDT132APG (4MB)**



RAS# → RAS#: SDRAMs U1, U2
 CAS# → CAS#: SDRAMs U1, U2
 CS# → CS#: SDRAMs U1, U2
 WE# → WE#: SDRAMs U1, U2
 A0-A11 → A0-A10, BA: SDRAMs U1, U2

CK0 → U2

CK1 → U1

V_{DD} → SDRAMs U1, U2

V_{SS} → SDRAMs U1, U2

U1, U2 = MT48LC1M16A1TG SDRAMs

PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
A33, A29, A20	RAS#, CAS#, WE#	Input	Command Inputs: RAS#, CAS# and WE# (along with S0#-S3#) define the command being entered.
A26, A27	TCK0, TCK1	Input	Clock: TCK0 and TCK1 are driven by the system clock. All SDRAM input signals are sampled on the positive edge of CK. CK also increments the internal burst counter and controls the output registers.
A47	CS#	Input	Chip Select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# is considered part of the command code.
A65, B56, B17, A10	DQM0-DQM3	Input	Input/Output Mask: DQMB is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked when DQMB is sampled HIGH during a WRITE cycle. The output buffers are placed in a High-Z state (after a two-clock latency) when DQMB is sampled HIGH during a READ cycle.
A35, A51, A54, A57, A56, A53, A50, A46, A39, A36, A41, A38	A0-A11/BA	Input	Address Inputs: A0-A11/BA are sampled during the ACTIVE command (row-address A0-A10) and READ/WRITE command (column-address A0-A7, with A10 defining auto precharge) to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine if both banks are to be precharged (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
B57, B60, B62, B63, B65, A60, A62, A63, B54, B53, B51, B46, B41, B39, B38, B36, B35, B33, B30, B29, B27, B26, B21, B20, A12, A15, A17, B8, B10, B11, B12, B15	DQ0-DQ31	Input/ Output	Data I/O: Data bus.
A64, B64, A58, B58, A52, B52, B47, A40, B40, A34, B34	V _{DDQ}	Supply	Ground.
A45, B45, A28, B28, A25, B25, A16, B16, A9, B9	V _{CC}	Supply	Power Supply: +3.3V ±0.3V.
B5, A5, B13, A13, B19, A19, B31, A31, A61, B61, A55, B55, A49, B49, A43, B43, A37, B37	GND	Supply	Ground
B1, A1, B2, B3, A3, B4, A4, B6, A6, B7, A7, A8, A11, B14, A14, B18, A18, A30, B32, A32, B42, A42, B44, A44, B48, A48, B50, B59, A59, B66, A66	NC	–	No Connects: These pins are not connected.

COMMANDS

Truth Table 1 provides a general reference of available commands. For a more detailed description of

commands and operations, refer to the 16 Meg x 16 SDRAM data sheet.

TRUTH TABLE 1 – COMMANDS AND DQM OPERATION

(Note: 1)

NAME (FUNCTION)	CS#	RAS#	CAS#	WE#	DQM	ADDR	DQs	NOTES
COMMAND INHIBIT (NOP)	H	X	X	X	X	X	X	
NO OPERATION (NOP)	L	H	H	H	X	X	X	
ACTIVE (Select bank and activate row)	L	L	H	H	X	Bank/Row	X	3
READ (Select bank and column, and start READ burst)	L	H	L	H	X	Bank/Col	X	4
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	X	Bank/Col	Valid	4
BURST TERMINATE	L	H	H	L	X	X	Active	
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	X	Code	X	5
AUTO REFRESH or SELF REFRESH (Enter self refresh mode)	L	L	L	H	X	X	X	6, 7
LOAD MODE REGISTER	L	L	L	L	X	Op-code	X	2
Write Enable/Output Enable	–	–	–	–	L	–	Active	8
Write Inhibit/Output High-Z	–	–	–	–	H	–	High-Z	8

- NOTE:**
1. CKE is HIGH for all commands shown except SELF REFRESH.
 2. A0-A10 define the op-code written to the Mode Register.
 3. A0-A10 provide row address, BA determines which bank is made active.
 4. A0-A7 provide column address; A10 HIGH enables the auto precharge feature (nonpersistent), while A10 LOW disables the auto precharge feature; BA0, BA1 determine which bank is being read from or written to.
 5. A10 LOW: BA0, BA1 determine which bank is being precharged. A10 HIGH: both banks are precharged and BA0, BA1 are "Don't Care."
 6. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
 7. Internal refresh counter controls row addressing; all inputs and I/Os are "Don't Care" except for CKE.
 8. Activates or deactivates the DQs during WRITES (zero-clock delay) and READs (two-clock delay).

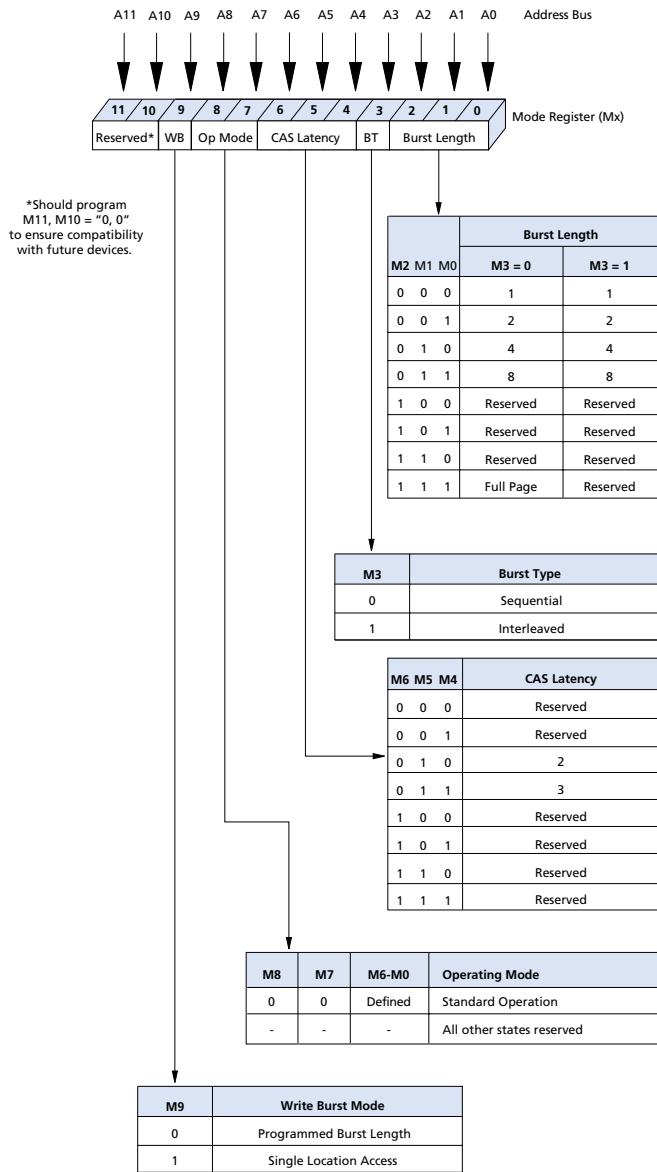


Figure 1
MODE REGISTER DEFINITION

Table 1
BURST DEFINITION

Burst Length	Starting Column Address	Order of Accesses Within a Burst	
		Type = Sequential	Type = Interleaved
2	A0		
	0	0-1	0-1
	1	1-0	1-0
4	A1 A0		
	0 0	0-1-2-3	0-1-2-3
	0 1	1-2-3-0	1-0-3-2
	1 0	2-3-0-1	2-3-0-1
	1 1	3-0-1-2	3-2-1-0
	1 1	3-0-1-2	3-2-1-0
8	A2 A1 A0		
	0 0 0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0 0 1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0 1 0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0 1 1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1 0 0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1 0 1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1 1 0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
1 1 1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0	
Full Page (256)	n = A0-A7 (location 0-255)	Cn, Cn + 1, Cn + 2 Cn + 3, Cn + 4... ...Cn - 1, Cn...	Not Supported

- NOTE:**
1. For a burst length of two, A1-A7 select the block-of-two burst; A0 selects the starting column within the block.
 2. For a burst length of four, A2-A7 select the block-of-four burst; A0-A1 select the starting column within the block.
 3. For a burst length of eight, A3-A7 select the block-of-eight burst; A0-A2 select the starting column within the block.
 4. For a full-page burst, the full row is selected, and A0-A7 select the starting column.
 5. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.
 6. For a burst length of one, A0-A7 select the unique column to be accessed, and Mode Register bit M3 is ignored.

ABSOLUTE MAXIMUM RATINGS*Voltage on V_{DD} Supply Relative to V_{SS} . -1V to +4.6V

Voltage on Inputs, NC or I/O Pins

Relative to V_{SS} -1V to +4.6VOperating Temperature, T_A (ambient) .. 0°C to +70°C

Storage Temperature (plastic) -55°C to +125°C

Power Dissipation 1W

*Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS(Notes: 1, 2) (V_{DD} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SUPPLY VOLTAGE	V _{DD}	3	3.6	V	
INPUT HIGH VOLTAGE: Logic 1; All inputs	V _{IH}	2	V _{DD} + 0.3	V	3
INPUT LOW VOLTAGE: Logic 0; All inputs	V _{IL}	-0.5	0.8	V	3
INPUT LEAKAGE CURRENT: Any input 0V ≤ V _{IN} ≤ V _{DD} (All other pins not under test = 0V)	DQM0-DQM3, CK0, CK1	I _{I1}	-5	5	μA
	RAS#, CAS#, CS#, WE#, A0-A11/BA	I _{I2}	-10	10	μA
OUTPUT LEAKAGE CURRENT: DQs are disabled; 0V ≤ V _{OUT} ≤ V _{DD}	I _{OZ}	-5	5	μA	
OUTPUT LEVELS: Output High Voltage (I _{OUT} = -4mA) Output Low Voltage (I _{OUT} = 4mA)	V _{OH}	2.4	-	V	
	V _{OL}	-	0.4	V	

- NOTE:**
1. All voltages referenced to V_{SS}.
 2. An initial pause of 100μs is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. The two AUTO REFRESH command wake-ups should be repeated any time the 'REF refresh requirement is exceeded.
 3. V_{IH} overshoot: V_{IH} (MAX) = V_{DD} + 1.2V for a pulse width ≤ 3ns, and the pulse width cannot be greater than one third of the cycle rate. V_{IL} undershoot: V_{IL} (MIN) = -1.2V for a pulse width ≤ 3ns, and the pulse width cannot be greater than one third of the cycle rate.

I_{DD} SPECIFICATIONS AND CONDITIONS

(Notes: 1-4) (V_{DD} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	SIZE	MAX	UNITS	NOTES	
			-6			
OPERATING CURRENT: Active Mode; Burst = 2; READ or WRITE; t _{RC} = t _{RC} (MIN); CAS latency = 3	I _{DD1}	4MB	290	mA	5, 6, 7, 8	
STANDBY CURRENT: Power-Down Mode; CKE = LOW; All banks idle	I _{DD2}	4MB	4	mA	8	
STANDBY CURRENT: Active Mode; CKE = HIGH; S0#-S3# = HIGH; All banks active after t _{RCD} met; No accesses in progress	I _{DD3}	4MB	90	mA	5, 7, 8, 9	
OPERATING CURRENT: Burst Mode; Continuous burst; READ or WRITE; All banks active; CAS latency = 3	I _{DD4}	4MB	280	mA	5, 6, 7, 8	
AUTO REFRESH CURRENT: CKE = HIGH; S0#-S3# = HIGH	t _{RC} = 15.625μs; CL = 3	I _{DD5}	4MB	90	mA	5, 6, 7, 8, 9
SELF REFRESH CURRENT: CKE ≤ 0.2V	I _{DD6}	4MB	2	mA	10	

- NOTE:**
- All voltages referenced to V_{SS}.
 - An initial pause of 100μs is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. The two AUTO REFRESH command wake-ups should be repeated any time the t_{REF} refresh requirement is exceeded.
 - AC timing tests have V_{IL} = 0V and V_{IH} = 3V, with timing referenced to 1.5V crossover point.
 - I_{DD} specifications are tested after the device is properly initialized.
 - I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
 - The I_{DD} current will decrease as the CAS latency is reduced. This is due to the fact that the maximum cycle rate is slower as the CAS latency is reduced.
 - Address transitions average one transition every two clocks.
 - t_{CK} = 8ns.
 - Other input signals are allowed to transition no more than once in any two-clock period and are otherwise at valid V_{IH} or V_{IL} levels.
 - Enables on-chip refresh and address counters.

CAPACITANCE

PARAMETER	SYMBOL	4MB		UNITS
		MIN	MAX	
Input Capacitance: CK0, CK1	C _{I1}	4	6	pF
Input Capacitance: DQM0-DQM3	C _{I2}	4	7	pF
Input Capacitance: RAS#, CAS#, CS#, A0-A11/BA	C _{I3}	6	8	pF
Input/Output Capacitance: DQ0-DQ31	C _{I0}	7	12	pF

NOTE: This parameter is sampled. V_{DD} = +3.3V; f = 1 MHz.

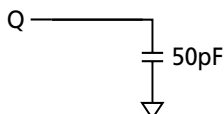
SDRAM COMPONENT* AC ELECTRICAL CHARACTERISTICS

(Notes: 1-5; notes appear below and on next page)

AC CHARACTERISTICS		-6			
PARAMETER		SYMBOL	MIN	MAX	UNITS NOTES
Access time from CLK (pos. edge)	CL = 3	t_{AC}		5.5	ns
	CL = 2	t_{AC}		8	ns
	CL = 1	t_{AC}		18	ns
Address hold time		t_{AH}	1		ns
Address setup time		t_{AS}	2		ns
CLK high-level width		t_{CH}	2.5		ns
CLK low-level width		t_{CL}	2.5		ns
Clock cycle time	CL = 3	t_{CK}	6		ns 6
	CL = 2	t_{CK}	8		ns 6
	CL = 1	t_{CK}	20		ns 6
CKE hold time		t_{CKH}	1		ns
CKE setup time		t_{CKS}	2		ns
CS#, RAS#, CAS#, WE#, DQM hold time		t_{CMH}	1		ns
CS#, RAS#, CAS#, WE#, DQM setup time		t_{CMS}	2		ns
Data-in hold time		t_{DH}	1		ns
Data-in setup time		t_{DS}	2		ns
Data-out high-impedance time	CL = 3	t_{HZ}		5.5	ns 7
	CL = 2	t_{HZ}		8	ns 7
	CL = 1	t_{HZ}		18	ns 7
Data-out low-impedance time		t_{LZ}	1		ns
Data-out hold time		t_{OH}	2		ns
ACTIVE to PRECHARGE command		t_{RAS}	42	120,000	ns
ACTIVE to ACTIVE command period		t_{RC}	60		ns
AUTO REFRESH period		t_{RCAR}	66		ns
ACTIVE to READ or WRITE delay		t_{RCD}	18		ns
Refresh period (4,096 cycles)		t_{REF}		64	ms
PRECHARGE command period		t_{RP}	18		ns
ACTIVE bank A to ACTIVE bank B command		t_{RRD}	12		ns
Transition time		t_T	0.3	1.2	ns 8
WRITE recovery time		t_{WR}	1 + 4ns		t_{CK} 9
			10		ns 10
Exit SELF REFRESH to ACTIVE command		t_{XSR}	80		ns 11

*Specifications for the SDRAM components used on the module.

- NOTE:**
1. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$) is ensured.
 2. An initial pause of $100\mu\text{s}$ is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. The two AUTO REFRESH command wake-ups should be repeated any time the t_{REF} refresh requirement is exceeded.
 3. In addition to meeting the transition rate specification, the clock and CKE must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
 4. Outputs measured at 1.5V with equivalent load:



5. AC timing tests have $V_{IL} = 0\text{V}$ and $V_{IH} = 3\text{V}$, with timing referenced to 1.5V crossover point.

NOTES: (continued)

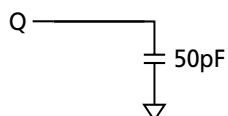
6. The clock frequency must remain constant during access or precharge states (READ, WRITE, including ^tWR, and PRECHARGE commands). CKE may be used to reduce the data rate.
7. ^tHZ defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}. The last valid data element will meet ^tOH before going High-Z.
8. AC characteristics assume ^tT = 1ns.
9. Auto precharge mode only. The precharge timing budget (^tRP) begins 10ns after the last WRITE is executed.
10. Precharge mode only.
11. CLK must be toggled a minimum of two times during this period.

AC FUNCTIONAL CHARACTERISTICS

(Notes: 1-6) ($0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$)

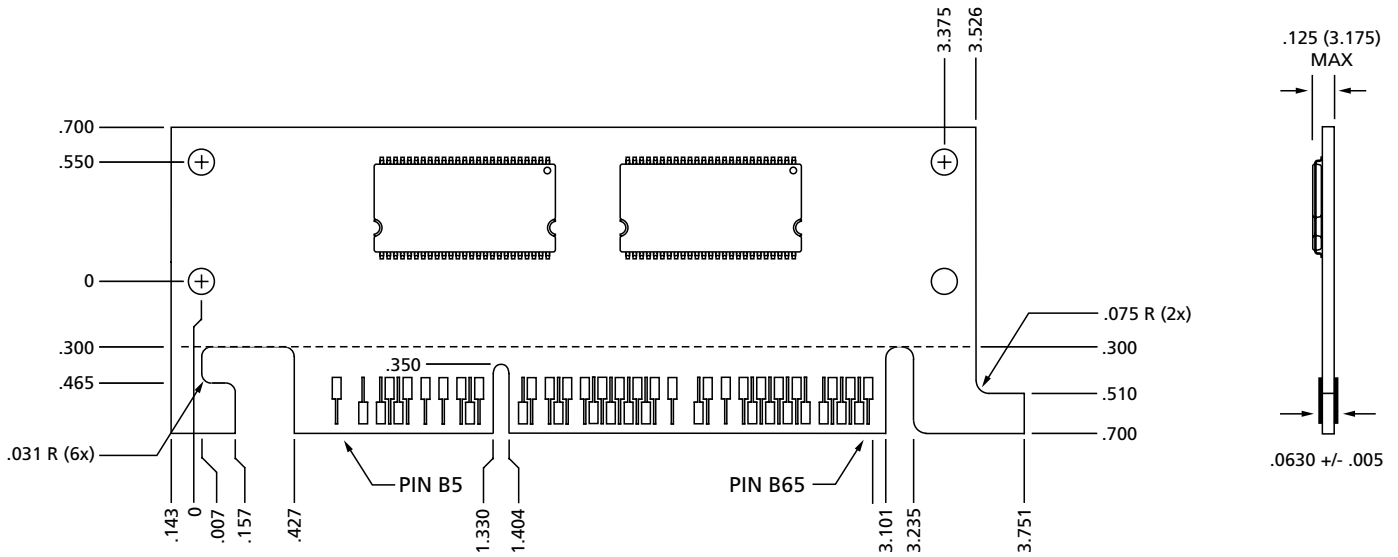
PARAMETER	SYMBOL	-6	UNITS	NOTES	
READ/WRITE command to READ/WRITE command	t^{CQD}	1	t^{CK}	7	
CKE to clock disable or power-down entry mode	t^{CKED}	1	t^{CK}	8	
CKE to clock enable or power-down exit setup mode	t^{PED}	1	t^{CK}	8	
DQM to input data delay	t^{DQD}	0	t^{CK}	7	
DQM to data mask during WRITES	t^{DQM}	0	t^{CK}	7	
DQM to data high-impedance during READs	t^{DQZ}	2	t^{CK}	7	
WRITE command to input data delay	t^{DWD}	0	t^{CK}	7	
Data-in to ACTIVE command	CL = 3	t^{DAL}	5	t^{CK}	9, 10
	CL = 2	t^{DAL}	4	t^{CK}	9, 10
	CL = 1	t^{DAL}	3	t^{CK}	9, 10
Data-in to PRECHARGE command	t^{DPL}	2	t^{CK}	10, 11	
Last data-in to burst STOP command	t^{BDL}	0	t^{CK}	7	
Last data-in to new READ/WRITE command	t^{CDL}	1	t^{CK}	7	
Last data-in to PRECHARGE command	t^{RDL}	1	t^{CK}	10, 11	
LOAD MODE REGISTER command to ACTIVE or REFRESH command	t^{MRD}	2	t^{CK}	12	
Data-out to high-impedance from PRECHARGE command	CL = 3	t^{ROH}	3	t^{CK}	7
	CL = 2	t^{ROH}	2	t^{CK}	7
	CL = 1	t^{ROH}	1	t^{CK}	7

- NOTE:**
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$) is ensured.
 - An initial pause of $100\mu\text{s}$ is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. The two AUTO REFRESH command wake-ups should be repeated any time the t^{REF} refresh requirement is exceeded.
 - AC characteristics assume $t^{\text{T}} = 1\text{ns}$.
 - In addition to meeting the transition rate specification, the clock and CKE must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
 - Outputs measured at 1.5V with equivalent load:



- AC timing tests have $V_{\text{IL}} = 0\text{V}$ and $V_{\text{IH}} = 3\text{V}$, with timing referenced to 1.5V crossover point.
- Required clocks are specified by JEDEC functionality and are not dependent on any timing parameter.
- Timing actually specified by t^{CKS} ; clock(s) specified as a reference only at minimum cycle rate.
- Timing actually specified by t^{WR} plus t^{RP} ; clock(s) specified as a reference only at minimum cycle rate.
- Based on $t^{\text{CK}} = 125\text{MHz}$.
- Timing actually specified by t^{WR} .
- JEDEC specifies three clocks.

AIMM



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