

## EPL242ED/EP/EJ

### CMOS ELECTRICALLY PROGRAMMABLE LOGIC

EPL242 is a programmable logic array of AND-(fixed) OR-register configuration (I/O delay time: 25 ns).

The user can program the device simply by writing to the EPROM cell assigned on the array. This greatly shortens the development time and simplifies circuit correction. Register usage can be selected, and the power consumption depends on the use rate of the product terms (30 mA at 35% use).

#### ■ FEATURES

- Low power consumption and high reliability based on CMOS-EPROM process
- 24 pins, 22 inputs, 8 outputs
- Ceramic package products can be erased with ultraviolet light.
- Packages :

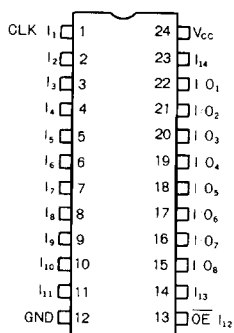
EPL242ED	24-pin	300 mil	CERDIP (with window)
EPL242EP	24-pin	300 mil	MOLDDIP
EPL242EJ	28-pin		PLCC
- Data copy prevention
- I/O propagation time : 25 ns (max.)  
Clock-input-to-output delay time : 15 ns (max.)
- Abundant functions based on macro I/O cell
  - A. Selecting combined and register outputs
  - B. Selecting output polarity
  - C. Selecting synchronous and asynchronous signals (External CLK, Internal CLK)
  - D. Asynchronous reset (AR1, AR2)
  - E. Asynchronous set (AS1, AS2)
- Power-on reset

■ PIN DESCRIPTION

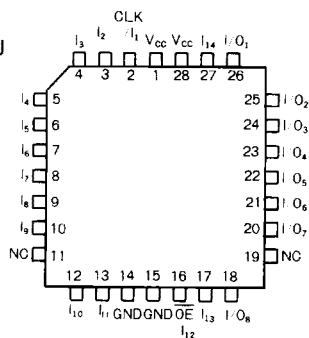
Pin No.		Pin Name	Function
DIP	PLCC	Logic Mode	Logic Mode
1	2	CLK/I <sub>1</sub>	Input Clock
2	3	I <sub>2</sub>	
3	4	I <sub>3</sub>	
4	5	I <sub>4</sub>	
5	6	I <sub>5</sub>	
6	7	I <sub>6</sub>	
7	8	I <sub>7</sub>	
8	9	I <sub>8</sub>	
9	10	I <sub>9</sub>	
10	12	I <sub>10</sub>	
11	13	I <sub>11</sub>	
12	14 · 15	GND	GND
13	16	OE/I <sub>12</sub>	Output Enable/Input
14	17	I <sub>13</sub>	Input
15	18	I/O <sub>8</sub>	Input/Output
16	20	I/O <sub>7</sub>	
17	21	I/O <sub>6</sub>	
18	22	I/O <sub>5</sub>	
19	23	I/O <sub>4</sub>	
20	24	I/O <sub>3</sub>	
21	25	I/O <sub>2</sub>	
22	26	I/O <sub>1</sub>	
23	27	I <sub>14</sub>	Input
24	1 · 28	Vcc	Vcc

■ PIN CONFIGURATION

EPL242ED  
EPL242EP



EPL242EJ



### ■ ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Condition	Rating	Unit
Vcc	Vcc Power Supply	With respect to GND	-0.3 ~ 7.0	V
Vpp	Vpp Power Supply		-0.3 ~ 14.5	V
Vi	Input Voltage		-0.3 ~ Vcc+0.3	V
Vo	Output Voltage		-0.3 ~ Vcc+0.3	V
Pd	Max. Power Consumption	Ta=25°C	0.8	W
Topr	Operating Ambient Temperature		0 ~ 70	°C
Tstg	Storage Temperature		-40 ~ 125	°C

### ■ RECOMMENDED OPERATING CONDITION (Ta=0~70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Power Supply	4.75	5.0	5.25	V
VIH	"H" Input Voltage	2.0		Vcc+0.3	V
VIL	"L" Input Voltage	-0.3		0.8	V

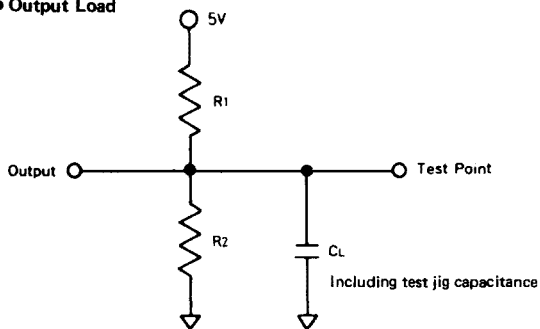
### ■ DC CHARACTERISTICS (Ta=0~70°C, Vcc=5V±5%)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
II	Input Leakage Current	VIN=0V~Vcc	-20		20	μA
ILO	Output Leakage Current for OFF state	Vo=0V~Vcc	-20		20	μA
VIL	"L" Input Voltage		-0.3		0.8	V
VIH	"H" Input Voltage		2.0		Vcc+0.3	V
VoL	"L" Output Voltage	Vcc=MIN, IOL=24mA			0.5	V
VoH	"H" Output Voltage	Vcc=MIN, IOH=-3.2mA	2.4			V
Icc1	Power Supply Current (Standby)	Vcc=MAX, VIN=GND or Vcc, f=0Hz			70	mA
Icc2	Power Supply Current (Operation)	Vcc=MAX, VIN=GND or Vcc, f=10MHz			80	mA

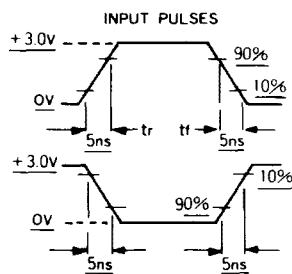
■ AC CHARACTERISTICS (Ta=0~70°C, Vcc=5V±5%)

Symbol	Parameter		Condition	Min.	Typ.	Max.	Unit	
	Clock	Parameters						
t <sub>PD</sub>	External Clock CLK (1 pin)	Input or I/O input to non-registered output	C <sub>L</sub> =50pF R <sub>1</sub> =200Ω R <sub>2</sub> =390Ω			25	ns	
t <sub>PIX</sub>		Input or I/O input to output disable				25	ns	
t <sub>PZ</sub>		Input or I/O input to output enable				25	ns	
t <sub>PXZ</sub>		OE (pin 13) to output disable				20	ns	
t <sub>PZX</sub>		OE (pin 13) to output enable				20	ns	
t <sub>SU1</sub>		Input or I/O input setup time			15			ns
t <sub>H1</sub>		Input or I/O input hold time			0			ns
t <sub>CLK1</sub>		Clock to output delay					15	ns
t <sub>FPD1</sub>		Clock to non-registered output from registered feed back					35	ns
t <sub>w1</sub>		External clock width			15			ns
t <sub>SET</sub>		Input or I/O input to asynchronous set					25	ns
t <sub>RST</sub>		Input or I/O input to asynchronous reset					25	ns
t <sub>P1</sub>		Minimum clock period (t <sub>SU1</sub> + t <sub>CLK1</sub> )					30	ns
f <sub>1</sub>		Maximum frequency (1/t <sub>P1</sub> )			33.3			MHz

● Output Load



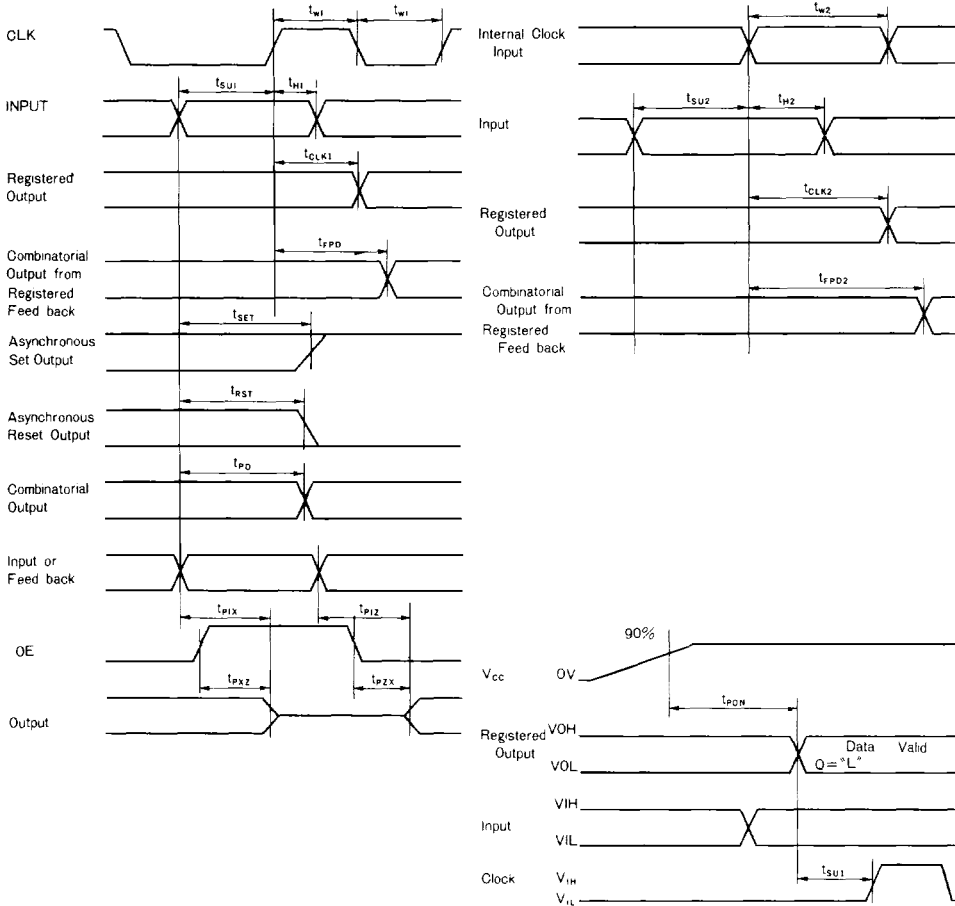
● Input Wave form



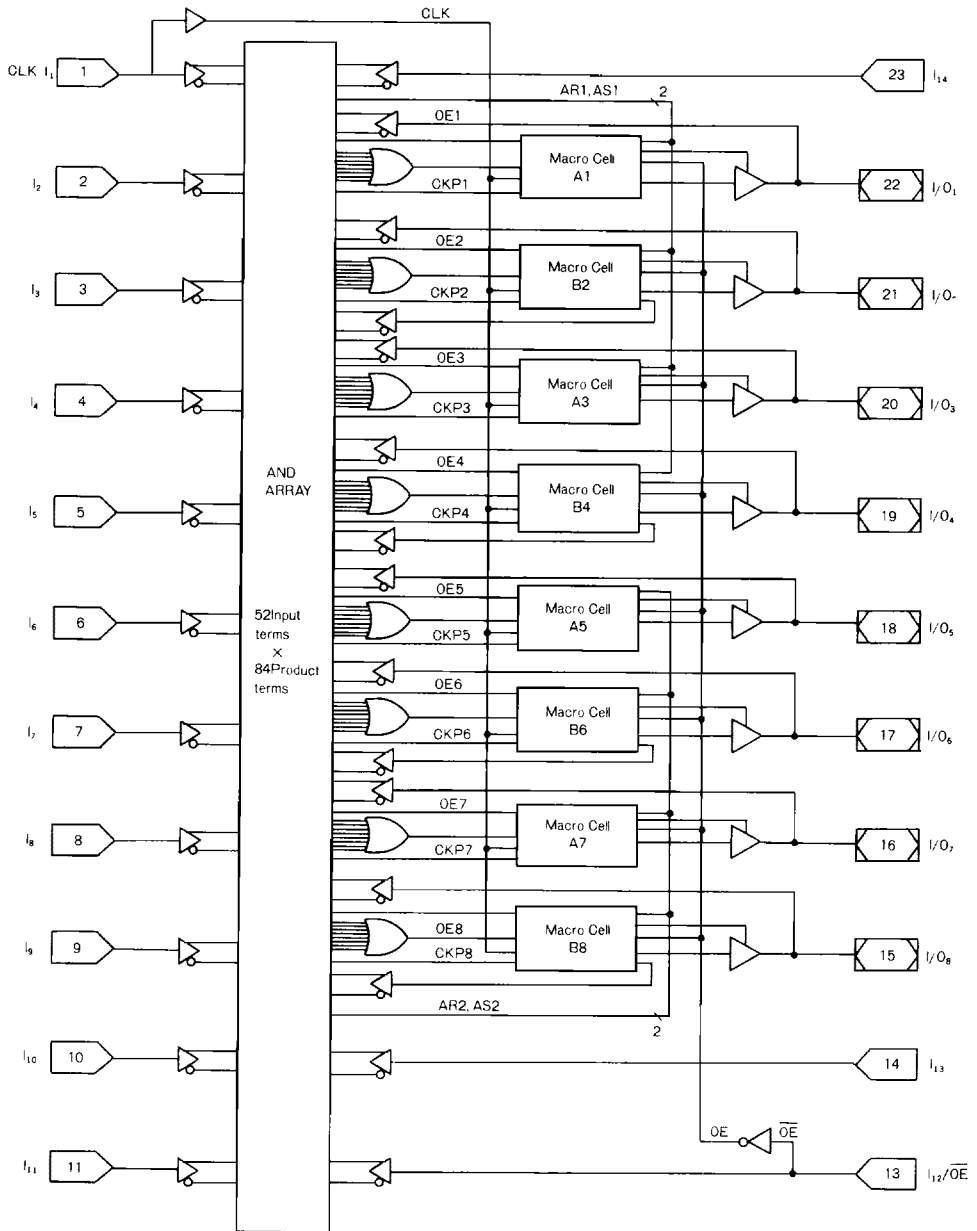
Note) A.C. Characteristics are measured at the Voltage of 1.5V on both input and output.

Symbol	Parameter		Condition	Min.	Typ.	Max.	Unit	
	Clock	Parameters						
t <sub>SU2</sub>	Internal Clock	Input or I/O input setup time	C <sub>L</sub> =50pF	5			ns	
t <sub>H2</sub>		Input or I/O input hold time		10			ns	
t <sub>CLK2</sub>		Clock P.T. input to output delay				30		ns
t <sub>FPD2</sub>	CKPn (n=1-8)	Clock P.T. input to non-registered output from registered feed back	R <sub>1</sub> =200Ω			50	ns	
t <sub>w2</sub>		Clock P.T. input width		15			ns	
t <sub>P2</sub>		Minimum Clock period (t <sub>SU2</sub> + t <sub>CLK2</sub> )		R <sub>2</sub> =390Ω			35	ns
f <sub>2</sub>		Maximum frequency (1/t <sub>P2</sub> )			28.6			MHz
t <sub>PON</sub>		Power on reset time			45			μs

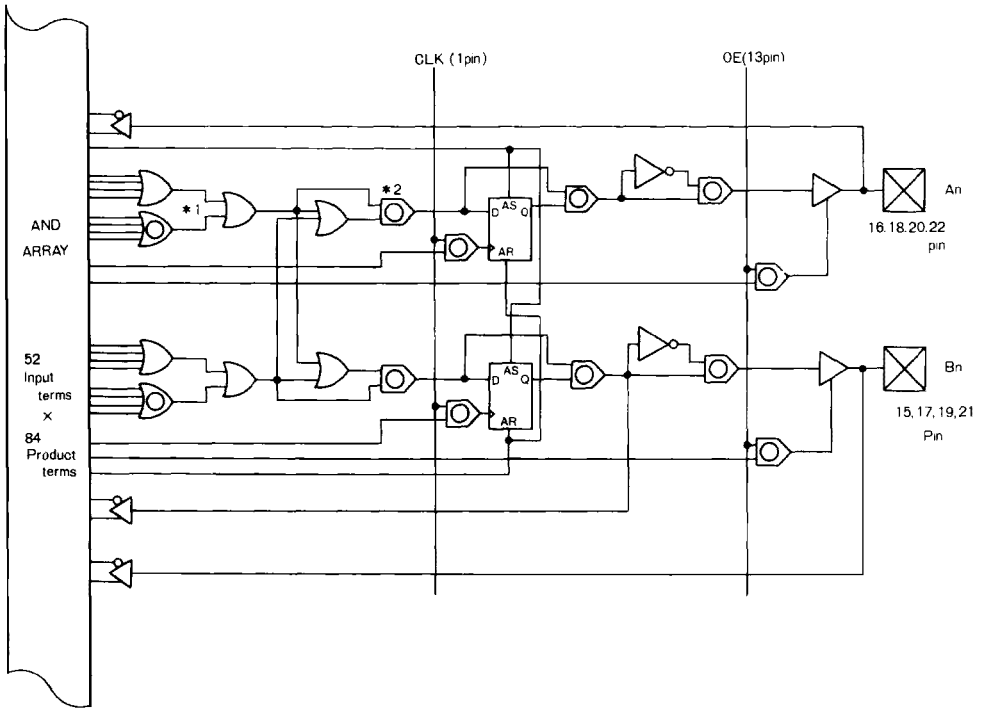
■ TIMING CHART




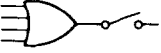

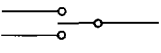
■ BLOCK DIAGRAM



■ I/O MACROCELL BLOCK DIAGRAM



**Note**

- \* 1 The symbol  denotes programmable switch 
- \* 2 The symbol  denotes programmable switch 

## ■ DESCRIPTION

### 1. Logic Function (logic mode)

EPL242 is an erasable, writable logic array that uses CMOS EPROM and has 52 input terms (22 inputs and 4 feedbacks) and 84 product terms.

All I/O pins perform normal logical operations at the TTL level. Register usage and output polarities can be selected by using the I/O macro cell described later.

All crosspoints on the AND array (crosspoints of product terms and input terms) have an EPROM cell connection. Upon initial delivery, all crosspoints are connected.

As illustrated in Fig. 1, if both positive input (I) and negative input ( $\bar{I}$ ) are not written to, the AND output (P1) is inactive. If both positive input (I) and negative input ( $\bar{I}$ ) are written to, the AND output (P2) is logically "Don't Care".

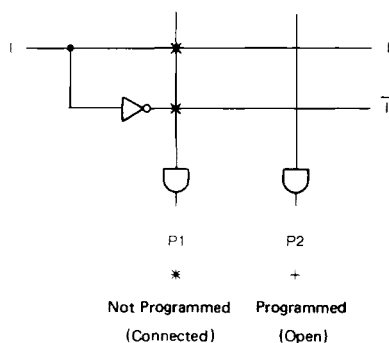


Fig. 1

### 2. I/O macro Cell

The I/O macro cell controls several operations including "OR" selection and OE selection. Operations are performed by writing to an EPROM cell, which is called the optional bit (O.B.).

The functions are described below (the switch positions are when O.B. is not written to).

#### (1) "OR" selection (Term Share)

EPL242 allows the user to select whether to obtain further "OR" with an adjacent output or to pass the first "OR" as is after obtaining "OR" for the eight product terms.

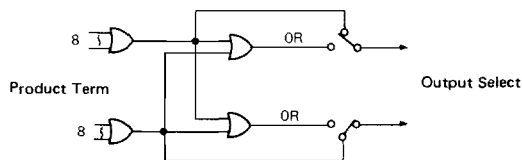


Fig. 2 "OR" Select

(2) OE selection

EPL242 allows the user to select, for each macro cell, whether to use external (13-pin) pin signals or internal signals from the product terms as the output buffer OE signal.

(3) Output selection and CLK selection

EPL242 allows the user to select, for each macro cell, whether to use the register, whether to use external clock signals (common to all registers) as register clock signals, and whether to use internal clocks (for each register).

Each register has asynchronous reset and set.

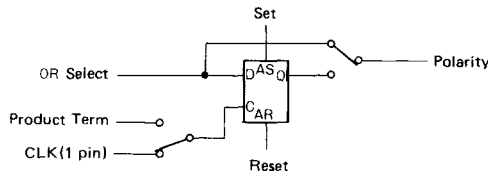


Fig. 3 Output Select, CLK Select

(4) Polarity

EPL242 allows the user to select the output signal polarity.

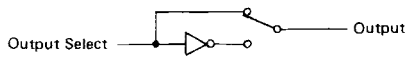
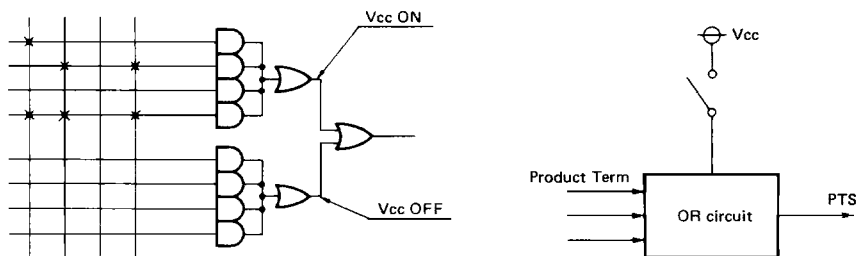


Fig. 4 Polarity

**(5) Power control (PWC)**

Current is supplied to the OR unit of the product term that is used logically. In other words, EPL242E connects two 4AND-1OR configurations using OR, and, to use one 4AND-1OR configuration only, stops the current to the other OR unit. This greatly reduces power consumption (see Fig. 5). (About 30 mA when the product term use rate is 35%.)



**Fig. 5 Power Control**

**(6) Power-on reset**

Upon power-on, each register of EPL242 is reset. When  $V_{cc}$  rises from 0 to 90% and  $t_{PON}$  ( $45\mu s$  min.) passes, the output of each register is determined as "L". (If a reverse polarity is specified, "H" is output to the output pin.)

### 3. Security bit

EPL242E does not operate meaningfully until the user writes data. In other words, data cannot be copied before the written data is read. EPL242E has a security circuit to prevent the written data from being read by a third party. The security circuit prevents the data from being read when the security fuse is written. The following describes the operation of the security circuit in reference to Fig. 6.

The AND array sense amplifier reads the EPROM memory cell signal of the AND array selected by the X and Y decoder. The security sense amplifier reads the security fuse signal. The output of the security sense amplifier (SEQ) is at the "H" level when the security fuse is written and is at the "L" level when the security fuse is not written. As shown in Fig. 6, the AND signal of the AND array output and SEQ is the input to the output buffer. Therefore, by writing the security fuse (SEQ = "L"), the output is set to the "L" level regardless of the AND array I/O signal. The security circuit does not affect the normal logic operation, because the signal flows during programming and logic operations are independent of each other and the security circuit only controls the signal flow during programming.

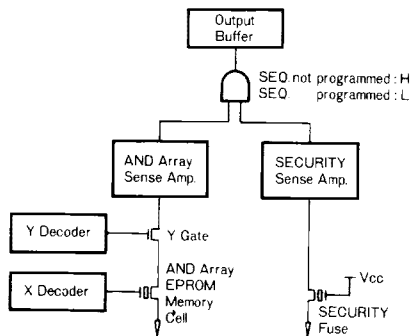
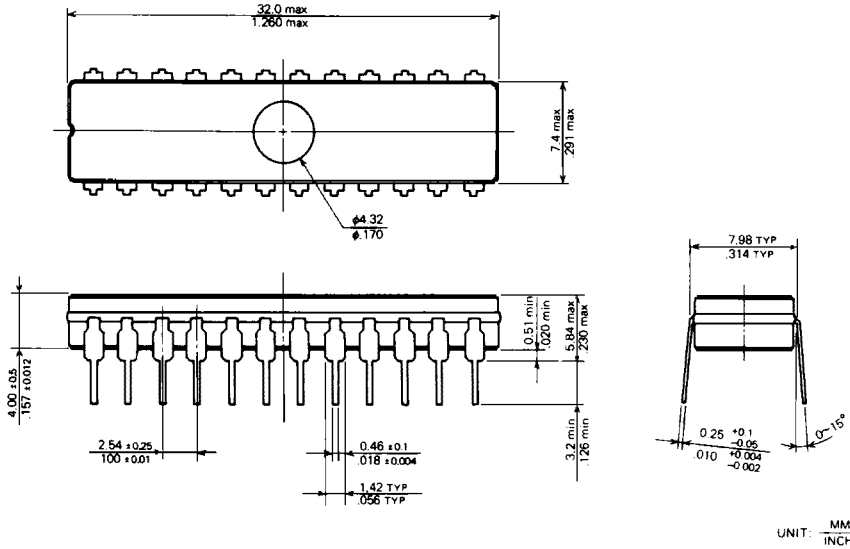


Fig. 6 Security Circuit

■ PACKAGE DIMENSION

● EPL242ED (24 PIN 300mil CERDIP)



● EPL242EP (24 PIN 300mil MOLD DIP)

