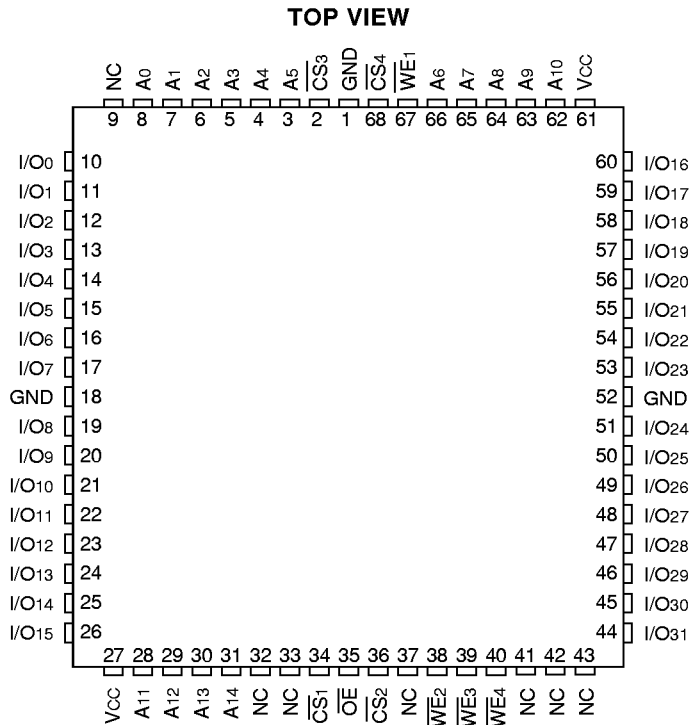






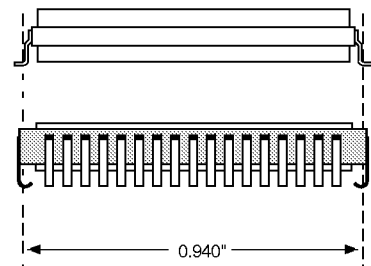
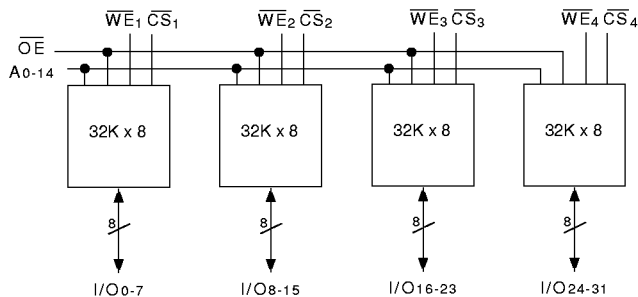
FIG. 2 PIN CONFIGURATION FOR WE32K32-XG2UX



**PIN DESCRIPTION**

I/O0-31	Data Inputs/Outputs
A0-14	Address Inputs
$\overline{WE}1-4$	Write Enables
$\overline{CS}1-4$	Chip Selects
$\overline{OE}$	Output Enable
Vcc	Power Supply
GND	Ground
NC	Not Connected

**BLOCK DIAGRAM**



The White 68 lead G2U CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2U has the TCE and lead inspection advantage of the CQFP form.



### ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol		Unit
Operating Temperature	T <sub>A</sub>	-55 to +125	°C
Storage Temperature	T <sub>STG</sub>	-65 to +150	°C
Signal Voltage Relative to GND	V <sub>G</sub>	-0.6 to +6.25	V
Voltage on $\overline{OE}$ and A9		-0.6 to +13.5	V

**NOTE:**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V <sub>CC</sub>	4.5	5.5	V
Input High Voltage	V <sub>IH</sub>	2.0	V <sub>CC</sub> + 0.3	V
Input Low Voltage	V <sub>IL</sub>	-0.5	+0.8	V
Operating Temp. (Mil.)	T <sub>A</sub>	-55	+125	°C
Operating Temp. (Ind.)	T <sub>A</sub>	-40	+85	°C

### TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O
H	X	X	Standby	High Z
L	L	H	Read	Data Out
L	H	L	Write	Data In
X	H	X	Out Disable	High Z/Data Out
X	X	H	Write	
X	L	X	Inhibit	

### CAPACITANCE

(T<sub>A</sub> = 25 °C)

Parameter	Symbol	Condition	Max	Unit
Address Input Capacitance OE Capacitance	C <sub>AD</sub> C <sub>OE</sub>	V <sub>IN</sub> = 0V, f = 1.0MHz	50	pF
$\overline{CS}$ 1-4 Capacitance	C <sub>CS</sub>	V <sub>IN</sub> = 0V, f = 1.0MHz	20	pF
$\overline{WE}$ 1-4 Capacitance	C <sub>WE</sub>	V <sub>IN</sub> = 0V, f = 1.0MHz	20	pF
Data I/O Capacitance	C <sub>I/O</sub>	V <sub>IN</sub> = 0V, f = 1.0MHz	20	pF

This parameter is guaranteed by design but not tested.

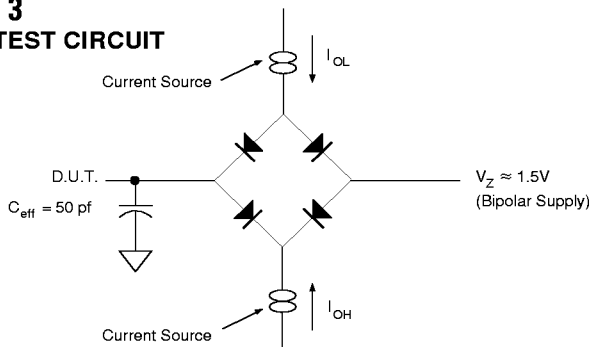
### DC CHARACTERISTICS

(V<sub>CC</sub> = 5.0V, GND = 0V, T<sub>A</sub> = -55°C to +125°C)

Parameter	Symbol	Conditions	-90		-120		-150		Units
			Min	Max	Min	Max	Min	Max	
Input Leakage Current	I <sub>LI</sub>	V <sub>CC</sub> = 5.5, V <sub>IN</sub> = GND to V <sub>CC</sub>		10		10		10	µA
Output Leakage Current	I <sub>LO x 32</sub>	$\overline{CS}$ = V <sub>IH</sub> , $\overline{OE}$ = V <sub>IH</sub> , V <sub>OUT</sub> = GND to V <sub>CC</sub>		10		10		10	µA
Operating Supply Current x 32 Mode	I <sub>CC x 32</sub>	$\overline{CS}$ = V <sub>IL</sub> , $\overline{OE}$ = V <sub>IH</sub> , f = 5MHz		250		200		150	mA
Standby Current	I <sub>SB</sub>	$\overline{CS}$ = V <sub>IH</sub> , $\overline{OE}$ = V <sub>IH</sub> , f = 5MHz		2.5		2.5		2.5	mA
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2.1 mA, V <sub>CC</sub> = 4.5V		0.45		0.45		0.45	V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -400µA, V <sub>CC</sub> = 4.5V	2.4		2.4		2.4		V

NOTE: DC test conditions: V<sub>IH</sub> = V<sub>CC</sub> - 0.3V, V<sub>IL</sub> = 0.3V

**FIG. 3**  
**AC TEST CIRCUIT**



### AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V <sub>IL</sub> = 0, V <sub>IH</sub> = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

**NOTES:**

V<sub>Z</sub> is programmable from -2V to +7V.  
I<sub>OL</sub> & I<sub>OH</sub> programmable from 0 to 16mA.  
Tester Impedance Z<sub>0</sub> = 75 Ω.  
V<sub>Z</sub> is typically the midpoint of V<sub>OH</sub> and V<sub>OL</sub>.  
I<sub>OL</sub> & I<sub>OH</sub> are adjusted to simulate a typical resistive load circuit.  
ATE tester includes jig capacitance.

**WRITE**

A write cycle is initiated when  $\overline{OE}$  is high and a low pulse is on  $\overline{WE}$  or  $\overline{CS}$  with  $\overline{CS}$  or  $\overline{WE}$  low. The address is latched on the falling edge of  $\overline{CS}$  or  $\overline{WE}$  whichever occurs last. The data is latched by the rising edge of  $\overline{CS}$  or  $\overline{WE}$ , whichever occurs first. A byte write operation will automatically continue to completion.

**WRITE CYCLE TIMING**

Figures 4 and 5 show the write cycle timing relationships. A write cycle begins with address application, write enable and chip select. Chip select is accomplished by placing the  $\overline{CS}$  line low. Write enable consists of setting the  $\overline{WE}$  line low. The write cycle begins when the last of either  $\overline{CS}$  or  $\overline{WE}$  goes low.

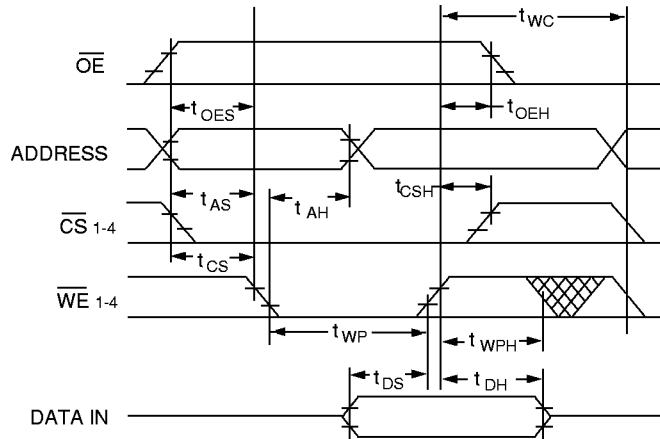
The  $\overline{WE}$  line transition from high to low also initiates an internal 150  $\mu$ sec delay timer to permit page mode operation. Each subsequent  $\overline{WE}$  transition from high to low that occurs before the completion of the 150  $\mu$ sec time out will restart the timer from zero. The operation of the timer is the same as a retriggerable one-shot.

**AC WRITE CHARACTERISTICS**  
(Vcc = 5.0V, GND = 0V, TA = -55°C to +125°C)

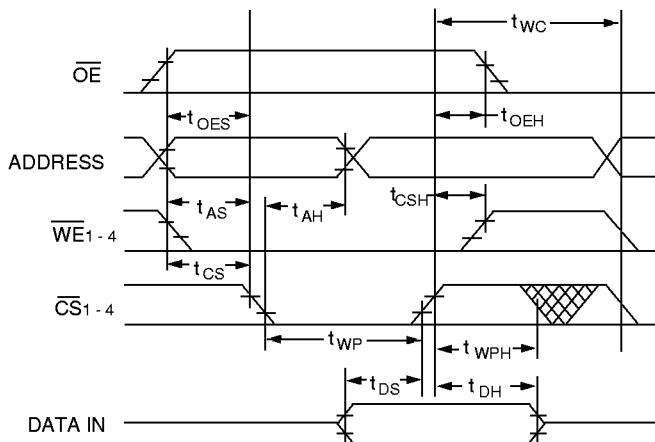
WRITE CYCLE Write Cycle Parameter	Symbol	-90		-120		-150		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time, TYP = 6ms	twc		10		10		10	ms
Address Set-up Time	tas	0		30		30		ns
Write Pulse Width ( $\overline{WE}$ or $\overline{CS}$ )	twp	100		150		150		ns
Chip Select Set-up Time	tcs	0		0		0		ns
Address Hold Time	tah	50		100		100		ns
Data Hold Time	tdh	0		10		10		ns
Chip Select Hold Time	tcsH	0		0		0		ns
Data Set-up Time	tds	50		100		100		ns
Write Pulse Width High	twpH	50		50		50		ns
Output Enable Set-up Time	toes	10		10		10		ns
Output Enable Hold Time	toeh	10		10		10		ns



**FIG. 4**  
**WRITE WAVEFORMS**  
**WE CONTROLLED**



**FIG. 5**  
**WRITE WAVEFORMS**  
**CS CONTROLLED**





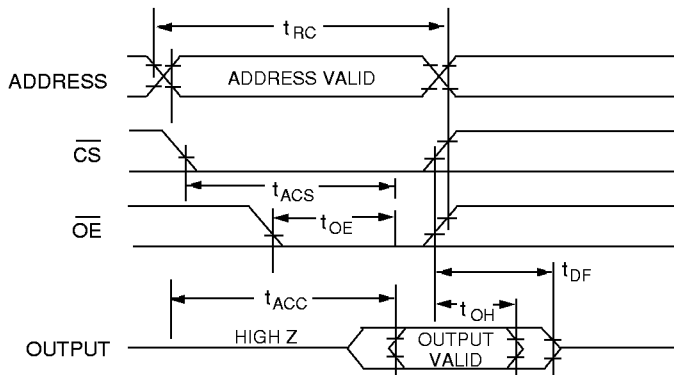
READ

The WE32K32-XXH stores data at the memory location determined by the address pins. When CS and OE are low and WE is high, this data is present on the outputs. When CS and OE are high, the outputs are in a high impedance state. This 2 line control prevents bus contention.

AC READ CHARACTERISTICS (See Figure 6)
(Vcc = 5.0V, GND = 0V, TA = -55°C to +125°C)

Table with 9 columns: READ CYCLE Parameter, Symbol, -90 Min, -90 Max, -120 Min, -120 Max, -150 Min, -150 Max, Unit. Rows include Read Cycle Time, Address Access Time, CS Access Time, Output Hold from Add. Change, OE or CS, Output Enable to Output Valid, and Chip Select or OE to Output in High Z.

FIG. 6 READ WAVEFORMS



NOTES:

- 1. OE may be delayed up to tACS - tOE after the falling edge of CS without impact on tOE or by tACC - tOE after an address change without impact on tACC.
2. tCHZ, tOHZ are specified from OE or CS whichever occurs first (CL = 5pF).
3. All I/O transitions are measured ±200 mV from steady state with loading as specified in "Load Test Circuits."



### DATA POLLING

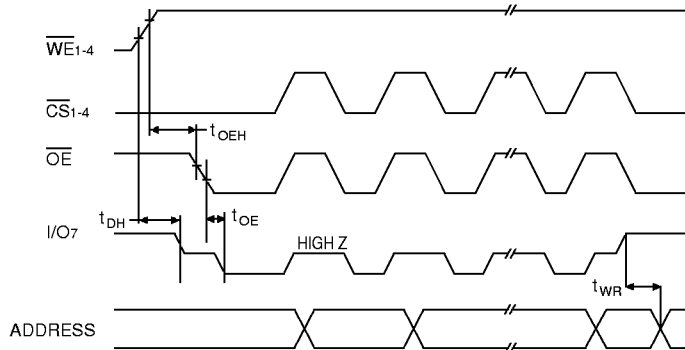
The WE32K32-XXX offers a data polling feature which allows a faster method of writing to the device. Figure 7 shows the timing diagram for this function. During a byte or page write cycle, an attempted read of the last byte written will result in the complement of the written data on D7 (for each chip.) Once the write cycle has been completed, true data is valid on all outputs and the next cycle may begin. Data polling may begin at any time during the write cycle.

### DATA POLLING CHARACTERISTICS

(Vcc = 5.0V, GND = 0V, TA = -55°C to +125°C)

Parameter	Symbol	Min	Max	Unit
Data Hold Time	t <sub>DH</sub>	10		ns
$\overline{OE}$ Hold Time	t <sub>OEH</sub>	10		ns
$\overline{OE}$ To Output Valid	t <sub>OE</sub>		100	ns
Write Recovery Time	t <sub>WR</sub>	0		ns

**FIG. 7**  
**DATA POLLING WAVEFORMS**





### PAGE WRITE OPERATION

The WE32K32-XXX has a page write operation that allows one to 64 bytes of data to be written into the device and consecutively loads during the internal programming period. Successive bytes may be loaded in the same manner after the first data byte has been loaded. An internal timer begins a time out operation at each write cycle. If another write cycle is completed within 150µs or less, a new time out period begins. Each write cycle restarts the delay period. The write cycles can be continued as long as the interval is less than the time out period.

The usual procedure is to increment the least significant address lines from A0 through A5 at each write cycle. In this manner a page of up to 64 bytes can be loaded in to the EEPROM in a burst mode before beginning the relatively long interval programming cycle.

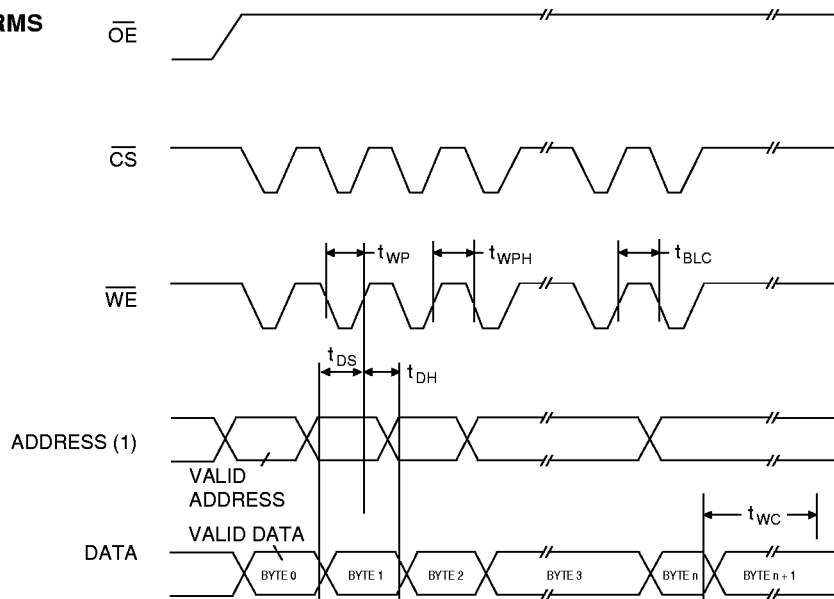
After the 150µs time out is completed, the EEPROM begins an internal write cycle. During this cycle the entire page of bytes will be written at the same time. The internal programming cycle is the same regardless of the number of bytes accessed.

### PAGE WRITE CHARACTERISTICS

(Vcc = 5.0V, GND = 0V, TA = -55°C to +125°C)

PAGE MODE WRITE CHARACTERISTICS Parameter	Symbol	-90		-120		-150		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time, TYP = 6ms	t <sub>wc</sub>		10		10		10	ms
Data Set-up Time	t <sub>ds</sub>	50		100		100		ns
Data Hold Time	t <sub>dH</sub>	0		10		10		ns
Write Pulse Width	t <sub>wP</sub>	100		150		150		ns
Byte Load Cycle Time	t <sub>BLC</sub>		150		150		150	µs
Write Pulse Width High	t <sub>wPH</sub>	50		50		50		ns

**FIG. 8**  
**PAGE WRITE WAVEFORMS**

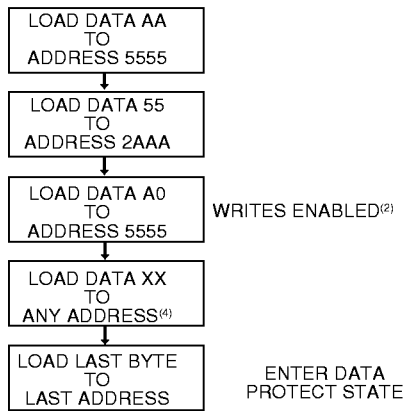


**NOTE:**

- Decoded Address Lines must be valid for the duration of the write.



**FIG. 9**  
**SOFTWARE BLOCK DATA**  
**PROTECTION ENABLE ALGORITHM<sup>(1)</sup>**

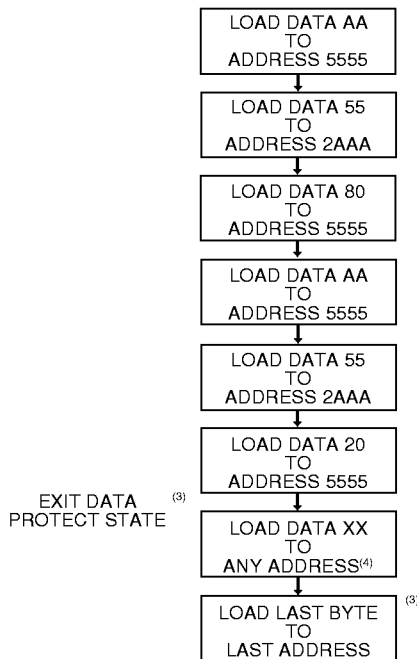


**NOTES:**

1. Data Format: D<sub>7</sub> - D<sub>0</sub> (Hex);  
Address Format: A<sub>14</sub> - A<sub>0</sub> (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 64 bytes of data may be loaded.



**FIG. 10**  
**SOFTWARE BLOCK DATA**  
**PROTECTION DISABLE ALGORITHM<sup>(1)</sup>**



**NOTES:**

1. Data Format: D7 - D0 (Hex);  
Address Format: A14 - A0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 64 bytes of data may be loaded.

**SOFTWARE DATA PROTECTION**

A software write protection feature may be enabled or disabled by the user. When shipped by White Microelectronics, the WE32K32-XXX has the feature disabled. Write access to the device is unrestricted.

To enable software write protection, the user writes three access code bytes to three special internal locations. Once write protection has been enabled, each write to the EEPROM must use the same three byte write sequence to permit writing. After setting software data protection, any attempt to write to the device without the three-byte command sequence will start the internal write timers. No data will be written to the device, however, for the duration of *t<sub>wc</sub>*. The write protection feature can be disabled by a six byte write sequence of specific data to specific locations. Power transitions will not reset the software write protection.

Each 32KByte block of the EEPROM has independent write protection. One or more blocks may be enabled and the rest disabled in any combination. The software write protection guards against inadvertent writes during power transitions, or unauthorized modification using a PROM programmer.

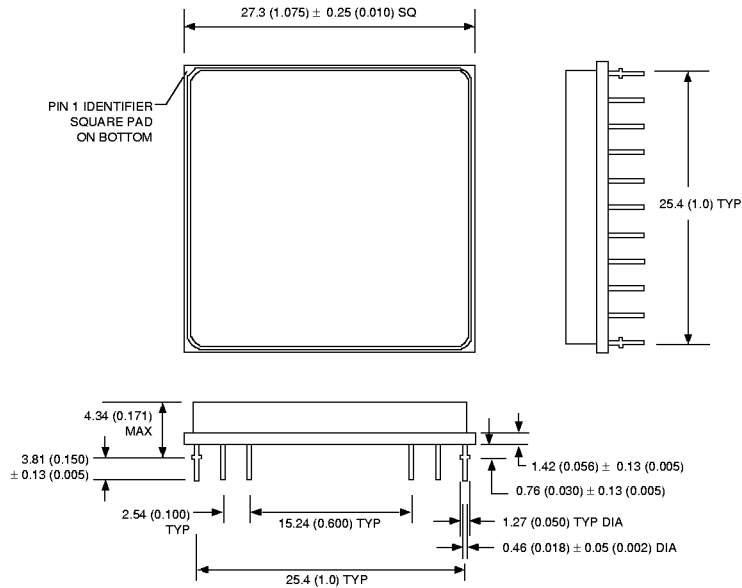
**HARDWARE DATA PROTECTION**

These features protect against inadvertent writes to the WE32K32-XXX. These are included to improve reliability during normal operation:

- a) **Vcc power on delay**  
As Vcc climbs past 3.8V typical the device will wait 5msec typical before allowing write cycles.
- b) **Vcc sense**  
While below 3.8V typical write cycles are inhibited.
- c) **Write inhibiting**  
Holding OE low and either  $\overline{CS}$  or  $\overline{WE}$  high inhibits write cycles.
- d) **Noise filter**  
Pulses of <8ns (typ) on  $\overline{WE}$  or  $\overline{CS}$  will not initiate a write cycle.



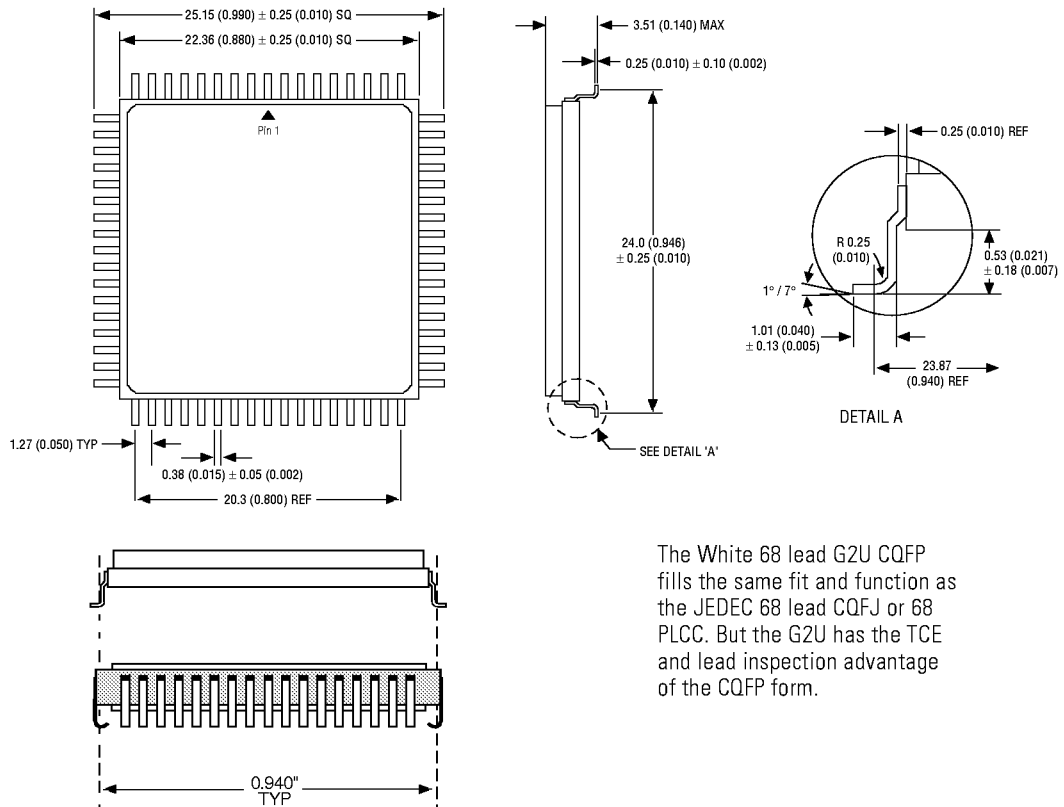
**PACKAGE 400: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H1)**



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



**PACKAGE 510: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G2U)**



The White 68 lead G2U CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2U has the TCE and lead inspection advantage of the CQFP form.

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



ORDERING INFORMATION

W E 32K32 X - XXX X X X

LEAD FINISH:

- Blank = Gold plated leads
- A = Solder dip leads

DEVICE GRADE:

- Q = MIL-STD-883 Compliant
- M = Military Screened -55°C to +125°C
- I = Industrial -40°C to +85°C
- C = Commercial 0 to +70°C

PACKAGE TYPE:

- H1 = Ceramic Hex In-line Package, HIP (Package 400)
- G2U = 22.4mm Ceramic Quad Flat Pack, CQFP Low Profile (Package 510)

ACCESS TIME (ns)

IMPROVEMENT MARK

- N = No Connect at pins 8, 21, 28, and 39 in HIP for upgrade

ORGANIZATION, 32K x 32

- User Configurable as 64Kx16 or 128Kx8

EEPROM

WHITE MICROELECTRONICS

DEVICE TYPE	SPEED	PACKAGE	SMD NO.
32K x 32 EEPROM Module	150ns	66 pin HIP (H1)	5962-94614 01HXX
32K x 32 EEPROM Module	120ns	66 pin HIP (H1)	5962-94614 02HXX
32K x 32 EEPROM Module	90ns	66 pin HIP (H1)	5962-94614 03HXX
32K x 32 EEPROM Module	150ns	68 lead CQFP/J (G2U)	5962-94614 01HZX
32K x 32 EEPROM Module	120ns	68 lead CQFP/J (G2U)	5962-94614 02HZX
32K x 32 EEPROM Module	90ns	68 lead CQFP/J (G2U)	5962-94614 03HZX