

## 80C451/83C451 I/O Expanded CMOS Microcontroller

### Product Specification

#### Military Microprocessor Products

#### DESCRIPTION

The Signetics 80C451/83C451 is an I/O expanded, single-chip microcontroller fabricated with Signetics high-density epitaxial CMOS technology. It is offered in a 68-pin LLCC and a 64-pin DIP. The Signetics CMOS technology combines the high-speed and high-density characteristics of HMOS with the low power of CMOS. Signetics epitaxial substrate minimizes latch-up sensitivity.

The 80C451/83C451 is a functional extension of the 80C31/80C51 microcontroller with three additional I/O ports and four I/O control lines. The LLCC version has a total of 68 pins. The DIP version has a total of 64 pins. The four added control lines associated with port 6 facilitate high-speed asynchronous I/O functions.

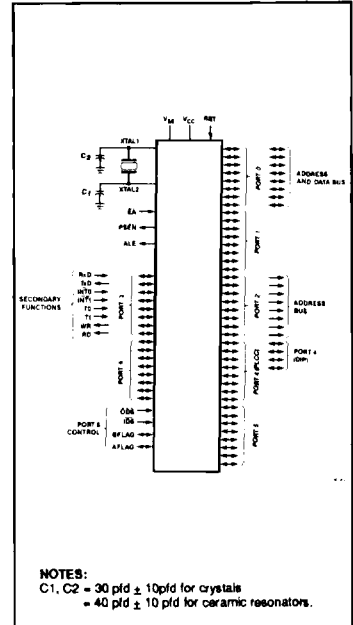
The 80C451/83C451 includes a 4k x 8 ROM; a 128 x 8 RAM; 56 (LLCC) or 52 (DIP) I/O lines; two 16-bit timer/counters; a five source, two priority level, nested interrupt structure; a serial I/O port for either a full-duplex UART, I/O expansion, or multiprocessor communications; and on-chip oscillator and clock circuits.

The 80C451/83C451 has two software selectable modes of reduced activity for further power reduction; idle mode and power-down mode. Idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning. Power-down mode freezes the oscillator, causing all other chip functions to be inoperative while maintaining the RAM contents.

#### FEATURES

- **80C451** — CPU with RAM and I/O
- **83C451** — 80C451 with mask-programmable ROM
- **68-pin LLCC and 64-pin DIP packages**
  - Seven 8-bit I/O ports (LLCC version)
  - Six 8-bit ports and one 4-bit port (DIP version)
- **Port 6 features:**
  - 8 data pins
  - 4 control pins
  - Direct MPU bus interface
  - Parallel printer interface
- **Pin compatible with 87C451 microcontroller**
- **On the microcontroller:**
  - 80C51 CPU
  - 4k x 8 ROM (83C451 only)
  - 128 x 8 RAM
  - Two 16-bit timer/counters
  - Full-duplex serial I/O
  - Two external interrupts
- **External memory addressing capability:**
  - 64k ROM and 64k RAM
- **Low power consumption:**
  - Normal operation: 24mA typical @ 5V, 12MHz
  - Idle mode: 3mA typical @ 5V, 12MHz
  - Power-down mode: 50µA typical @ 2V

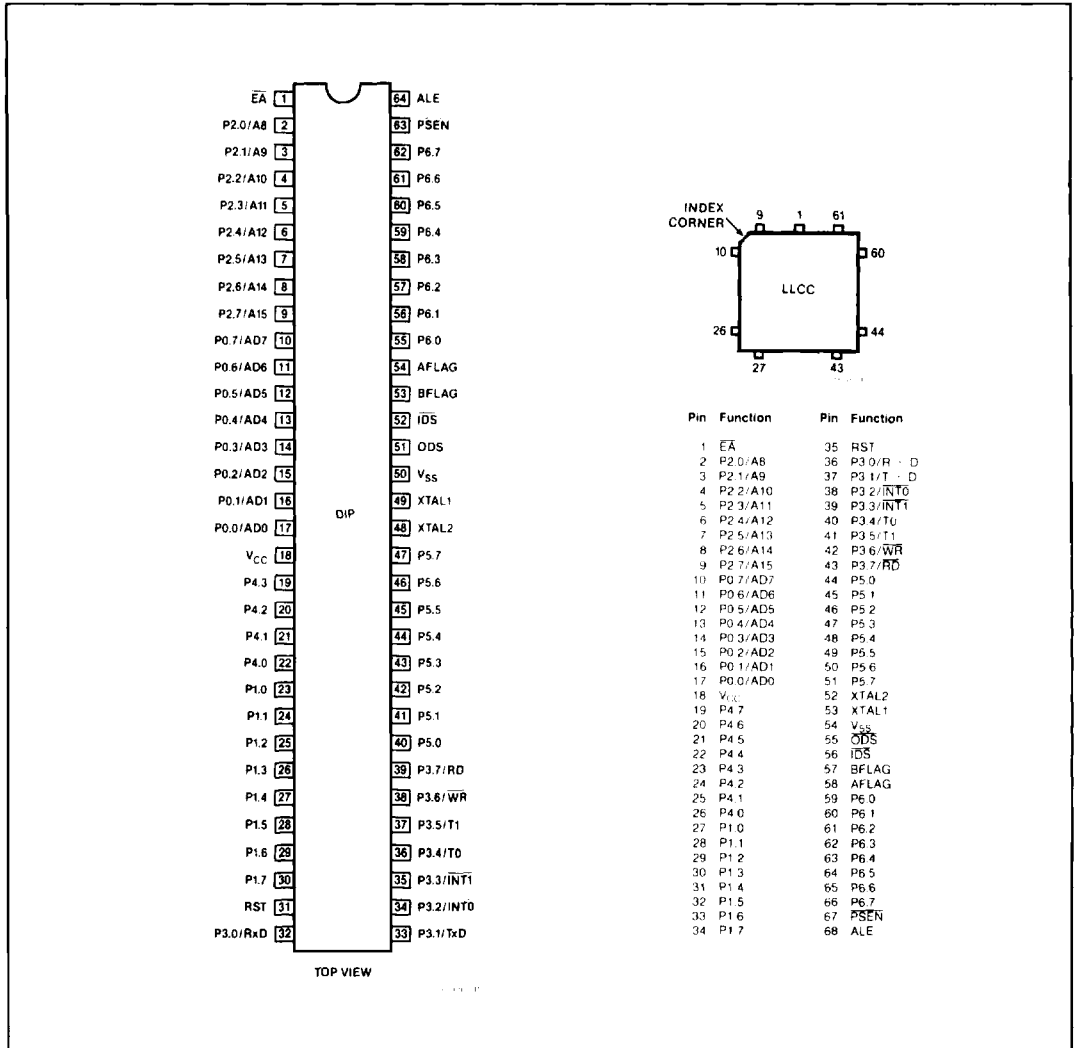
#### LOGIC SYMBOL



# I/O Expanded CMOS Microcontroller

# 80C451/83C451

## PIN CONFIGURATIONS



# I/O Expanded CMOS Microcontroller

# 80C451/83C451

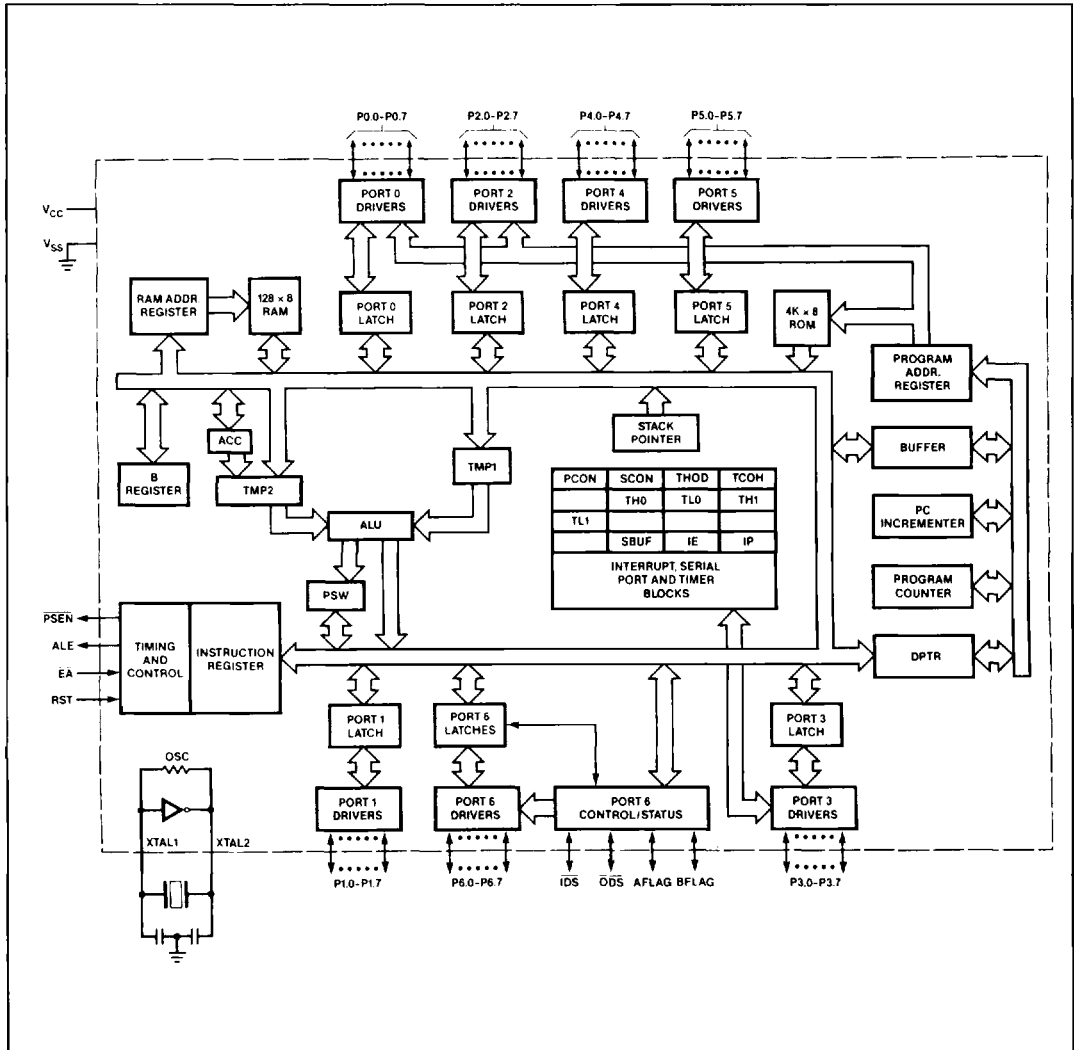
## ORDERING INFORMATION

PACKAGES	ORDER CODE	
64-Pin Ceramic DIP	80C451/BXA	83C451*/BXA
68-Pin LLCC	80C451/BUA	83C451*/BUA

### NOTES:

- \* Factory will assign a unique CVXXXX part number.

## BLOCK DIAGRAM



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PIN CONFIGURATION

MNEMONIC	PIN NUMBER			NAME AND FUNCTION
	DIP	LLCC	TYPE	
V <sub>SS</sub>	50	54		<b>Ground:</b> OV reference
V <sub>CC</sub>	18	18		<b>Power Supply:</b> +5V
P0.0-P0.7	17-10	17-10	I/O	<b>Port 0:</b> An 8-bit open drain, bidirectional I/O port. Port 0 is also the multiplexed low-order address and data bus during accesses to external memory, and outputs instruction bytes during program verification. External pull-ups are required during program verification. Port 0 can sink/source eight LS TTL inputs.
P1.0-P1.7	23-30	27-34	I/O	<b>Port 1:</b> An 8-bit bidirectional I/O port with internal pull-ups. Port 1 receives the low-order address bytes during program verification. In the 83C451, port 1 can sink/source three LS TTL inputs, and drive CMOS inputs without external pull-ups.
P2.0-P2.7	2-9	2-9	I/O	<b>Port 2:</b> An 8-bit bidirectional I/O port with internal pull-ups. Port 2 emits the high-order address bytes during accesses to external memory and receives the high-order address bit and control signals during program verification in the 83C451. Port 2 can sink/source three LS TTL inputs and drive CMOS inputs without external pull-ups.
P3.0-P3.7	32-39	36-43	I/O	<b>Port 3:</b> An 8-bit bidirectional I/O port with internal pull-ups. Port 3 can sink/source three LS TTL inputs and drive CMOS inputs without external pull-ups. Port 3 also serves the 83C451 special functions listed below: RXD (P3.0): Serial input port TXD (P3.1): Serial output port INTO (P3.2): External interrupt 0 INTT (P3.3): External interrupt 1 T0 (P3.4): Timer 0 external input T1 (P3.5): Timer 1 external input WR (P3.6): External data memory write strobe RD (P3.7): External data memory read strobe
P4.0-P4.3	22-19		I/O	<b>Port 4:</b> A 4- or 8-bit bidirectional I/O port with internal pull-ups. Port 4 can sink/source three LS TTL inputs and drive CMOS inputs without external pull-ups.
P4.0-P4.7		26-19	I/O	
P5.0-P5.7	40-47	44-51	I/O	<b>Port 5:</b> An 8-bit I/O port with internal pull-ups. Port 5 can sink/source three LS TTL inputs and drive CMOS inputs without external pull-ups.
P6.0-P6.7	55-62	59-66	I/O	<b>Port 6:</b> A specialized 8-bit bidirectional I/O port with internal pull-ups. This special port can sink/source three LS TTL inputs and drive CMOS inputs without external pull-ups. Port 6 can be used in a strobed or non-strobed mode of operation, and in conjunction with four control pins that serve the functions listed below. <b>Port 6 Control Lines:</b> ODS: Output data strobe IDS: Input data strobe BFLAG: A bidirectional I/O pin with internal pull-ups A FLAG: A bidirectional I/O pin with internal pull-ups
ODS	51	55	I	
IDS	52	56	I	
BFLAG	53	57	I/O	
AFLAG	54	58	I/O	
RST	31	35	I	<b>RESET:</b> A High level on this pin for two machine cycles while the oscillator is running resets the device. An internal pull-down resistor permits power-on reset using only a capacitor connected to the V <sub>CC</sub> .
ALE	64	68	O	<b>Address Latch Enable:</b> An output for latching the Low byte of the address during accesses to external memory. ALE is activated at a constant rate of 1/6 the oscillator frequency except during an external data memory access, at which time one ALE is skipped. ALE can sink/source eight LS TTL inputs and drive CMOS inputs without an external pull-up.
PSEN	63	67	O	<b>Program Store Enable:</b> This output is the read strobe to external program memory. PSEN is activated twice each machine cycle during fetches from external program memory; however, when executing out of external program memory, two activations of PSEN are skipped during each access to external data memory. PSEN is not activated during fetches from internal program memory. PSEN can sink/source eight LS TTL inputs and drive CMOS inputs without an external pull-up.
EA	1	1	I	<b>Instruction Execution Control:</b> When EA is held High, the CPU executes out of internal program memory, unless the program counter exceeds 0FFFH. When EA is held Low, the CPU executes out of external program memory. EA must never be allowed to float.
XTAL1	49	53	I	<b>Crystal 1:</b> An input to the inverting amplifier that forms the oscillator. This input receives the external oscillator when an external oscillator is used.
XTAL2	48	52	O	<b>Crystal 2:</b> Output of the inverting amplifier that forms the oscillator. This pin should be floated when an external oscillator is used.

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### ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

SYMBOL	PARAMETER	RATING	UNIT
T <sub>STG</sub>	Storage temperature range	-65 to +150	°C
V <sub>CC</sub>	Voltage from V <sub>CC</sub> to V <sub>SS</sub> <sup>2</sup>	-0.5 to +6.5	V
V <sub>I</sub>	Voltage from any pin to V <sub>SS</sub> <sup>2</sup>	-0.5 to V <sub>CC</sub> +0.5	V
PD	Power dissipation	200	mW

### DC ELECTRICAL CHARACTERISTICS T<sub>A</sub> = -55°C to +125°C, V<sub>CC</sub> = 5V ± 20%, V<sub>SS</sub> = 0V.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
V <sub>IL</sub>	Input Low voltage, except EA		-0.5	0.2 V <sub>CC</sub> - 0.1	V
V <sub>IL1</sub>	Input Low voltage, EA		-0.5	0.2 V <sub>CC</sub> - 0.3	V
V <sub>IH</sub>	Input High voltage, except XTAL1, RST		0.2 V <sub>CC</sub> + 0.9	V <sub>CC</sub> + 0.5	V
V <sub>IH1</sub>	Input High voltage, XTAL1, RST		0.7 V <sub>CC</sub>	V <sub>CC</sub> + .05	V
V <sub>OL</sub>	Output Low voltage, ports 1,2,3,4,5,6, AFLAG, BFLAG	I <sub>OL</sub> = 1.6mA <sup>4</sup>		0.45	V
V <sub>OL1</sub>	Output Low voltage, port 0, ALE, PSEN	I <sub>OL</sub> = 3.2mA <sup>4</sup>		0.45	V
V <sub>OH</sub>	Output High voltage, ports 1,2,3,4,5,6, AFLAG, BFLAG	V <sub>CC</sub> = 5V ± 10% I <sub>OH</sub> = -60µA	2.4		V
		I <sub>OH</sub> = -25µA	0.75V <sub>CC</sub>		V
		I <sub>OH</sub> = -10µA	0.9V <sub>CC</sub>		V
V <sub>OH1</sub>	Output High voltage, port 0 in external bus mode, ALE, PSEN	V <sub>CC</sub> = 5V ± 10% I <sub>OH</sub> = -400µA	2.4		V
		I <sub>OH</sub> = -150µA	0.75V <sub>CC</sub>		V
		I <sub>OH</sub> = -40µA <sup>5</sup>	0.9V <sub>CC</sub>		V
I <sub>IL</sub>	Logical 0 input current, ports 1,2,3,4,5,6, AFLAG, BFLAG	V <sub>IN</sub> = 0.45V		-50	µA
I <sub>TL</sub>	Logical 1 to 0 transition current, ports 1,2,3,4,5,6, AFLAG, BFLAG	V <sub>IN</sub> = 2V		-650	µA
I <sub>LI</sub>	Input leakage, current port 0, EA, TDS, ODS	0.45V ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>		±10	µA
R <sub>RST</sub>	Reset pulldown resistor		50	150	kΩ
C <sub>IO</sub>	Pin capacitance <sup>9</sup>	Test freq = 1MHz, T <sub>A</sub> = 25°C		10	pF
I <sub>PD</sub>	Power-down current	V <sub>CC</sub> = 2V to 6V <sup>6</sup>		50	µA

### MAXIMUM I<sub>CC</sub> (mA)

FREQUENCY/SUPPLY VOLTAGE	OPERATING <sup>7</sup>			IDLE <sup>8</sup>			UNITS
	4V	5V	6V	4V	5V	6V	
3.5MHz <sup>10</sup>	5.0	7.0	9.0	1.5	2.5	3.5	mA
8.0MHz <sup>10</sup>	11.0	14.5	18.0	2.0	3.5	4.5	mA
12MHz	15.0	20.0	25.0	2.5	4.0	5.0	mA

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**AC ELECTRICAL CHARACTERISTICS**  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V_{CC} = 5V \pm 20\%$ ,  $V_{SS} = 0V$ , load capacitance for port 0, ALE, and PSEN = 100pF, load capacitance for all other outputs = 80 pF<sup>3</sup>

SYMBOL	PARAMETER	12MHz CLOCK		VARIABLE CLOCK ( $f = 1/t_{CLCL}$ )		UNIT
		Min	Max	Min	Max	
$1/t_{CLCL}$	Speed range (see ordering code)					
	0			3.5	12	MHz
	1			3.5	16	
2			0.5	12		
$t_{LHLL}$	ALE pulse width	127		$2t_{CLCL}-40$		ns
$t_{AVLL}$	Address valid to ALE Low	28		$t_{CLCL}-55$		ns
$t_{LLAX}$	Address hold after ALE Low	48		$t_{CLCL}-35$		ns
$t_{LLIV}$	ALE Low to valid instr in		234		$4t_{CLCL}-100$	ns
$t_{LLPL}$	ALE Low to PSEN Low	43		$t_{CLCL}-40$		ns
$t_{PLPH}$	PSEN pulse width	205		$3t_{CLCL}-45$		ns
$t_{PLIV}$	PSEN Low to valid instr in		145		$3t_{CLCL}-105$	ns
$t_{PXIX}$	Input instr hold after PSEN	0		0		ns
$t_{PXIZ}$	Input instr float after PSEN		59		$t_{CLCL}-25$	ns
$t_{AVIV}$	Address to valid instr in		312		$5t_{CLCL}-105$	ns
$t_{PLAZ}$	PSEN Low to address float		20		20	ns
$t_{RLRH}$	RD pulse width	400		$6t_{CLCL}-100$		ns
$t_{WLWH}$	WR pulse width	400		$6t_{CLCL}-100$		ns
$t_{RLDV}$	RD Low to valid data in		252		$5t_{CLCL}-165$	ns
$t_{RHDX}$	Data hold after RD	0		0		ns
$t_{RHDX}$	Data float after RD		97		$2t_{CLCL}-70$	ns
$t_{LLDV}$	ALE Low to valid data in		517		$8t_{CLCL}-150$	ns
$t_{AVDV}$	Address to valid data in		585		$9t_{CLCL}-165$	ns
$t_{LLWL}$	ALE Low to RD or WR Low	200	300	$3t_{CLCL}-50$	$3t_{CLCL}+50$	ns
$t_{QVWX}$	Data valid to WR transition	23		$t_{CLCL}-60$		ns
$t_{WHDX}$	Data hold after WR	33		$t_{CLCL}-50$		ns
$t_{RLAZ}$	RD Low to address float		0		0	ns
$t_{WHLH}$	RD or WR High to ALE High	43	123	$t_{CLCL}-40$	$t_{CLCL}+40$	ns
<b>Port 6 Input (Input rise and fall times <math>\leq 5ns</math>)</b>						
$t_{LH}$	IDS width	270		$3t_{CLCL}+20$		ns
$t_{DVIH}$	Data setup to IDS High	10		10		ns
$t_{HDX}$	Data hold after IDS	30		30		ns
$t_{FLIL}$	PE to IDS	25		25		ns
$t_{VFFV}$	IDS to BFLAG (IBF) delay		130		130	ns
<b>Port 6 output</b>						
$t_{LOH}$	ODS width	270		$3t_{CLCL}+20$		ns
$t_{FVDV}$	SEL to data out delay		85		85	ns
$t_{OLDV}$	ODS to data out delay		80		80	ns
$t_{OHDX}$	ODS to data float delay		35		35	ns
$t_{OVFV}$	ODS to AFLAG (OBF) delay		100		100	ns
$t_{FLDV}$	PE to data out delay		120		120	ns
$t_{OHFH}$	ODS High to AFLAG (SEL) delay	100		100		ns

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**NOTES:**

1. Stress above those listed under Absolute Maximum Rating may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
2. This product includes circuitry specifically designed for the protection on its internal devices from damaging effects of excessive static charge. Nonetheless it is suggested that conventional precautions be taken to avoid applying voltages greater than the rated maximum.
3. Parameters are valid over operating temperature range unless otherwise specified.
4. Capacitive loading on ports 0 and 2 can cause spurious noise to be superimposed on the  $V_{OLs}$  of ALE and ports 1 and 3. The noise is caused by external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases it could be desirable to qualify ALE with a Schmitt trigger, or use an address latch with a Schmitt trigger STROBE input.
5. Capacitive loading on ports 0 and 2 can cause the  $V_{OH}$  on ALE and  $\overline{PSEN}$  to momentarily fall before the  $0.9V_{CC}$  specification when the address bits are stabilizing.
6. Power-down  $I_{CC}$  is measured with all output pins disconnected;  $\overline{EA}$  = port 0 =  $V_{CC}$ ; XTAL2 N.C.; RST =  $V_{SS}$ .
7.  $I_{CC}$  is measured with all output pins disconnected; XTAL1 driven with  $t_{CLCH}$ ,  $t_{CHCL}$  = 5ns,  $V_{IL}$  =  $V_{SS} + 0.5V$ ,  $V_{IH}$  =  $V_{CC} - 0.5V$ ; XTAL1 N.C.;  $\overline{EA}$  = RST = Port 0 =  $V_{CC}$ .  $I_{CC}$  will be slightly higher if a crystal oscillator is used.
8. Idle  $I_{CC}$  is measured with all output pins disconnected; XTAL1 driven with  $t_{CLCH}$ ,  $t_{CHCL}$  = 5ns,  $V_{IL}$  =  $V_{SS} + 0.5V$ ,  $V_{IH}$  =  $V_{CC} - 0.5V$ ; XTAL N.C.; port 0 =  $V_{CC}$ ;  $\overline{EA}$  = RST =  $V_{SS}$ .
9.  $C_{IO}$  is measured initially and after any design changes which may affect capacitance.
10. This parameter is guaranteed, but not tested.

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## PORTS 4 and 5

Ports 4 and 5 are bidirectional I/O ports with internal pull-ups. Port 4 is an 8-bit port (LLCC version) or a 4-bit port (DIP version). Port 4 and port 5 pins, with ones written to them, are pulled High by the internal pull-ups, and in that state can be used as inputs. Ports 4 and 5 are addressed at the special function register addresses shown in Table 1.

## PORT 6

Port 6 is a special 8-bit bidirectional I/O port with internal pull-ups. (See Figure 1.) This port can be used as a standard I/O port, or in strobed modes of operation in conjunction with four special control lines:  $\bar{O}DS$ ,  $IDS$ , AFLAG, and BFLAG. Port 6 operating modes are controlled by the port 6 control status register (CSR). Port 6 and the CSR are addressed at the special function register addresses when in Table 1. The following four control pins are used in conjunction with port 6:

**$\bar{O}DS$ :** Output data strobe input for port 6.  $\bar{O}DS$  can be programmed to control the port 6 output drivers and the output buffer full flag (OBF), or to clear only the OBF flag bit in the CSR (output-always mode).  $\bar{O}DS$  is active Low for output driver control. The OBF flag can be programmed to be cleared on the negative or positive edge of  $\bar{O}DS$ .

**$IDS$ :** Input data strobe input for port 6.  $IDS$  is used to control the port 6 input latch and input buffer full flag (IBF) bit in the CSR. The input data latch can be programmed to be

transparent when the  $IDS$  is Low and latched on the positive transition of  $IDS$ , or to latch only on the positive transition of  $IDS$ . Correspondingly, the IBF flag is set on the negative or positive transition of  $IDS$ .

**AFLAG:** A bidirectional I/O pin. AFLAG can be programmed to be an output set High or Low under program control, or to output the state of the output buffer full flag. AFLAG can also be programmed to be an input which selects whether the contents of the output buffer, or the contents of the port 6 control status register will be output on port 6. This feature grants complete port 6 status to external devices.

**BFLAG:** A bidirectional I/O pin. BFLAG can be programmed to be an output, set High or Low under program control, or to output the state of the input buffer full flag. BFLAG can also be programmed to input an enable signal for port 6. When BFLAG is used as an enable input, port 6 output drivers are in the High impedance state, and the input latch does not respond to the  $IDS$  strobe when BFLAG is High. Both features are enabled when BFLAG is Low. This feature facilitates the use of the 83C451 in bused multiprocessor systems.

control status register bits can be read and written by the CPU, except bits 0 and 1, which are read only. Reset writes ones to bits 2 through 7, and writes zeros to bits 0 and 1.

### CSR.0 — Input Buffer Full Flag (IBF) (Read only)

The IBF bit is set to a logic 1 when port 6 data is loaded into the input buffer under control of  $IDS$ . This can occur on the negative or positive edge of  $IDS$ , as determined by CSR.2. IBF is cleared when the CPU reads the input buffer register.

### CSR.1 — Output Buffer Full Flag (OBF) (Read only)

The OBF flag is set to a logic 1 when the CPU writes to the port 6 output data buffer. OBF is cleared by the positive or negative edge of  $\bar{O}DS$ , as determined by CSR.3.

### CSR.2 — $IDS$ Mode Select (IDSM)

When CSR.2 = 0, a Low-to-High transition on the  $IDS$  pin sets the IBF flag. The port 6 input buffer is loaded on the  $IDS$  positive edge. When CSR.2 = 1, a High-to-Low transition on the  $IDS$  pin sets the IBF flag. The port 6 input buffer is transparent when  $IDS$  is Low, and latched when  $IDS$  is High.

### CSR.3 — Output Buffer Full Flag Clear Mode (OBFc)

When CSR.3 = 1, the positive edge of the  $\bar{O}DS$  input clears the OBF flag. When CSR.3 = 0, the negative edge of the  $\bar{O}DS$  input clears the OBF flag.

## CONTROL STATUS REGISTER

The control status register (CSR) establishes the mode of operation for port 6 and indicates the current status of the port 6 I/O registers. All

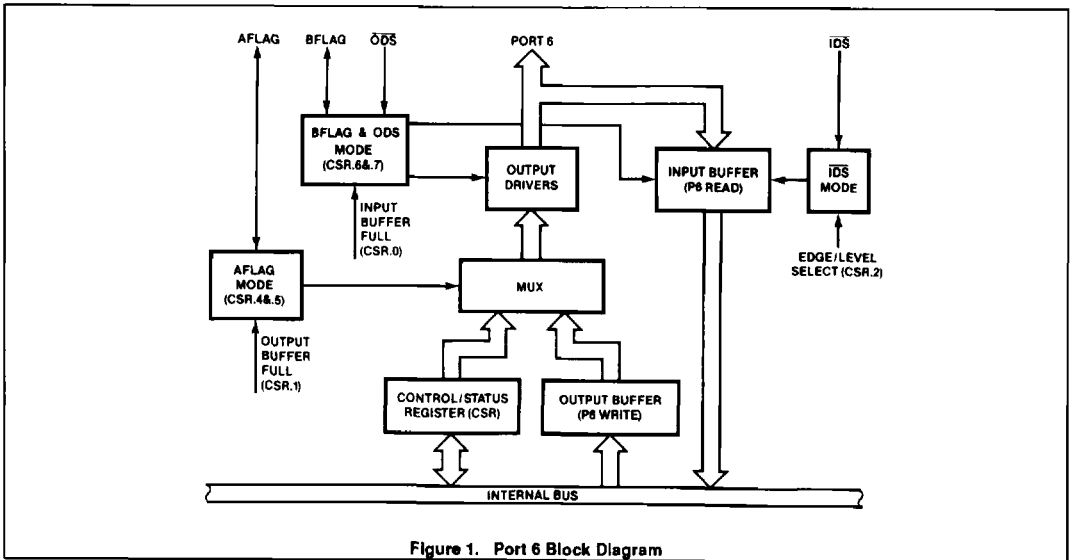


Figure 1. Port 6 Block Diagram

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### CSR.4, CSR.5 — AFLAG Mode Select (MA0, MA1)

Bits 4 and 5 select the mode of operation for the AFLAG pin, as follows:

MA1	MA0	AFLAG Function
0	0	Logic 0 output
0	1	Logic 1 output
1	0	OBF flag output (CSR.1)
1	1	Select (SEL) input mode

The select (SEL) input mode is used to determine whether the port 6 data register or the con-

trol status register is output on port 6. When the select feature is enabled, the AFLAG input controls the source of port 6 output data. A logic 0 on AFLAG input selects the port 6 data register, and a logic 1 on AFLAG input selects the control status register.

### CSR.6, CSR.7 — BFLAG Mode Select (MB0, MB1)

Bits 6 and 7 select the mode of operation for the BFLAG pin, as follows:

MB1	MB0	BFLAG Function
0	0	Logic 0 output
0	1	Logic 1 output
1	0	IBF flag output (CSR.0)
1	1	Port enable (PE)

In the port enable mode,  $\overline{IDS}$  and  $\overline{ODS}$  inputs are disabled when BFLAG input is High. When the BFLAG input is Low, the port is enabled for I/O.

## CONTROL STATUS REGISTER

(CSR)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	MB1	MB0	MA1	MA0	OBFC	IDSM	OBF	IBF
	BFLAG mode select		AFLAG mode select		Output buffer flag clear mode	Input data strobe mode	Output buffer full flag	Input buffer full flag
	0/0 = Logic 0 output* 0/1 = Logic 1 output* 1/0 = IBF output 1/1 = PE input (0 = Select) (1 = disable I/O)		0/0 = Logic 0 output 0/1 = Logic 1 output 1/0 = OBF output* 1/1 = SEL input (0 = Data) (1 = Control/status)		0 = Negative edge of $\overline{ODS}$  1 = Positive edge of $\overline{ODS}$	0 = Positive edge of $\overline{IDS}$  1 = Low level of $\overline{IDS}$	0 = Output data buffer empty 1 = Output data buffer full	0 = Input data buffer empty 1 = input data buffer full

\* Output-always mode: MB1 = 0, MA1 = 1, and MA0 = 0. In this mode port 6 is always enabled for output.  $\overline{ODS}$  only clears the OBF flag.

## SPECIAL FUNCTION REGISTER ADDRESSES

Special function register addresses for the 83C451 are identical to those of the 80C51, except for the additional registers listed in Table 1.

Table 1. Special Function Register Addresses

REGISTER ADDRESS			BIT ADDRESS								
Name	Symbol	Address	MSB	C7	C6	C5	C4	C3	C2	C1	LSB
Port 4	P4	C0		C7	C6	C5	C4	C3	C2	C1	C0
Port 5	P5	C8		CF	CE	CD	CC	CB	CA	C9	C8
Port 6 data	P6	D8		DF	DE	DD	DC	DB	DA	D9	D8
Port 6 control status	CSR	E8		EF	EE	ED	EC	EB	EA	E9	E8

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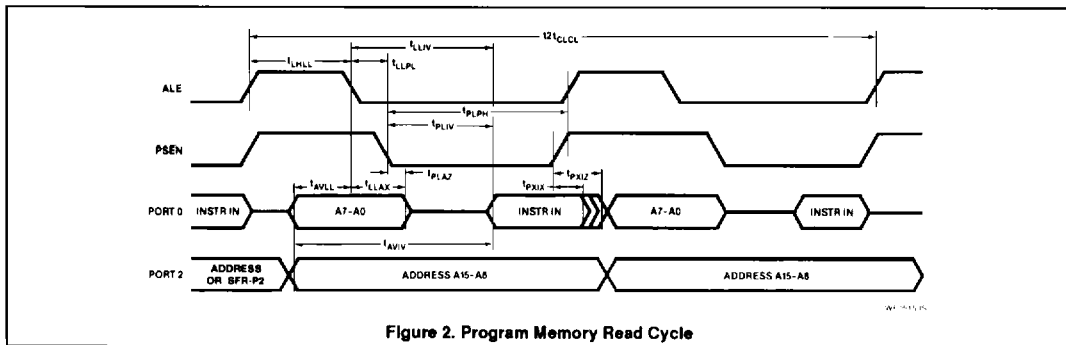


Figure 2. Program Memory Read Cycle

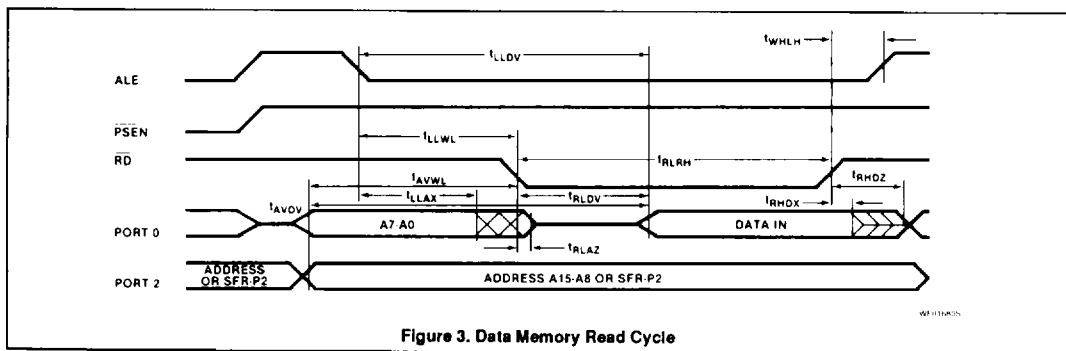


Figure 3. Data Memory Read Cycle

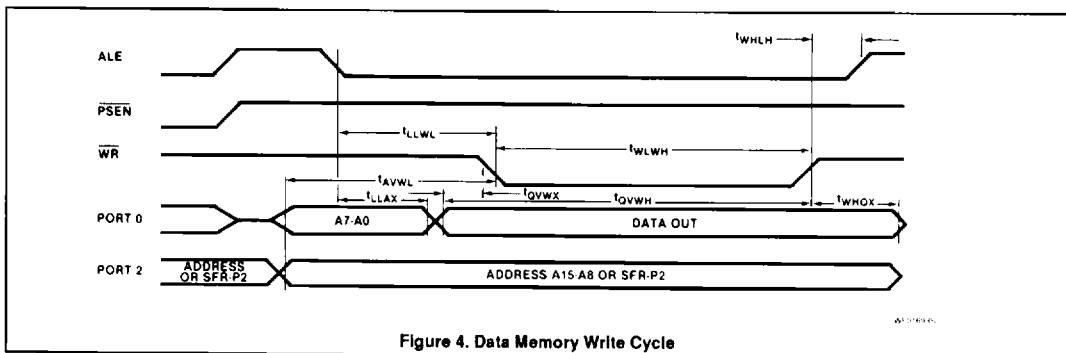


Figure 4. Data Memory Write Cycle

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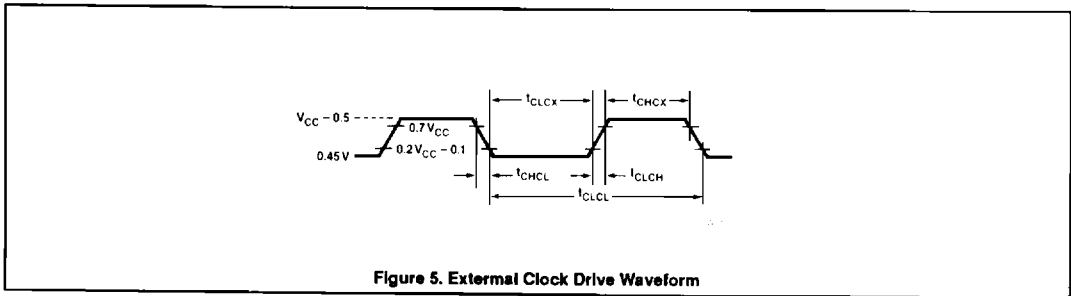


Figure 5. External Clock Drive Waveform

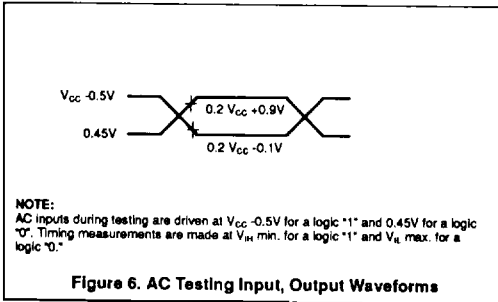


Figure 6. AC Testing Input, Output Waveforms

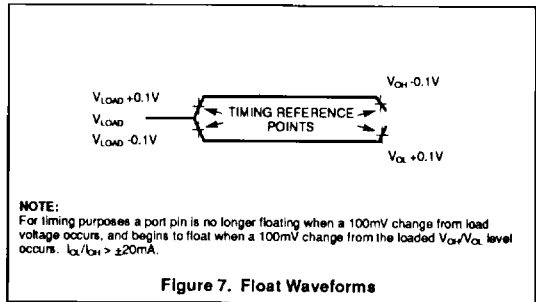


Figure 7. Float Waveforms

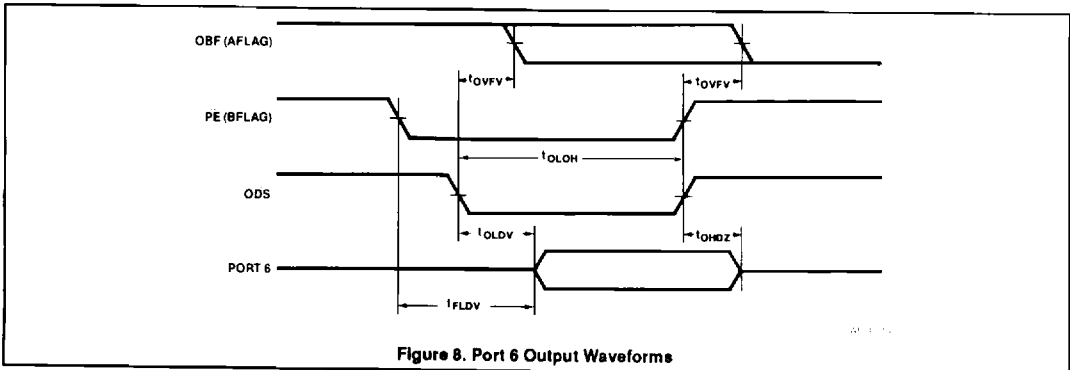


Figure 8. Port 6 Output Waveforms

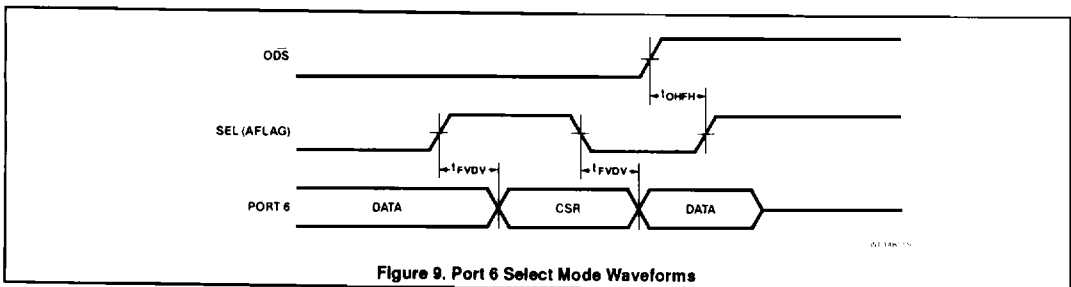


Figure 9. Port 6 Select Mode Waveforms

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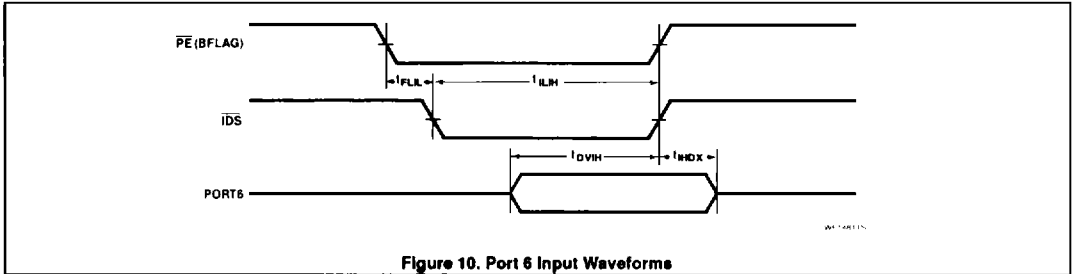


Figure 10. Port 6 Input Waveforms

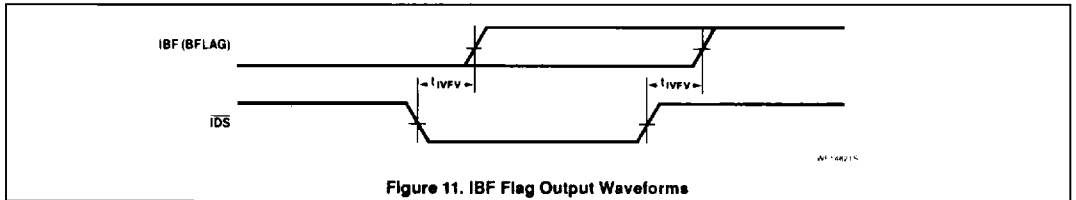
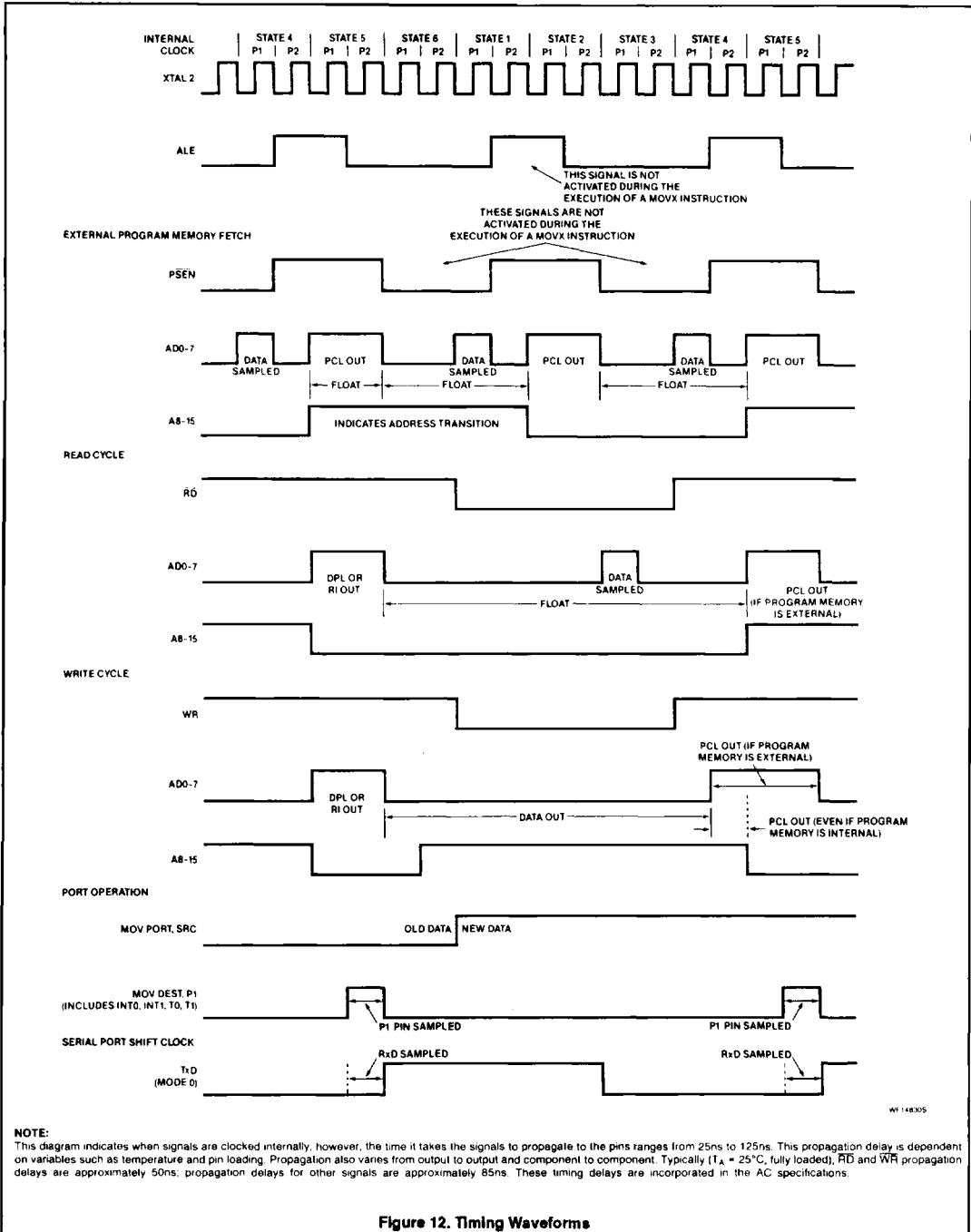


Figure 11. IBF Flag Output Waveforms

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**NOTE:** This diagram indicates when signals are clocked internally. However, the time it takes the signals to propagate to the pins ranges from 25ns to 125ns. This propagation delay is dependent on variables such as temperature and pin loading. Propagation also varies from output to output and component to component. Typically ( $T_A = 25^\circ\text{C}$ , fully loaded), RD and WR propagation delays are approximately 50ns, propagation delays for other signals are approximately 85ns. These timing delays are incorporated in the AC specifications.

Figure 12. Timing Waveforms

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Table 2. Instruction Set

MNEMONIC		DESCRIPTION	BYTE	CYCLES
<b>Arithmetic operations</b>				
ADD	A,Rn	Add register to accumulator	1	1
ADD	A,direct	Add direct byte to accumulator	2	1
ADD	A,@Ri	Add indirect RAM to accumulator	1	1
ADD	A,#data	Add immediate data to accumulator	2	1
ADDC	A,Rn	Add register to accumulator with carry	1	1
ADDC	A,direct	Add direct byte to A with carry flag	2	1
ADDC	A,@Ri	Add indirect RAM to A with carry flag	1	1
ADDC	A,#data	Add immediate data to A with carry flag	2	1
SUBB	A,Rn	Subtract register from A with borrow	1	1
SUBB	A,direct	Subtract direct byte from A with borrow	2	1
SUBB	A,@Ri	Subtract indirect RAM from A w/borrow	1	1
SUBB	A,#data	Subtract immed. data from A w/borrow	2	1
INC	A	Increment accumulator	1	1
INC	Rn	Increment register	1	1
INC	direct	Increment direct byte	2	1
INC	@Ri	Increment indirect RAM	1	1
DEC	A	Decrement accumulator	1	1
DEC	Rn	Decrement register	1	1
DEC	direct	Decrement direct byte	2	1
DEC	@Ri	Decrement indirect RAM	1	1
INC	DPTR	Increment data pointer	1	2
MUL	AB	Multiply A & B	1	4
DIV	AB	Divide A by B	1	4
DA	A	Decimal adjust accumulator	1	1
<b>Logical operations</b>				
ANL	A,Rn	AND register to accumulator	1	1
ANL	A,direct	AND direct byte to accumulator	2	1
ANL	A,@Ri	AND indirect RAM to accumulator	1	1
ANL	A,#data	AND immediate data to accumulator	2	1
ANL	direct,A	AND accumulator to direct byte	2	1
ANL	direct,#data	AND immediate data to direct byte	3	2
ORL	A,Rn	OR register to accumulator	1	1
ORL	A,direct	OR direct byte to accumulator	2	1
ORL	A,@Ri	OR indirect RAM to accumulator	1	1
ORL	A,#data	OR immediate data to accumulator	2	1
ORL	direct,A	OR accumulator to direct byte	2	1
ORL	direct,#data	OR immediate data to direct byte	3	2
XRL	A,Rn	Exclusive-OR register to accumulator	1	1
XRL	A,direct	Exclusive-OR direct byte to accumulator	2	1
XRL	A,@Ri	Exclusive-OR indirect RAM to A	1	1
XRL	A,#data	Exclusive-OR immediate data to A	2	1
XRL	direct,A	Exclusive-OR accumulator to direct byte	2	1
XRL	direct,#data	Exclusive-OR immediate data to direct	3	2
CLR	A	Clear accumulator	1	1
CPL	A	Complement accumulator	1	1
RL	A	Rotate accumulator left	1	1
RLC	A	Rotate A left through the carry flag	1	1
RR	A	Rotate accumulator right	1	1
RRC	A	Rotate A right through carry flag	1	1
SWAP	A	Swap nibbles within the accumulator	1	1
<b>Data transfer</b>				
MOV	A,Rn	Move register to accumulator	1	1
MOV	A,direct	Move direct byte to accumulator	2	1
MOV	A,@Ri	Move indirect RAM to accumulator	1	1
MOV	A,#data	Move immediate data to accumulator	2	1
MOV	Rn,A	Move accumulator to register	1	1
MOV	Rn,direct	Move direct byte to register	2	2
MOV	Rn,#data	Move immediate data to register	2	1
MOV	direct,A	Move accumulator to direct byte	2	1
MOV	direct,Rn	Move register to direct byte	2	2
MOV	direct,direct	Move direct byte to direct	3	2
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2
MOV	direct,#data	Move immediate data to direct byte	3	2
MOV	@Ri,A	Move accumulator to indirect RAM	1	1
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2

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Table 2. Instruction Set (Continued)

MNEMONIC		DESCRIPTION	BYTE	CYCLES
<b>Data transfer (continued)</b>				
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1
MOV	DPTR,#data16	Load data pointer with a 16-bit constant	3	2
MOVC	A,@A + DPTR	Move code byte relative to DPTR to A	1	2
MOVC	A,@A + PC	Move code byte relative to PC to A	1	2
MOVX	A,@Ri	Move external RAM (8-bit addr) to A	1	2
MOVX	A,@DPTR	Move external RAM (16-bit addr) to A	1	2
MOVX	@Ri,A	Move A to external RAM (8-bit addr)	1	2
MOVX	@DPTR,A	Move A to external RAM (16-bit addr)	1	2
PUSH	direct	Push direct byte onto stack	2	2
POP	direct	Pop direct byte from stack	2	2
XCH	A,Rn	Exchange register with accumulator	1	1
XCH	A,direct	Exchange direct byte with accumulator	2	1
XCH	A,@Ri	Exchange indirect RAM with A	1	1
XCHD	A,#Ri	Exchange low-order digit ind. RAM w/A	1	1
<b>Boolean variable manipulation</b>				
CLR	C	Clear carry flag	1	1
CLR	bit	Clear direct bit	2	1
SETB	C	Set carry flag	1	1
SETB	bit	Set direct bit	2	1
CPL	C	Complement carry flag	1	1
CPL	bit	Complement direct bit	2	1
ANL	c,bit	AND direct bit to carry flag	2	2
ANL	c,/bit	AND complement of direct bit to carry	2	2
ORL	c,bit	OR direct bit to carry flag	2	2
ORL	c,/bit	OR complement of direct bit to carry	2	2
MOV	C,bit	Move direct bit to carry flag	2	1
MOV	bit,C	Move carry flag to direct bit	2	2
<b>Program and machine control</b>				
ACALL	addr11	Absolute subroutine call	2	2
LCALL	addr16	Long subroutine call	3	2
RET		Return from subroutine	1	2
RETI		Return from interrupt	1	2
AJMP	addr11	Absolute jump	2	2
LJMP	addr16	Long jump	3	2
SJMP	rel	Short jump (relative addr)	2	2
JMP	@A + DPTR	Jump indirect relative to the DPTR	1	2
JZ	rel	Jump if accumulator is zero	2	2
JNZ	rel	Jump if accumulator is not zero	2	2
JC	rel	Jump if carry flag is set	2	2
JNC	rel	Jump if no carry flag	2	2
JB	bit,rel	Jump if direct bit set	3	2
JNB	bit,rel	Jump if direct bit not set	3	2
JBC	bit,rel	Jump if direct bit is set & clear bit	3	2
CJNE	A,direct,rel	Compare direct to A & jump if not equal	3	2
CJNE	A,#data,rel	Comp. immed. to A & jump if not equal	3	2
CJNE	Rn,#data,rel	Comp. immed. to reg. & jump if not equal	3	2
CJNE	@Ri,#data,rel	Comp. immed. to ind. & jump if not equal	3	2
DJNZ	Rn,rel	Decrement register & jump if not zero	2	2
DJNZ	direct,rel	Decrement direct & jump if not zero	3	2
NOP		No operation	1	1

**Notes on data addressing modes:**

- Rn —Working register R0-R7  
 direct —128 internal RAM locations, any I/O port, control or status register  
 @Ri —Indirect internal RAM location addressed by register R0 or R1  
 #data —8-bit constant included in instruction  
 #data16 —16-bit constant included as bytes 2 & 3 of instruction  
 bit —128 software flags, any I/O pin, control or status bit

**Notes on program addressing modes:**

- addr16 —Destination address for LCALL & LJMP may be anywhere within the 64-kilobyte program memory address space.  
 addr11 —Destination address for ACALL & AJMP will be within the same 2-kilobyte page of program memory as the first byte of the following instruction.  
 rel —SJMP and all conditional jumps include an 8-bit offset byte. Range is +127 – 128 bytes relative to first byte of the following instruction.

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Table 3. Instruction Opcodes in Hexadecimal Order

HEX CODE	NUMBER OF BYTES	MNEMONIC	OPERANDS	HEX CODE	NUMBER OF BYTES	MNEMONIC	OPERANDS
00	1	NOP		40	2	JC	code addr
01	2	AJMP	code addr	41	2	AJMP	code addr
02	3	LJMP	code addr	42	2	ORL	data addr,A
03	1	RR	A	43	3	ORL	data addr,#data
04	1	INC	A	44	2	ORL	A,#data
05	2	INC	data addr	45	2	ORL	A,data addr
06	1	INC	@R0	46	1	ORL	A,@R0
07	1	INC	@R1	47	1	ORL	A,@R1
08	1	INC	R0	48	1	ORL	A,R0
09	1	INC	R1	49	1	ORL	A,R1
0A	1	INC	R2	4A	1	ORL	A,R2
0B	1	INC	R3	4B	1	ORL	A,R3
0C	1	INC	R4	4C	1	ORL	A,R4
0D	1	INC	R5	4D	1	ORL	A,R5
0E	1	INC	R6	4E	1	ORL	A,R6
0F	1	INC	R7	4F	1	ORL	A,R7
10	3	JBC	bit addr, code addr	50	2	JNC	code addr
11	2	ACALL	code addr	51	2	ACALL	code addr
12	3	LCALL	code addr	52	2	ANL	data addr,A
13	1	RRC	A	53	3	ANL	data addr,#data
14	1	DEC	A	54	2	ANL	A,#data
15	2	DEC	data addr	55	2	ANL	A,data addr
16	1	DEC	@R0	56	1	ANL	A,@R0
17	1	DEC	@R1	57	1	ANL	A,@R1
18	1	DEC	R0	58	1	ANL	A,R0
19	1	DEC	R1	59	1	ANL	A,R1
1A	1	DEC	R2	5A	1	ANL	A,R2
1B	1	DEC	R3	5B	1	ANL	A,R3
1C	1	DEC	R4	5C	1	ANL	A,R4
1D	1	DEC	R5	5D	1	ANL	A,R5
1E	1	DEC	R6	5E	1	ANL	A,R6
1F	1	DEC	R7	5F	1	ANL	A,R7
20	3	JB	bit addr, code addr	60	2	JZ	code addr
21	2	AJMP	code addr	61	2	AJMP	code addr
22	1	RET		62	2	XRL	data addr,A
23	1	RL	A	63	3	XRL	data addr,#data
24	2	ADD	A,#data	64	2	XRL	A,#data
25	2	ADD	A,data addr	65	2	XRL	A,data addr
26	1	ADD	A,@R0	66	1	XRL	A,@R0
27	1	ADD	A,@R1	67	1	XRL	A,@R1
28	1	ADD	A,R0	68	1	XRL	A,R0
29	1	ADD	A,R1	69	1	XRL	A,R1
2A	1	ADD	A,R2	6A	1	XRL	A,R2
2B	1	ADD	A,R3	6B	1	XRL	A,R3
2C	1	ADD	A,R4	6C	1	XRL	A,R4
2D	1	ADD	A,R5	6D	1	XRL	A,R5
2E	1	ADD	A,R6	6E	1	XRL	A,R6
2F	1	ADD	A,R7	6F	1	XRL	A,R7
30	3	JNB	bit addr, code addr	70	2	JNZ	code addr
31	2	ACALL	code addr	71	2	ACALL	code addr
32	1	RETI		72	2	ORL	C,bit addr
33	1	RLC	A	73	1	JMP	@A + DPTR
34	2	ADDC	A,#data	74	2	MOV	A,#data
35	2	ADDC	A,data addr	75	3	MOV	data addr,#data
36	1	ADDC	A,@R0	76	2	MOV	@R0,#data
37	1	ADDC	A,@R1	77	2	MOV	@R1,#data
38	1	ADDC	A,R0	78	2	MOV	R0,#data
39	1	ADDC	A,R1	79	2	MOV	R1,#data
3A	1	ADDC	A,R2	7A	2	MOV	R2,#data
3B	1	ADDC	A,R3	7B	2	MOV	R3,#data
3C	1	ADDC	A,R4	7C	2	MOV	R4,#data
3D	1	ADDC	A,R5	7D	2	MOV	R5,#data
3E	1	ADDC	A,R6	7E	2	MOV	R6,#data
3F	1	ADDC	A,R7	7F	2	MOV	R7,#data

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Table 3. Instruction Opcodes In Hexadecimal Order (Continued)

HEX CODE	NUMBER OF BYTES	MNEMONIC	OPERANDS	HEX CODE	NUMBER OF BYTES	MNEMONIC	OPERANDS
80	2	SJMP	code addr	C0	2	PUSH	data addr
81	2	AJMP	code addr	C1	2	AJMP	code addr
82	2	ANL	C,bit addr	C2	2	CLR	bit addr
83	1	MOVC	A,@A + PC	C3	1	CLR	C
84	1	DIV	AB	C4	1	SWAP	A
85	3	MOV	data addr,data addr	C5	2	XCH	A,data addr
86	2	MOV	data addr,@R0	C6	1	XCH	A,@R0
87	2	MOV	data addr,@R1	C7	1	XCH	A,@R1
88	2	MOV	data addr,R0	C8	1	XCH	A,R0
89	2	MOV	data addr,R1	C9	1	XCH	A,R1
8A	2	MOV	data addr,R2	CA	1	XCH	A,R2
8B	2	MOV	data addr,R3	CB	1	XCH	A,R3
8C	2	MOV	data addr,R4	CC	1	XCH	A,R4
8D	2	MOV	data addr,R5	CD	1	XCH	A,R5
8E	2	MOV	data addr,R6	CE	1	XCH	A,R6
8F	2	MOV	data addr,R7	CF	1	XCH	A,R7
90	3	MOV	DPTR,#data	D0	2	POP	data addr
91	2	ACALL	code addr	D1	2	ACALL	code addr
92	2	MOV	bit addr,C	D2	2	SETB	bit addr
93	1	MOVC	A,@A + DPTR	D3	1	SETB	C
94	2	SUBB	A,#data	D4	1	DA	A
95	2	SUBB	A,data addr	D5	3	DJNZ	data addr,code addr
96	1	SUBB	A,@R0	D6	1	XCHD	A,@R0
97	1	SUBB	A,@R1	D7	1	XCHD	A,@R1
98	1	SUBB	A,R0	D8	2	DJNZ	R0,code addr
99	1	SUBB	A,R1	D9	2	DJNZ	R1,code addr
9A	1	SUBB	A,R2	DA	2	DJNZ	R2,code addr
9B	1	SUBB	A,R3	DB	2	DJNZ	R3,code addr
9C	1	SUBB	A,R4	DC	2	DJNZ	R4,code addr
9D	1	SUBB	A,R5	DD	2	DJNZ	R5,code addr
9E	1	SUBB	A,R6	DE	2	DJNZ	R6,code addr
9F	1	SUBB	A,R7	DF	2	DJNZ	R7,code addr
A0	2	ORL	C,/bit addr	E0	1	MOVX	A,@ DPTR
A1	2	AJMP	code addr	E1	2	AJMP	code addr
A2	2	MOV	C,bit addr	E2	1	MOVX	A,@R0
A3	1	INC	DPTR	E3	1	MOVX	A,@R1
A4	1	MUL	AB	E4	1	CLR	A
A5		reserved		E5	2	MOV	A,data addr
A6	2	MOV	@R0,data addr	E6	1	MOV	A,@R0
A7	2	MOV	@R1,data addr	E7	1	MOV	A,@R1
A8	2	MOV	R0,data addr	E8	1	MOV	A,R0
A9	2	MOV	R1,data addr	E9	1	MOV	A,R1
AA	2	MOV	R2,data addr	EA	1	MOV	A,R2
AB	2	MOV	R3,data addr	EB	1	MOV	A,R3
AC	2	MOV	R4,data addr	EC	1	MOV	A,R4
AD	2	MOV	R5,data addr	ED	1	MOV	A,R5
AE	2	MOV	R6,data addr	EE	1	MOV	A,R6
AF	2	MOV	R7,data addr	EF	1	MOVX	A,R7
B0	2	ANL	C,/bit addr	F0	1	MOVX	@ DPTR,A
B1	2	ACALL	code addr	F1	2	ACALL	code addr
B2	2	CPL	bit addr	F2	1	MOVX	@R0,A
B3	1	CPL	C	F3	1	MOVX	@R1,A
B4	3	CJNE	A,#data,code addr	F4	1	CPL	A
B5	3	CJNE	A,data addr,code addr	F5	2	MOV	data addr,A
B6	3	CJNE	@R0,#data,code addr	F6	1	MOV	@R0,A
B7	3	CJNE	@R1,#data,code addr	F7	1	MOV	@R1,A
B8	3	CJNE	R0,#data,code addr	F8	1	MOV	R0,A
B9	3	CJNE	R1,#data,code addr	F9	1	MOV	R1,A
BA	3	CJNE	R2,#data,code addr	FA	1	MOV	R2,A
BB	3	CJNE	R3,#data,code addr	FB	1	MOV	R3,A
BC	3	CJNE	R4,#data,code addr	FC	1	MOV	R4,A
BD	3	CJNE	R5,#data,code addr	FD	1	MOV	R5,A
BE	3	CJNE	R6,#data,code addr	FE	1	MOV	R6,A
BF	3	CJNE	R7,#data,code addr	FF	1	MOV	R7,A