SONET/SDH/ATM OC-12 CLOCK RECOVERING TRANSCEIVER

PRELIMINARY INFORMATION
SY69712

FEATURES

- **A complete SONET/SDH Transmitter & Receiver**
- **Complies with Bellcore, CCITT and ANSI Specifications**
- **Two on-chip PLLs: One for clock generation & another for clock recovery**
- **SONET 622.08Mbit/sec data rates (OC-12)**
- **Reference frequency of 19.44MHz or 51.84MHz**
- **Compatible with optic modules with and without on-board clock recovery**
- **TTL/CMOS-compatible Parallel I/O**
- **Differential PECL high-speed Serial I/O**
- **Single +5 volt power supply**
- **Lock Detect & Frame Detect output**
- **Compact 100-pin PowerQuad2 package**
- **Typical power dissipation of only 2.9 watts**
- **Seamless operation with PMC-Sierra's PM5355 S/UNI-622**

DESCRIPTION

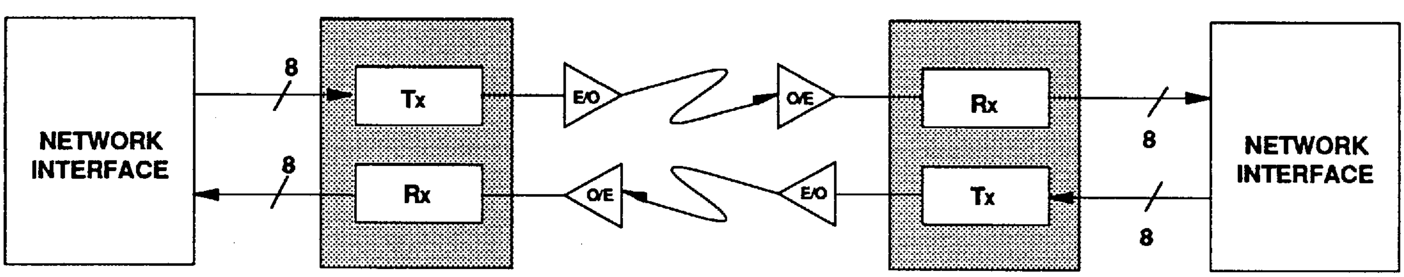
Synergy's SY69712 Transceiver with integrated clock recovery contains a fully-integrated serialization/deserialization SONET OC-12 (622.08 Mbit/s) interface circuit. This device performs all necessary serial-to-parallel and parallel-to-serial conversions per SONET and SDH standards. The SY69712 is ideally suited for SONET -based ATM applications, and is fabricated in Synergy's proprietary ASSET bipolar process.

On-chip clock generation is performed by a low-jitter phase-locked loop (PLL), allowing use of the 19.44MHz or 51.84MHz clock as a reference. Clock recovery is performed by synchronizing the on-chip VCO directly to the incoming data stream. The SY69712 can also perform SONET/SDH frame detection and alignment on the input data stream.

Compliance with the bit-error rate requirements of the Bellcore, CCITT and ANSI standards is ensured by Synergy's advanced PLL technology and Positive-ECL (PECL) I/O.

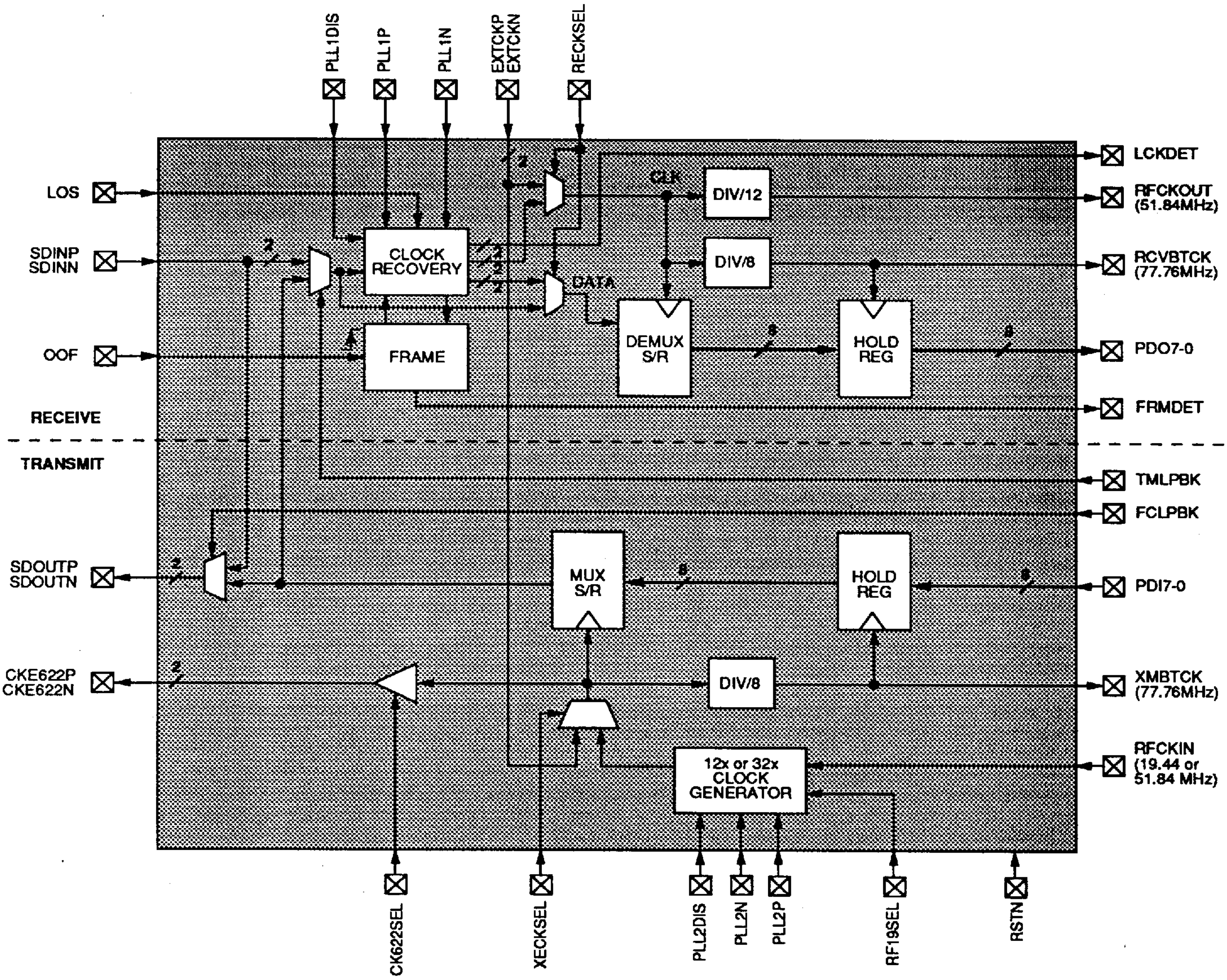
Synergy's circuit design techniques coupled with ASSET technology result in not only ultra-fast performance, but allow device operation at lower power dissipation than similar competing products. Outstanding reliability is achieved in volume production.

BLOCK DIAGRAM

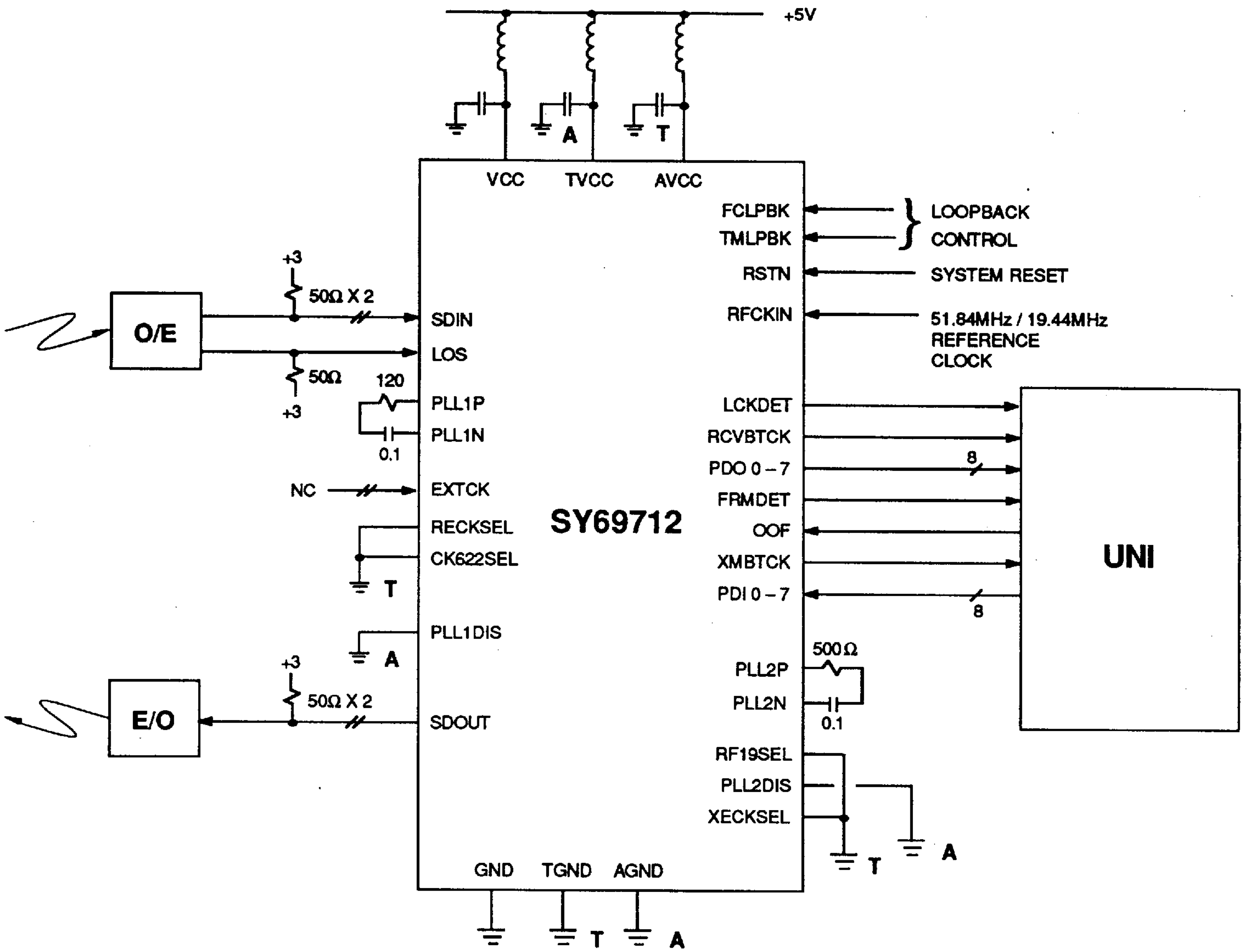


Rev.: H Amendment:/1
Issue Date: January, 1996

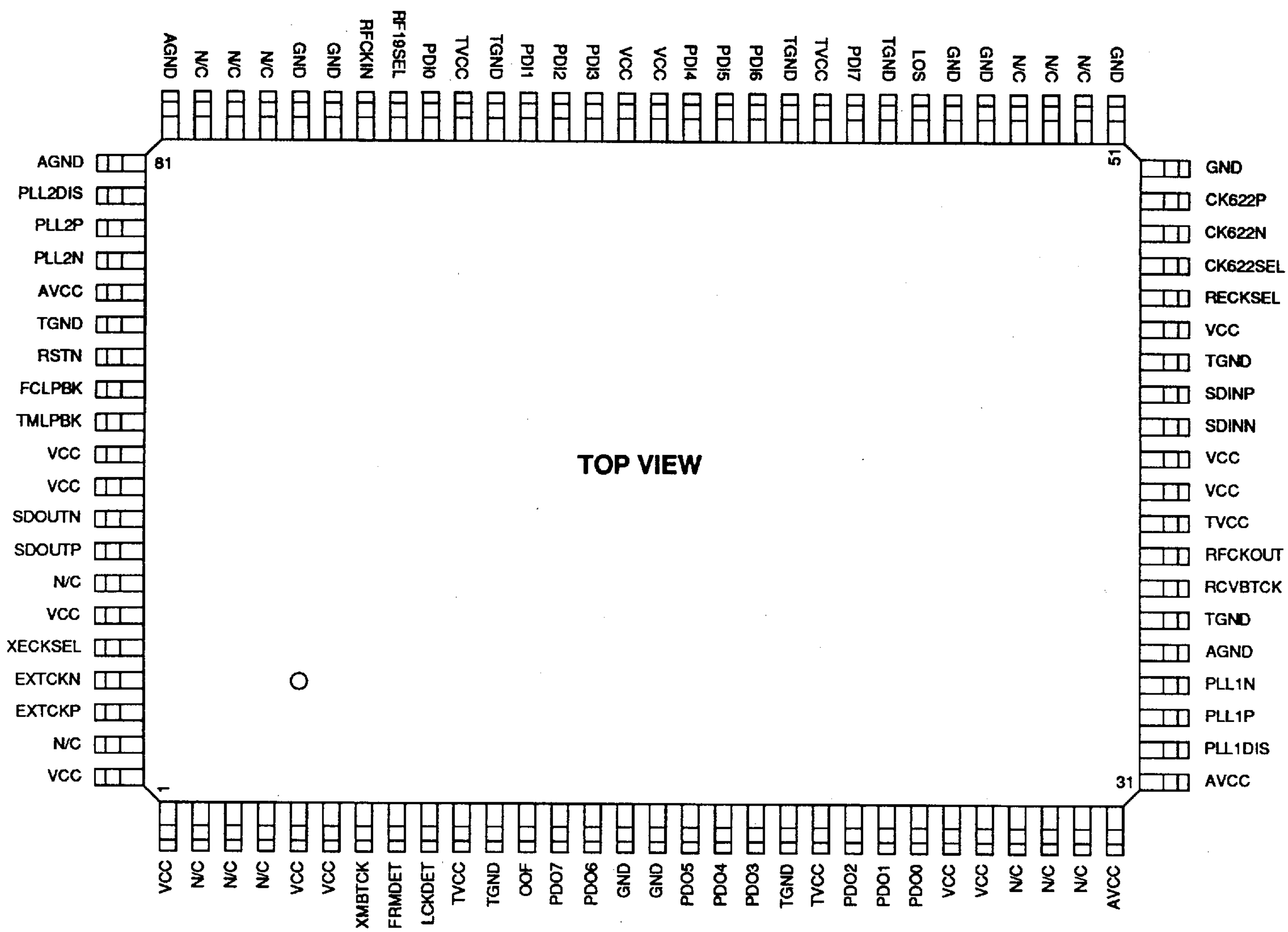
FUNCTIONAL BLOCK DIAGRAM



SYSTEM CONNECTION DIAGRAM



PINOUT



PIN NAMES

INPUTS

SDINP, SDINN [Serial Data Input] Differential PECL.
These pins are normally connected to the optical receiver module. Clock is recovered from the transitions on the SDINP and SDINN inputs.

PDI7-0 [Parallel Data Input] TTL.
A 77.76 Mbyte/s word aligned to the XMBTCLK transmit byte clock. PDI7 is the most significant bit (corresponding to bit 1 of each PCM word, the first bit transmitted). PDI7-0 is sampled on the rising edge of XMBTCK.

OOF [Out Of Frame Input] TTL.
Signal used to enable/disable the framing pattern detection logic. The framing pattern detection logic is enabled on the rising edge of OOF and remains enabled until frame boundary is detected or when OOF is set low. OOF is an asynchronous signal with a minimum pulse width of one RCVBTCK period.

RFCKIN [Reference Clock Input] TTL.
Input normally used to generate the XMBTCK. This signal is also used to generate the 'training' frequency for the clock recovery circuit to keep it centered at 622.08 MHz in the absence of data coming in on the SDIN, /SDIN inputs. The RFCKIN can be either 19.44MHz or 51.84MHz and can be selected with RF19SEL.

RF19SEL [Reference Clock Select Input] TTL.
Signal used to select the RFCKIN frequency. A high (>2.4V) selects 19.44MHz as the Reference Clock and a low (<0.8V) selects 51.84MHz as the Reference Clock. A 51.84MHz referenced clock should be used in SONET applications.

PIN NAMES (contd.)

LOS [Loss of Signal] PECL.
A single-ended active high input to be driven by the external optical receiver module to indicate a loss of received optical power. When LOS is high, the data on the Serial Data Input (SDINP, SDINP) pins will be internally forced to a constant low (zero), LCKDET forced low, and the clock recovery PLL forced to lock to the 622.08MHz clock generated from the RFCKIN. When LOS is low, data on the SDINP, SDINN pins will be processed normally.

TMLPBK [Terminal Loopback] TTL.
Selects terminal loopback diagnostic mode. When TMLPBK is low, the parallel data presented on PDI7-0 is looped back via the serial receive side and presented back on the PD7-0 along with the recovered clock. Should be HIGH (>2.4V) for normal operation.

FCLPBK [Facility Loopback] TTL.
Selects facility loopback diagnostic mode. When FCLPBK is low, the serial data coming on the SDINP, SDINN pins is routed out via the SDOUTP, SDOUTN pins. Clock recovery on the receive side is diabled. Should be HIGH (>2.4V) for normal operation.

RSTN [Master Reset] TTL.
An active low signal that resets the device. Frame detection is disabled after master reset. RSTN must be low for 1 millisecond minimum. Should be HIGH (>2.4V) for normal operation.

PLL1N, PLL1P [Loop Filter 1]
Loop filter pins for the clock recovery PLL.

PLL2N, PLL2P [Loop Filter 2]
Loop filter pins for the clock synthesis PLL.

PLL1DIS, PLL2DIS [PLL Disable]
Normally connected to AGND these inputs can be used to disable the respective PLLs for test purposes. These are active high inputs. i.e. a high (>2.4V) on PLL1DIS will disable the clock recovery PLL.

CK622SEL [622.08MHz Clock Out Select] TTL.
A high (>2.4V) on this pin will present either the synthesized or the external 622.08 MHz clock on the CKE622P and CKE622N pins. A LOW (<0.8V) disables the output & minimizes noise.

XECKSEL [Transmit External Clock Select] TTL.
A high (>2.4V) on this pin allows the EXTCKP and EXTCKN inputs to be used as the 622.08MHz transmit clock. This is tied to TGND for normal (internal clock recovery) operation.

RECKSEL [Receive External Clock Select] TTL.
A high (>2.4V) on this pin allows the EXTCKP and EXTCKN inputs to be used as recovered clock inputs. This makes it possible to use this device with optical receiver modules that provide on-board clock recovery. This is tied to TGND for normal (internal clock recovery) operation.

EXTCKP, EXTCKN [External 622.08MHz Clock Input]
Differential PECL.
These pins are normally connected to the optical receiver module that have on-board clock recovery.

OUTPUTS

SDOUTP, SDOUTN [Serial Data Output] Differential PECL.
These pins are normally connected to the optical transmitter module.

LCKDET [Lock Detect] TTL.
Active high signal indicating when the internal clock recovery PLL has locked onto the incoming data stream. LCKDET will go high if LOS is low and good data with acceptable run length and transition density is detected on the incoming data stream. LCKDET is an asynchronous output.

PDO7-0 [Parallel Data Output] TTL.
A 77.76 Mbyte/s word aligned to the RCVBTCK receive byte clock. PDO7 is the most significant bit (corresponding to bit 1 of each PCM word, the first bit transmitted). PDO7-0 is updated on the falling edge of RCVBTCK.

RFCKOUT [Reference Clock Output] TTL.
A 51.84MHz clock provided as a reference clock.

RCVBTCK [Receive Byte Clock] TTL.
A 77.76MHz clock that is aligned to the PDO7-0 parallel data output. It is nominally 50% duty cycle clock that updates PDO7-0 on the falling edge.

XMBTCK [Transmit Byte Clock] TTL.
A 77.76MHz reference clock generated from the RFCKIN. It is to be used to coordinate byte transfers for serial transmission. PDI7-0 is sampled on the rising edge of XMBTCK.

FRMDET [Frame Detect] TTL.
Indicates SONET frame boundaries in the incoming data stream (SDIN, SDIN). If the framing pattern detection is enabled, with OOF input, FRMDET pulses high for one RCVBTCK cycle when a 48-bit sequence matching the framing pattern is detected on the SDINP, SDINN inputs. FRMDET is updated on the falling edge of RCVBTCLK.

CKE622P, CKE622N [622.08 Mhz Transmit Clock Output]
Differential PECL.
These pins provide the 622.08MHz transmit clock depending on the state of the CK622SEL pin. When CK622SEL is disabled (<0.8V) the CKE622P will remain high (PECL) and CKE622N will remain low (PECL). These pins can be connected to optical transmit modules that require both data and clock inputs.

Other

Vcc	ECL +5V	**AVCC**	Analog +5V
GND	ECL Ground	**AGND**	Analog Ground
TVCC	TTL +5V	**N/C**	No Connect
TGND	TTL Ground		

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter		Rating	Unit
V_{CC}, TVCC, AVCC	Power Supply (GND, TGND, AGND = 0V)		0 to +7	VDC
V_I	Input Voltage (GND, TGND, AGND = 0V)		0 to Vcc	VDC
I_{OUT}	Output Current	Continuous	50	mA
		Surge	100	
T_A	Operating Temperature Range		0 to +75	°C
T_{STG}	Storage Temperature Range		-65 to +150	°C

Note:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS — PECL(1)

V_{CC}, TVCC, AVCC = 4.75V to 5.25V; GND, TGND, AGND = 0V

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +75°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	3.98	4.16	4.02	4.19	4.08	4.265	V
V_{OL}	Output LOW Voltage	3.05	3.37	3.05	3.37	3.05	3.4	V
V_{IH}	Input HIGH Voltage	3.83	4.16	3.87	4.19	3.93	4.265	V
V_{IL}	Input LOW Voltage	3.05	3.52	3.05	3.52	3.05	3.55	V
I_{IL}	Input LOW Current	0.5	—	0.5	—	0.3	—	µA
I_{EE}	Total Power Supply Current	—	400	—	400	—	400	mA

Note:
1. To provide adequate cooling a heatsink is recommended with this device. Please contact factory for details.

DC ELECTRICAL CHARACTERISTICS — TTL

V_{CC}, TVCC, AVCC = 4.75V to 5.25V; GND, TGND, AGND = 0V, T_A = 0°C to +75°C

Symbol	Parameter	Min.	Max.	Unit	Condition
V_{OH}	Output HIGH Voltage	2.4	—	V	I_{OH} = –2mA
V_{OL}	Output LOW Voltage	—	0.5	V	I_{OL} = 8mA
I_{OS}	Output Short Circuit Current	–150	–60	mA	V_{OUT} = Vcc
I_{EE}	Total Power Supply Current	—	400	mA	—

AC ELECTRICAL CHARACTERISTICS

Vcc, TVCC, AVCC = 4.75V to 5.25V; GND, TGND, AGND = 0V, TA = 0°C to +75°C

Parameter	Min.	Typ.	Max.	Units	Condition
VCO Center Frequency	622.08 ±12%			MHz	Nominal
Reference Clock (RFCKIN) Frequency Tolerance		±20 ±10		ppm ppm	51.84MHz 19.44MHz
Reference Clock (RFCKIN) Input Duty Cycle	45		55	% of UI	
Reference Clock (RFCKOUT) Output Duty Cycle	40		60	% of UI	15pF load
Acquisition Lock Time			15	µsec	
TTL Output Rise/Fall Time			2	ns	10% to 90% of amplitude, 15pF load
PECL Output Rise/Fall Time			500	ps	10% to 90%, 50Ω load, 5pF cap
tPDI – PDI7-0 set-up with respect to XMBTCK	1.8			ns	15pF load
tDHI – PDI7-0 hold time with respect to XMBTCK	1			ns	15pF load
tOOF – OOF pulse width	11.0			ns	
tRSD – PDO7-0 & FRMDET valid before RCVBTCK	4			ns	15pF load
tRHD – PDO7-0 & FRMDET valid after RCVBTCK	4			ns	15pF load
XMBTCK & RCVBTCK Duty Cycle	40		60	% of UI	
CKE622 Output Duty Cycle	45		55	% of UI	
tTSD – SDOUTP valid before CKE622	0.30			ns	
tTHD – SDOUTP valid after CKE622	0.30			ns	
tRST – RSTN pulse width	1			µsec	

JITTER CHARACTERISTICS

Jitter Generation Definition

Bellcore TR-NWT-000499 (Issue 4), section 7.3.3 "Jitter generation is the process whereby jitter appears at the output port of an individual unit of digital equipment in the assence of applied input jitter."

Jitter Generation Requirement

Bellcore TA-NWT-000253 (Issue 2), section 5.6.5.2 "For Category II interfaces, jitter generation shall not exceed 0.01 UI rms. For OC-N and STSX-N interfaces, a high-pass measurement filter with a 12kHz cutoff frequency shall be used." The low-pass cutoff frequency of the measurement filter shall be higher than 5MHz.

The characteristic of the measurement filter is shown below.

SONET OC-12 Category II Jitter Generation Measurement Filter Characteristics

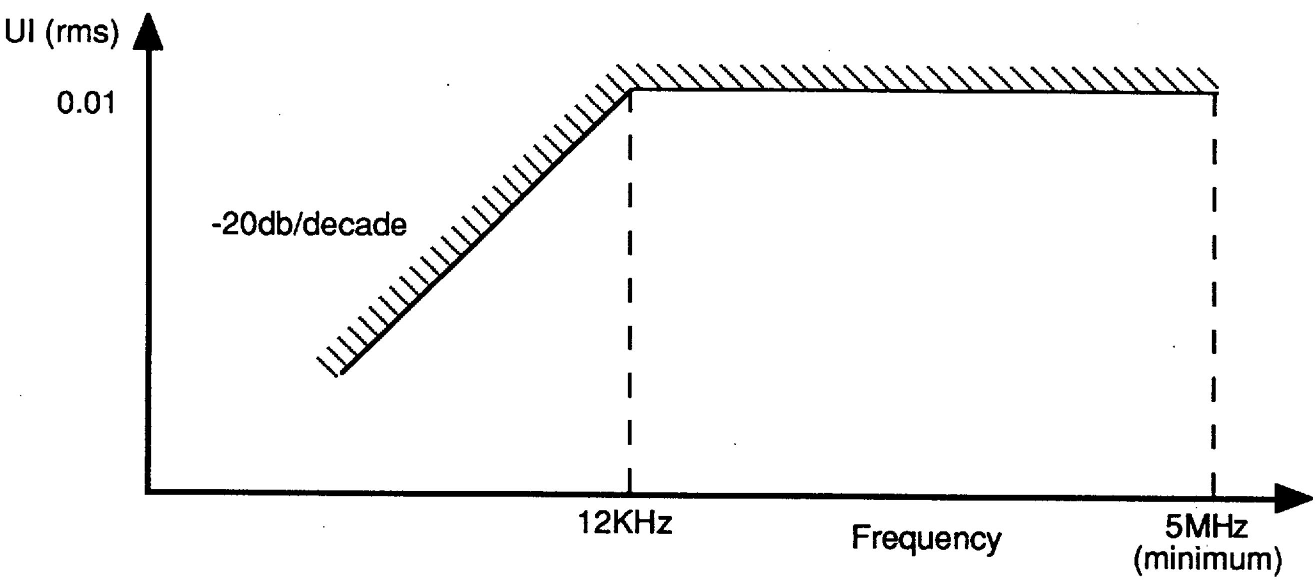


Figure 1

Jitter Generation Measurement on the SY69712

Jitter generation is measured on the CKE622 output from the device. This output is a differential ECL signal at the 622.08MHz rate that is synthesized from the reference clock input of 51.84MHz or 19.44MHz. Figure 2 shows the test setup for measuring jitter generation.

Test Setup for Measuring Jitter Generation on the SY69712

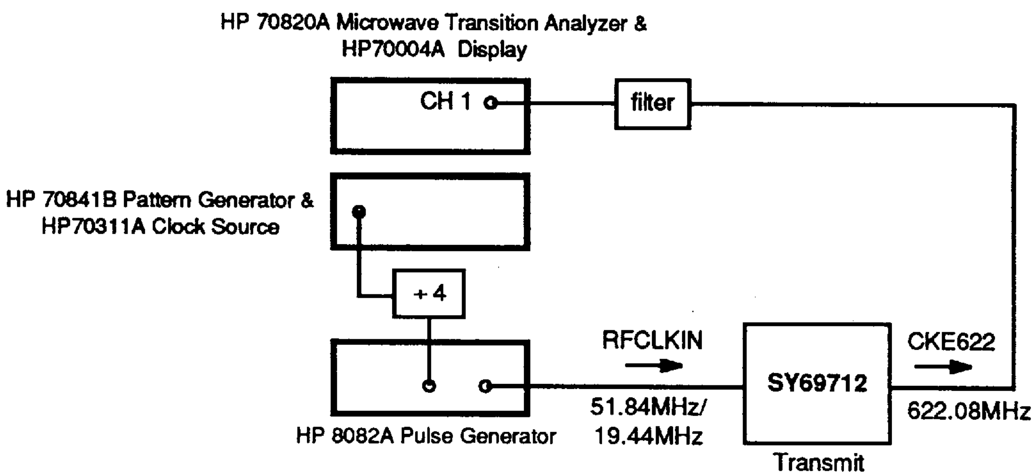


Figure 2

JITTER TRANSFER

Jitter Transfer Definition

Bellcore TR-NWT-000499 (Issue 4), section 7.3.2:
"The transfer of jitter through an individual unit of digital equipment is characterized by the relationship between the applied input jitter and the resulting output jitter as a function of frequency. For equipment in which a linear process describes the transfer of jitter from the input to the output port, the jitter transfer function is the ratio of the output jitter spectrum to the applied (deterministic) input jitter spectrum. (The term transfer function implies a linear process, where the conventional definition of linearity applies, i.e., a process that is both additive and homegeneous.)"

Jitter Transfer Requirement

Bellcore TA-NWT-000253 (Issue 2), section 5.6.3.2:
"For Category II interfaces, the jitter transfer function shall be under the curve in Figure 5-14, when input sinusoidal jitter up to the mask level in Figure 5-15 is applied, with the parameters specified in Figure 5-14 for each OC-N rate."

Figure 5-14 and 5-15 from the Bellcore specification are shown on the following page as Figures 3 and 4, respectively.

ITU/CCITT Recommendation G.958, section 6.3.2, is stated similarly to Bellcore specification

SONET OC-12 Category II Jitter Transfer Function
(after Bellcore Fig. 5-14)

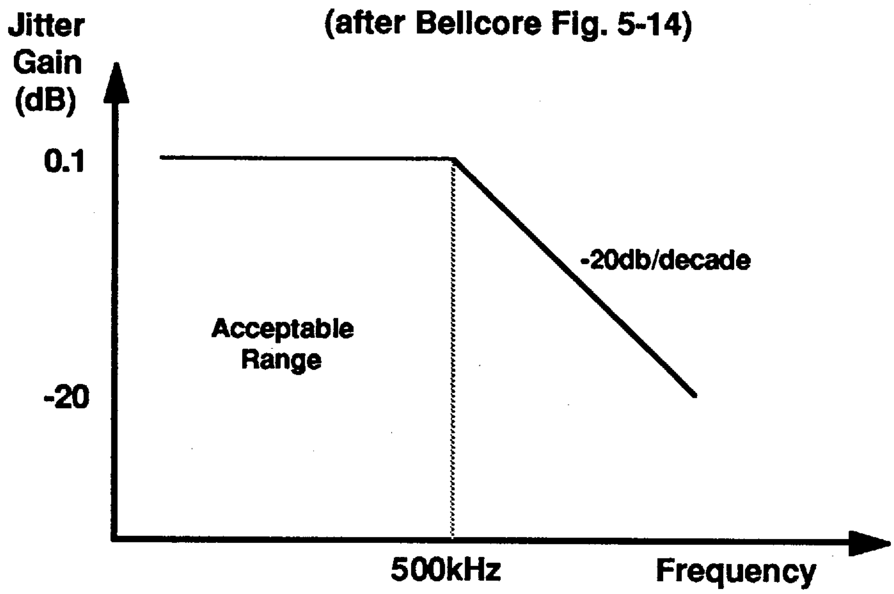


Figure 3

SONET OC-12 Category II Input Jitter Mask
for Jitter Transfer and Jitter Tolerance Measurement
(after Bellcore Fig. 5-15)

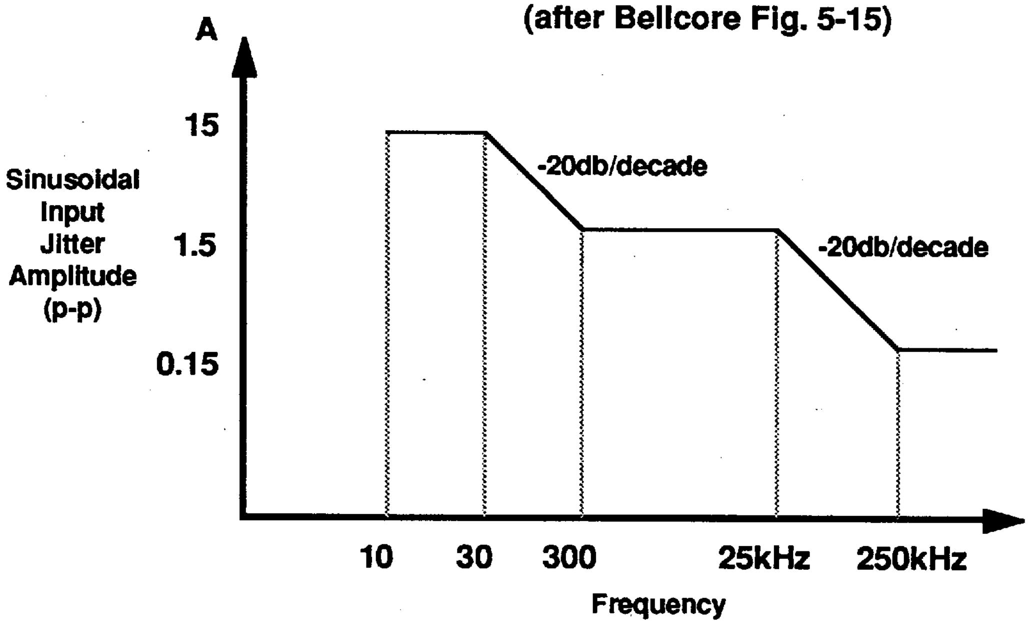


Figure 4

JITTER TOLERANCE

Jitter Tolerance Definition

Bellcore TA-NWT-000253 (Issue 2), section 5.6.4.2: "For Category II SONET interfaces, jitter tolerance is defined as the peak-to-peak amplitude of sinusoidal jitter applied on the input OC-N/STS-N signal that causes a 1-dB power penalty. This is a stress test intended to ensure that no additional penalty is incurred under operating conditions."

Jitter Tolerance Requirement

Bellcore TA-NWT-000253 (Issue 2), section 5.6.4.2: "OC-3/STS-3 and OC-12 Category II SONET interfaces shall tolerate, as a minimum, the input jitter applied according to the mask in Figure 5-15, with the parameters specified in the figure for OC-3 and OC-12, respectively.

Measuring Jitter Tolerance on the SY69712

The SY69712 differs from a simple regenerator in that it includes a parallel-to-serial interface (PISO) in the transmit section and a serial-to-parallel interface (SIPO) in the receive section. This means the jitter transfer is not measured in the conventional manner associated with a serial-in serial-out device.

For that reason, the transmit and receive sections of the same device are connected in tandem at their parallel interfaces, to provide a serial-in serial-out function for jitter tolerance measurements.

On the SY69712 jitter tolerance is measured by applying sinusoidal input jitter at the serial data input to the receive section. The receive section then recovers the data and presents it in a parallel format at the PDO 7-0 outputs. This parallel data is then fed back to the parallel data inputs of the transmit section through the PDI 7-0 inputs. Jitter tolerance is measured at the serial data out of the transmit section.

Test Setup for Measuring Jitter Tolerance on the SY69712

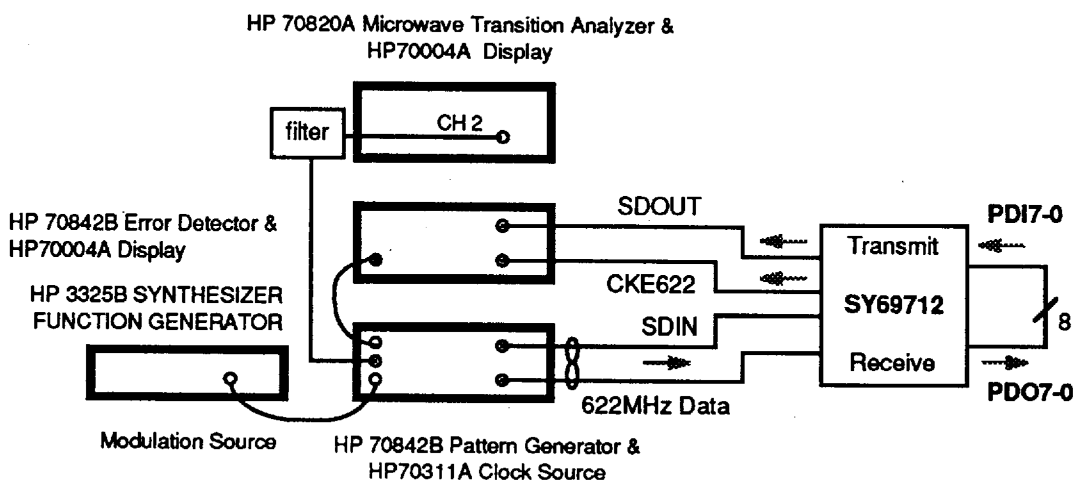


Figure 5

APPENDIX

Equipment List

HP3325B Synthesizer Function Generator

HP 70004A Display with the following modules

- Eye Diagram Analyzer
- HP 70820A Microwave Transition Analyzer with 70874B Jitter Analyzer Personality Card
- HP 0955-0732 622 Mb/s Bandpass Filter (2)

HP 70004A Display with the following modules

- HP 70842B Error Detector with 85700A 32 kbyte RAM

HP 70001A Mainframe

- HP 70841B Pattern Generator (Range 0.1 - Gbit/s)
- HP 70311A Clock Source (Range 16.1MHz - 3.3GHz)
  - 70874B Jitter Analyzer Personality Card

HP 7090A Measurement Plotting System

Tektronix 11801B Digital Sampling Oscilloscope

- SD26 Sampling Heads (4)

HP53132A 225 MHz Universal Counter with high frequency option

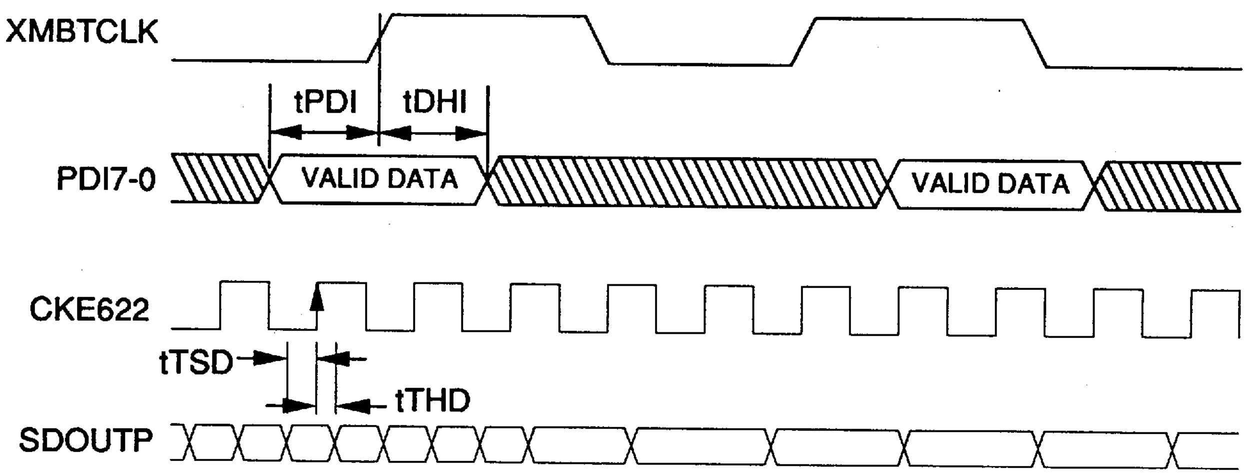
HP 8082A Pulse Generator

Synergy Semiconductor Evaluation Board Rev. C with Johnstech Socket

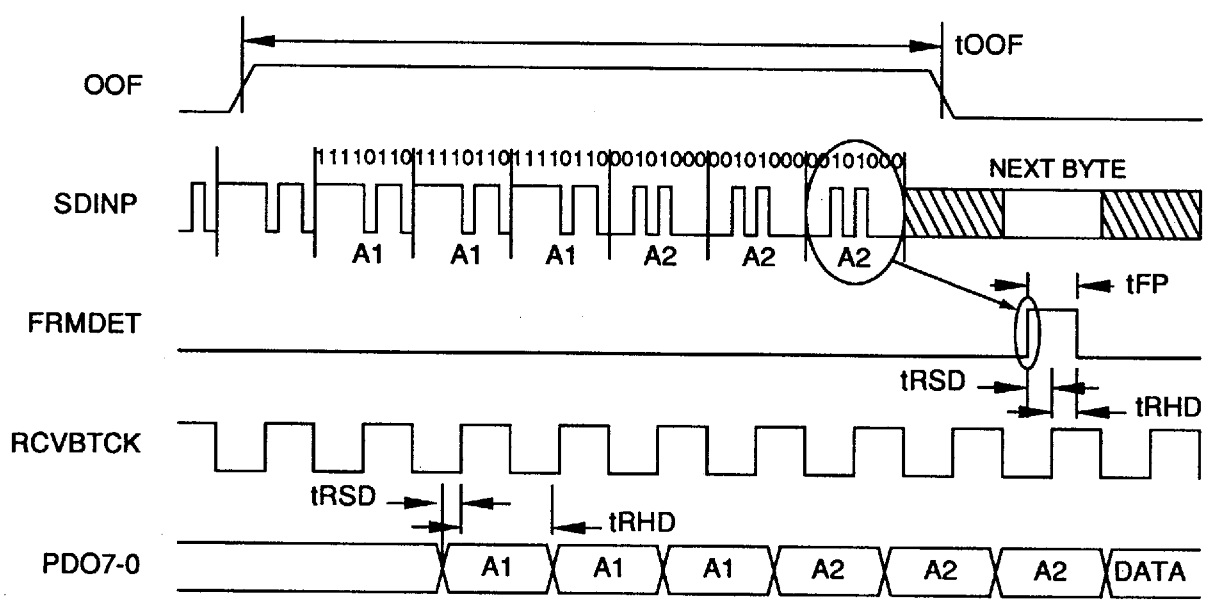
PMC PM5355 S/UNI-622 COMPATABILITY TABLE

PMC Symbol	PMC SUNI-622 Parameter	Min	Max	SY69712 Parameter	Min	Max	Units
	TRANSMIT SECTION						
	TCLK Frequency (nominally 77.76MHz)		78	XMBTCK Frequency		78	MHz
	TCLK Duty Cycle	40	60	XMBTCK Duty Cycle	48	50	%
tPFPOUT	TCLK High to FPOUT Valid	1	11	n/a (valid after 12 C1 bytes)			ns
tPPOUT	TCLK High to POUT[7:0] Valid	1	11	PDI[7:0] set-up wrt XMBTCK	2.44		ns
				PDI[7:0] hold wrt XMBTCK	–0.25		ns
tPGTOCLK	TCLK Edge to GTOCLK Edge	2	25	n/a (XMBTCK/4)			ns
	TSICLK Frequency (nominally 51.84MHz)		52	n/a (STS-1 mode)			MHz
	TSICLK Duty Cycle 33	67		n/a (STS-1 mode)			%
tPTSOUT	TSICLK High to TSOUT Valid Prop Delay	2	18	n/a (STS-1 mode)			ns
tPGTOCLK	TSICLK High to GTOCLK Valid Prop Delay	4	25	n/a (STS-1 mode)			ns
	RECEIVE SECTION						
	PICLK Frequency (nominally 77.76 MHz)		78	RCVBTCK Frequency		78	MHz
	PICLK Duty Cycle	40	60	RCVBTCK Duty Cycle	48	50	%
tSPIN	PIN[7:0] Setup-up time to PICLK	3		PDO[7:0] valid before RCVBTCK	3.8		ns
tHPIN	PIN[7:0] Hold time to PICLK	1		PDO[7:0] valid after RCVBTCK	7.5		ns
tSFPIN	FPIN Set-up time to PICLK	3		FRMDET valid before RCVBTCK	4		ns
tHFPIN	FPIN Hold time to PICLK	1		FRMDET valid after RCVBTCK	7.6		ns
tPOOF	RCVBTCK High to OOF Valid	3	30	OOF Pulse Width	11.6		
	RSICLK Frequency (nominally 51.84MHz)		52	n/a (STS-1 mode)			MHz
	RSICLK Duty Cycle	33	67	n/a (STS-1 mode)			%
tSRSIN	RSIN Set-up Time to RSICLK	5		n/a (STS-1 mode)			ns
tHRSIN	RSIN Hold Time to RSICLK	1		n/a (STS-1 mode)			ns
tPGROCLK	RSICLK High to GROCLK Valid Prop Dly	5	30	n/a (STS-1 mode)			ns

TRANSMIT TIMING WAVEFORMS



RECEIVE TIMING WAVEFORMS



NOTES:

The example shown above is for a partial OC-12 framing sequence.

SONET OVERVIEW

Synchronous Optical Network (SONET) is a standard for connecting one fiber system to another at the optical level. SONET, together with Synchronous Digital Hierarchy (SDH) administered by the CCITT, forms a single international standard for fiber interconnect between telephone networks of different countries. SONET is capable of accommodating a variety of transmission rates and applications.

The SONET standard is layered protocol with four separate layers defined as follows:

- Photonic
- Section
- Line
- Path

Figure 6 shows the layers and their functions. Each of the layers has overhead bandwidth dedicated to administration and maintenance. The photonic layer simply handles the conversion from electrical to optical and back with no overhead. It is responsible for transmitting the electrical signals in optical form over the physical media. The section layer handles the transport of the framed electrical signals across the optical cable from one end to the other. The main function of this layer are framing, scrambling, and error monitoring. The line layer is responsible for the reliable transmission of the path layer information stream carrying voice, data, and video signals. Its main functions are synchronization, multiplexing, and reliable transport. The path layer is responsible for the actual transport of services at the appropriate signal rates.

Data Rates and Signal Hierarchy

Table 1 contains the data rates and signal designations of the SONET hierarchy. The lowest level is the SONET signal referred to as the synchronous transport signal level-1 (STS-1). An STS-*N* signal is made up of *N* byte-interleaved STS-1 signals. The optical counterpart of each STS-*N* signal is an optical carrier level-*N* (OC-*N*). The SY69712 supports OC-12 rates (622.08 Mbit/s).

Frame and Byte Boundary Detection

The SONET/SDH fundamental frame format for STS-1 consists of 9 rows and 90 columns of a byte each. The first three bytes of each row are called transport overhead bytes (TOH). These are followed by 87 bytes called the Synchronous Payload Envelope (SPE) bytes. Thus the full STS-1 frame consists of 9 rows x 90 bytes/columns = 810 bytes. The STS-1 rate is specified as 8000 frames/sec with each frame containing 810 bytes. This equates to 51.840 Mbit/s (8000 frames/s x 810 bytes/frame x 8 bits/byte) or one SONET frame transmitted every 125µs. Other SONET frames can be interleaved in multiples of an STS-1 frame (STS-3, STS-12, etc.). An STS-12/OC-12 frame is shown in Figure 7.

For more details on SONET rates, format and operation, refer to the ANSI T1.105-1991 Optical Interface Rates and Formats Specifications.

Table 1. SONET Signal Hierarchy

Elec.	CCITT	Optical	Data Rate (Mbit/s)
STS-1		OC-1	51.84
STS-3	STM-1	OC-3	155.52
STS-12	STM-4	OC-12	622.08
STS-24		OC-24	1244.16
STS-48	STM-16	OC-48	2488.32

Figure 6. SONET Structure

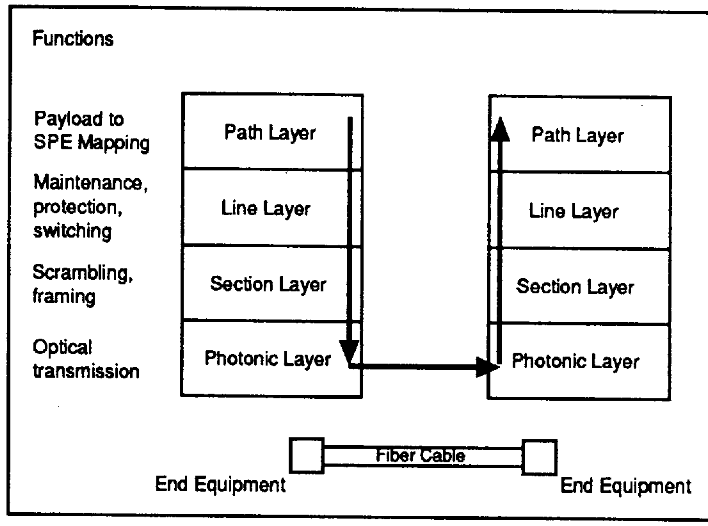
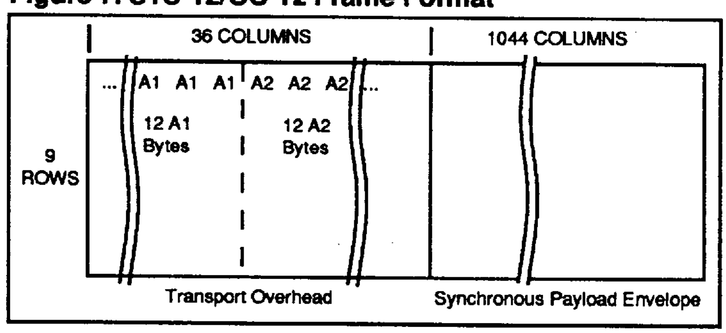


Figure 7. STS-12/OC-12 Frame Format



APPLICATION EXAMPLE

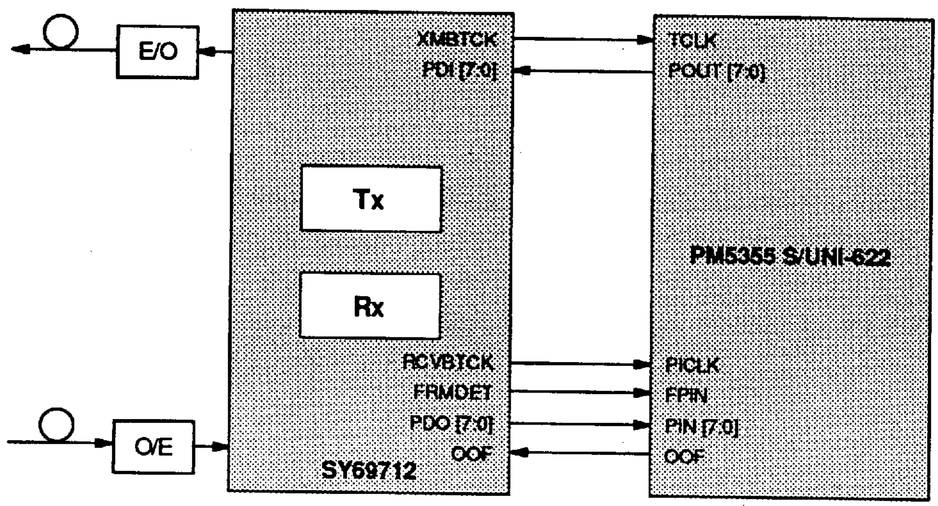
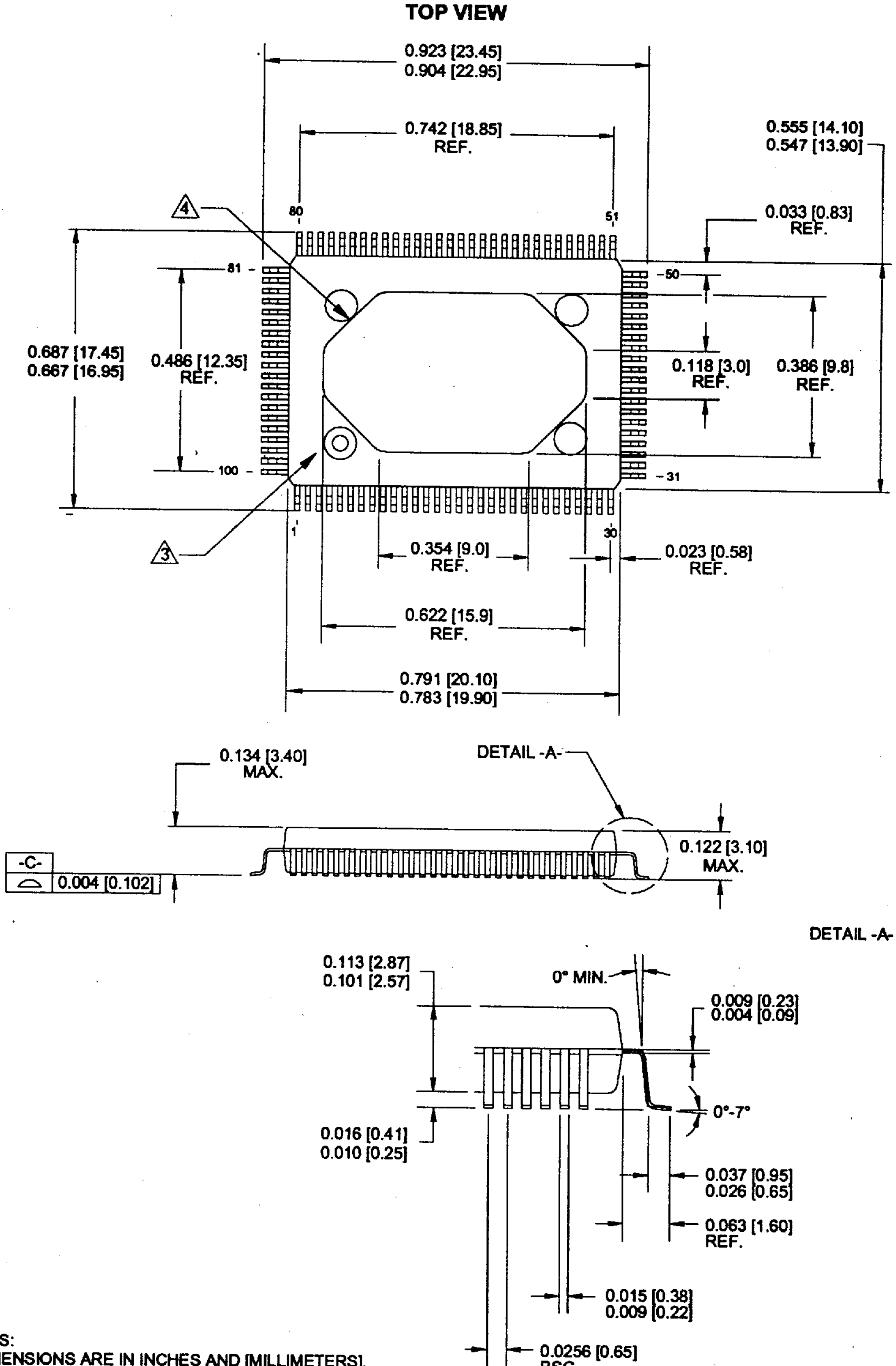


Figure 8. SY69712 Interface with S/UNI–622

100 LEAD PLASTIC QUAD FLATPACK WITH HEAT SPREADER - DIE DOWN (R100-2)



NOTES:
1. DIMENSIONS ARE IN INCHES AND [MILLIMETERS].
2. CONTROLLING DIMENSION: [MILLIMETERS].
3. THE PIN 1 ID MARK IS ROUNDED AT THE BOTTOM.
   THE REMAINING MARKS ARE FLAT AT THE BOTTOM.
4. HEATSPREADER LOCATED ON PACKAGE BOTTOM.