

7494

Shift Register

4-Bit Shift Register
Product Specification

Logic Products

FEATURES

- 4-bit parallel-to-serial converter
- Two asynchronous ones transfer parallel data ports
- Buffered active HIGH Master Reset
- Buffered positive edge-triggered clock

DESCRIPTION

The '94 is a 4-bit shift register with serial and parallel (ones transfer) data entry. To facilitate parallel ones transfer from two sources, two Parallel Load inputs (PL₀ and PL₁) with associated Parallel Data inputs (D_{0a} - D_{0d} and D_{1a} - D_{1d}) are provided. To accommodate these extra inputs only the output of the last stage is available. The asynchronous Master Reset (MR) is active HIGH. When MR is HIGH, it overrides the clock and clears the register, forcing Q_d LOW.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT
7494	25ns	35mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V _{CC} = 5V ±5%; T _A = 0°C to +70°C
Plastic DIP	N7494N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

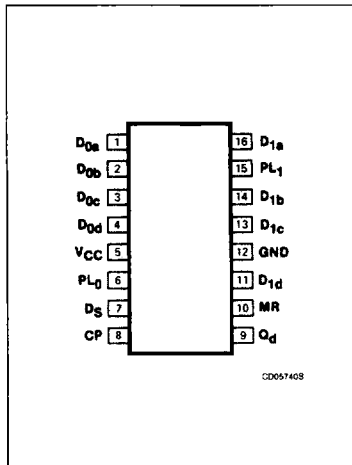
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74
PL ₀ , PL ₁	Parallel load inputs	4ul
D _S , D _n , CP, MR	All other inputs	1ul
Q _d	Serial Data output	10ul

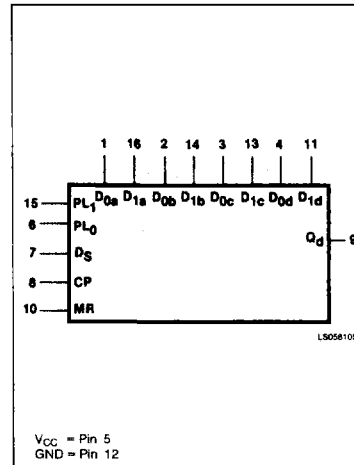
NOTE:

Where a 74 unit load (ul) is understood to be 40μA I_{HH} and -1.6mA I_{LL}.

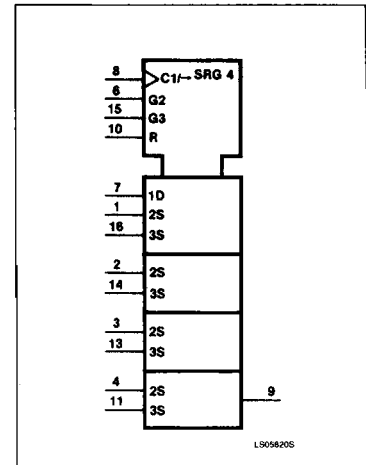
PIN CONFIGURATION



LOGIC SYMBOL



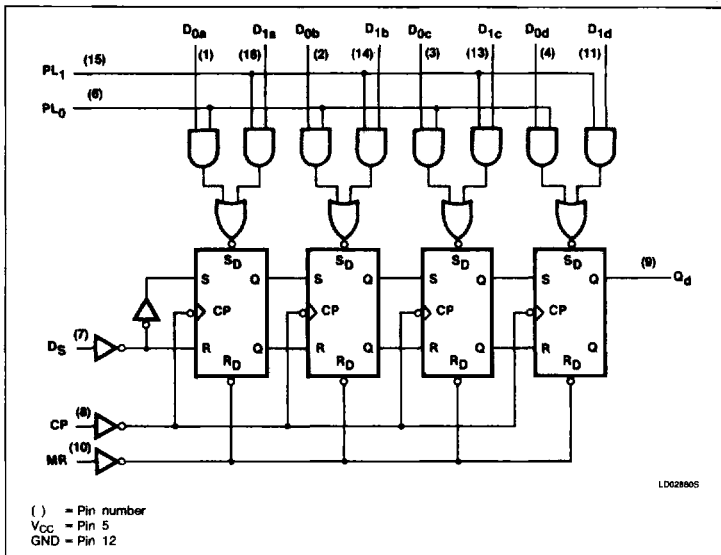
LOGIC SYMBOL (IEEE/IEC)



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LOGIC DIAGRAM



Four flip-flops are connected so that shifting is synchronous; they change state when the clock goes from LOW-to-HIGH. Data is accepted at the serial D_S input prior to this clock transition. Two Parallel Load inputs and Parallel Data inputs allow an asynchronous ones transfer from two sources. The flip-flops can be set independently to the HIGH state when the appropriate Parallel input is activated. Parallel inputs D_{0a} through D_{0d} are activated during the time the PL₀ is HIGH and Parallel inputs D_{1a} through D_{1d} are activated when PL₁ is HIGH. If both sets of inputs are activated, a HIGH on either input will set the flip-flops to a HIGH. The register should not be clocked while the Parallel Load inputs are activated. The Parallel Load and Parallel Data inputs will override the MR if both are activated simultaneously. However, for predictable operation, both signals should not be deactivated simultaneously.

FUNCTION TABLE

OPERATING MODE	INPUTS							OUTPUTS			
	PL ₀	PL ₁	D _{0n}	D _{1n}	MR	CP	D _S	Q _a	Q _b	Q _c	Q _d
Parallel load	H	L	L	X	X	X	X	Q _a	Q _b	Q _c	Q _d
	H	L	H	X	X	X	X	H	H	H	H
	L	H	X	L	X	X	X	Q _a	Q _b	Q _c	Q _d
	L	H	X	H	X	X	X	H	H	H	H
Reset (clear)	L	L	X	X	H	X	X	L	L	L	L
Shift right	L	L	X	X	L	↑	l	L	q _a	q _b	q _c
	L	L	X	X	L	↑	h	H	q _a	q _b	q _c

- H = HIGH voltage level.
- h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition.
- L = LOW voltage level.
- l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition.
- q_n = Lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition.
- X = Don't care.
- ↑ = LOW-to-HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	74	UNIT
V _{CC} Supply voltage	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	V
I _{IN} Input current	-30 to +5	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	0 to 70	°C

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RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			UNIT
	Min	Nom	Max	
V _{CC} Supply voltage	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage	2.0			V
V _{IL} LOW-level input voltage			+0.8	V
I _{IK} Input clamp current			-12	mA
I _{OH} HIGH-level output current			-400	μA
I _{OL} LOW-level output current			16	mA
T _A Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	7494			UNIT
		Min	Typ ²	Max	
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.4	3.4		V
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OL} = MAX		0.2	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5	V
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5V			1.0	mA
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.4V	PL ₀ , PL ₁ inputs		160	μA
		Other inputs		40	μA
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V	PL ₀ , PL ₁ inputs		-6.4	mA
		Other inputs		-1.6	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX	-18		-57	mA
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX		35	58	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with Parallel Load inputs grounded. Master Reset grounded following momentary application of 4.5V, all other inputs at 4.5V and outputs open.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74		UNIT
		C _L = 15pF, R _L = 400Ω		
		Min	Max	
f _{MAX} Maximum clock frequency	Waveform 1	10		MHz
t _{PLH} Propagation delay t _{PHL} Clock to output	Waveform 1		40 40	ns
t _{PLH} Propagation delay Parallel Load or Parallel Data to output	Waveform 2		35	ns
t _{PHL} Propagation delay MR to output	Waveform 2		40	ns

NOTE:

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

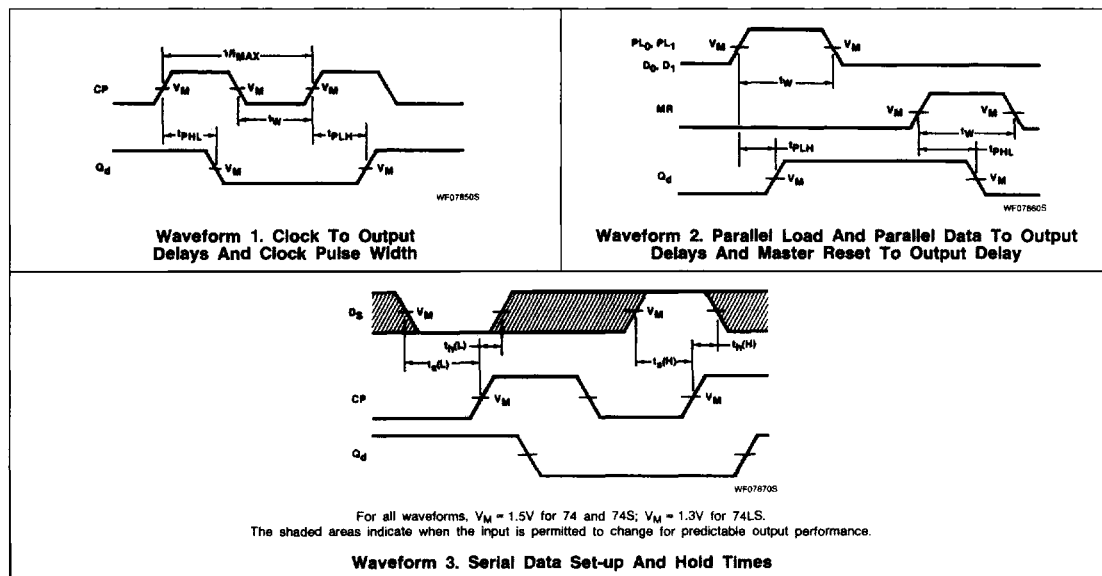
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AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS ¹	74		UNIT
		Min	Max	
$t_{W(L)}$ Clock pulse width, LOW	Waveform 1	35		ns
$t_{W(H)}$ MR pulse width, HIGH	Waveform 2	30		ns
$t_{W(H)}$ Parallel load or data pulse width, HIGH	Waveform 2	30		ns
$t_s(H)$ Set-up time HIGH, D_S to CP	Waveform 3	35		ns
$t_s(L)$ Set-up time LOW, D_S to CP	Waveform 3	25		ns
t_h Hold time HIGH or LOW, D_S to CP	Waveform 3	0		ns

AC WAVEFORMS



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TEST CIRCUITS AND WAVEFORMS

$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns