silicon systems®
A TDK Group Company

SSI 32C9340
PCMCIA Combo Controller with Reed Solomon, 48 Mbit/s
Target Specification

January 1994

DESCRIPTION

The SSI 32C9340 is a CMOS VLSI device which integrates major portions of the hardware needed to build a PCMCIA and/or ATA drive hard disk controller. The SSI 32C9340's place in the Silicon Systems' chip family is illustrated in the hierarchy chart in Figure 1. It provides most of the functional circuitry necessary to build a PCMCIA intelligent disk.

The SSI 32C9340 is capable of supporting interleaved host and disk transfers while maintaining a disk data transfer rate of up to 48 Mbit/s.

The SSI 32C9340 includes a multi-port Buffer Manager, a storage controller and a high performance PCMCIA host interface block that incorporates extensive hardware support — including direct connection to a PCMCIA or ATA bus.

The SSI 32C9340 performs all the controller functions for the peripheral device including: Serialization and deserialization of data; and, ECC generation, checking and on-the-fly data correction.

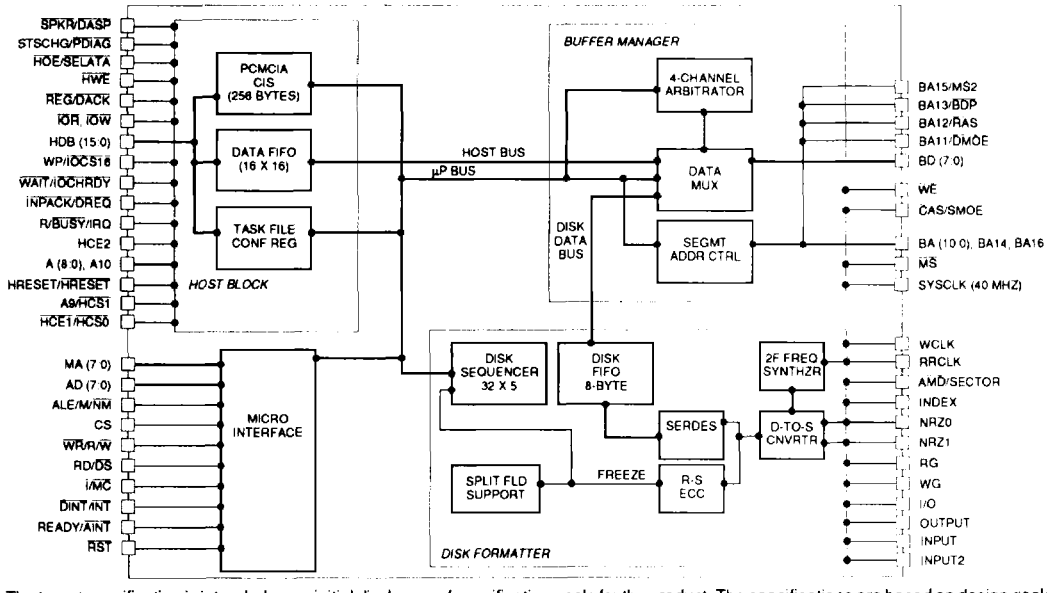
FEATURES

HOST INTERFACE:

- **PCMCIA/ATA and ATA compatible host interface**
- **Hardware and software compatible with PCMCIA bus standard, revision 2.0**
- **Programmable 256-byte PCMCIA CIS integrated**
- **High Current drivers for direct connection to the PCMCIA or AT bus**
- **Both memory and I/O interfaces supported for PCMCIA**
- **Includes IBM AT compatible Task File registers and PCMCIA configuration registers**
- **Hardware added to provide Multi-Sector data transfers without microprocessor intervention**
- **Automatic BUSY, INTRQ**
- **16 byte FIFO to improve throughput**
- **PC transfers to 4(6.7@5V) megawords/second**

(continued)

BLOCK DIAGRAM



SSI 32C9340
PCMCIA Combo Controller with Reed Solomon, 48 Mbit/s

FEATURES (continued)

- Automatic command decoding of write, write long, write DMA, write multiple, write buffer and format commands
- Automatic update of the host task file registers in both LBA mode and Cyl/Hd/Sec mode
- Support for ATA master/slave operation
- Power-down IO pins

BUFFER MANAGER:

- Supports Buffer RAM throughput up to:
  5V: 20 MByte/sec for SRAM and 17.78 MByte/sec for DRAM (with 40MHz SYSCLK)
  3.3V: 16 MByte/sec for SRAM and 14 MByte/sec for DRAM (with 30 MHz SYSCLK)
- Programmable microprocesssor scratch pad area
- Auto data streaming capability
- Supports Multiple sector host data transfer
- Supports up to 1M byte DRAM and up to 128K SRAM
- Supports variable DRAM and SRAM timings and sizes
- Reload transfer counter and host address pointers
- Supports page mode DRAM access
- Programmable DRAM page mode burst length
- Programmable DRAM refresh period
- Separate host, disk, and microprocessor buffer RAM address pointers
- Provides protection logic for buffer data allowing simultaneous host and disk accesses to the same buffer segment.

DISK FORMATTER:

- Advanced sequencer organized in 31 x 5 bytes
- Advanced branch and interrupt logic
- Defect management support
- Supports multiple-sector data transfers
- NRZ byte synchronization time out timer
- Three-index counter providing limit of search and retry
- 8-byte stack for header information storage
- 16-byte disk data FIFO
- Sector header or microprocessor-based split data field processing logic supporting embedded servo and zone-bit recording
- Supports variable data field length
- Disk transfer rate up to 48 Mbit/s NRZ
- Power Down Mode

MICROPROCESSOR INTERFACE:

- High speed internal register access
- Programmable wait state insertion
- Supports both Intel and Motorola type microprocessers

ERROR CORRECTION LOGIC:

- Enhanced 16-bit CRC polynomial with one order of magnitude better burst error detection than CCITT-CRC16
- Non-interleaved 88-bit Reed Solomon Code of degree 8 operation on 10-bit symbols
- Automatic on-the-fly in-buffer error correction
- Selectable on-the-fly error correction span of 11 bits signal burst
- Calculation of buffer offsets and masks for on-the-fly ECC within one half of a sector time
- On the fly in-buffer correction accomplished in no more than 3 buffer reads and writes through an independent channel
- Capable of correcting by software four 10-bit symbols in error
- Guaranteed to correct by software one 31-bit burst or two 11-bit bursts
- Detects up to one 51-bit burst or three 11-bit bursts

OTHERS:

- Automatic power supply level detection circuit
- JEDEC conformant 3.3V specification
- TTL-Level compatible input receivers at 3.3V or 5V
- Avaiable in 120-pin surface mount TQFP

FUNCTIONAL DESCRIPTION

The SSI 32C9340 is capable of operating in either a 3.3 volt or 5 volt environment.

The SSI 32C9340 contains the following four major functional blocks:

Microprocessor Interface

PCMCIA/ATA Interface

Disk Formatter

Buffer Manager

The Microprocessor Interface allows the local microprocessor access to all of the SSI 32C9340 internal control registers and any location within the buffer memory. The microprocessor, by writing and reading the internal registers, can control all activities of the SSI 32C9340. The microprocessor can elect to perform host and/or disk operations directly, or it can enable the advanced features of the SSI 32C9340 which can perform these operations automatically.

The PCMCIA/ATA Interface block can interface with the PCMCIA interface as a PCMCIA/ATA device or with a PC AT bus. The SSI 32C9340 has on-board sensing logic to help determine whether it is operating in either the PCMCIA or ATA mode. The interface includes 12 mA (8 mA @3.3V) drivers allowing for direct connection of the SSI 32C9340 to either the PCMCIA or PC AT bus. The interface is highly automated, capable of performing multiple block transfers without micro- controller involvement. The PCMCIA/ATA block interfaces directly with the Buffer Manager via an internal speed matching FIFO. This FIFO, the bandwidth capabilities of the Buffer Manager, plus the advanced features of the PCMCIA/ATA Interface guarantee sustained full speed transfers.

The Disk Formatter performs the serialization and deserialization of data. It provides all of the necessary functions to control track formatting, header search, and the reading and writing of data. The heart of the Disk Formatter is an advanced programmable sequencer. The sequencer can contain 31 instructions, each of which is 5 bytes (40 bits) in width. The width of the instructions allows for sophisticated branching techniques which increase the flexibility and power of the sequencer. The disk interface can be configured through a wide range of capabilities. This allows the SSI 32C9340 to interface with nearly any read/write channel. This allows the user of the SSI 32C9340 to select the read/write channel best suited to the device. Of course, by selecting the SSI 32C9340 controller and the SSI 32P4330 Read Channel with 1,7 ENDEC, you are guaranteed a problem free interface.

Within the Disk Formatter are the ECC generator/checker and ECC corrector. The generator/checker provides the ability to generate or check a 32 bit ECC for headers and an 88 bit Reed Solomon code for data. If the checker detects an error in an 88 bit Reed Solomon data field, the syndrome information is transferred into the corrector. The corrector then performs the necessary operations to determine if the error was correctable and, if it was correctable, the corrector interfaces directly with the buffer controller and performs the correction automatically. The corrector performs its correction within one half of a sector. This guarantees that the corrector will always be available to correct the next sector if necessary.

The Buffer Manager manages the data buffer of the controller. The Buffer Manager can support either SRAM or DRAM. When configured to operate with DRAM, the Buffer Manager automatically performs necessary refresh cycles. The buffer manager creates all of the necessary timing and control signals for a wide range of memory types and speeds. Besides interfacing with the buffer memory, the Buffer Manager interfaces with the ATA Interface block, the Disk Formatter block, the ECC corrector and the microprocessor. If more than one of these devices requires access to the buffer memory, the Buffer Manager arbitrates the requests automatically. The Buffer Manager of the SSI 32C9340 can sustain ATA operations at the rate of 4 (6.7 @ 5V) megawords per second, Disk Formatter operations at 48 megabits per second and still have sufficient bandwidth left to handle on-the-fly ECC corrections and microprocessor accesses without degrading performance on any of the interfaces.

SSI 32C9340
PCMCIA Combo Controller with Reed Solomon, 48 Mbit/s

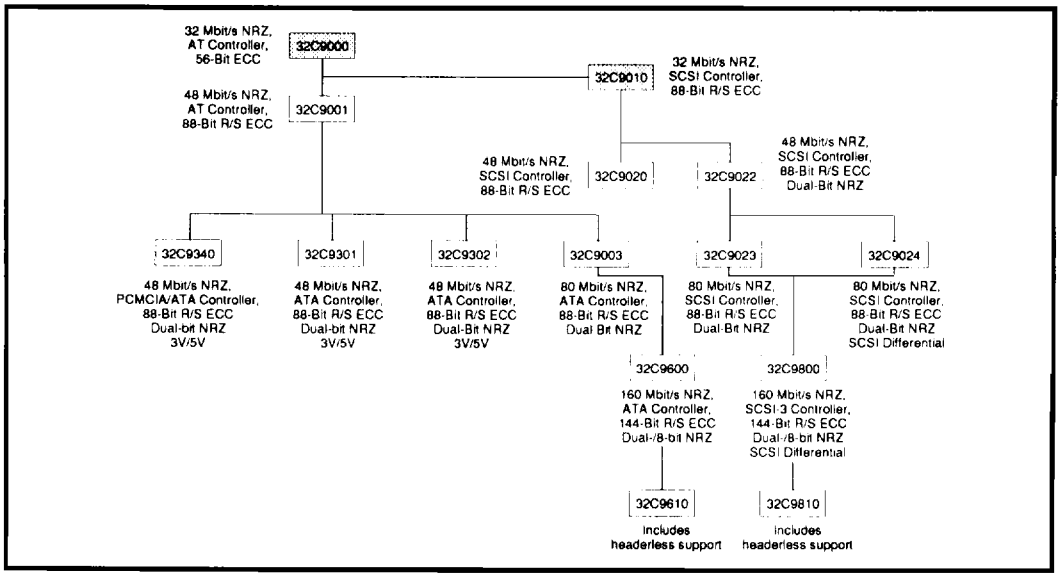


FIGURE 1: Silicon Systems's Disk Controller Chip Hierarchy

PIN DESCRIPTION

I = input, O = output; Z = tri-state output, OD = open drain output. All unused inputs must be tied to the inactive state to VCC or GND, respectively.

BUFFER MANAGER INTERFACE

NAME	TYPE	DESCRIPTION
BA16	I/O	BUFFER ADDRESS 16. In SRAM mode, this pin may be configured as buffer address 16.
BA15/$\overline{MS2}$	O	BUFFER ADDRESS 15/MEMORY SELECT. In SRAM mode, this pin may be configured as buffer address 15 or memory select 2 for 2nd bank of memory. After $\overline{RST}$ is asserted, this signal will be high.
BA14	I/O	BUFFER MEMORY ADDRESS 14. This signal is used for addressing the buffer memory in SRAM mode.
BA13/BDP	I/O	BUFFER MEMORY ADDRESS 13/BUFFER MEMORY PARITY. This signal is used for addressing the buffer memory in SRAM mode, or as the buffer data parity value in DRAM mode.
BA12/$\overline{RAS}$	O	BUFFER MEMORY ADDRESS 12/ROW ADDRESS STROBE: This signal is used for addressing the buffer memory in SRAM mode or as the row address strobe in DRAM mode. After $\overline{RST}$ is asserted, this signal will be high.
BA11/$\overline{DMOE}$	O	BUFFER MEMORY ADDRESS 11/DRAM MEMORY OUTPUT ENABLE. This signal is used for addressing the buffer memory in SRAM mode, or as the memory output enable pin in DRAM mode. After $\overline{RST}$ is asserted, this signal will be high.
BA(10:0)	O	BUFFER MEMORY ADDRESS LINES. These are signals 10-0 for addressing the buffer memory.
BD(7:0)	I/O	BUFFER MEMORY DATA BUS. These eight signals are bits 7-0 of the 8-bit parallel data lines to/from the buffer memory. Note that BD6 is used to select between the Intel- and Motorola-style microprocessor interfaces. If BD6 is externally pulled up when $\overline{RST}$ is asserted, Intel mode is used; if BD6 is externally pulled down when $\overline{RST}$ is asserted, Motorola mode is used.
$\overline{CAS}$/$\overline{SMOE}$	O	COLUMN ADDRESS STROBE/SRAM MEMORY OUTPUT ENABLE. This signal is used as the column address strobe in DRAM mode, or the memory output enable in SRAM mode. After RST is asserted, this signal will be high.
$\overline{MS}$	O	MEMORY SELECT. An active low signal indicates external memory is selected (chip enabled) or 1st bank of memory is selected.
SYSCLK	I	SYSTEM CLOCK. This signal is used to synchronize the buffer RAM access, including the generation of memory address lines, write enable WE, and memory output enable MOE. In power down mode, this signal is shut off from the internal logic and hence buffer memory access is inhibited.
WE	O	WRITE ENABLE. This active low output signal is used to strobe the data into the RAMs from the DAta bus. For both buffer memory applications, this line is tied directly to the SRAM or DRAM control pin.

PIN DESCRIPTION (continued)

MICROPROCESSOR INTERFACE

NAME	TYPE	DESCRIPTION
$\overline{RST}$	I	RESET. An asserted active low input generates a component reset that holds the internal registers of the SSI 32C9001 at reset, stops all operations within the chip, and deasserts all output signals. All input/output signals and Host outputs are set to the high-Z state.
ALE/M/$\overline{NM}$	I	ADDRESS LATCH ENABLE/MULTIPLEXED/NON-MULTIPLEXED ADDRESS SELECT. When tied high, the microprocessor interface is configured as non-multiplexed. When driven low, the microprocessor interface is configured as multiplexed. In this case this pin functions as the address latch enable, and the MA(7:0) pins are the demultiplexed address outputs.
CS	I	CHIP SELECT. This signal must be asserted high for all microprocessor accesses to the registers of this chip.
$\overline{WR}$/R/$\overline{W}$	I	WRITE STROBE/READ/WRITE. In the Multiplexed address/data bus mode, when an active low signal is present with CS signal asserted high, the data on the AD0:7 is written to the internal registers. In the Non-Multiplexed address/data bus mode, this signal acts as the R/$\overline{W}$ signal. A high on this input along with the $\overline{RD}$/DS signal asserted and the CS signal asserted high indicates a read operation. A low on this input along with the $\overline{RD}$/DS signal asserted and the CS signal asserted high indicates a write operation. See table below.

CS	$\overline{WR}$/R/$\overline{W}$	$\overline{RD}$/DS	Mux/Non-Mux	Action
High	Low	High	Intel Multiplexed	Write to internal registers.
High	High	Low	Intel Multiplexed	Read from internal registers.
High	Low	High	Motorola Multiplexed	Write to internal registers.
High	Low	Low	Non-Multiplexed	Write to internal registers.
High	High	High	Motorola Multiplexed	Read from internal registers.
High	High	Low	Non-Multiplexed	Read from internal registers.
Low	X	X	M or N	No action.

Note: X denotes don't care.

$\overline{RD}$/DS	I	READ STROBE/DATA STROBE. In the Multiplexed address data bus mode, when an active low signal is present with CS signal high, internal registers will be accessed. In the Non-Multiplexed address data mode, this signal acts as the DS signal. A high on R/$\overline{W}$, with the CS and DS signals asserted, indicates a read operation. A low on the R/$\overline{W}$ signal, with the DS and the CS symbols asserted, indicates a write operation to the internal registers. Note: DS is active high in multiplexed mode, active low in non-multiplexed.

NAME	TYPE	DESCRIPTION
$\overline{\text{DINT}}/\overline{\text{INT}}$	O, OD	INTERRUPT. This signal is an interrupt line to the microprocesor. It is the combined interrupt line of the disk side and host side interrupts when pin READY/$\overline{\text{AINT}}$ is programmed as ready; otherwise, it only signals the occurrence of disk side interrupt events. This signal is programmable for either a push-pull or open-drain output circuit. This signal powers up as an open drain output. May be programmed as active high or low; reset state is active low.
AD(7:0)	I/O	ADDRESS/DATA BUS. When configured in the Multiplexed address data mode, these lines are multiplexed, bidirectional data path to the microprocessor. During the beginning of the memory cycle the bus captures the low order byte of the microprocessor address. These lines provide communication with the controller device's internal registers and the buffer memory. When configured in the Non-Multiplexed Microprocessors mode, these lines are bidirectional data lines only.
MA(7:0)	I/O	MICROPROCESSOR ADDRESS BUS. This 8-bit output bus is the AD(7:0) bus latched by the ALE pin during the address phase of a Multiplexed address data type microprocessor cycle. These signals are the address input when used with a non-multiplexed bus microprocessor.
READY/$\overline{\text{AINT}}$	O, OD	READY/HOST SIDE INTERRUPT. When programmed as the Ready function, this signal is deasserted low for the microprocessor to insert wait states to allow time for the chip to respond to the access. When programmed as the host side interrupt, this pin interrupts the microprocessor when there is a host related interrupt event. The interrupt signal is programmable for either a push-pull or open-drain output circuit. This signal powers up as the 'Ready' function.

DISK FORMATTER INTERFACE

INDEX	I	INDEX. This pin serves as the index function for the disk sequencer.
INPUT	I	INPUT. This signal is used to synchronize the disk sequencer to an external event.
INPUT2 (FAULT)	I	INPUT2. This pin is an input to the sequencer for tracking operations or can be used as a fault function to stop the sequencer.
OUTPUT	O	DISK SEQUENCER OUTPUT. This pin is controlled by bit 2 of the Control Field of the disk sequencer.
$\overline{\text{AMD}}$/SECTOR	I/O	ADDRESS MARK DETECT/SECTOR. In Hard Sector mode, this is the input for the sector pulse from the disk drive. In Soft Sector mode, a low-level input during a read indicates an address mark was detected.
RG	O	READ GATE. This active high output enables the reading of the disk. It is asserted by the sequencer Control Field bits 5 and 6. It is automatically deasserted at the end of the CRC or ECC.
WG	O	WRITE GATE. This active high output enables writing onto the disk. It is asserted and deasserted by the sequencer Control Field bits 5 and 6.
RRCLK	I	READ/REFERENCE CLOCK. This pin is used in conjunction with the NRZ pin to clock data in and out of the SSI 32C9001 device. This input must be glitch-free to ensure correct operation of the chip.

PIN DESCRIPTION (continued)

DISK FORMATTER INTERFACE (continued)

NAME	TYPE	DESCRIPTION
WCLK	O	WRITE CLOCK. This signal clocks the NRZ data out
NRZ0	I/O	NRZ BIT 0. This signal is the read data input from the disk drive when the read gate signal is asserted; it is the write data output to the disk drive when the srite gate signal is asserted. This pin is used for the least significant bit in dual bit NRZ mode; it is used for the serial data stream in single bit NRZ mode.
NRZ1	I/O	NRZ BIT1. This signal is the read data input from the disk drive when the read gate signal is asserted; it is the write data output to the disk drive when the write gate signal is asserted. This pin is used for the most significant bit in dual bit NRZ mode; it is not used in single bit NRZ mode.

HOST INTERFACE PINS

WP/$\overline{\text{IOCS16}}$	O, OD	WRITE PROTECT OR 16-BIT DATA SELECT. This signal can be used for write protect or 16-bit transfer for PCMCIA common memory mode. In ATA mode it indicates a 16-bit transfer is active on the host busl.
R/$\overline{\text{BUSY}}$/IRQ	O, Z	READY/$\overline{\text{BUSY}}$/HOST INTERRUPT REQUEST. In PCMCIA mode, this pin is the Ready/$\overline{\text{BUSY}}$ signal when configured with a memory interface. In ATA mode, or in PCMCIA mode when configured with an I/O interface, this pin is the host interrupt request, and is asserted to indicate to the host that the controller needs attention. As an interrupt request, this pin is active high in ATA mode, but active low in PCMCIA mode. This pin is always driven in PCMCIA mode, but will be tri-stated when the drive is not selected or interrupts are not enabled in ATA mode. This pin is driven low while $\overline{\text{RST}}$ is asserted, and remains so until the interface mode (PCMCIA or ATA) is determined. If PCMCIA mode is selected after reset, the chip is configured with a memory interface, and this pin will reflect the status of the BUSY bit in the Drive Status Register.
A(8:0), A10	I	HOST ADDRESS LINES. The host address lines A(8:0) and A10 are used to access the various PC/AT control, status, and data registers.
A9/$\overline{\text{HCS1}}$	I	A9/$\overline{\text{HCS1}}$. This is a multiplexed input pin. When in PCMCIA mode, or when register 4CH, bit 3 is reset, this is host address line A9. When register 4CH, bit 3 is set in ATA mode, this is Host chip select 1 (active low).
$\overline{\text{HCE1}}$/$\overline{\text{HCS0}}$	I	HOST CHIP SELECT 0/CARD ENABLE 1. This signal when low, selects access to the control, status, and data registers. It is configured as $\overline{\text{HCS0}}$ in ATA mode, and as $\overline{\text{HCE1}}$ (card enable 1) in PCMCIA mode.
WAIT/IOCHRDY	O, Z	WAIT/I/O CHANNEL READY. This signal is asserted low to extend host transfer cycles when the controller is not ready to respond. This pin is always driven in PCMCIA mode, but will be tri-stated when a read or write is not in progress in ATA mode. This pin is tri-state while $\overline{\text{RST}}$ is asserted, and remains so until the interface mode (PCMCIA or ATA) is determined.

NAME	TYPE	DESCRIPTION
INPACK/DREQ	O, Z	INPUT ACKNOWLEDGE/DMA REQUEST. In PCMCIA mode, this pin is configured as INPACK, and is asserted when a valid address and chip select are present. In ATA mode, this pin is configured as the DMA request signal, and is used during DMA transfer between the host and the controller. In ATA mode, this pin is tri-stated when DMA transfers are not enabled. This pin is tri-state while RST is asserted, and remains so until the interface mode (PCMCIA or ATA) is determined.
REG/DACK	I	REGISTER SELECT AND I/O ENABLE/DMA ACKNOWLEDGE. In PCMCIA mode, this pin is configured as REG, and selects the attribute memory space or I/O space when asserted. In ATA mode, this pin is configured as DACK, and is used as the DMA acknowledge signal during DMA data transfers.
IOR	I	I/O READ. Asserted by the host during a host I/O read operation. When asserted with a valid address and chip selects, status or data is enabled onto the host data bus.
IOW	I	I/O WRITE. Asserted by the host during a host I/O write operation. When asserted with a valid address and chip selects, data from the host data bus is strobed into the controller.
HRESET/HRESET	I	HOST RESET. This signal, when active, initializes the control/status registers and stops any command in process. It is active low in ATA mode, but active high in PCMCIA mode.
HDB(15:0)	I/O	HOST DATA BUS. This bus is used to transfer data and status between the host and the controller. These pins are not driven while RST is asserted, and remain so until the interface mode (PCMCIA or ATA) is determined.
HCE2	I	CARD ENABLE 2. This signal, when low, selects access to the control, status, and data registers and may enable use of the upper half of the data bus. It is used only in PCMCIA mode.
HOE/SELATA	I	OUTPUT ENABLE/SELECT ATA MODE. To determine which host interface to use, this pin is sampled starting at least 8 µs after RST is deasserted, and continuing until at least 25 µs after RST is deasserted. If this pin is high at any time during this sampling period, the interface will immediately be configured for PCMCIA mode, and the sampling will end. If the pin remains low throughout the sampling period, the interface will be configured for ATA mode. Once in PCMCIA mode, this pin is configured as output enable (HOE), and is asserted by the host during a common memory or attribute memory read. When asserted with a valid address and chip select, data is enabled onto the host data bus. In ATA mode, this signal is ignored.

PIN DESCRIPTION (continued)

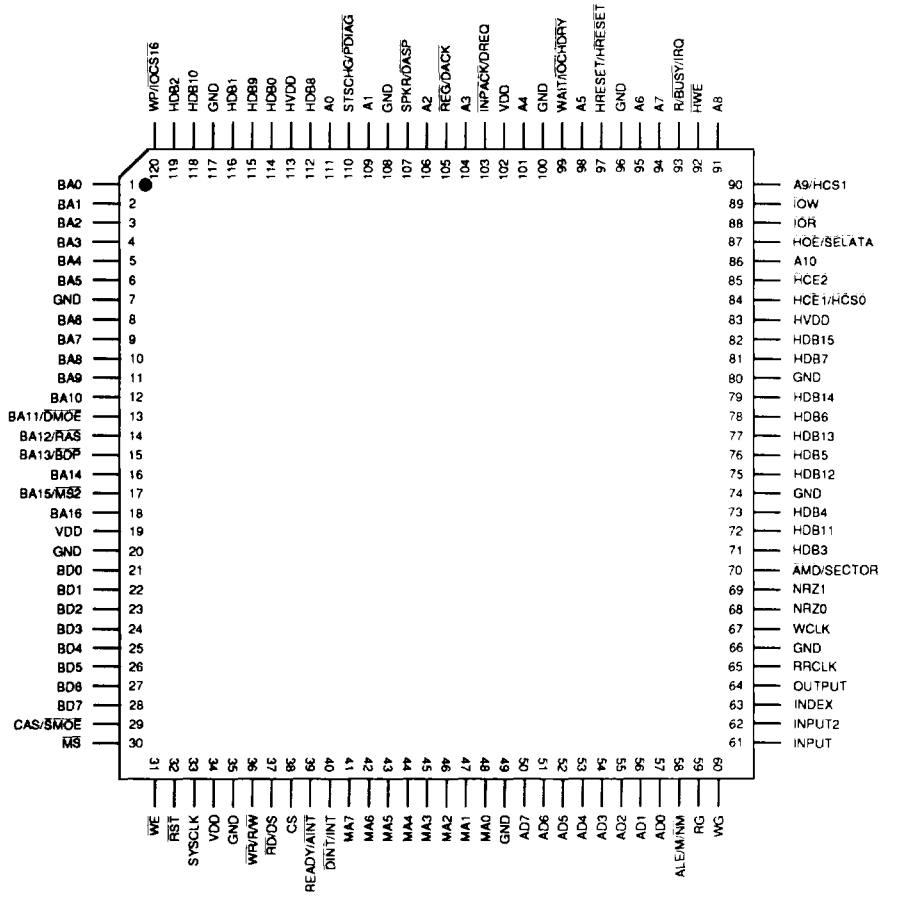
HOST INTERFACE PINS (continued)

NAME	TYPE	DESCRIPTION
$\overline{HWE}$	I	WRITE ENABLE. In PCMCIA mode, this signal is asserted by the host during a common memory or attribute memory write. When asserted with a valid address and chip select, data from the host data bus is strobed into the controller. In ATA mode, this signal is ignored.
$\overline{STSCHG}/\overline{PDIAG}$	I, O	STATUS CHANGED/PASSED DIAGNOSTICS. In PCMCIA mode, this pin is used as the Status Changed output. In ATA mode, this pin is used as the Passed Diagnostics signal and may be an input or an open-drain output. This pin is tri-state while $\overline{RST}$ is asserted, and remains so until the interface mode (PCMCIA or ATA) is determined.
$\overline{SPKR}/\overline{DASP}$	I/OD	SPEAKER/DRIVE ACTIVE-SLAVE PRESENT. In PCMCIA mode, this pin is used as the Speaker pin, and is a push-pull output. In ATA mode, this pin is used as the Drive Active/Slave Present signal, and is an input or an open-drain output. In ATA mode, this pin is used for Master/Slave drive communications and/or for driving an LED. This pin is tri-state while $\overline{RST}$ is asserted, and remains so until the interface mode (PCMCIA or ATA) is determined.

PACKAGE PIN DESIGNATIONS

(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



120-Lead TQFP

Target Specification: The target specification is intended as an initial disclosure of specification goals for the product. The specifications are based on design goals, subject to change and are not guaranteed.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 573-6000, FAX: (714) 573-6914