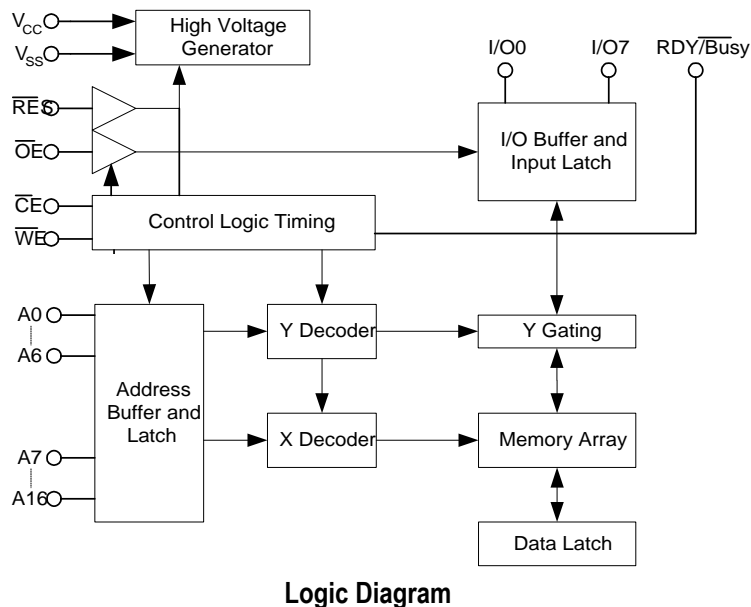
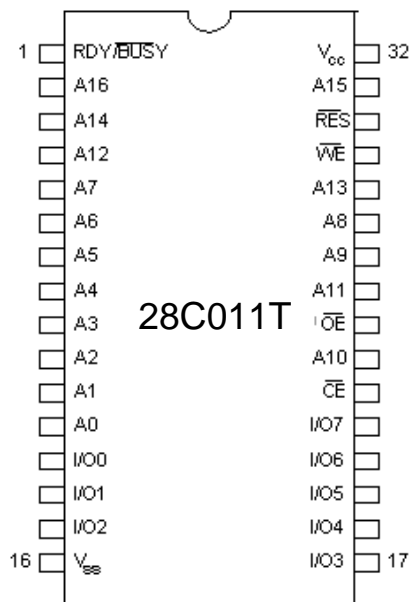


28C011T

1 Megabit (128K x 8-Bit) EEPROM



FEATURES:

- 128k x 8-bit EEPROM
- RAD-PAK® radiation-hardened against natural space radiation
- Total dose hardness:
 - > 100 krad (Si), depending upon space mission
- Excellent Single event effects @ 25°C
 - $SEL_{TH} > 120 \text{ MeV cm}^2/\text{mg}$ (Device)
 - $SEU_{TH} > 90 \text{ MeV cm}^2/\text{mg}$ (Memory Cells)
 - $SEU_{TH} > 18 \text{ MeV cm}^2/\text{mg}$ (Write Mode)
 - $SET_{TH} > 40 \text{ MeV cm}^2/\text{mg}$ (Read Mode)
- Package:
 - 32-pin RAD-PAK® flat package
 - 32-pin Rad-Tolerant flat package
 - JEDEC-approved byte-wide pinout
- High speed:
 - 120, 150, and 200 ns maximum access times available
- High endurance:
 - 10,000 erase/write (in Page Mode),
 - 10 year data retention
- Page write mode:
 - 1 to 128 bytes
- Low power dissipation
 - 20 mW/MHz active (typical)
 - 110 μW standby (maximum)

DESCRIPTION:

DDC's 28C011T high-density 1 Megabit (128K x 8-Bit) EEPROM microcircuit features a greater than 100 krad (Si) total dose tolerance, depending upon space mission. The 28C011T is capable of in-system electrical byte and page programmability. It has a 128-byte page programming function to make its erase and write operations faster. It also features data polling and a Ready/Busy signal to indicate the completion of erase and programming operations. In the 28C010T, hardware data protection is provided with the RES pin, in addition to noise protection on the WE signal and write inhibit on power on and off. Software data protection is implemented using the JEDEC optional standard algorithm.

DDC's patented RAD-PAK® packaging technology incorporates radiation shielding in the microcircuit package. It eliminates the need for box shielding while providing the required radiation shielding for a lifetime in orbit or space mission. In a GEO orbit, RAD-PAK® provides greater than 100 krad (Si) radiation dose tolerance. This product is available with screening up to DDC's self-defined Class S.

TABLE 1. 28C011T PINOUT DESCRIPTION

PIN	SYMBOL	DESCRIPTION
12-5, 27, 26, 23, 25, 4, 28, 3, 31, 2	A0-A16	Address
24	\overline{OE}	Output Enable
22	\overline{CE}	Chip Enable
29	\overline{WE}	Write Enable
32	V_{CC}	Power Supply
16	V_{SS}	Ground
1	RDY/BUSY	Ready/Busy
30	RES	Reset

TABLE 2. 28C011T ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage (Relative to V_{SS})	V_{CC}	-0.6	+7.0	V
Input Voltage (Relative to V_{SS})	V_{IN}	-0.5 ¹	+7.0	V
Operating Temperature Range	T_{OPR}	-55	+125	°C
Storage Temperature Range	T_{STG}	-65	+150	°C

1. V_{IN} min = -3.0V for pulse width \leq 50ns.

TABLE 3. DELTA LIMITS

PARAMETER	VARIATION
I_{CC1}	$\pm 10\%$
I_{CC2}	$\pm 10\%$
I_{CC3A}	$\pm 10\%$
I_{CC3B}	$\pm 10\%$

TABLE 4. 28C011T RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	V_{CC}	4.5	5.5	V
Input Voltage	V_{IL}	-0.3 ¹	0.8	V
	V_{IH}	2.2	$V_{CC} + 0.3$	
	V_H	$V_{CC} - 0.5$	$V_{CC} + 1$	
$\overline{RES_PIN}$				
Operating Temperature Range	T_{OPR}	-55	+125	°C

1. V_{IL} min = -1.0V for pulse width \leq 50 ns

TABLE 5. 28C011T CAPACITANCE
($T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Capacitance: $V_{IN} = 0V$ ¹	C_{IN}	--	6	pF
Output Capacitance: $V_{OUT} = 0V$ ¹	C_{OUT}	--	12	pF

1. Guaranteed by design.

TABLE 6. 28C011T DC ELECTRICAL CHARACTERISTICS
($V_{CC} = 5V \pm 10\%$, $T_A = -55$ TO $+125^\circ\text{C}$, UNLESS OTHERWISE SPECIFIED)

PARAMETER	TEST CONDITION	SUBGROUPS	SYMBOL	MIN	MAX	UNITS
Input Leakage Current	$V_{CC} = 5.5V$, $V_{IN} = 5.5V$	1, 2, 3	I_{IL}	--	2 ¹	μA
Output Leakage Current	$V_{CC} = 5.5V$, $V_{OUT} = 5.5V/0.4V$	1, 2, 3	I_{LO}	--	2	μA
Standby V_{CC} Current	$\overline{CE} = V_{CC}$	1, 2, 3	I_{CC1}	--	20	μA
	$\overline{CE} = V_{IH}$		I_{CC2}	--	1	mA
Operating V_{CC} Current	$I_{OUT} = 0\text{mA}$, Duty = 100%, Cycle = $1\mu\text{s}$ at $V_{CC} = 5.5V$	1, 2, 3	I_{CC3}	--	15	mA
	$I_{OUT} = 0\text{mA}$, Duty = 100%, Cycle = 150ns at $V_{CC} = 5.5V$	1, 2, 3		--	50	
Input Voltage $\overline{RES_PIN}$		1, 2, 3	V_{IL}	--	0.8	V
			V_{IH}	2.2	--	
			V_H	$V_{CC}-0.5$	--	
Output Voltage	$I_{OL} = 2.1\text{ mA}$	1, 2, 3	V_{OL}	--	0.4	V
	$I_{OH} = -0.4\text{ mA}$		V_{OH}	2.4	--	
	$I_{OH} = -0.1\text{mA}$		V_{OH}	$V_{CC}-0.3V$		

1. I_{LI} on RES = 100 μA max.

TABLE 7. 28C011T AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION ¹
($V_{CC} = 5V \pm 10\%$, $T_A = -55$ TO $+125^\circ\text{C}$)

PARAMETER	SYMBOL	SUBGROUPS	MIN	MAX	UNITS
Address Access Time $\overline{CE} = OE = V_{IL}$, $\overline{WE} = V_{IH}$ -120 -150 -200	t_{ACC}	9, 10, 11			ns
Chip Enable Access Time $\overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$ -120 -150 -200	t_{CE}	9, 10, 11			ns
			--	120	
			--	150	
			--	200	

TABLE 7. 28C011T AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION ¹ $(V_{CC} = 5V \pm 10\%, T_A = -55 \text{ TO } +125 \text{ }^\circ\text{C})$

PARAMETER	SYMBOL	SUBGROUPS	MIN	MAX	UNITS
Output Enable Access Time $\overline{CE} = V_{IL}, \overline{WE} = V_{IH}$ -120 -150 -200	t_{OE}	9, 10, 11	0 0 0	75 75 100	ns
Output Hold to Address Change $\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$ -120 -150 -200	t_{OH}	9, 10, 11	0 0 0	-- -- --	ns
Output Disable to High-Z ² $\overline{CE} = V_{IL}, \overline{WE} = V_{IH}$ -120 -150 -200	t_{DF}	9, 10, 11	0 0 0	50 50 60	ns
$\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$ -120 -150 -200	t_{DFR}		0 0 0	300 350 450	
RES to Output Delay ³ $\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$ -120 -150 -200	t_{RR}	9, 10, 11	-- -- --	400 450 650	ns

1. Test conditions: Input pulse levels - 0.4V to 2.4V; input rise and fall times < 20ns; output load - 1 TTL gate + 100pF (including scope and jig); reference levels for measuring timing - 0.8V/1.8V.
2. t_{DF} and t_{DFR} are defined as the time at which the output becomes an open circuit and data is no longer driven.
3. Guaranteed by design.

TABLE 8. 28C011T AC ELECTRICAL CHARACTERISTICS FOR PAGE/BYTE ERASE AND BYTE WRITE OPERATIONS

 $(V_{CC} = 5V \pm 10\%, T_A = -55 \text{ TO } +125 \text{ }^\circ\text{C})$

PARAMETER	SYMBOL	SUBGROUPS	MIN ¹	MAX	UNITS
Address Setup Time -120 -150 -200	t_{AS}	9, 10, 11	0 0 0	-- -- --	ns
Chip Enable to Write Setup Time (\overline{WE} controlled) -120 -150 -200	t_{CS}	9, 10, 11	0 0 0	-- -- --	ns

TABLE 8. 28C011T AC ELECTRICAL CHARACTERISTICS FOR PAGE/BYTE ERASE AND BYTE WRITE OPERATIONS

($V_{CC} = 5V \pm 10\%$, $T_A = -55$ TO $+125$ °C)

PARAMETER	SYMBOL	SUBGROUPS	MIN ¹	MAX	UNITS
Write Pulse Width \overline{CE} controlled -120 -150 -200 \overline{WE} controlled -120 -150 -200	t_{CW}	9, 10, 11			ns
			200	--	
			250	--	
	t_{WP}		350	--	
			200	--	
			250	--	
Address Hold Time -120 -150 -200	t_{AH}	9, 10, 11			ns
			150	--	
			150	--	
			200	--	
Data Setup Time -120 -150 -200	t_{DS}	9, 10, 11			ns
			75	--	
			100	--	
			150	--	
Data Hold Time -120 -150 -200	t_{DH}	9, 10, 11			ns
			10	--	
			10	--	
			10	--	
Chip Enable Hold Time (\overline{WE} controlled) -120 -150 -2000	t_{CH}	9, 10, 11			ns
			0	--	
			0	--	
			0	--	
Write Enable to Write Setup Time (\overline{CE} controlled) -120 -150 -200	t_{WS}	9, 10, 11			ns
			0	--	
			0	--	
			0	--	
Write Enable Hold Time (\overline{CE} controlled) -120 -150 -200	t_{WH}	9, 10, 11			ns
			0	--	
			0	--	
			0	--	
Output Enable to Write Setup Time -120 -150 -200	t_{OES}	9, 10, 11			ns
			0	--	
			0	--	
			0	--	
Output Enable Hold Time -120 -150 -200	t_{OEH}	9, 10, 11			ns
			0	--	
			0	--	
			0	--	

TABLE 8. 28C011T AC ELECTRICAL CHARACTERISTICS FOR PAGE/BYTE ERASE AND BYTE WRITE OPERATIONS

($V_{CC} = 5V \pm 10\%$, $T_A = -55$ TO $+125$ °C)

PARAMETER	SYMBOL	SUBGROUPS	MIN ¹	MAX	UNITS
Write Cycle Time ² -120 -150 -200	t_{WC}	9, 10, 11	-- -- --	10 10 10	ms
Data Latch Time -120 -150 -200	t_{DL}	9, 10, 11	250 300 400	-- -- --	ns
Byte Load Window -120 -150 -200	t_{BL}	9, 10, 11	100 100 200	-- -- --	μ s
Byte Load Cycle -120 -150 -200	t_{BLC}	9, 10, 11	0.55 0.55 0.95	30 30 30	μ s
Time to Device Busy -120 -150 -200	t_{DB}	9, 10, 11	100 120 170	-- -- --	ns
Write Start Time ³ -120 -150 -200	t_{DW}	9, 10, 11	150 150 250	-- -- --	ns
RES to Write Setup Time -120 -150 -200	t_{RP}	9, 10, 11	100 100 200	-- -- --	μ s
V_{CC} to RES Setup Time ⁴ -120 -150 -200	t_{RES}	9, 10, 11	1 1 3	-- -- --	μ s

1. Use this device in a longer cycle than this value.
2. t_{WC} must be longer than this value unless polling techniques or RDY/BUSY are used. This device automatically completes the internal write operation within this value.
3. Next read or write operation can be initiated after t_{DW} if polling techniques or RDY/BUSY are used.
4. Gauranteed by design.

TABLE 9. 28C011T MODE SELECTION ¹

PARAMETER	\overline{CE}	\overline{OE}	\overline{WE}	I/O	\overline{RES}	RDY/ \overline{BUSY}
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	V_H	High-Z
Standby	V_{IH}	X	X	High-Z	X	High-Z
Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}	V_H	High-Z --> V_{OL}
Deselect	V_{IL}	V_{IH}	V_{IH}	High-Z	V_H	High-Z
Write Inhibit	X	X	V_{IH}	--	X	--
	X	V_{IL}	X	--	X	--
Data Polling	V_{IL}	V_{IL}	V_{IH}	Data Out (I/O7)	V_H	V_{OL}
Program	X	X	X	High-Z	V_{IL}	High-Z

1. X = Don't care.

FIGURE 1. READ TIMING WAVEFORM

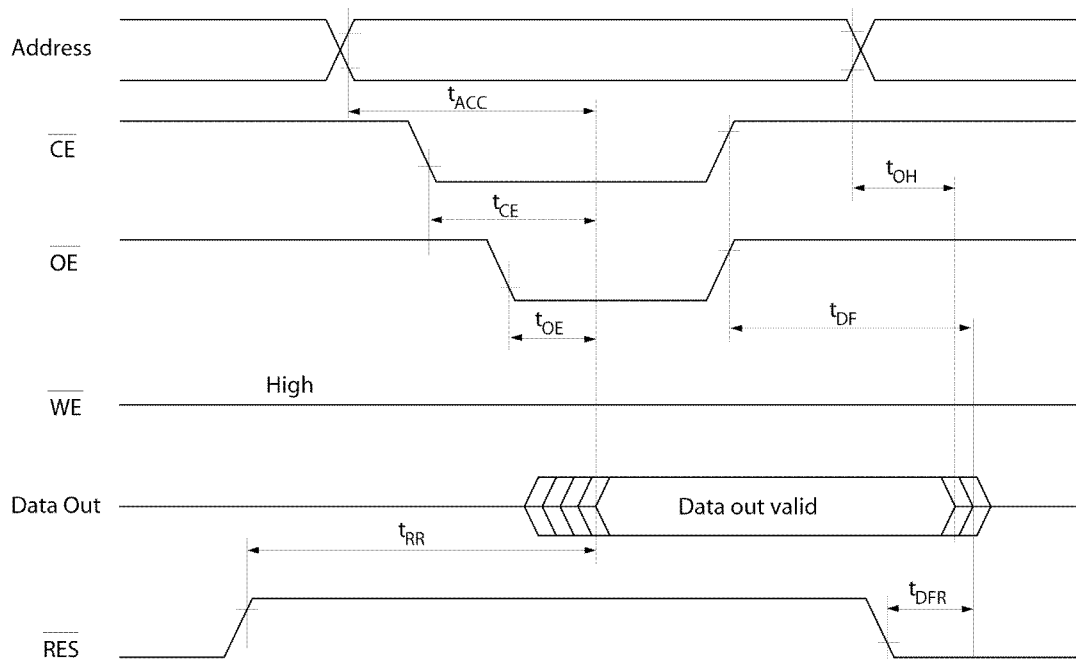


FIGURE 2. BYTE WRITE TIMING WAVEFORM(1) (\overline{WE} CONTROLLED)

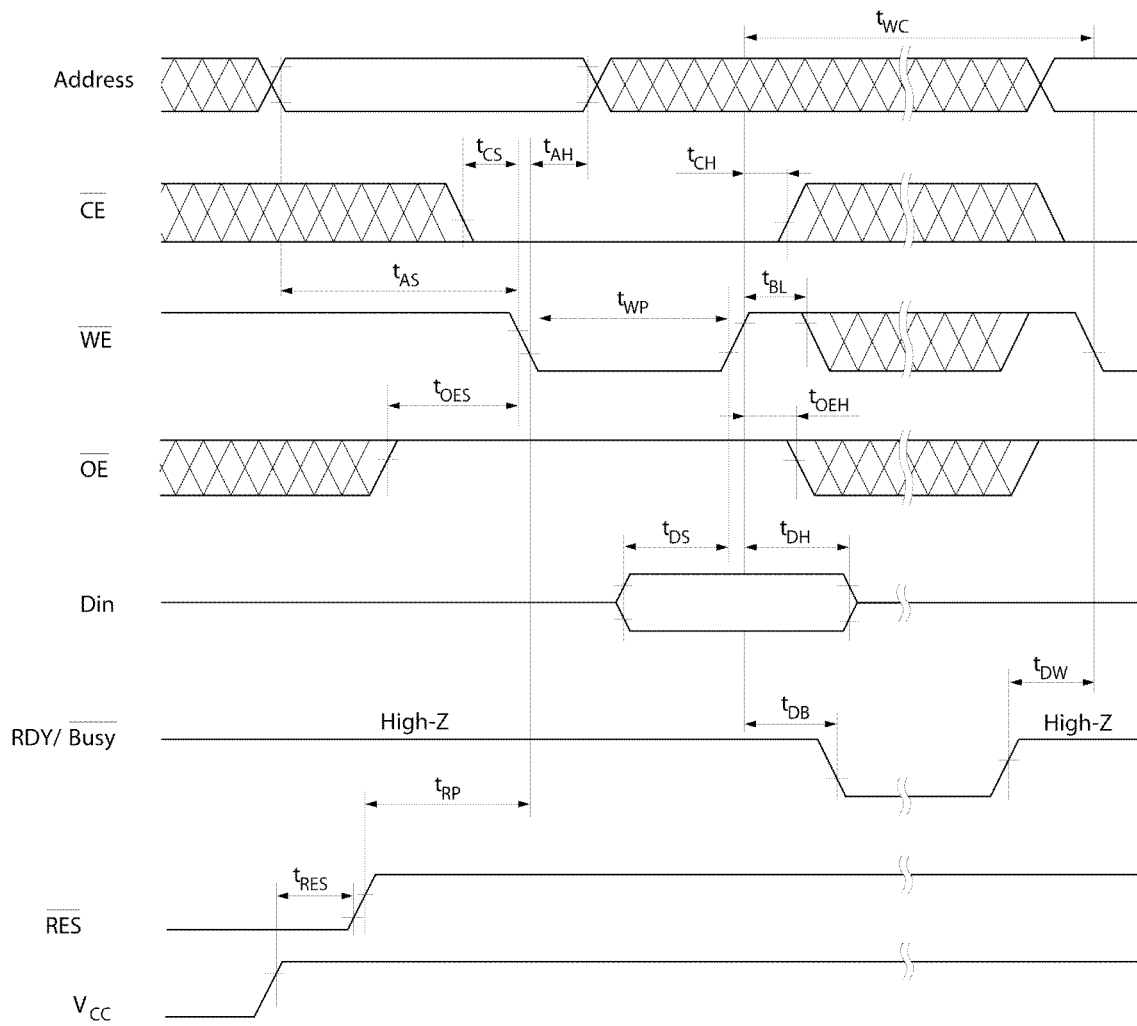


FIGURE 3. BYTE WRITE TIMING WAVEFORM (2) (\overline{CE} CONTROLLED)

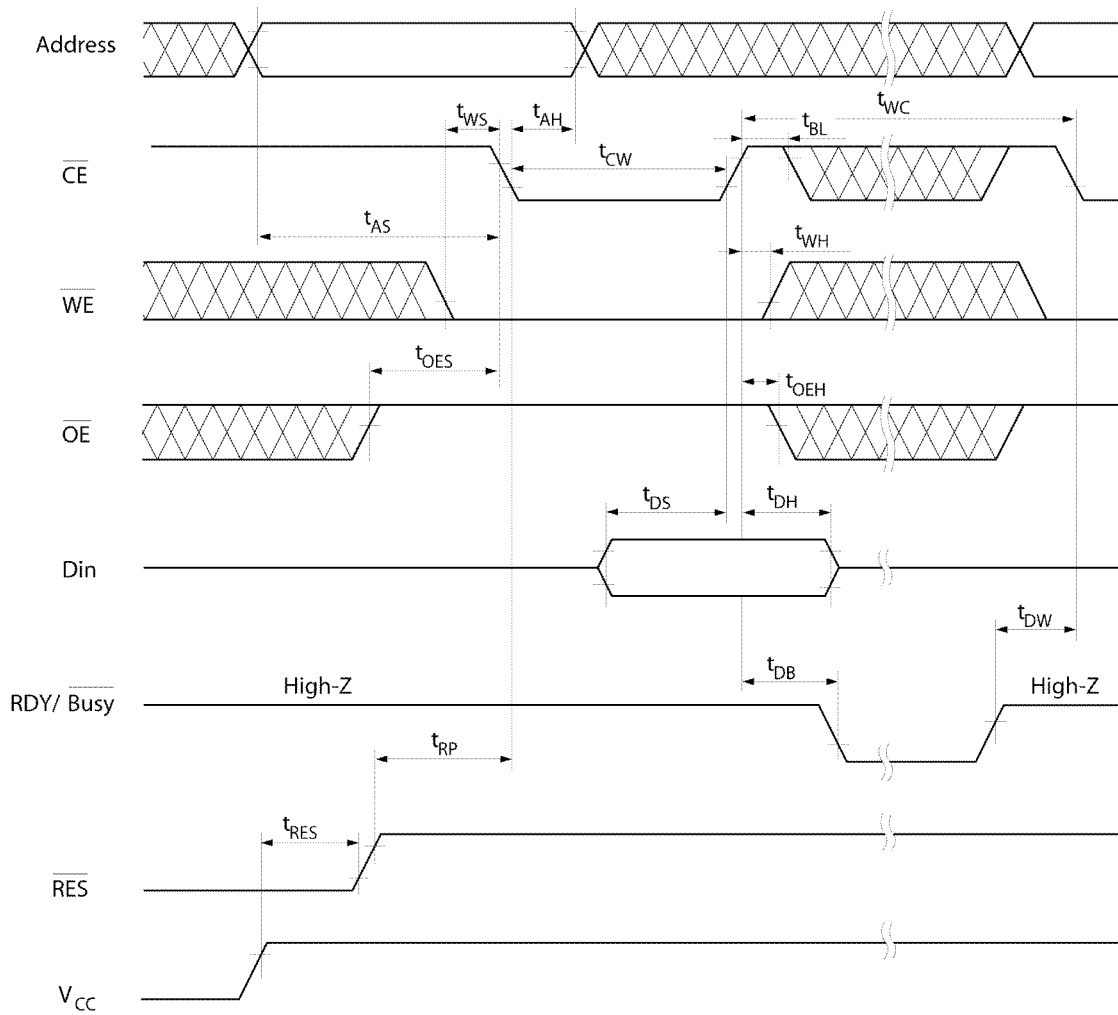


FIGURE 4. PAGE WRITE TIMING WAVEFORM(1) (\overline{WE} CONTROLLED)

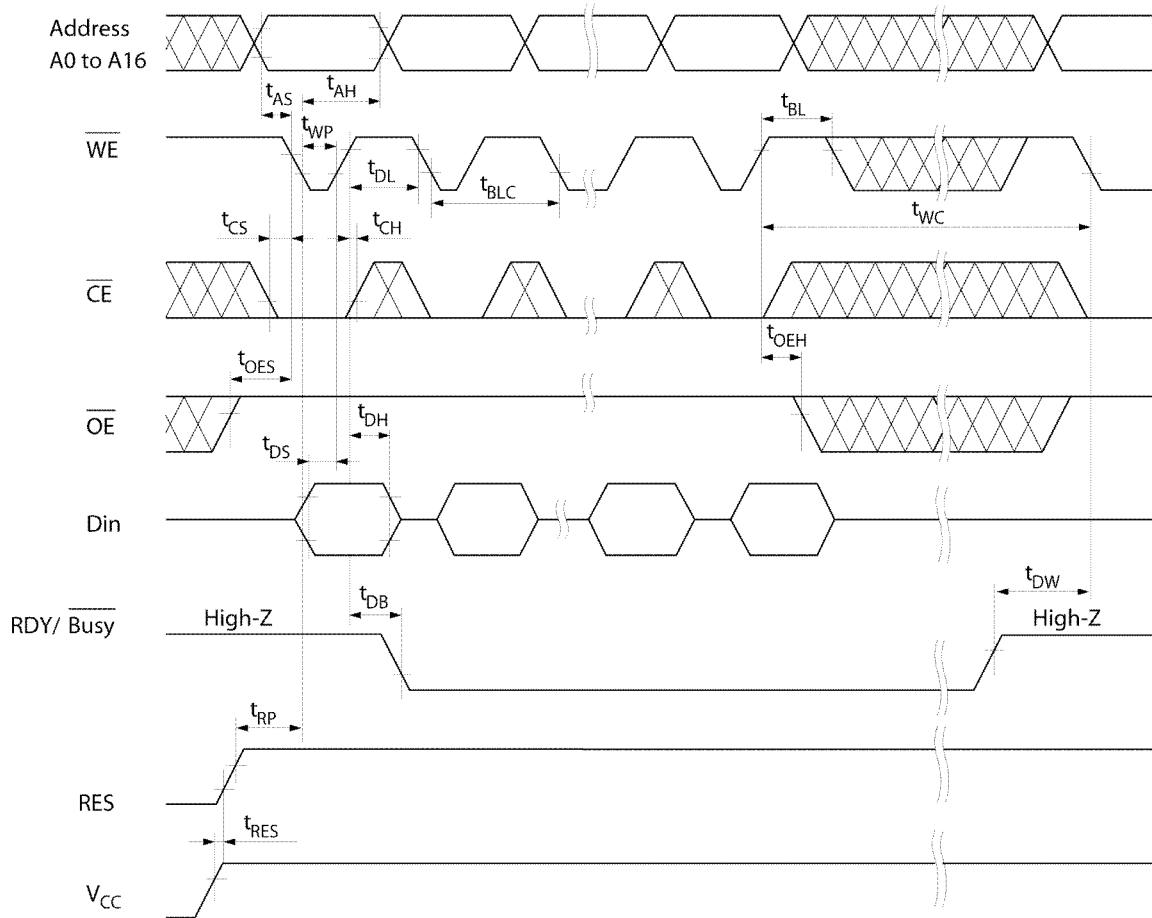


FIGURE 5. PAGE WRITE TIMING WAVEFORM(2) (\overline{CE} CONTROLLED)

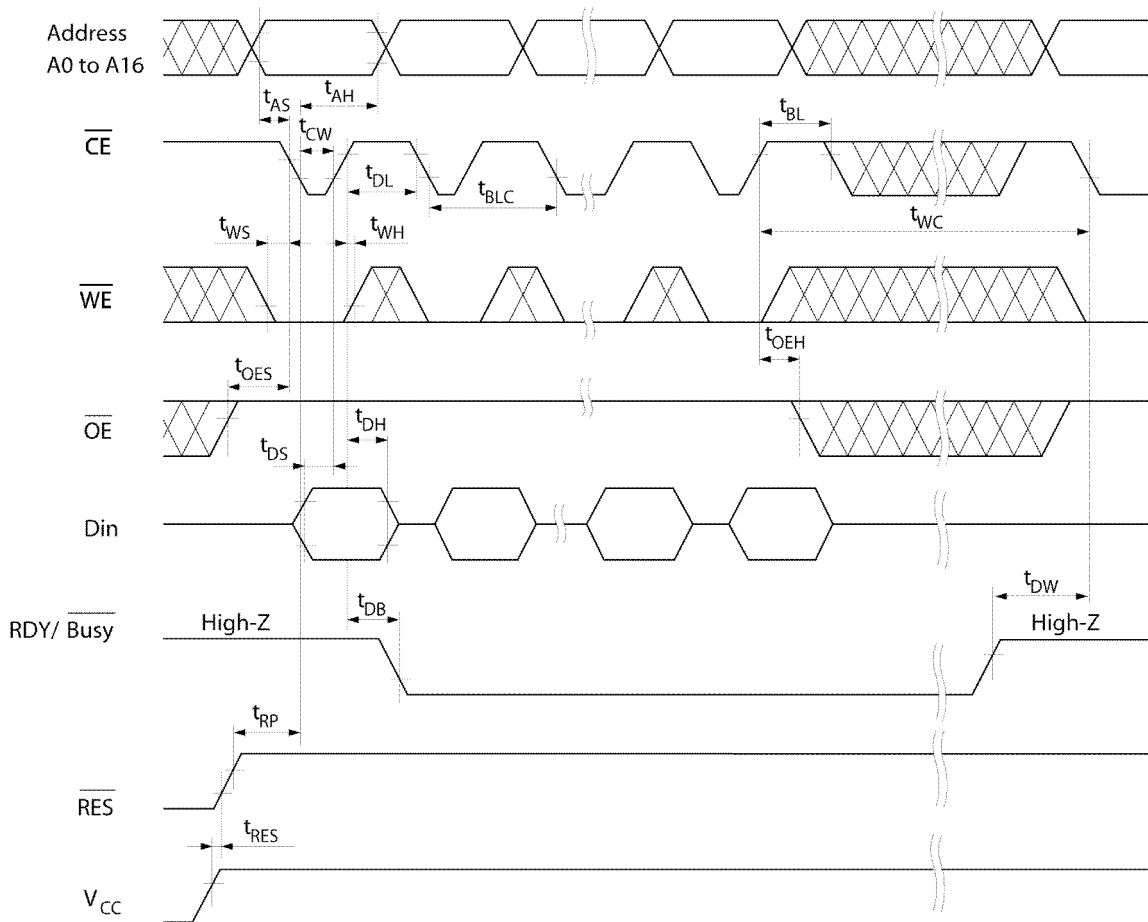


FIGURE 6. DATA POLLING TIMING WAVEFORM

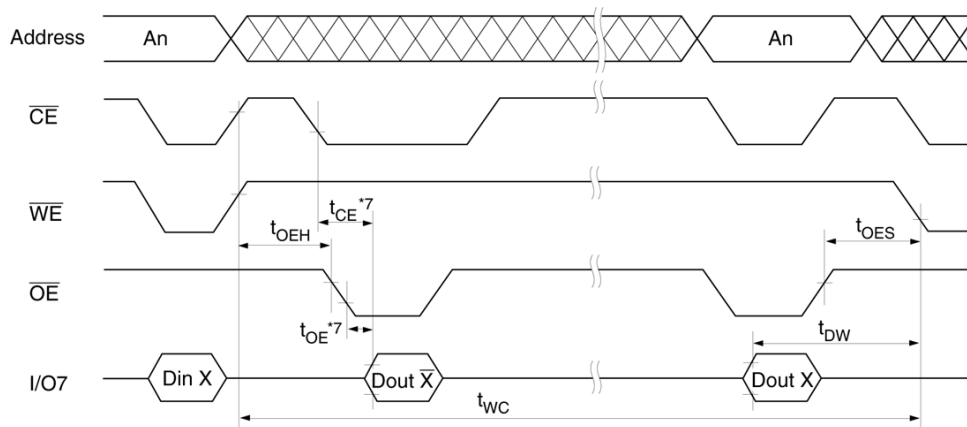


FIGURE 7. SOFTWARE DATA PROTECTION TIMING WAVEFORM(1) (IN PROTECTION MODE)

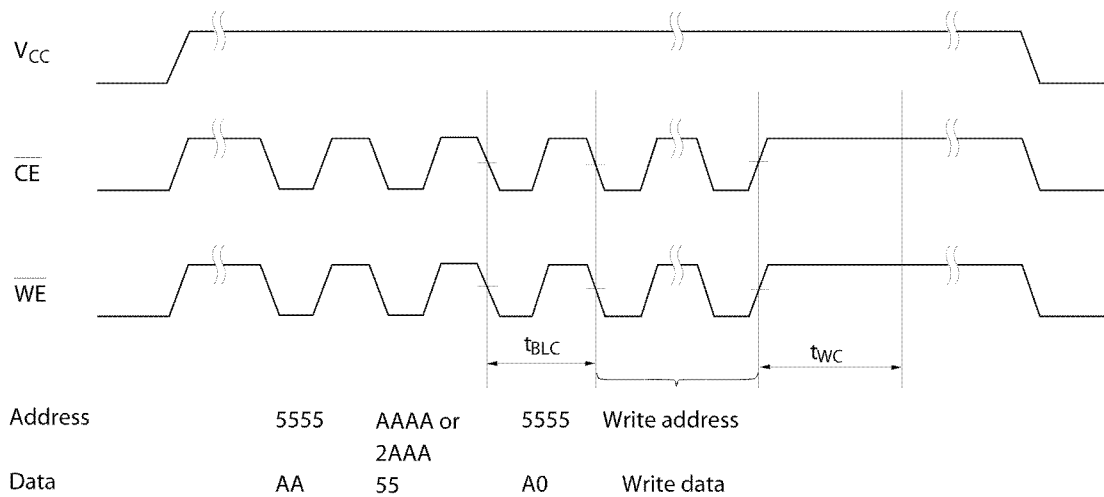
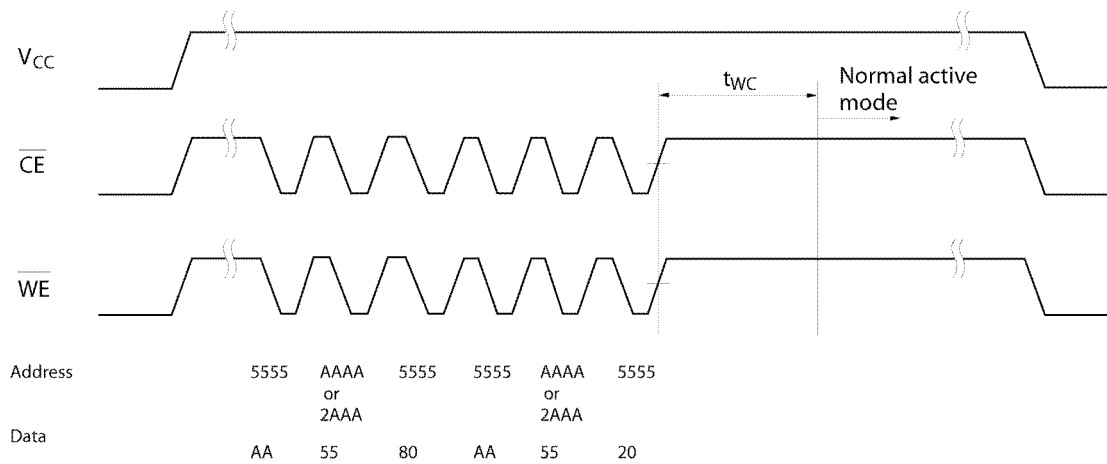


FIGURE 8. SOFTWARE DATA PROTECTION TIMING WAVEFORM(2) (IN NON-PROTECTION MODE)



EEPROM APPLICATION NOTES

This application note describes the programming procedures for the EEPROM modules and with details of various techniques to preserve data protection.

Automatic Page Write

Page-mode write feature allows 1 to 128 bytes of data to be written into the EEPROM in a single write cycle, and allows the undefined data within 128 bytes to be written corresponding to the undefined address (A0 to A6). Loading the first byte of data, the data load window opens 30µs for the second byte. In the same manner each additional byte of data can be loaded within 30µs. In case CE and WE are kept high for 100 µs after data input, EEPROM enters erase and write mode automatically and only the input data are written into the EEPROM.

\overline{WE} , \overline{CE} Pin Operation

During a write cycle, addresses are latched by the falling edge of \overline{WE} or \overline{CE} , and data is latched by the rising edge of \overline{WE} or \overline{CE} .

Data Polling

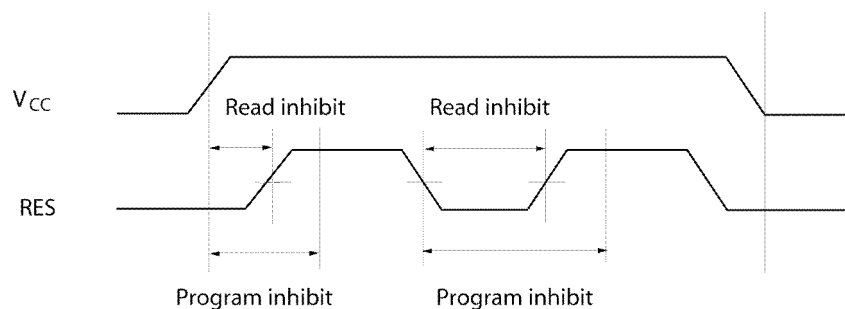
Data Polling function allows the status of the EEPROM to be determined. If EEPROM is set to read mode during a write cycle, an inversion of the last byte of data to be loaded outputs from I/O 7 to indicate that the EEPROM is performing a write operation.

RDY/ \overline{Busy} Signal

RDY/ \overline{Busy} signal also allows a comparison operation to determine the status of the EEPROM. The RDY/ \overline{Busy} signal has high impedance except in write cycle and is lowered to V_{OL} after the first write signal. At the end of a write cycle, the RDY/ \overline{Busy} signal changes state to high impedance.

\overline{RES} Signal

When \overline{RES} is LOW, the EEPROM cannot be read and programmed. Therefore, data can be protected by keeping \overline{RES} low when V_{CC} is switched. \overline{RES} should be high during read and programming because it doesn't provide a latch function.

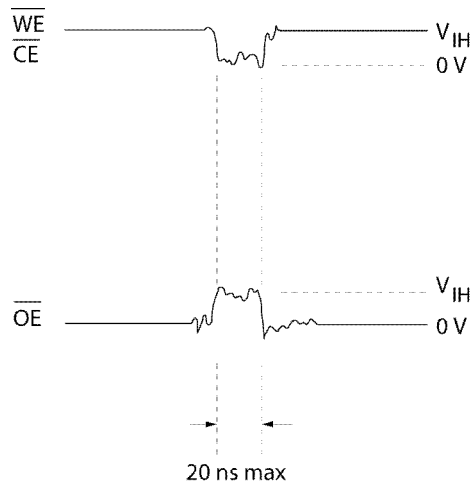


Data Protection

To protect the data during operation and power on/off, the EEPROM has the internal functions described below.

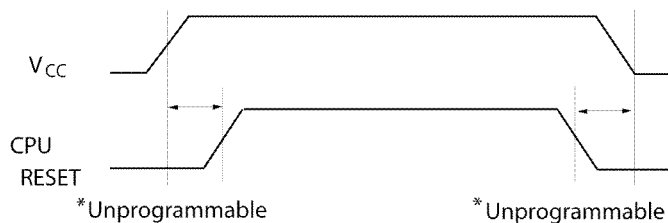
1. Data Protection against Noise of Control Pins (\overline{CE} , \overline{OE} , \overline{WE}) during Operation.

During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to programming mode by mistake. To prevent this phenomenon, the EEPROM has a noise cancellation function that cuts noise if its width is 20ns or less in programming mode. Be careful not to allow noise of a width of more than 20ns on the control pins.

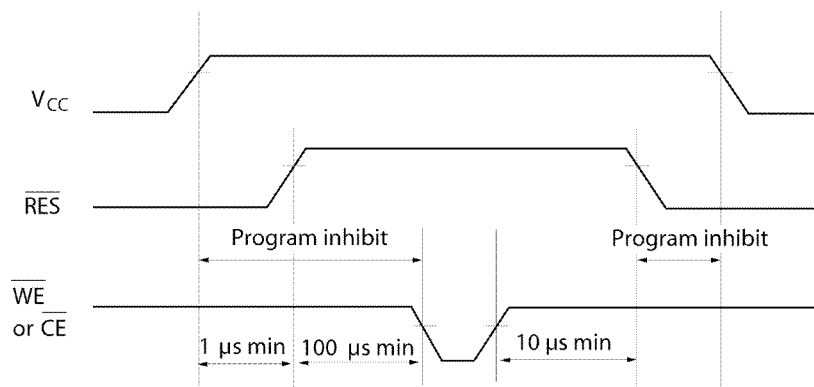


2. Data Protection at V_{CC} on/off

When V_{CC} is turned on or off, noise on the control pins generated by external circuits, such as CPUs, may turn the EEPROM to programming mode by mistake. To prevent this unintentional programming, the EEPROM must be kept in unprogrammable state during V_{CC} on/off by using a CPU reset signal to \overline{RES} pin.



\overline{RES} should be kept at V_{SS} level when V_{CC} is turned on or off. The EEPROM breaks off programming operation when \overline{RES} become low, programming operation doesn't finish correctly in case that \overline{RES} falls low during programming operation. \overline{RES} should be kept high for 10 ms after the last data input.

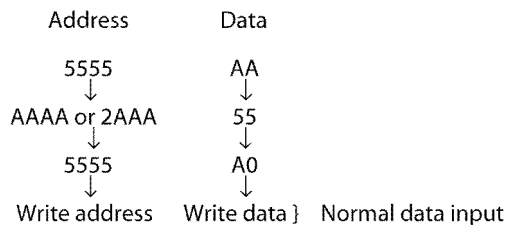


3. Software Data Protection

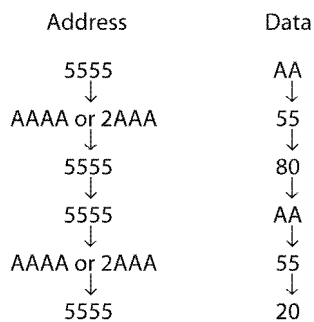
1 Megabit (128K x 8-Bit) EEPROM

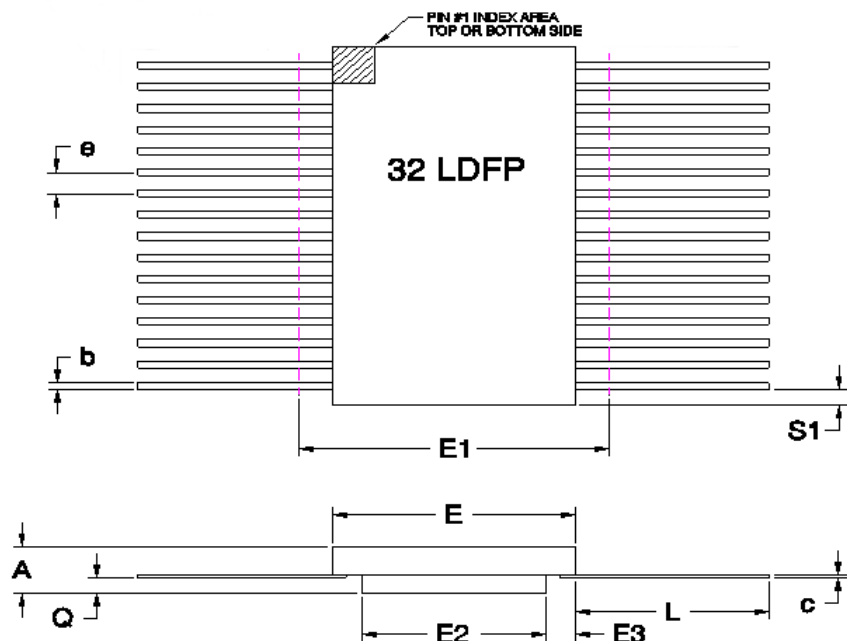
28C011T

The software data protection function is to prevent unintentional programming caused by noise generated by external circuits. In software data protection mode, 3 bytes of data must be input before write data as follows. These bytes can switch the non-protection mode to the protection mode.



Software data protection mode can be canceled by inputting the following 6 bytes. Then, the EEPROM turns to the non-protection mode and can write data normally. However, when the data is input in the canceling cycle, the data cannot be written.

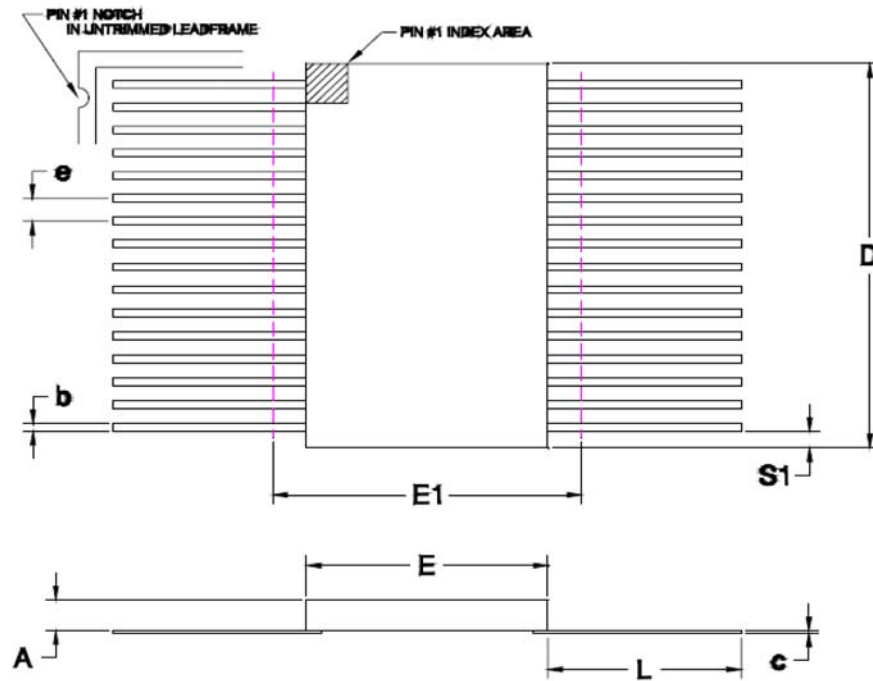




32-PIN RAD-PAK® FLAT PACKAGE

SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	0.117	0.130	0.143
b	0.015	0.017	0.022
c	0.004	0.005	0.009
D	--	0.820	0.830
E	0.404	0.410	0.416
E1	--	--	0.440
e	0.050BSC		
L	0.350	0.370	0.390
Q	0.021	0.033	0.036
S1	0.005	0.027	--
N	32		

Note: All dimensions in inches
 Top and Bottom of the package are connected internally to ground.



28C011T 32-PIN RAD-TOLERANT FLAT PACKAGE

SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	0.078	0.087	0.096
b	0.015	0.017	0.022
c	0.004	0.005	0.009
D	--	0.820	0.830
E	0.404	0.410	0.416
E1	--	--	0.426
e	0.050BSC		
L	0.390	0.400	0.410
Q	0.020	0.035	0.045
S1	0.005	0.027	--
N	32		

Note: All dimensions in inches.

Top and Bottom of the package are connected internally to ground.

Important Notice:

These data sheets are created using the chip manufacturers published specifications. DDC verifies functionality by testing key parameters either by 100% testing, sample testing or characterization.

The specifications presented within these data sheets represent the latest and most accurate information available to date. However, these specifications are subject to change without notice and DDC assumes no responsibility for the use of this information.

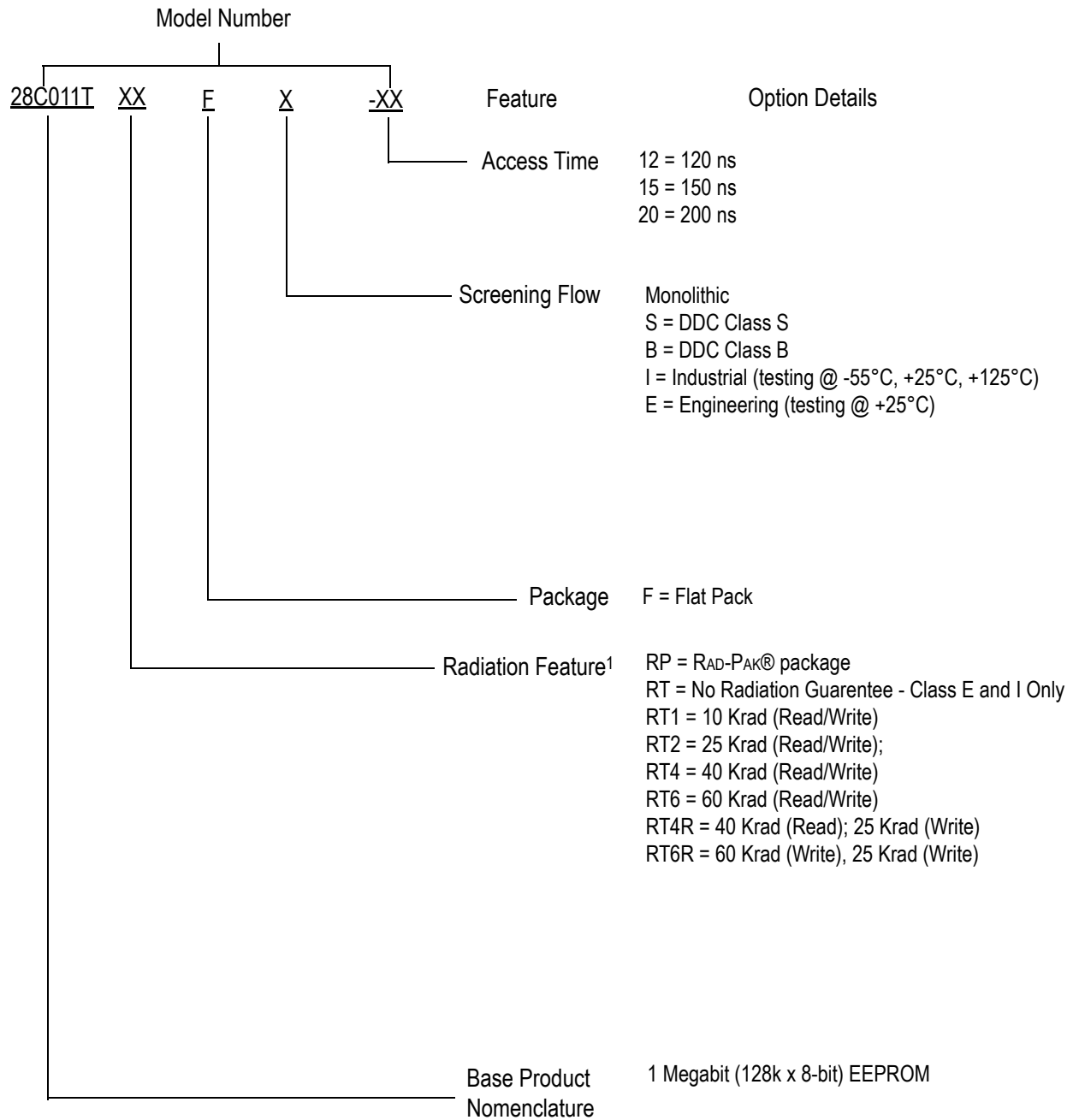
DDC's products are not authorized for use as critical components in life support devices or systems without express written approval from DDC.

Any claim against DDC must be made within 90 days from the date of shipment from DDC
DDC's liability shall be limited to replacement of defective parts.

1 Megabit (128K x 8-Bit) EEPROM

28C011T

Product Ordering Options



- 1) Products are manufactured and screened to DDC's self-defined Class B and Class S.
- 2) The device will meet the specified read mode TID level, at the die level, if it is not written to during irradiation. Writing to the device during irradiation will reduce the device's TID tolerance to the specified write mode TID level. Writing to the device before irradiation does not alter the device's read mode TID level.