Document Title

2Mx16 bit Low Low Power 1T/1C Pseudo SRAM

Revision History

Revision No.	History	Draft Date	Remark
0.0	Initial Draft	Jan. 2004	Preliminary
1.0	Addition : Power-up timing diagram (page 06)	Apr. 2005	Preliminary

2M x 16 bit Low Low Power 1T/1C SRAM

DESCRIPTION

The HY64SD16322B is a 32Mbit 1T/1C SRAM featured by high-speed operation and super low power consumption. The HY64SD16322B adopts one transistor memory cell and is organized as 2,097,152 words by 16bits. The HY64SD16322B operates in the extended range of temperature and supports a wide operating voltage range. The HY64SD16322B also supports the deep power down mode for a super low standby current. The HY64SD16322B delivers the high-density low power SRAM capability to the high-speed low power system.

FEATURES

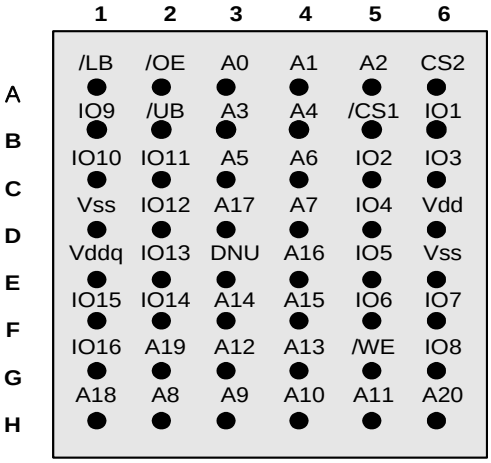
- CMOS Process Technology
- 2M x 16 Bit Organization
- Three State Outputs
- Deep Power Down : Memory Cell Data Hold Invalid
- Standard Pin Configuration : 48-FBGA(6mmX8mm)
- Data Mask Function by /LB, /UB

PRODUCT FAMILY

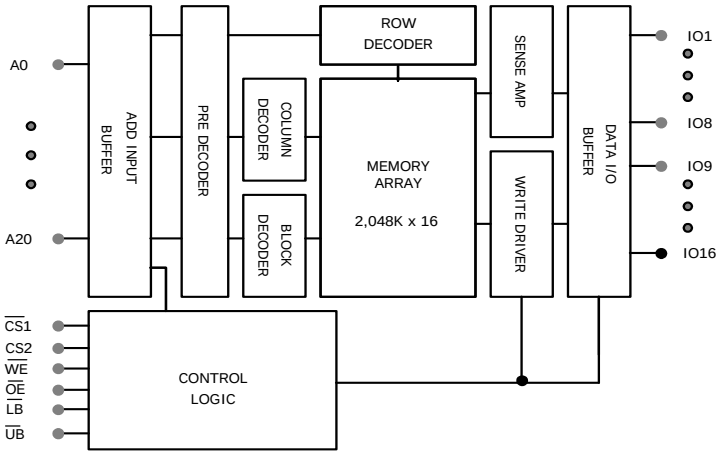
Product No.	Voltage [V]	Mode	Power Dissipation			Speed tRC[ns]	Temp. [℃]
			(ISB1, Max)	(IDPD, Max)	(ICC2, Max)		
HY64SD16322B-DF85E	1.8~1.95	1CS with /UB, /LB:tCS[1]	120	5uA	20mA	85	-25~85
HY64SD16322B-DF85I			120	5uA	20mA	85	-40~85

Note: 1. tCS - /UB, /LB=High: Chip Deselect.

PIN CONNECTION(Top View)



BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Speed [ns]	Power	Temperature	Package
HY64SD16322B-E	85	LL-Part	E[1]	FBGA
HY64SD16322B-I	85	LL-Part	I[2]	FBGA

Note: 1. E: Extended Temp. (-25℃~85℃)

2. I: Industrial Temp. (-40℃~85℃)

ORDERING INFORMATION

Symbol	Parameter	Rating	Unit	Remark
V_{IN}	Input Voltage	-0.3 to 2.5	V	
V_{OUT}	Output Voltage	-0.3 to 2.5	V	
Vdd	Power Supply	-0.3 to 2.5	V	
T_A	Ambient Temperature	-25 to 85	℃	HY64SD16322B-E
		-40 to 85	℃	HY64SD16322B-I
T_{STG}	Storage Temperature	-55 to 150	℃	
P_D	Power Dissipation	1.0	W	
T_{SOLDER}	Ball Soldering Temperature & Time	260·10	°C · sec	

Note: 1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and the functional operation of the device under these or any other conditions above those indicated in the operation of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect reliability.

TRUTH TABLE

/CS1	CS2	/WE	/OE	/LB	/UB	MODE	I/O PIN		Power
							I/O1~I/O8	I/O9~I/O16	
H	H	X	X	X	X	Deselected	High-Z	High-Z	Standby
X	H	X	X	H	H	Deselected	High-Z	High-Z	Standby
X	L	X	X	X	X	Deselected	High-Z	High-Z	Deep Power Down
L	H	H	H	X	X	Output Disabled	High-Z	High-Z	Active
L	H	H	L	L	L	Read	Dout	Dout	Active
				L	H		Dout	High-Z	Active
				H	L		High-Z	Dout	Active
L	H	L	X	L	L	Write	Din	Din	Active
				L	H		Din	High-Z	Active
				H	L		High-Z	Din	Active

Note: 1. See Mode Register Setting Entry/Exit Timing on page 8.

2. See Deep Power Down Mode Entry/Exit Timing on page8.

3. H=V_{IH}, L=V_{IL}, X=Don't Care (V_{IL} or V_{IH})

RECOMMENDED DC OPERATING CONDITION

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vdd	Power Supply	1.8	-	1.95	V
Vss	Ground	0	-	0	V
V_{IH}	Input High Voltage	1.4	-	Vdd+0.3	V
V_{IL}	Input Low Voltage	-0.2[1]	-	0.4	V

Note: 1. V_{IL}=-1.5V for pulse width less than 10ns.

Undershoot is sampled, not 100% tested.

RECOMMENDED DC OPERATING CONDITION

Vdd=1.8V~1.95V, T_A=-25℃ to 85℃(E) / -40℃ to 85℃(I)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I_{LI}	Input Leakage Current	$V_{SS} \le V_{IN} \le$ Vdd	-1	1	uA
I_{LO}	Output Leakage Current	$V_{SS} \le V_{IO} \le$ Vdd, /CS1=V_{IH}, CS2=V_{IH}, /OE=V_{IH} or /WE=V_{IL}	-1	1	uA
ICC	Operating Power Supply Current	/CS1=V_{IL}, CS2=V_{IH}, V_{IN}=V_{IH} or V_{IL}, $I_{I/O}$=0mA	-	3	mA
ICC1	Average Operating Current	/CS1 ≤ 0.2V, CS2 ≥ Vdd-0.2V, $V_{IN} \le$ 0.2V or $V_{IN} \ge$ Vdd-0.2V, Cycle Time=1us. 100% Duty, $I_{I/O}$=0mA	-	5	mA
ICC2		/CS1=V_{IL}, CS2=V_{IH}, V_{IN}=V_{IH} or V_{IL}, Cycle Time=Min., 100% Duty, $I_{I/O}$=0mA	-	20	mA
ISB1	Standby Current (CMOS Input)	/CS1,CS2Vdd-0.2V, /UB,/LB≤0.2V or /UB, /LB≥Vdd-0.2V, otherwise CS2, /UB, /LB ≥ Vdd-0.2V, /CS1 ≤ 0.2V or /CS1 ≥ Vdd-0.2V	-	120	uA
I_{DPD}	Deep Power Down	CS2 ≤ VSS+0.2V	-	5	uA
V_{OH}	Output High Voltage	IOH=-0.1mA	1.4	-	V
V_{OL}	Output Low Voltage	IOL=0.1mA	-	0.2	V

CAPACITANCE

(Temp.=25℃, f=1.0MHz)

Symbol	Parameter	Condition	Max.	Unit
C_{IN}	Input Capacitance (ADD, /CS1, CS2, /WE, /OE, /UB, /LB)	V_{IN}=0V	8	pF
C_{OUT}	Output Capacitance (I/O)	$V_{I/O}$=0V	10	pF

Note: 1. These parameters are sampled and not 100% tested.

AC CHARACTERISTICS

Vdd=1.8V~1.95V, TA=-25℃ to 85℃(E) / -40℃ to 85℃(I), unless otherwise specified

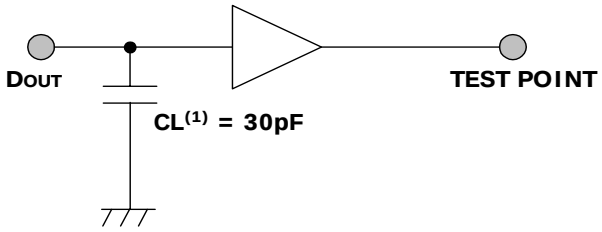
#	Symbol	Parameter	Speed		Unit
Read Cycle			**Min**	**Max**	
1	tRC	Read Cycle Time	85	10,000	ns
2	tAA	Address Access Time	-	85	ns
3	tACS	Chip Select Access Time	-	85	ns
4	tOE	Output Enable to Output Valid	-	35	ns
5	tBA	/LB, /UB Access Time	-	85	ns
6	tCLZ	Chip Select to Output in Low Z	10	-	ns
7	tOLZ	Output Enable to Output in Low Z	5	-	ns
8	tBLZ	/LB, /UB Enable to Output in Low Z	10	-	ns
9	tCHZ	Chip Disable to Output in High Z	0	25	ns
10	tOHZ	Output Disable to Output in High Z	0	25	ns
11	tBHZ	/LB, /UB Disable to Output in High Z	0	25	ns
12	tOH	Output Hold from Address Change	5	-	ns
Write Cycle			**Min**	**Max**	
1	tWC	Write Cycle Time	85	10,000	ns
2	tCW	Chip Selection to End of Write	75	-	ns
3	tAW	Address Valid to End of Write	75	-	ns
4	tBW	/LB, /UB Valid to End of Write	75	-	ns
5	tAS	Address Set-up Time	0	-	ns
6	tWP	Write Pulse Width	60	-	ns
7	tWR	Write Recovery Time	0	-	ns
8	tWHZ	Write to Output in High Z	0	25	ns
9	tDW	Data to Write Time Overlap	30	-	ns
10	tDH	Data Hold from Write Time	0	-	ns
11	tOW	Output Active from End of Write	5	-	ns

AC TEST CONDITIONS

TA=-25℃ to 85℃(E) / -40℃ to 85℃(I), unless otherwise specified

Parameter	Value
Input Pulse Level	0.2V to (Vcc-0.2)V
Input Rising and Fall Time	5ns
Input Timing Reference Level	Vcc/2
Output Timing Reference Level	Vcc/2
Output Load	See Below

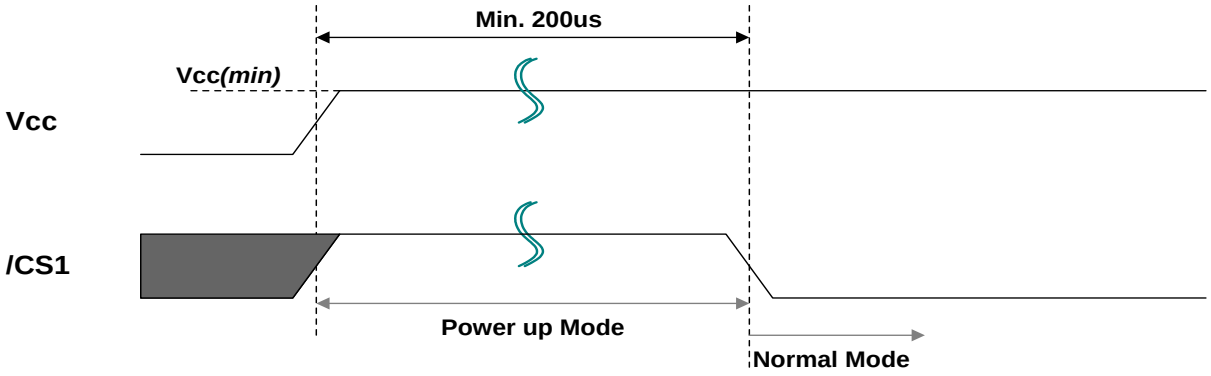
AC TEST LOADS



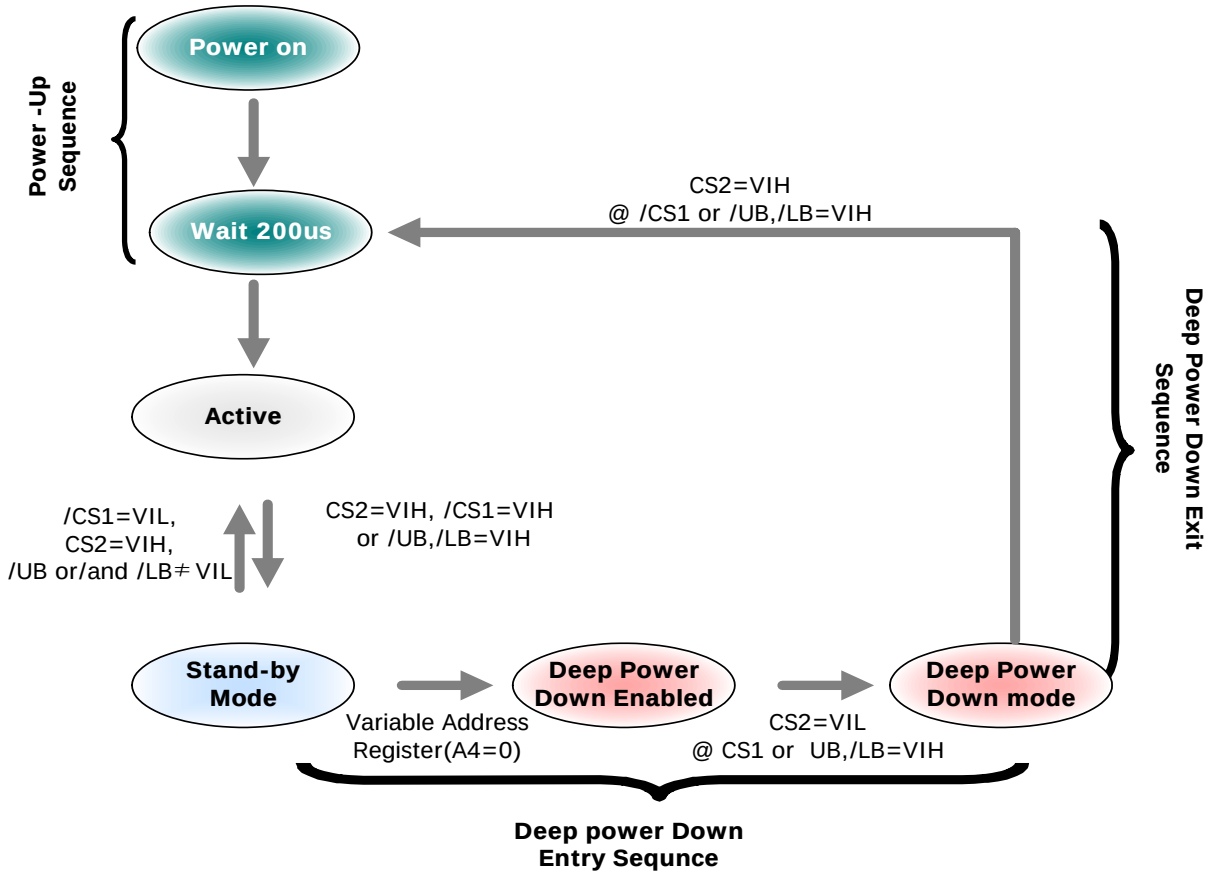
Note: 1. Include jig and scope capacitance.

POWER-UP SEQUENCE

1. Supply power with /CS1 high.
2. Maintain stable power for longer than 200us with /CS1 high.



STATE DIAGRAM



STANDBY MODE CHARACTERISTICS

Mode	Memory Cell Data	Standby Current[uA]	Wait Time[us]
Standby	Valid	120	0
Deep Power Down	Invalid	5	200

MODE REGISTER SET

VARIABLE ADDRESS REGISTER

A20-A6	A5	A4	A3-A0

Reserved: A20-A6, A3-A0

Mode Set	Address Pin	Code	Setting
Deep Power Down Mode Enable / Disable	A4	L	Deep Power Down Mode Enabled
		H	Deep Power Down Mode Disabled (Default)
Special Mode	A5	L	MRS Mode (Default)
		H	Special Test Mode

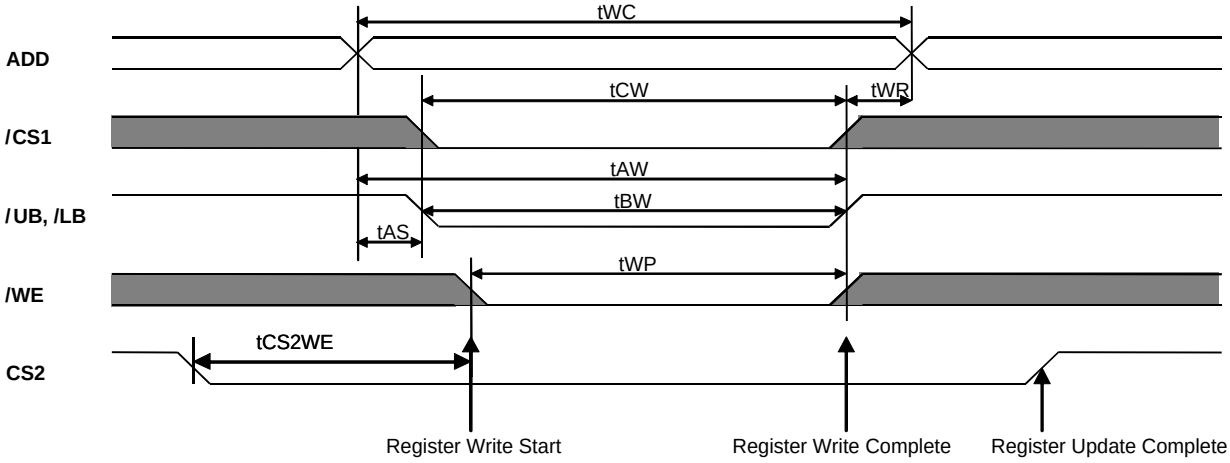
Note: 1. H=VIH, L=VIL, X=Don't Care (VIL or VIH)

2. The MRS mode is set by using timing diagram shown on the next page. The MRS mode is enabled after CS2 goes high and remains enabled after CS2 goes high. To change to a different mode, the variable address register will have to be rewritten.

3. The Deep Power Down function is not standard for the Hynix part. The part will default to Deep Power Down Disabled. If the variable address register is written to enable the Deep Power Down function, the part will go into Deep Power Down Mode during the following time that CS2 is driven low and there is no variable address register update. When CS2 is driven high, all of the register settings will return to default state for the part (i.e. full array refresh, Deep Power Down Disabled.)

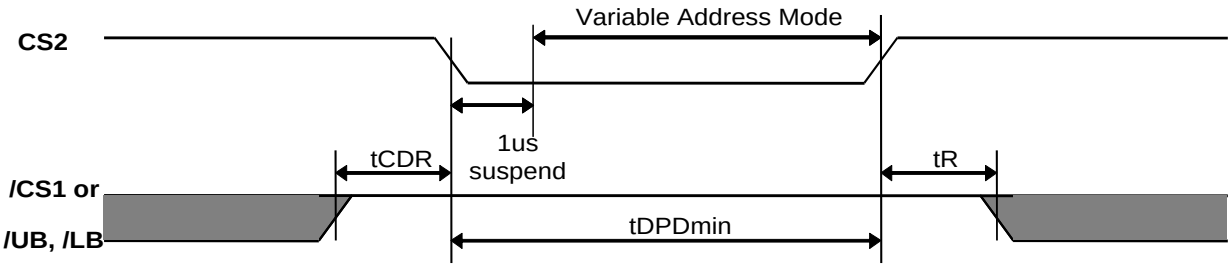
LOW POWER MODE

VARIABLE ADDRESS REGISTER UPDATE TIMING



Note : The register update takes place on the rising edge of CS2. Once the register is updated, the next time CS2 goes low, without any updates to the register starting within the tCS2WE max time of 1?s, the part will refresh the array selected. The data bus is a don't care when CS2 is low during the register updates.

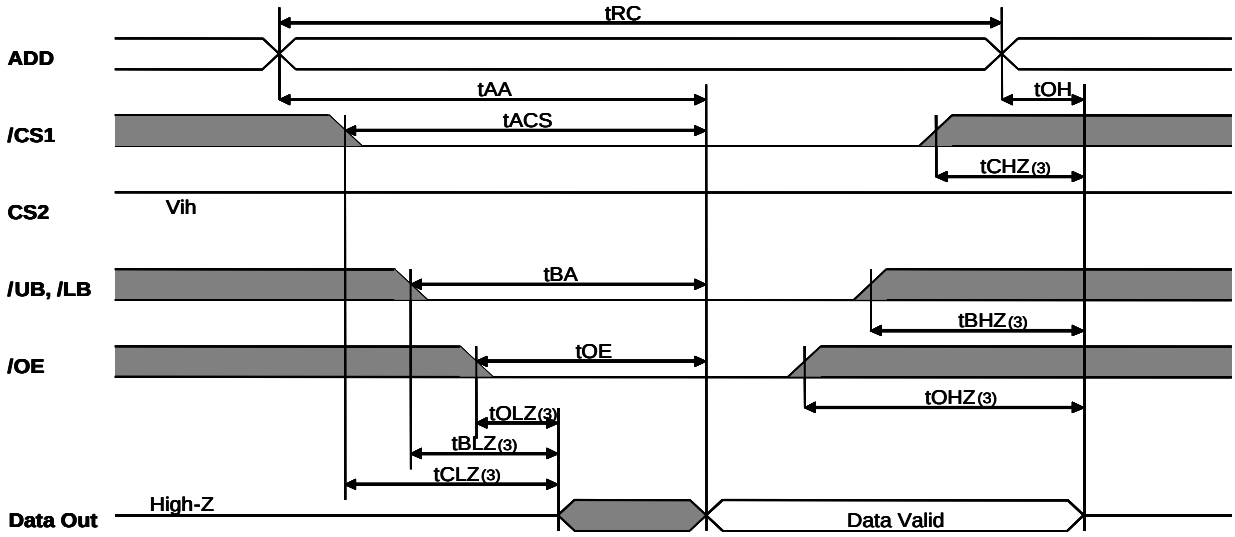
DEEP POWER DOWN MODE ENTRY/EXIT TIMING



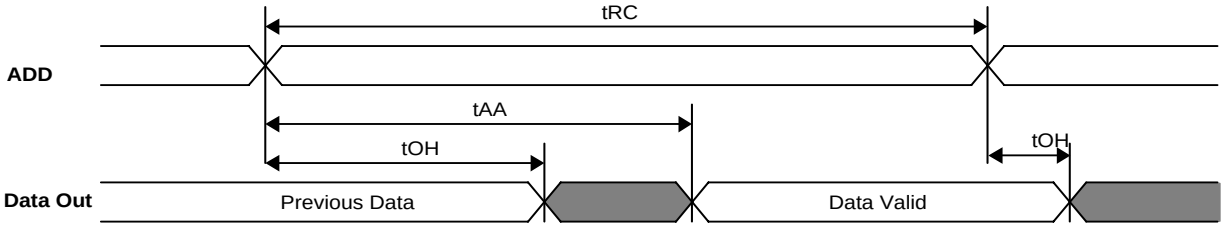
Parameter	Array On/Off	Min	Max	Units
tCS2WE	CS2 Low to Write Enable Low		1000	ns
tCDR	Chip Deselect to CS2 Low	0		ns
tR	Operation Recovery Time		200(Deep Power Down Mode Only)	us
tDPDmin	Deep Power Down Mode Time	10		us

TIMING DIAGRAM

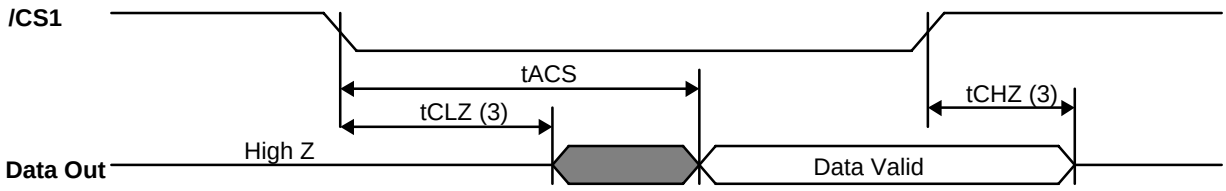
READ CYCLE 1 (Note 1, 4)



READ CYCLE 2 (Note 1, 2, 4) (CS2=Vih)



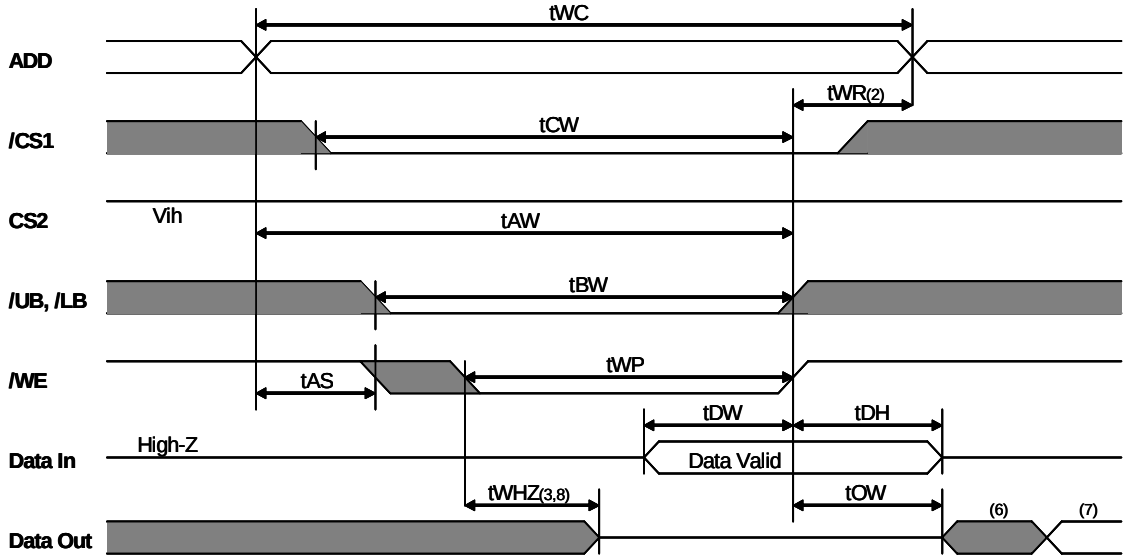
READ CYCLE 3 (Note 1, 2, 4)(CS2=Vih)



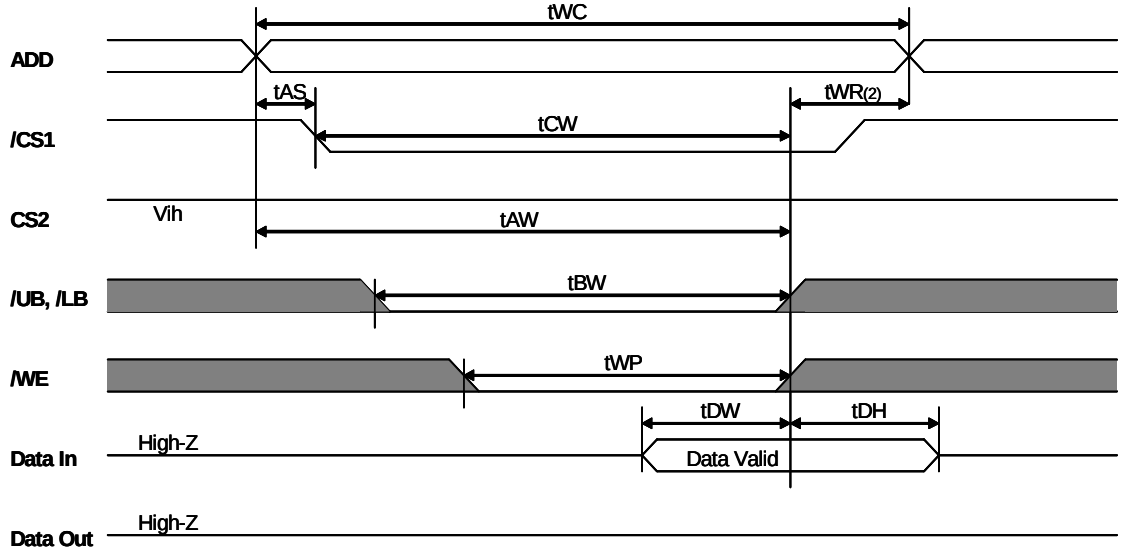
Notes :

1. Read Cycle occurs whenever a high on the /WE and /OE is low, while /UB and/or /LB and /CS1 and CS2 are in active status.
2. /OE = VIL
3. tCHZ, tBHZ and tOHZ are defined as the time at which the outputs achieve the high impedance state and tOLZ,tBLZ and tCLZ are defined as the time at which the outputs achieve the low impedance state. These are not referenced to output voltage levels. At any given temperature and voltage condition, tCHZ(Max.) is less than tCLZ(Min.) both for a given device and from device to device interconnection.
4. /CS1 is high for the standby, low for active. /UB and /LB are high for the standby, low for active.
5. If /CS1, /UB and /LB are low , all address pulse widths should be within the maximum limits of 10us.

WRITE CYCLE 1 (Note 1, 4, 5, 9, 10) (/WE Controlled)



WRITE CYCLE 2 (Note 1, 4, 5, 9, 10) (/CS1 Controlled)



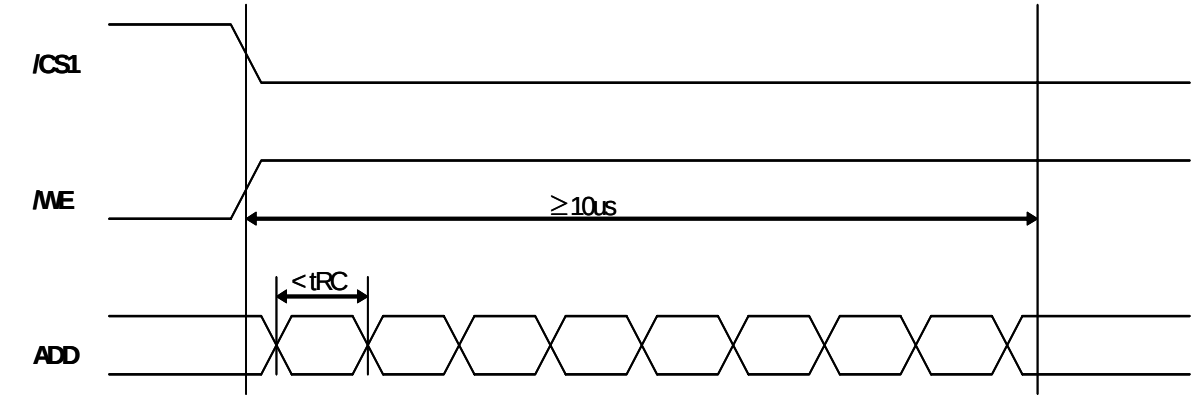
Notes :

1. A write occurs during the overlap of low /CS1, low /WE and low /UB and/or /LB.
2. tWR is measured from the earlier of /CS1, /LB, /UB, or /WE going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.
4. If the /CS1, /LB and /UB low transitions occur simultaneously with the /WE low transition or after the /WE transition, outputs remain in a high impedance state.
5. /OE is continuously low (/OE=VIL)
6. Q(data out) is the invalid data.
7. Q(data out) is the read data of the next address.
8. tWHZ is defined as the time at which the outputs achieve the high impedance state. It is not referenced to output voltage levels.
9. /CS1 is high for the standby, low for active. /UB and /LB are high for the standby, low for active.
10. Do not input data to the I/O pins while they are in the output state.
11. If /CS1, /UB and /LB are low, all address pulse widths should be within the maximum limits of 10us.

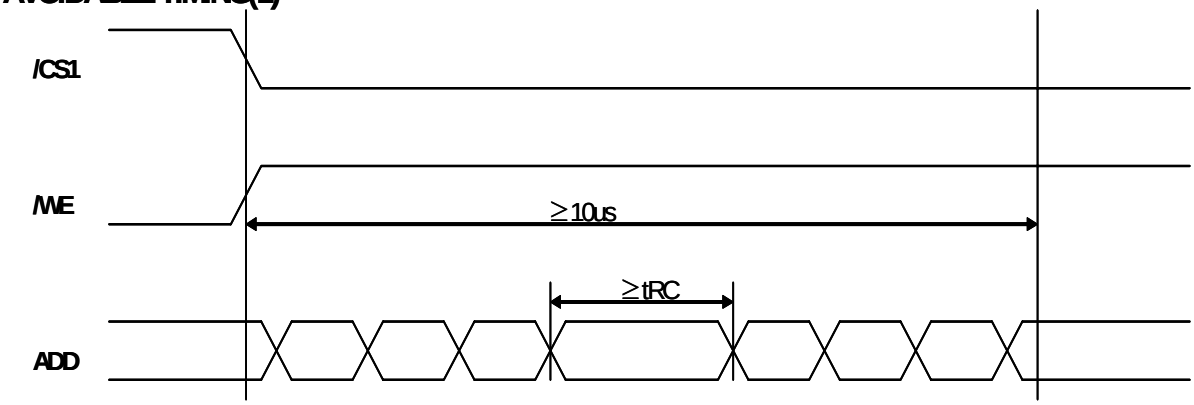
AVOID TIMING

Hynix 1T/1C SRAM has a timing which is not supported at read operation. If your system has multiple invalid address signal shorter than tRC during over 10us at read operation which showed in abnormal timing, Hynix 1T/1C SRAM needs a normal read timing at least during 10us which showed in avoidable timing(1) or toggle the /CS1 to high(≥ tRC) one time at least which showed in avoidable timing(2)

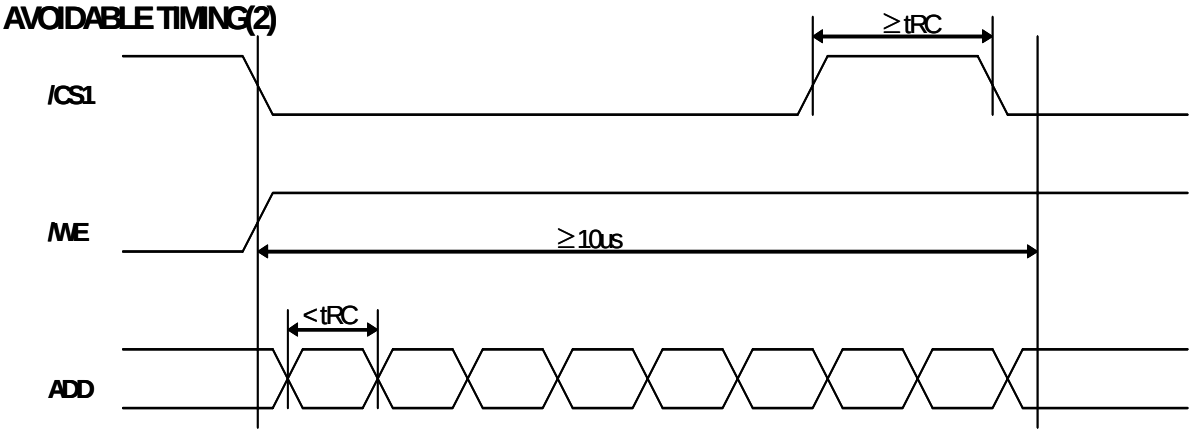
ABNORMAL TIMING



AVOIDABLE TIMING(1)

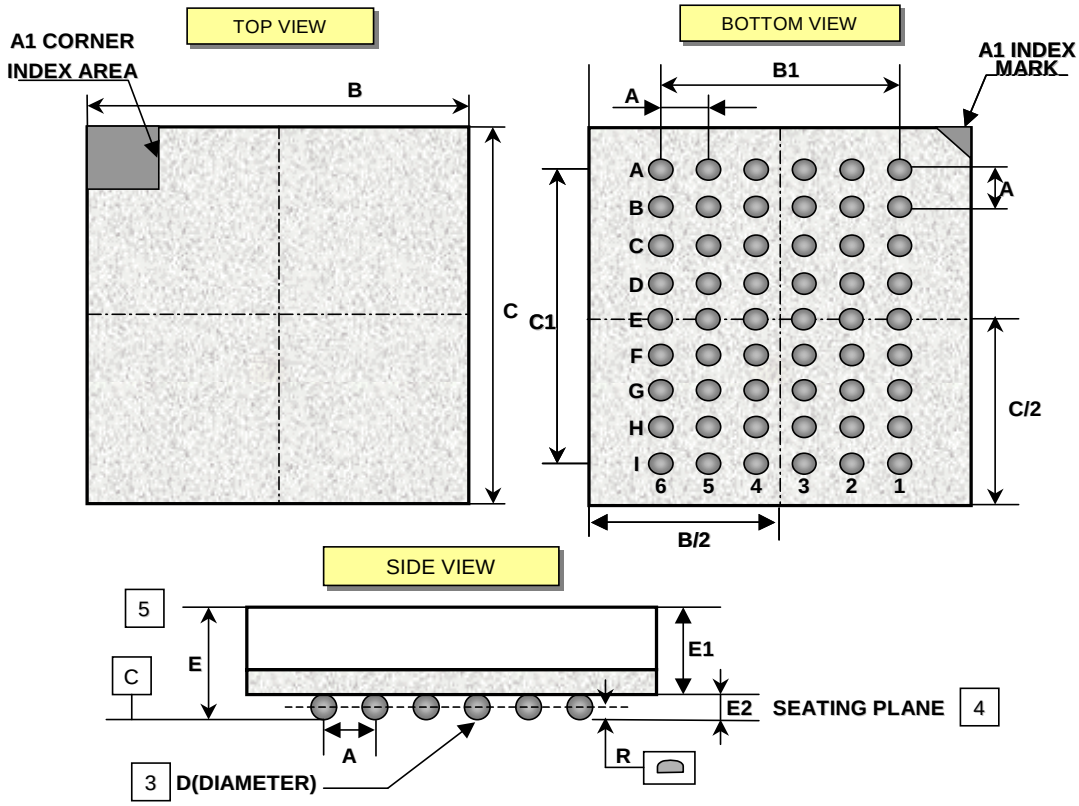


AVOIDABLE TIMING(2)



PACKAGE DIMENSION

48ball Fine Pitch Ball Grid Array Package(F)



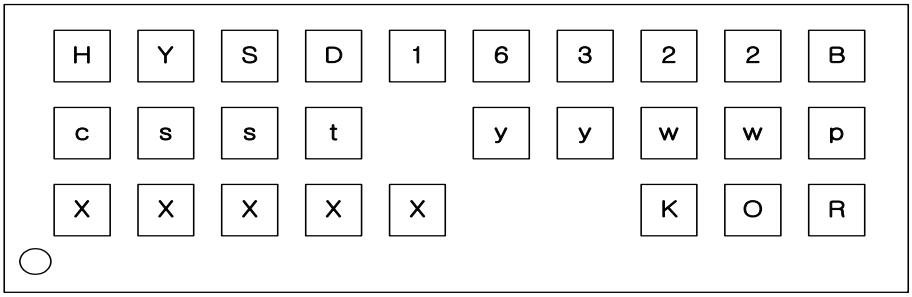
Unit: mm

Symbol	Min.	Typ.	Max.
A	-	0.75	-
B	5.90	6.00	6.10
B1	-	3.75	-
C	7.90	8.00	8.10
C1	-	5.25	-
D	0.30	0.35	0.40
E	-	1.00	1.10
E1	-	0.75	-
E2	0.20	0.25	0.30
R	-	-	0.08

NOTE.

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE MILLIMETERS.
3. DIMENSION “D” IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
4. PRIMARY DATUM C(SEATING PLANE) IS DEFINED BY THE CROWN OF THE SOLDER BALLS.
5. THIS IS A CONTROLLING DIMENSION.

MARKING INFORMATION

Packag	Marking
FBGA	

Index

- HYSD16322B	: Part Name	
HY	: HYNIX	
S	: Power Supply	: Vdd=1.80V~1.95V
D	: Tech. + Classification	: 1T+1C
16	: Bit Organization	: x16
32	: Density	: 32M
2	: Mode	: 1CS with /UB, /LB;tCS
B	: Version	: 3rd Generation
- c	: Power Consumption	: D-Low Low Power
- ss	: Speed	: 85-85ns
- t	: Temperature	: E- Extended(-25~85℃) I- Industrial(-40~85℃)
- yy	: Year (ex: 02=year 2002, 03= year 2003)	
- ww	: Work Week (ex: 12= work week 12)	
- p	: Process Code	
- xxxxx	: Lot No.	
- KOR	: Origin Country	

Note

- Captial Letter	: Fixed Item
- Small Letter	: Non-fixed Item