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80C652/83C652/87C652

CMOS single-chip 8-bit microcontroller

DESCRIPTION

The 80C652/83C652/87C652 Single-Chip 8-Bit Microcontroller is manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family. The 80C652/83C652/87C652 has the same instruction set as the 80C51. Three versions of the derivative exist:

83C652 – 8k bytes mask programmable ROM

80C652 – ROMless version

87C652 – EPROM version

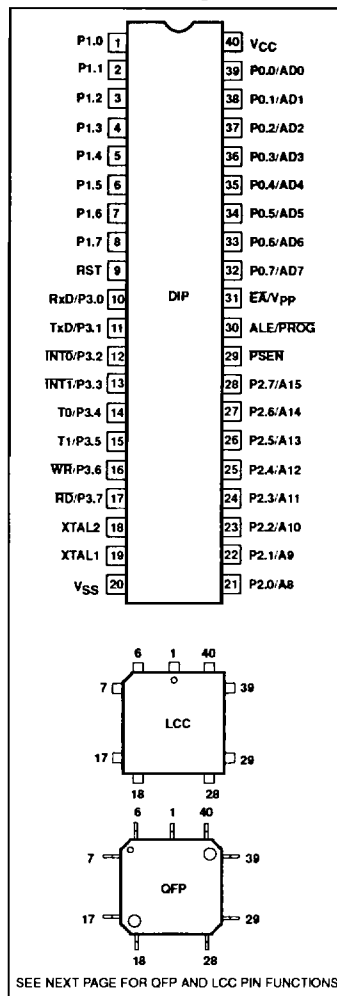
This device provides architectural enhancements that make it applicable in a variety of applications for general control systems. The 8XC652 contains a non-volatile 8k X 8 read-only program memory (83C652) EPROM (87C652), a volatile 256 X 8 read/write data memory, four 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51), a multi-source, two-priority-level, nested interrupt structure, an I²C interface, UART and on-chip oscillator and timing circuits. For systems that require extra capability, the 8XC652 can be expanded using standard TTL compatible memories and logic.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte and 17 three-byte. With a 12MHz crystal, 58% of the instructions are executed in 1µs and 40% in 2µs. Multiply and divide instructions require 4µs.

FEATURES

- 80C51 central processing unit
- 8k x 8 ROM expandable externally to 64k bytes (87C652 EPROM is not expandable)
- 256 x 8 RAM, expandable externally to 64k bytes
- Two standard 16-bit timer/counters
- Four 8-bit I/O ports
- I²C-bus serial I/O port with byte oriented master and slave functions
- Full-duplex UART facilities
- Power control modes
 - Idle mode
 - Power-down mode
- Five package styles
- Extended temperature ranges
- OTP package available

PIN CONFIGURATION



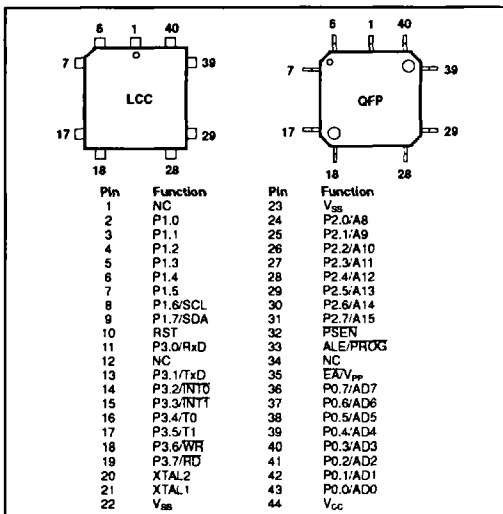
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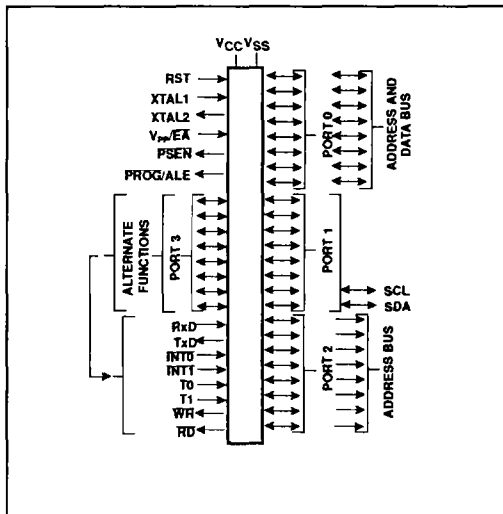
PART NUMBER SELECTION

PHILIPS		PHILIPS COMPONENTS-SIGNETICS			TEMPERATURE °C AND PACKAGE	FREQ. MHz
ROMless	ROM	ROMless	ROM	EPROM		
PCB80C652P	PCB83C652P	S80C652-1N40	S83C652-1N40	S87C652-1N40	0 to +70, PDIP	12
				S87C652-1F40	0 to +70, CDIP	12
PCB80C652WP	PCB83C652WP	S80C652-1A44	S83C652-1A44	S87C652-1A44	0 to +70, PLCC	12
				S87C652-1K44	0 to +70, CLCC	12
PCB80C652H	PCB83C652H	S80C652-1B44	S83C652-1B44		0 to +70, PQFP	12
PCF80C652P	PCF83C652P	S80C652-2N40	S83C652-2N40	S87C652-2N40	-40 to +85, PDIP	12
				S87C652-2F40	-40 to +85, CDIP	12
PCF80C652WP	PCF83C652WP	S80C652-2A44	S83C652-2A44	S87C652-2A44	-40 to +85, PLCC	12
				S87C652-2K44	-40 to +85, CLCC	12
PCF80C652H	PCF83C652H	S80C652-2B44	S83C652-2B44		-40 to +85, PQFP	12
				S87C652-4N40	0 to +70, PDIP	16
				S87C652-4F40	0 to +70, CDIP	16
				S87C652-4A44	0 to +70, PLCC	16
				S87C652-4K44	0 to +70, CLCC	16
				S87C652-5N40	-40 to +85, PDIP	16
				S87C652-5F40	-40 to +85, CDIP	16
				S87C652-5A44	-40 to +85, PLCC	16
				S87C652-5K44	-40 to +85, CLCC	16
PCA80C652P	PCA83C652P	S80C652-6N40	S83C652-6N40		-40 to +125, PDIP	12
PCA80C652WP	PCA83C652WP	S80C652-6A44	S83C652-6A44		-40 to +125, PLCC	12
PCA80C652H	PCA83C652H	S80C652-6B44	S83C652-6B44		-40 to +125, PQFP	12

LCC AND QFP PIN FUNCTIONS



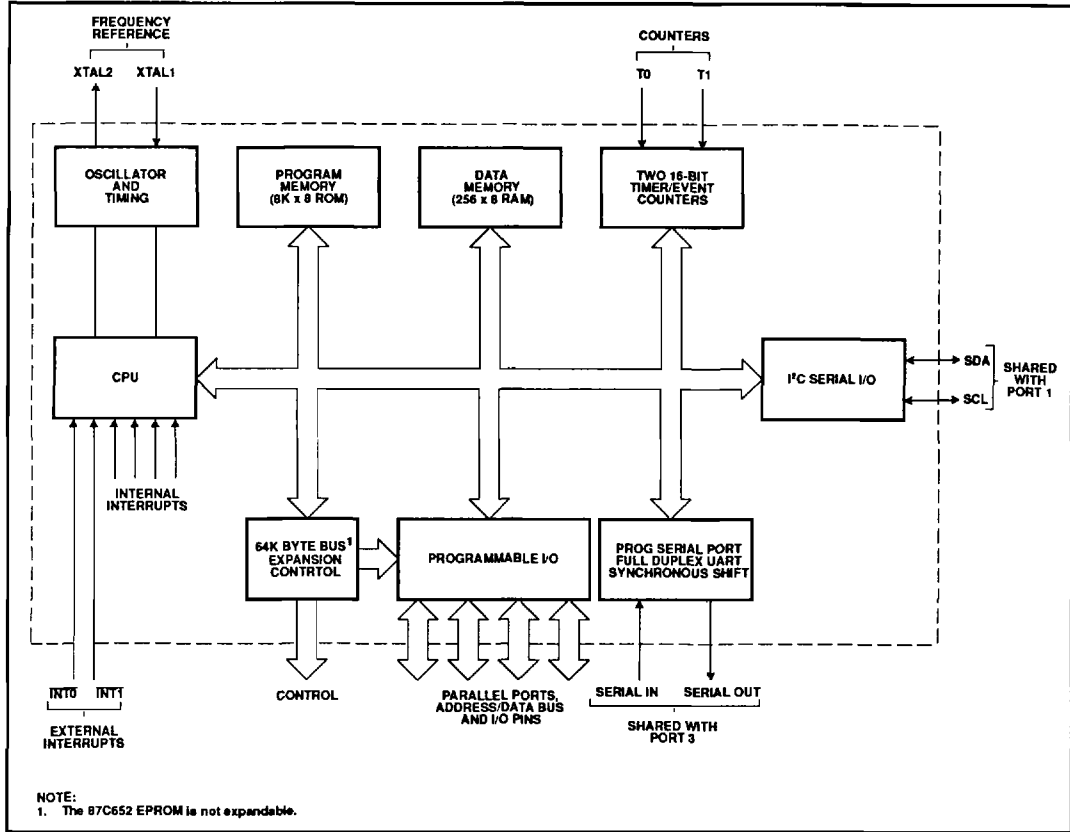
LOGIC SYMBOL



CMOS single-chip 8-bit microcontroller

80C652/83C652/87C652

BLOCK DIAGRAM



CMOS single-chip 8-bit microcontroller

80C652/83C652/87C652

PIN DESCRIPTION

MNEMONIC	PIN NO.		TYPE	NAME AND FUNCTION
	DIP	LCC/ QFP		
V _{SS}	20	22	I	Ground: 0V reference.
V _{CC}	40	44	I	Power Supply: This is the power supply voltage for normal, idle, and power-down operation.
P0.0–P0.7	39–32	43–46	I/O	Port 0: Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s. Port 0 also outputs the code bytes during program verification in the 87C652. External pull-ups are required during program verification.
P1.0–P1.7	1–8	2–9	I/O	Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pull-ups, except P1.6 and P1.7 which are open drain. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I _{IL}). Port 1 also receives the low-order address byte during program memory verification. Alternate functions include:
P1.6	7	8	I/O	SCL: I ² C-bus serial port clock line.
P1.7	8	9	I/O	SDA: I ² C-bus serial port data line.
P2.0–P2.7	21–28	24–31	I/O	Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 2 pins that are externally being pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I _{IL}). Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOV @Ri), port 2 emits the contents of the P2 special function register.
P3.0–P3.7	10–17	11, 13–19	I/O	Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups. (See DC Electrical Characteristics: I _{IL}). Port 3 also serves the special features of the 80C51 family, as listed below:
	10	11	I	RxD (P3.0): Serial input port
	11	13	O	TxD (P3.1): Serial output port
	12	14	I	INT0 (P3.2): External interrupt
	13	15	I	INT1 (P3.3): External interrupt
	14	16	I	T0 (P3.4): Timer 0 external input
	15	17	I	T1 (P3.5): Timer 1 external input
	16	18	O	WR (P3.6): External data memory write strobe
	17	19	O	RD (P3.7): External data memory read strobe
RST	9	10	I	Reset: A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V _{SS} permits a power-on reset using only an external capacitor to V _{CC} .
ALE/PROG	30	33	I/O	Address Latch Enable/Program Pulse: Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the program pulse input (PROG) during EPROM programming.
PSEN	29	32	O	Program Store Enable: The read strobe to external program memory. When the 87C652 is executing code from the external program memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory. PSEN is not activated during fetches from internal program memory.
EAV _{PP}	31	35	I	External Access Enable/Programming Supply Voltage: E \bar{A} must be externally held low to enable the device to fetch code from external program memory locations 0000H and 1FFFH. If E \bar{A} is held high, the device executes from internal program memory unless the program counter contains an address greater than 1FFFH. This pin also receives the 12.75V programming supply voltage (V _{PP}) during EPROM programming.
XTAL1	19	21	I	Crystal 1: Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	18	20	O	Crystal 2: Output from the inverting oscillator amplifier.

NOTE:

To avoid "latch-up" effect at power-on, the voltage on any pin at any time must not be higher than V_{CC} + 0.5V or V_{SS} - 0.5V, respectively.

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OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier. The pins can be configured for use as an on-chip oscillator, as shown in the logic symbol, page 2.

To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, because the input to the internal clock circuitry is through a divide-by-two flip-flop. However, minimum and maximum high and low times specified in the data sheet must be observed.

RESET

A reset is accomplished by holding the RST pin high for at least two machine cycles (24

oscillator periods), while the oscillator is running. To insure a good power-on reset, the RST pin must be high long enough to allow the oscillator time to start up (normally a few milliseconds) plus two machine cycles. At power-on, the voltage on V_{CC} and RST must come up at the same time for a proper start-up.

IDLE MODE

In the idle mode, the CPU puts itself to sleep while all of the on-chip peripherals stay active. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The CPU contents, the on-chip RAM, and all of the special function registers remain intact during this mode. The idle mode

can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power-on reset.

POWER-DOWN MODE

In the power-down mode, the oscillator is stopped and the instruction to invoke power-down is the last instruction executed. Only the contents of the on-chip RAM are preserved. A hardware reset is the only way to terminate the power-down mode. The control bits for the reduced power modes are in the special function register PCON. Table 1 shows the state of the I/O ports during low current operating modes.

Table 1. External Pin Status During Idle and Power-Down Mode

MODE	PROGRAM MEMORY	ALE	PSEN	PORT 0	PORT 1	PORT 2	PORT 3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

Serial Control Register (S1CON) – See Table 2

S1CON (D8H)

CR2	ENS1	STA	STO	SI	AA	CR1	CR0
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Bits CR0, CR1 and CR2 determine the serial clock frequency that is generated in the master mode of operation.

Table 2. Serial Clock Rates

CR2 ¹	CR1	CR0	BIT FREQUENCY (kHz) AT f _{OSC}			f _{OSC} DIVIDED BY
			6MHz	12MHz	16MHz ¹	
0	0	0	23	47	62.5	256 ¹
0	0	1	27	54	71	224 ¹
0	1	0	31.25	62.5	83.3	192 ¹
0	1	1	37	75	100	160 ¹
1	0	0	6.25	12.5	17	960
1	0	1	50	100	133 ²	120
1	1	0	100	200 ²	267 ²	60
1	1	1	0.25 < 31.25	0.5 < 62.5	0.67 < 83.3	96 x (256 - (reload value Timer 1)) (Reload value range: 0 - 254 in mode 2)

NOTES:

- The CR2 control bit is only implemented on the 16MHz version.
- These frequencies exceed the upper limit of 100kHz of the I²C-bus specification and cannot be used in an I²C-bus application.

CMOS single-chip 8-bit microcontroller**80C652/83C652/87C652****ABSOLUTE MAXIMUM RATINGS^{1, 2, 3}**

PARAMETER	RATING	UNIT
Storage temperature range	-65 to +150	°C
Voltage on $E\bar{A}/V_{PP}$ to V_{SS} (87C652 only)	-0.5 to +13	V
Voltage on any other pin to V_{SS}	-0.5 to +6.5	V
Input, output current on any single pin	± 5	mA
Input, output current on any two pins	± 10	mA
Power dissipation (based on package heat transfer limitations, not device power consumption)	1	W

NOTES:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
2. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.
3. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

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DC ELECTRICAL CHARACTERISTICS

 $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, or $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}/+125^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	V
I_{CC}	Supply current: Active mode Idle mode Power-down mode	See note 1 See notes 2 and 3 See notes 2 and 4 See notes 3 and 5 See notes 4 and 5 See notes 3, 6, and 7 See notes 4, 6, and 7		24 27 5.0 6.0 50 120	mA mA mA mA μA μA
Inputs					
V_{IL}	Input low voltage, except \overline{EA} , P1.6/SCL, P1.7/SDA		-0.5	$0.2V_{CC}-0.1$	V
V_{IL1}	Input low voltage to \overline{EA}		-0.5	$0.2V_{CC}-0.3$	V
V_{IL2}	Input low voltage to P1.6/SCL, P1.7/SDA ⁸		-0.5	1.5	V
V_{IH}	Input high voltage, except XTAL1, RST, P1.6/SCL, P1.7/SDA		$0.2V_{CC}+0.9$	$V_{CC}+0.5$	V
V_{IH1}	Input high voltage, XTAL1, RST		$0.7V_{CC}$	$V_{CC}+0.5$	V
V_{IH2}	Input high voltage, P1.6/SCL, P1.7/SDA ⁸		3.0	6.0	V
$-I_{IL}$	Logical 0 input current, ports 1, 2, 3, 4, except P1.6/SCL, P1.7/SDA	$V_{IN} = 0.45\text{V}$		50	μA
$-I_{TL}$	Logical 1-to-0 transition current, ports 1, 2, 3, except P1.6/SCL, P1.7/SDA	See note 9		-650	μA
$\pm I_{IL1}$	Input leakage current, port 0, \overline{EA}	$0.45\text{V} < V_I < V_{CC}$		10	μA
$\pm I_{IL2}$	Input leakage current, P1.6/SCL, P1.7/SDA	$0\text{V} < V_I < 6\text{V}$ $0\text{V} < V_{CC} < 5.5\text{V}$		10	μA
Outputs					
V_{OL}	Output low voltage, ports 1, 2, 3, except P1.6/SCL, P1.7/SDA	$I_{OL} = 1.6\text{mA}^{10}$		0.45	V
V_{OL1}	Output low voltage, port 0, ALE, PSEN	$I_{OL} = 3.2\text{mA}^{10}$		0.45	V
V_{OL2}	Output low voltage, P1.6/SCL, P1.7/SDA	$I_{OL} = 3.0\text{mA}$		0.4	V
V_{OH}	Output high voltage, ports 1, 2, 3	$-I_{OH} = 60\mu\text{A}$ $-I_{OH} = 25\mu\text{A}$ $-I_{OH} = 10\mu\text{A}$	2.4 $0.75V_{CC}$ $0.9V_{CC}$		V V V
V_{OH1}	Output high voltage (port 0 in external bus mode, ALE, PSEN) ¹¹	$-I_{OH} = 400\mu\text{A}$ $-I_{OH} = 150\mu\text{A}$ $-I_{OH} = 40\mu\text{A}$	2.4 $0.75V_{CC}$ $0.9V_{CC}$		V V V
R_{RST}	Internal reset pull-down resistor		50	150	kohm
C_{IO}	Pin capacitance	Test freq = 1MHz, $T_A = 25^\circ\text{C}$		10	pF

NOTES: See next page.

CMOS single-chip 8-bit microcontroller**80C652/83C652/87C652****NOTES FOR DC ELECTRICAL CHARACTERISTICS:**

1. See Figures 8 through 11 for I_{CC} test conditions.
2. The operating supply current is measured with all output pins disconnected; XTAL1 driven with $t_r = t_f = 10\text{ns}$; $V_{IL} = V_{SS} + 0.5\text{V}$; $V_{IH} = V_{CC} - 0.5\text{V}$; XTAL2 not connected; $\overline{EA} = \text{RST} = \text{Port } 0 = \text{P1.6} = \text{P1.7} = V_{CC}$; $f_{CLK} = 12\text{MHz}$. See Figure 8.
3. This applies to 0 to 70°C and -40 to $+85^\circ\text{C}$ temperature range devices.
4. This applies to the -40 to $+125^\circ\text{C}$ temperature range device.
5. The idle mode supply current is measured with all output pins disconnected; XTAL1 driven with $t_r = t_f = 10\text{ns}$; $V_{IL} = V_{SS} + 0.5\text{V}$; $V_{IH} = V_{CC} - 0.5\text{V}$; XTAL2 not connected; $\overline{EA} = \text{Port } 0 = \text{P1.6} = \text{P1.7} = V_{CC}$; $f_{CLK} = 12\text{MHz}$. See Figure 9.
6. The power-down current is measured with all output pins disconnected; XTAL2 not connected; $\overline{EA} = \text{Port } 0 = \text{P1.6} = \text{P1.7} = V_{CC}$; $\text{RST} = V_{SS}$. See Figure 11.
7. $2\text{V} \leq V_{PD} \leq V_{CCmax}$.
8. The input threshold voltage of P1.6 and P1.7 (SIO1) meets the I²C specification, so an input voltage below 1.5V will be recognized as a logic 0 while an input voltage above 3.0V will be recognized as a logic 1.
9. Pins of ports 1, 2, and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2V.
10. Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the V_{OLS} of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading $> 100\text{pF}$), the noise pulse on the ALE pin may exceed 0.8V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input. I_{OL} can exceed these conditions provided that no single output sinks more than 5mA and no more than two outputs exceed the test conditions.
11. Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and PSEN to momentarily fall below the $0.9V_{CC}$ specification when the address bits are stabilizing.

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AC ELECTRICAL CHARACTERISTICS

 $T_A = 0^\circ\text{C to } +70^\circ\text{C}$, or $T_A = -40^\circ\text{C to } +85^\circ\text{C}/+125^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}^{1,2}$

SYMBOL	FIGURE	PARAMETER	12MHz CLOCK		VARIABLE CLOCK		UNIT
			MIN	MAX	MIN	MAX	
$1/t_{CLCL}$	1	Oscillator frequency			1.2	16	MHz
t_{LHLL}	1	ALE pulse width	127		$2t_{CLCL}-40$		ns
t_{AVLL}	1	Address valid to ALE low	28		$t_{CLCL}-55$		ns
t_{LLAX}	1	Address hold after ALE low	48		$t_{CLCL}-35$		ns
t_{LLIV}	1	ALE low to valid instruction in		233		$4t_{CLCL}-100$	ns
t_{LLPL}	1	ALE low to PSEN low	43		$t_{CLCL}-40$		ns
t_{PLPH}	1	PSEN pulse width	205		$3t_{CLCL}-45$		ns
t_{PLIV}	1	PSEN low to valid instruction in		145		$3t_{CLCL}-105$	ns
t_{PXIX}	1	Input instruction hold after PSEN	0		0		ns
t_{PXIZ}	1	Input instruction float after PSEN		59		$t_{CLCL}-25$	ns
t_{AVIV}	1	Address to valid instruction in		312		$5t_{CLCL}-105$	ns
t_{PLAZ}	1	PSEN low to address float		10		10	ns
Data Memory							
t_{AVLL}	2, 3	Address valid to ALE low	48		$t_{CLCL}-35$		ns
t_{RLRH}	2, 3	RD pulse width	400		$6t_{CLCL}-100$		ns
t_{WLWH}	2, 3	WR pulse width	400		$6t_{CLCL}-100$		ns
t_{RLDV}	2, 3	RD low to valid data in		252		$5t_{CLCL}-165$	ns
t_{RHDX}	2, 3	Data hold after RD	0		0		ns
t_{RHDX}	2, 3	Data float after RD		97		$2t_{CLCL}-70$	ns
t_{LLDV}	2, 3	ALE low to valid data in		517		$8t_{CLCL}-150$	ns
t_{AVDV}	2, 3	Address to valid data in		585		$9t_{CLCL}-165$	ns
t_{LLWL}	2, 3	ALE low to RD or WR low	200	300	$3t_{CLCL}-50$	$3t_{CLCL}+50$	ns
t_{AVWL}	2, 3	Address valid to WR low or RD low	203		$4t_{CLCL}-130$		ns
t_{QVWX}	2, 3	Data valid to WR transition	23		$t_{CLCL}-60$		ns
t_{DW}	2, 3	Data setup time before WR	433		$7t_{CLCL}-150$		ns
t_{WHDX}	2, 3	Data hold after WR	33		$t_{CLCL}-50$		ns
t_{RLAZ}	2, 3	RD low to address float		0		0	ns
t_{WHLH}	2, 3	RD or WR high to ALE high	43	123	$t_{CLCL}-40$	$t_{CLCL}+40$	ns
Shift Register³							
t_{XLXL}	4	Serial port clock cycle time ⁴	1.0		$12t_{CLCL}$		μs
t_{QVXH}	4	Output data setup to clock rising edge ⁴	700		$10t_{CLCL}-133$		ns
t_{XHDX}	4	Output data hold after clock rising edge ⁴	50		$2t_{CLCL}-117$		ns
t_{XHDX}	4	Input data hold after clock rising edge ⁴	0		0		ns
t_{XHDX}	4	Clock rising edge to input data valid ⁴		700		$10t_{CLCL}-133$	ns
External Clock							
t_{CHCX}	5	High time ⁴	20		20	$t_{CLCL} - t_{LOW}$	ns
t_{CLCX}	5	Low time ⁴	20		20	$t_{CLCL} - t_{HIGH}$	ns
t_{CLCH}	5	Rise time ⁴		20		20	ns
t_{CHCL}	5	Fall time ⁴		20		20	ns

NOTES:

- Parameters are valid over operating temperature range unless otherwise specified.
- Load capacitance for port 0, ALE, and PSEN = 100pF, load capacitance for all other outputs = 80pF.
- The shift register has been characterized for the 87C652 only.
- These values are characterized but not 100% production tested.

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80C652/83C652/87C652

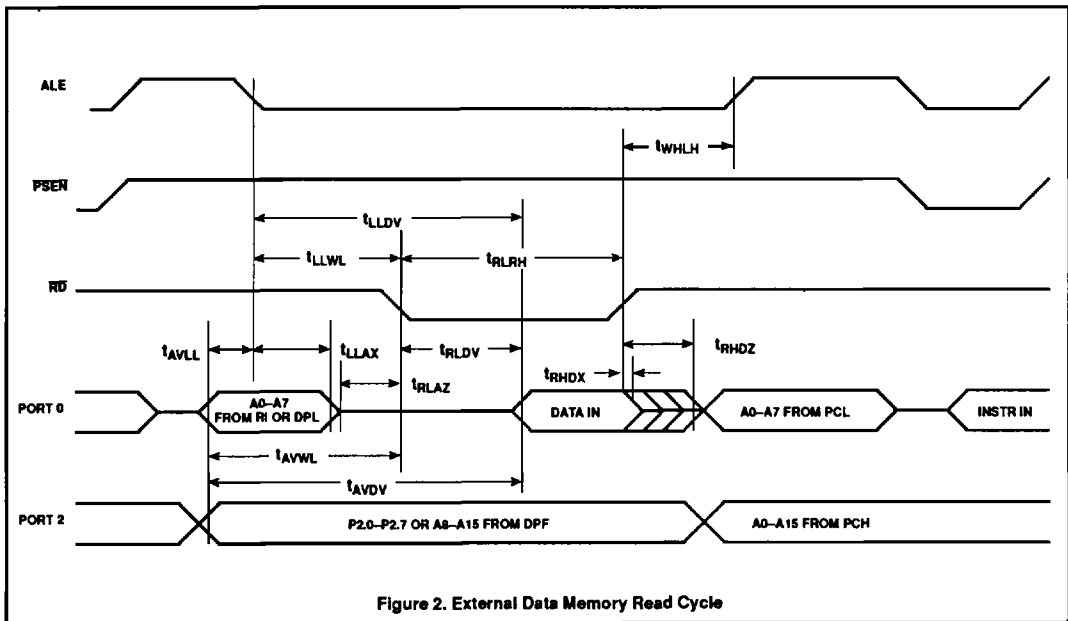
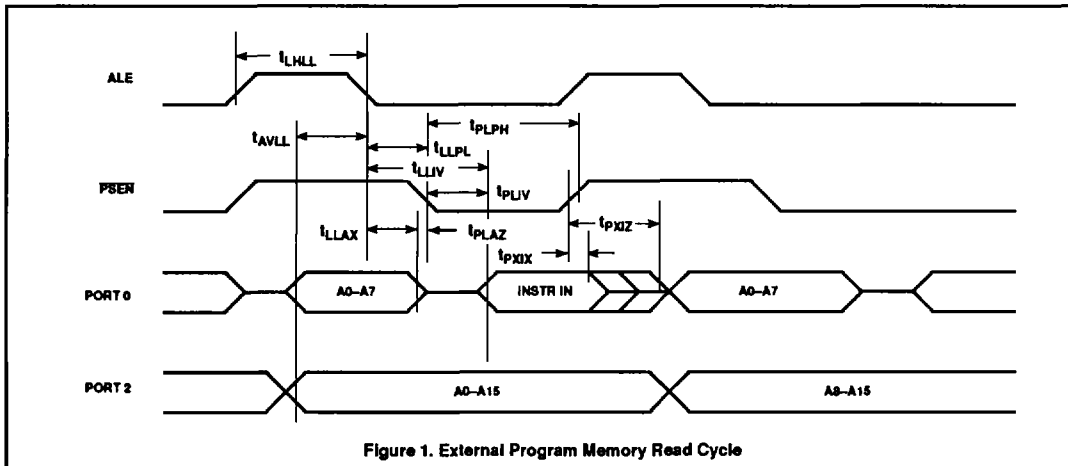
EXPLANATION OF THE AC SYMBOLS

Each timing symbol has five characters. The first character is always 't' (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal. The designations are:

- A - Address
- C - Clock
- D - Input data
- H - Logic level high
- I - Instruction (program memory contents)
- L - Logic level low, or ALE

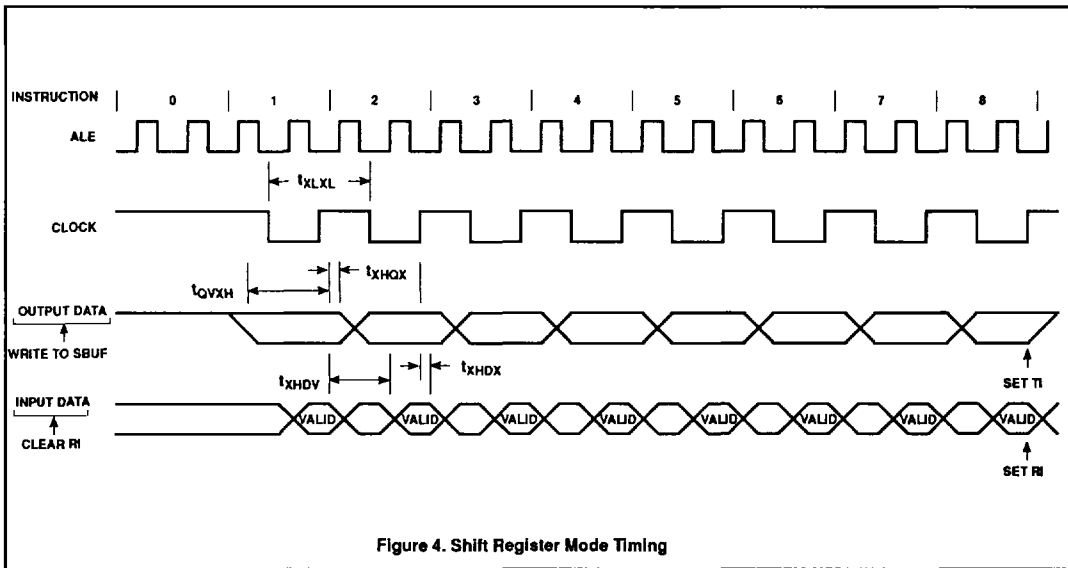
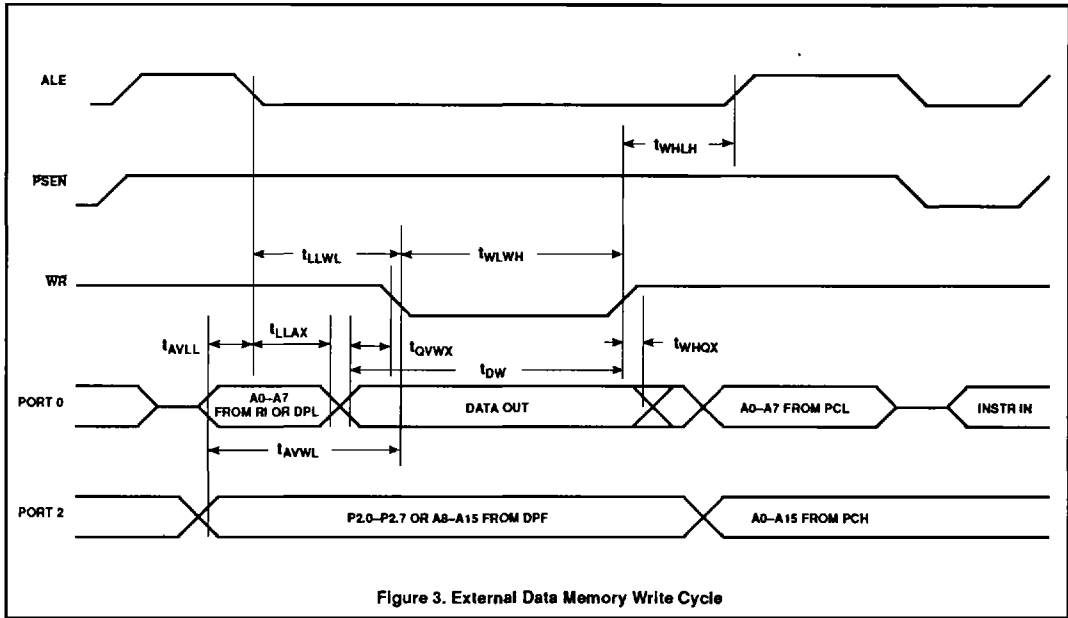
- P - PSEN
- Q - Output data
- R - RD signal
- t - Time
- V - Valid
- W - WR signal
- X - No longer a valid logic level
- Z - Float

Examples: t_{AVLL} = Time for address valid to ALE low.
 t_{LLPL} = Time for ALE low to PSEN low.



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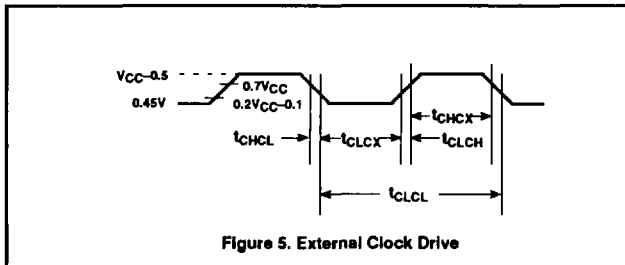


Figure 5. External Clock Drive

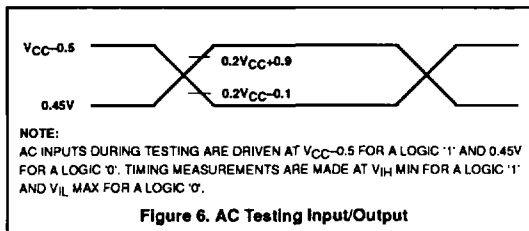


Figure 6. AC Testing Input/Output

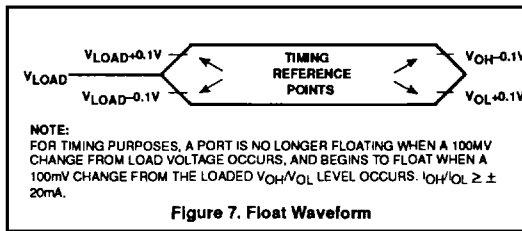
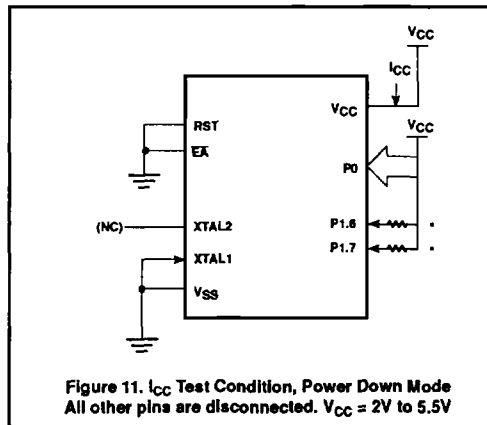
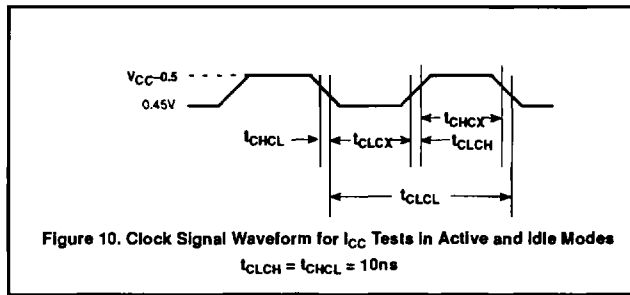
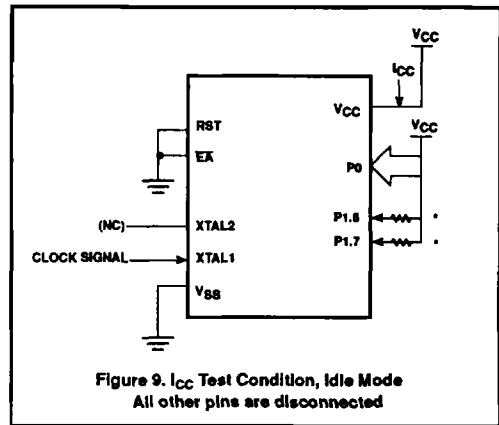
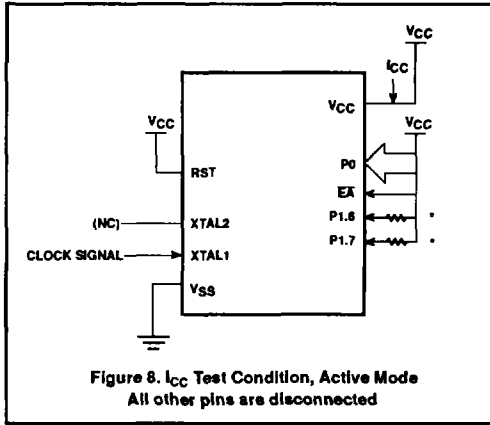


Figure 7. Float Waveform

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* NOTE:
Ports 1.6 and 1.7 should be connected to V_{CC} through resistors of sufficiently high value such that the sink current into these pins does not exceed the i_{OL1} specification.

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EPROM CHARACTERISTICS

The 87C652 is programmed by using a modified Quick-Pulse Programming™ algorithm. It differs from older methods in the value used for V_{PP} (programming supply voltage) and in the width and number of the ALE/PROG pulses.

The 87C652 contains two signature bytes that can be read and used by an EPROM programming system to identify the device. The signature bytes identify the device as an 87C652 manufactured by Philips Components.

Table 3 shows the logic levels for reading the signature byte, and for programming the program memory, the encryption table, and the lock bits. The circuit configuration and waveforms for quick-pulse programming are shown in Figures 12 and 13. Figure 14 shows the circuit configuration for normal program memory verification.

Quick-Pulse Programming

The setup for microcontroller quick-pulse programming is shown in Figure 12. Note that the 87C652 is running with a 4 to 6MHz oscillator. The reason the oscillator needs to be running is that the device is executing internal address and program data transfers.

The address of the EPROM location to be programmed is applied to ports 1 and 2, as shown in Figure 12. The code byte to be programmed into that location is applied to port 0. RST, PSEN and pins of ports 2 and 3 specified in Table 3 are held at the 'Program Code Data' levels indicated in Table 3. The ALE/PROG is pulsed low 25 times as shown in Figure 13.

To program the encryption table, repeat the 25 pulse programming sequence for addresses 0 through 1FH, using the 'Pgm Encryption Table' levels. Do not forget that after the encryption table is programmed, verification cycles will produce only encrypted data.

To program the lock bits, repeat the 25 pulse programming sequence using the 'Pgm Lock Bit' levels. After one lock bit is programmed, further programming of the code memory and encryption table is disabled. However, the other lock bit can still be programmed.

Note that the \overline{EA}/V_{PP} pin must not be allowed to go above the maximum specified V_{PP} level for any amount of time. Even a narrow glitch above that voltage can cause permanent damage to the device. The V_{PP} source should be well regulated and free of glitches and overshoot.

Program Verification

If lock bit 2 has not been programmed, the on-chip program memory can be read out for program verification. The address of the program memory locations to be read is applied to ports 1 and 2 as shown in Figure 14. The other pins are held at the 'Verify Code Data' levels indicated in Table 3. The contents of the address location will be emitted on port 0. External pull-ups are required on port 0 for this operation.

If the encryption table has been programmed, the data presented at port 0 will be the exclusive NOR of the program byte with one of the encryption bytes. The user will have to know the encryption table contents in order to correctly decode the verification data. The encryption table itself cannot be read out.

Reading the Signature Bytes

The signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P3.6 and P3.7 need to be pulled to a logic low. The values are:

(030H) = 5H indicates manufactured by Philips
(031H) = 99H indicates 87C652

Program/Verify Algorithms

Any algorithm in agreement with the conditions listed in Table 3, and which satisfies the timing specifications, is suitable.

Erase Characteristics

Erase of the EPROM begins to occur when the chip is exposed to light with wavelengths shorter than approximately 4,000 angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room level fluorescent lighting) could cause inadvertent erasure. For this and secondary effects, it is recommended that an opaque label be placed over the window. For elevated temperature or environments where solvents are being used, apply Kapton tape Fluorglas part number 2345-5, or equivalent.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 angstroms) to an integrated dose of at least 15W-sec/cm². Exposing the EPROM to an ultraviolet lamp of 12,000uW/cm² rating for 20 to 39 minutes, at a distance of about 1 inch, should be sufficient. Erasure leaves the array in an all 1s state.

Table 3. EPROM Programming Modes

MODE	RST	PSEN	ALE/PROG	\overline{EA}/V_{PP}	P2.7	P2.6	P3.7	P3.6
Read signature	1	0	1	1	0	0	0	0
Program code data	1	0	0*	V_{PP}	1	0	1	1
Verify code data	1	0	1	1	0	0	1	1
Pgm encryption table	1	0	0*	V_{PP}	1	0	1	0
Pgm lock bit 1	1	0	0*	V_{PP}	1	1	1	1
Pgm lock bit 2	1	0	0*	V_{PP}	1	1	0	0

NOTES:

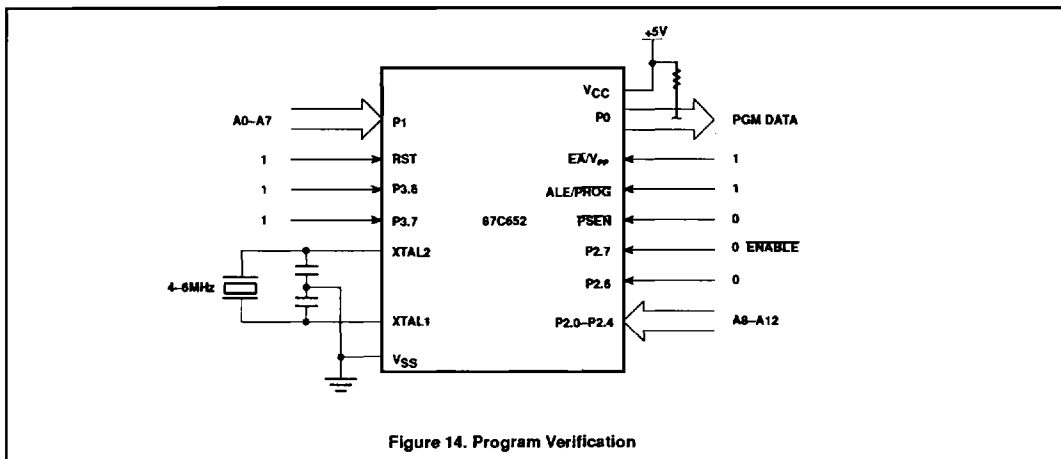
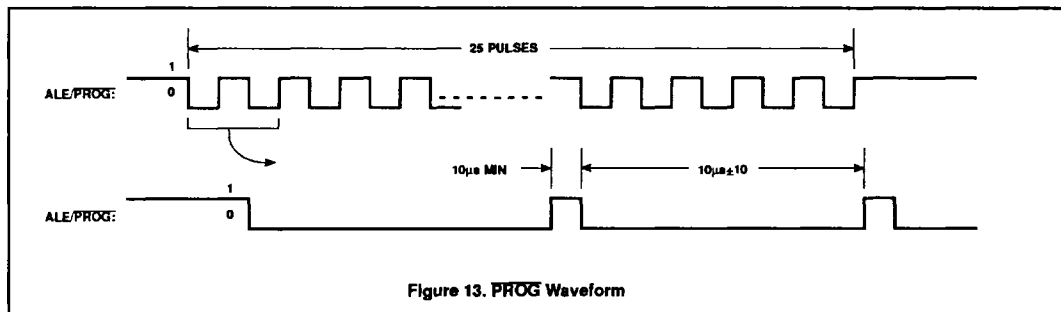
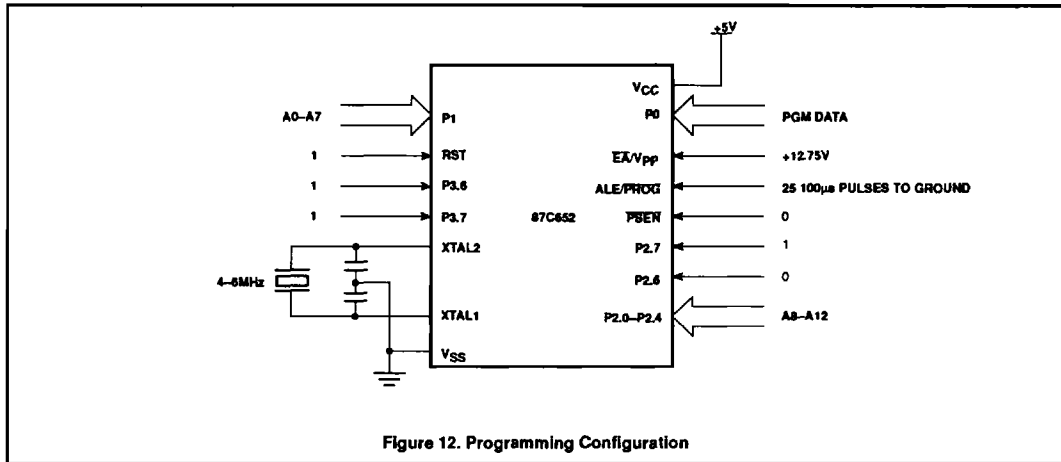
- 0* = Valid low for that pin, '1' = valid high for that pin.
- $V_{PP} = 12.75V \pm 0.25V$.
- $V_{CC} = 5V \pm 10\%$ during programming and verification.

*ALE/PROG receives 25 programming pulses while V_{PP} is held at 12.75V. Each programming pulse is low for 100 μ s ($\pm 10\mu$ s) and high for a minimum of 10 μ s.

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EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

 $T_A = 21^\circ\text{C}$ to $+27^\circ\text{C}$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$ (See Figure 15)

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{PP}	Programming supply voltage	12.5	13.0	V
I_{PP}	Programming supply current		50	mA
$1/t_{CLCL}$	Oscillator frequency	4	6	MHz
t_{AVGL}	Address setup to PROG low	$48t_{CLCL}$		
t_{GHAX}	Address hold after PROG	$48t_{CLCL}$		
t_{DVGL}	Data setup to PROG low	$48t_{CLCL}$		
t_{GHDX}	Data hold after PROG	$48t_{CLCL}$		
t_{ESH}	P2.7 (ENABLE) high to V_{PP}	$48t_{CLCL}$		
t_{SHGL}	V_{PP} setup to PROG low	10		μs
t_{GHSL}	V_{PP} hold after PROG	10		μs
t_{GLGH}	PROG width	90	110	μs
t_{AVQV}	Address to data valid		$48t_{CLCL}$	
t_{ELOZ}	ENABLE low to data valid		$48t_{CLCL}$	
t_{EHOZ}	Data float after ENABLE	0	$48t_{CLCL}$	
t_{GHGL}	PROG high to PROG low	10		μs

