1.0 INTRODUCTION

1.1 GENERAL DESCRIPTION

The SBP 9961 Controller is a ruggedized, monolithic, programmable, multifunction system support device fabricated with oxide separated Integrated Injection Logic (I^2L) technology. The SBP 9961 provides the SBP 9900 series Family of Microprocessors with a maskable prioritized interrupt encoding capability. I^2L technology enables the SBP 9961's static logic and TTL compatible I/O to operate over a very wide ambient temperature range from a single d-c power source.

1.2 KEY FEATURES

- SBP 9900 Series Microprocessor Family Peripheral
- 15 Dedicated, Maskable, Prioritized, Encoded Interrupts
- 12 mA Current Sinking Outputs
- 40-Pin Package
- TTL Compatible I/O
- Wide Ambient Temperature Operation
  - SBP 9961NJ: −55°C to +125°C (with high-reliability processing) (screened to MIL-STD 883B)
- I^2L Technology
  - Constant-Current Power Source
  - Fully Static Operation
  - Single-Phase Edge-Triggering Clock
  - Wide Temperature Stability

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2.0 FUNCTIONAL DESCRIPTION

2.1 SBP 9961/CPU INTERFACE

The SBP 9961 communicates with the CPU through the Communications Register Unit (CRU) interface as shown in Figures 1 and 3. The SBP 9961's CRU interface consists of: a) five CRU address select lines (S0-S4) b) a single chip enable (CE), c) a 9961-to-CPU serial data-bit line (CRUIN), d) a CPU-to-9961 serial data-bit line (CRUOUT), and e) a CPU-to-9961 serial data-bit clock (CRUCLK). When $\overline{CE}$ is activated (logic-level low), S0-S4 selects a specific CRU bit function as indicated in Table 1. In the case of a SBP 9961 write operation, the datum is transferred from the CPU to the SBP 9961 via the CRUOUT line. The CRUOUT datum is strobed into the selected 9961 CRU bit function by CRUCLK. In the case of a SBP 9961 read operation, the selected CRU bit function is sampled by the CPU via the CRUIN line.

TABLE 1 – CRU BIT ASSIGNMENTS

CRU BIT	S0	S1	S2	S3	S4	CRU READ DATA	CRU WRITE DATA
0	0	0	0	0	0	Control Bit	Control Bit(1)
1	0	0	0	0	1	$\overline{INT1}$ (2)	Mask1 (3)
2	0	0	0	1	0	$\overline{INT2}$	Mask2
3	0	0	0	1	1	$\overline{INT3}$	Mask3
4	0	0	1	0	0	$\overline{INT4}$	Mask4
5	0	0	1	0	1	$\overline{INT5}$	Mask5
6	0	0	1	1	0	$\overline{INT6}$	Mask6
7	0	0	1	1	1	$\overline{INT7}$	Mask7
8	0	1	0	0	0	$\overline{INT8}$	Mask8
9	0	1	0	0	1	$\overline{INT9}$	Mask9
10	0	1	0	1	0	$\overline{INT10}$	Mask10
11	0	1	0	1	1	$\overline{INT11}$	Mask11
12	0	1	1	0	0	$\overline{INT12}$	Mask12
13	0	1	1	0	1	$\overline{INT13}$	Mask13
14	0	1	1	1	1	$\overline{INT14}$	Mask14
15	0	1	1	1	1	$\overline{INT15}/\overline{INTREQ}$	Mask 15

NOTES: (1) 0 = Interrupt Mode; 1 = No operation except CRU bit 15 – $\overline{INTREQ}$
(2) Data present on $\overline{INT}$ input will be read regardless of mask value.
(3) While in the Interrupt Mode (Control Bit = 0), writing a "1" into a mask will enable interrupt, "0" will disable.

2.2 INTERRUPT CONTROL

A block diagram of the SBP 9961 interrupt control section is shown in Figure 2. The interrupt inputs are sampled on the positive-going edge of CLOCK and are ANDed with their respective mask bits. If an interrupt input is active (low) and enabled (MASK = 1), the signal is passed through the priority encoder where the highest priority signal is encoded into a 4-bit binary word as shown in Table 2. This word, along with an interrupt request, is then output to the CPU on the positive-going edge of the next CLOCK.

The output signals will remain valid until either the corresponding interrupt input is removed, the interrupt is disabled (MASK = 0), or a higher priority enabled interrupt becomes active. When the highest priority enabled interrupt is removed, the code corresponding to the next highest priority enabled interrupt is output. If no enabled interrupt is active, $\overline{INTREQ}$ will be pulled to logic-level high with IC0–IC3 retaining the last asserted interrupt code. $\overline{RESET}$ (power-up reset) will force the interrupt code IC0–IC3 to (0,0,0,0) with $\overline{INTREQ}$ pulled high, and will reset all mask bits low (interrupts disabled). Individual interrupts can be subsequently enabled (disabled) by programming the appropriate mask bits. Unused interrupt inputs may be used as data inputs by disabling the interrupt (MASK = 0).

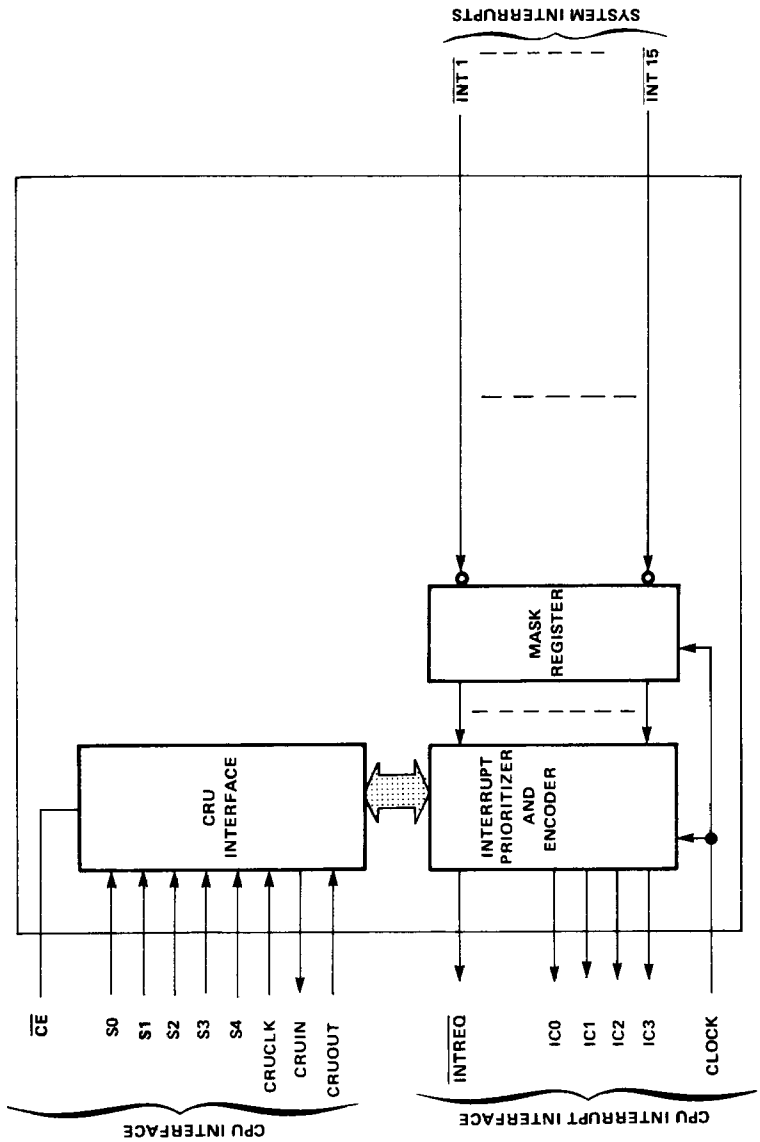

FIGURE 1 – SBP 9961 BLOCK DIAGRAM

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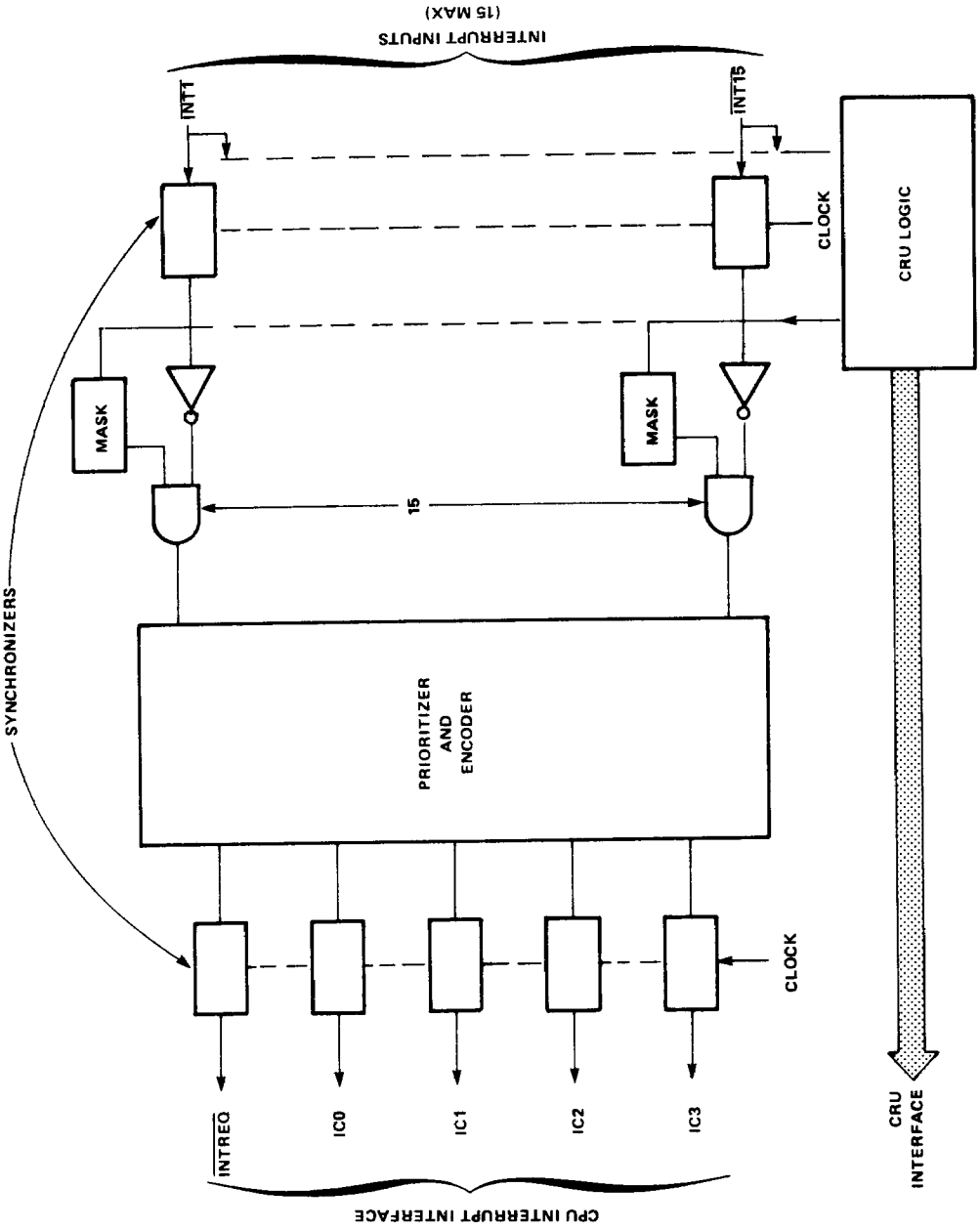

FIGURE 2 – INTERRUPT CONTROL LOGIC

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TABLE 2
INTERRUPT CODE GENERATION

INTERRUPT/STATE	PRIORITY	I_{C0}	I_{C1}	I_{C2}	I_{C3}	$\overline{INTREQ}$
$\overline{INT}$ 1	1 (HIGHEST)	0	0	0	1	0
$\overline{INT}$ 2	2	0	0	1	0	0
$\overline{INT}$ 3	3	0	0	1	1	0
$\overline{INT}$ 4	4	0	1	0	0	0
$\overline{INT}$ 5	5	0	1	0	1	0
$\overline{INT}$ 6	6	0	1	1	0	0
$\overline{INT}$ 7	7	0	1	1	1	0
$\overline{INT}$ 8	8	1	0	0	0	0
$\overline{INT}$ 9	9	1	0	0	1	0
$\overline{INT}$ 10	10	1	0	1	0	0
$\overline{INT}$ 11	11	1	0	1	1	0
$\overline{INT}$ 12	12	1	1	0	0	0
$\overline{INT}$ 13	13	1	1	0	1	0
$\overline{INT}$ 14	14	1	1	1	0	0
$\overline{INT}$ 15	15 (LOWEST)	1	1	1	1	0
NO INTERRUPT	–	Note 1	Note 1	Note 1	Note 1	1

(1) IC0-IC3 hold the level code of the previous interrupt.

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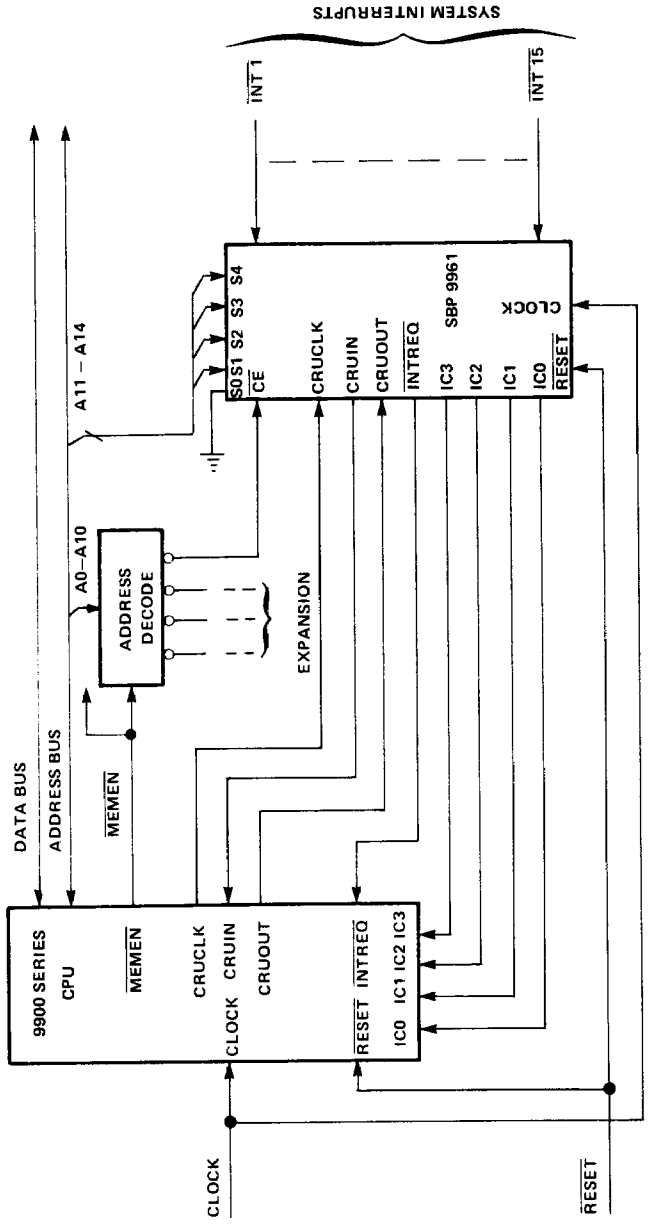

FIGURE 3 – SBP 9961 SYSTEM CONFIGURATION

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2.6 SBP 9961 PIN ASSIGNMENTS AND FUNCTIONS

SIGNATURE	PIN	I/O	DESCRIPTION
S0	33	IN	ADDRESS SELECT LINES. The data bit being accessed by the CRU interface is specified by the 4-bit code appearing on S1–S4. S0 is used as the high order select line when the SBP 9961 is used with the SBP 9960. Otherwise, tie S0 to logic-level low.
S1	35	IN	
S2	31	IN	
S3	34	IN	
S4	32	IN	
CRUIN	28	OUT	CRU DATA IN (to CPU). Data specified by S0-S4 is transmitted to the CPU by CRUIN. When $\overline{CE}$ is not active, CRUIN is logic-level high.
CRUOUT	17	IN	CRU DATA OUT (from CPU). When $\overline{CE}$ is active, data present on the CRUOUT input will be sampled during CRUCLK and written into the CRU bit specified by S0-S4.
CRUCLK	1	IN	CRU CLOCK (from CPU). CRUCLK specifies that valid data is present on the CRUOUT line.
$\overline{RESET}$	38	IN	POWER-UP RESET. When active (low), $\overline{RESET}$ forces all interrupt masks to "0", and disables the clock.
$\overline{CE}$	2	IN	CHIP ENABLE. When active (low), data transfers may occur between the CPU and the SBP 9961.
	11	NC	
	24	NC	
	30	NC	
	36	NC	
	39	NC	
IC0	3	OUT	INTERRUPT CODE LINES (to CPU). IC0 (MSB) through IC3 output the binary code corresponding to the highest priority enabled interrupt most recently asserted.
IC1	4	OUT	
IC2	5	OUT	
IC3	6	OUT	
$\overline{INTREQ}$	7	OUT	INTERRUPT REQUEST (to CPU). When active (low) $\overline{INTREQ}$ indicates to the CPU that an enabled interrupt has been asserted, prioritized, and encoded.
CLOCK	9	IN	CPU SYSTEM CLOCK. Used by the SBP 9961 to synchronize the interrupt interface ($\overline{INTREQ}$, IC0-IC3) to the CPU.
INJ	40		Supply Current
GND	19, 20		Ground
V_{CC}	37		Common voltage return/reference for all output pull-up resistors.
$\overline{INT1}$	12	IN	INTERRUPT INPUTS. When active (low), the signal is ANDed with its corresponding mask bit and if enabled sent to the interrupt control section. $\overline{INT1}$ has highest priority.
$\overline{INT2}$	13	IN	
$\overline{INT3}$	21	IN	
$\overline{INT4}$	14	IN	
$\overline{INT5}$	15	IN	
$\overline{INT6}$	16	IN	
$\overline{INT7}$	18	IN	
$\overline{INT8}$	8	IN	
$\overline{INT9}$	10	IN	
$\overline{INT10}$	22	IN	
$\overline{INT11}$	23	IN	
$\overline{INT12}$	25	IN	
$\overline{INT13}$	26	IN	
$\overline{INT14}$	27	IN	
$\overline{INT15}$	29	IN	

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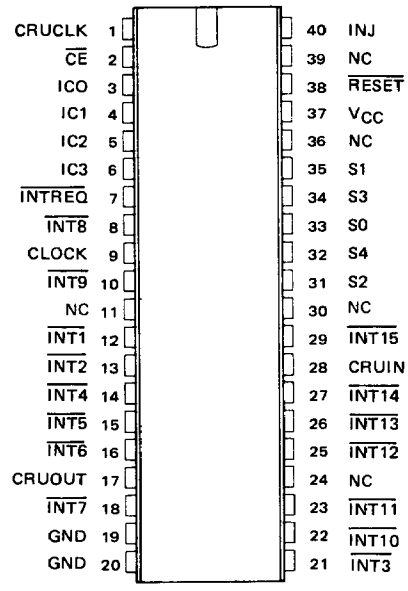

3.0 ELECTRICAL SPECIFICATIONS

3.1 RECOMMENDED OPERATING CONDITIONS, UNLESS OTHERWISE NOTED I_{CC}= 130 mA

	MIN	NOM	MAX	UNIT
Supply current, I_{CC}	115	130	145	mA
High-level output voltage, V_{OH}			5.5	V
Low-level output current, I_{OL}			12	mA
Operating free-air temperature, T_A	−55		125	°C

3.2 ELECTRICAL CHARACTERISTICS (OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE, UNLESS OTHERWISE NOTED)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	I_{CC} = MIN,	I_I = −12 mA			−1.5	V
I_{OH}	High-level output current	I_{CC} = 130 mA, V_{IL} = 0.8 V,	V_{IH} = 2 V, V_{OH} = 5.5 V			−400	μA
V_{OL}	Low-level output voltage	I_{CC} = 130 mA, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 12 mA			0.5	V
I_I	Input current	I_{CC} = 130 mA,	V_I = 2.4 V		180		μA

†For conditions shown as MAX, use the appropriate value specified under recommended operating conditions

‡All typical values are at I_{CC} = 130 mA, T_A = 25°C.

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3.3 TIMING REQUIREMENTS OVER FULL RANGE OF OPERATING CONDITIONS

	PARAMETER	MIN	NOM	MAX	UNIT
t_c	Clock cycle time	333			ns
t_r	Clock rise time		10	20	ns
t_f	Clock fall time		10	20	ns
t_{wL}	Clock pulse low width	111			ns
t_{wH}	Clock pulse high width	222			ns
t_{su}	Setup time for S0-S4, $\overline{CE}$, or CRUOUT before CRUCLK		200		ns
t_{su}	Setup time, input before valid CRUIN		200		ns
t_{su}	Setup time, interrupt before clock high		60		ns
$t_{w(CRUCLK)}$	CRU clock pulse width		100		ns
t_h	Address hold time		80		ns

3.4 SWITCHING CHARACTERISTICS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PD}	Propagation delay, ↑ CLOCK to valid $\overline{INTREQ}$, IC0-IC3	C_L = 100 pF, R_L = 390 Ω		150		ns
t_{PD}	Propagation delay, S0-S4 or $\overline{CE}$ to valid CRUIN	C_L = 100 pF, R_L = 390 Ω		330		ns

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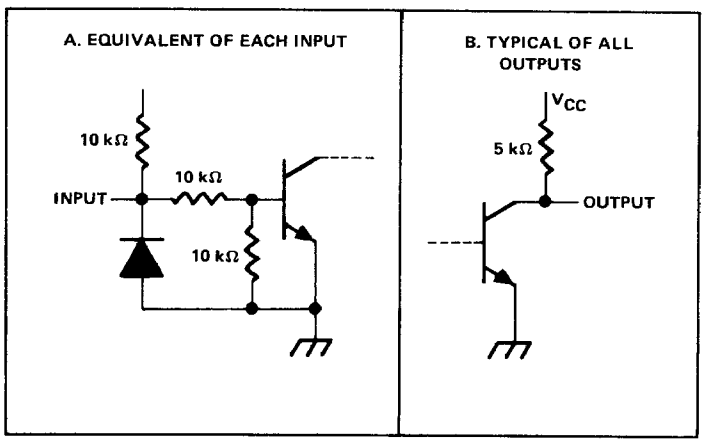
4.0 INPUT, OUTPUT STRUCTURES



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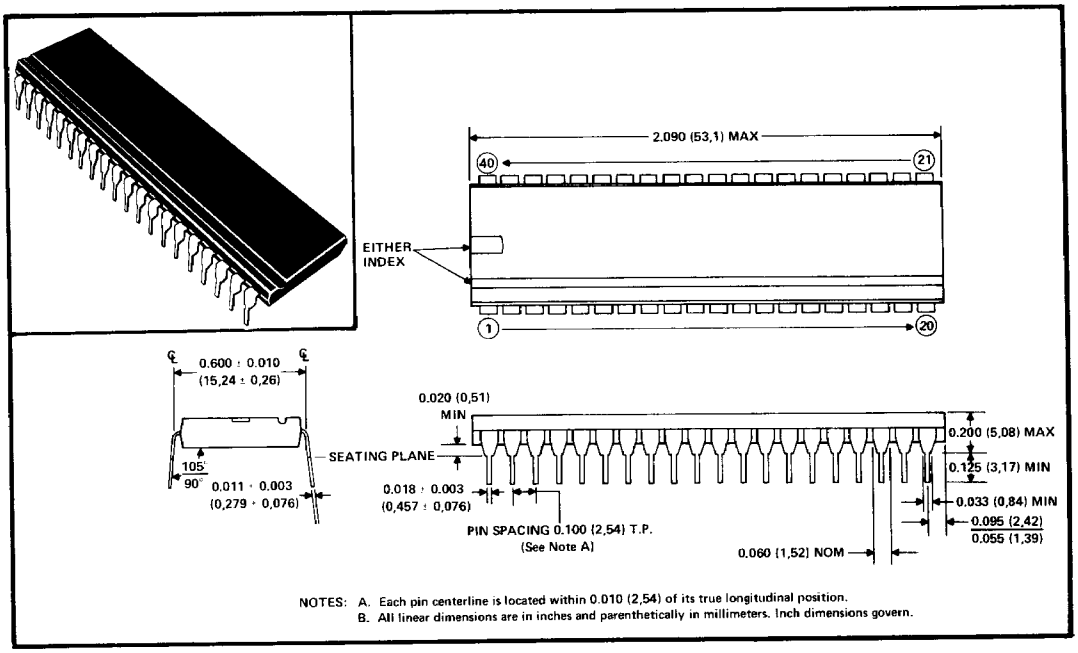
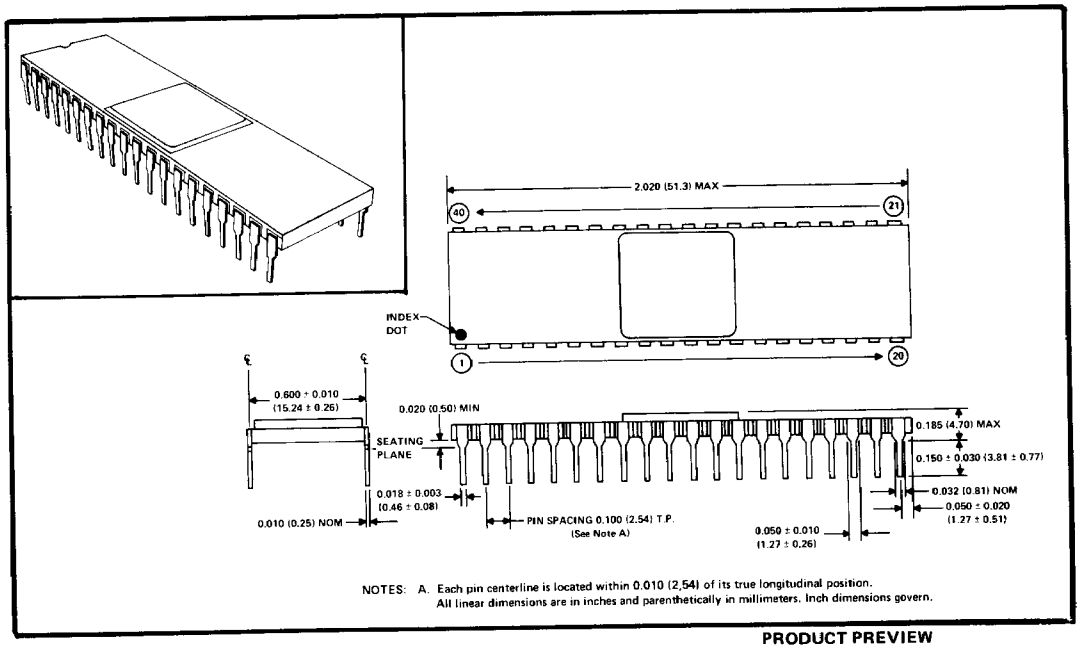
5.0 MECHANICAL DATA

5.1 40-PIN PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. Each pin centerline is located within 0.010 (2,54) of its true longitudinal position.
B. All linear dimensions are in inches and parenthetically in millimeters. Inch dimensions govern.

5.2 40-PIN CERAMIC DUAL-IN-LINE PACKAGE



NOTES: A. Each pin centerline is located within 0.010 (2,54) of its true longitudinal position.
All linear dimensions are in inches and parenthetically in millimeters. Inch dimensions govern.

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