SuperH™ RISC engine Peripheral LSI

HD64413A Q2SD

User's Manual

HITACHI

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Cautions

Preface

With the recent advent of home video-game machines that offer a fast, responsive man-machine interface and high-resolution graphics at a low price, there is a demand for a similar revolution in graphics quality in the entire home information market, covering such products as car navigation systems and Internet TVs.

In addition to the need for a powerful and simple means of handling the necessary processing, there are growing demands for the preservation of upward-compatibility of software and data bases. At the same time, there is the question of how best to handle the increasingly complex graphics algorithms required for these applications.

In response to this demand, Hitachi has developed the Q Series of graphics accelerators, offering high-speed rendering and display processing in a chip set that includes a SuperH family microcomputer.

The Q ("Quick") Series is designed for use in a chip set with a SuperH family microcomputer to provide a compact system capable of the high-speed geometric, rendering, and display processing required by graphics display systems.

Q Series devices perform rendering and display processing compatible with the SuperH family, based on the concepts of simplicity, realtime operation, and upgradability.

The HD64413A (Q2SD) is a 2D graphics renderer for Q Series minimum system configuration use, featuring minimized graphics memory (one 16-Mbit memory), unified handling of graphics and natural images, realtime software 3D graphics drawing, and improved system bus utilization. The Q2SD makes it possible to implement a compact graphics processing system with high-level drawing capabilities for a wide range of multimedia terminals, including car navigation systems, medium-definition OA products such as Internet computers, display systems in industrial equipment, and AV products such as Internet TVs and karaoke systems.

For examples of the use of this LSI, see Q Series Application Notes—HD64413A Q2SD.

Contents

Section 1 Overview of Q2SD (Quick 2D Graphics Renderer with Synchronous DRAM Interface)

1.1 Q2SD Overview

The Q2SD (Quick 2D Graphics Renderer) is a 2D graphics renderer for minimum system configuration use in the SH microcomputer graphics accelerator “Quick” series (Q Series), based on the concepts of simplicity, realtime operation, and upgradability.

The use of unified graphics memory (UGM) and a double-buffering system that switches drawing and display buffers in frame units, providing a high-speed drawing performance of 60 screens per second, has made possible minimization of graphics memory (with the use of a single 16-Mbit memory), unified handling of graphics and natural images, and realtime software 3D graphics drawing. The clear separation of geometric operations (handled by the CPU) and rendering operations (handled by the Q2SD) has also resulted in improved system bus utilization.

The Q2SD is a high-performance graphics rendering LSI for multimedia applications, which provides both drawing and display functions integrated into a single chip.

A sample Q2SD system configuration is shown in figure 1.1.

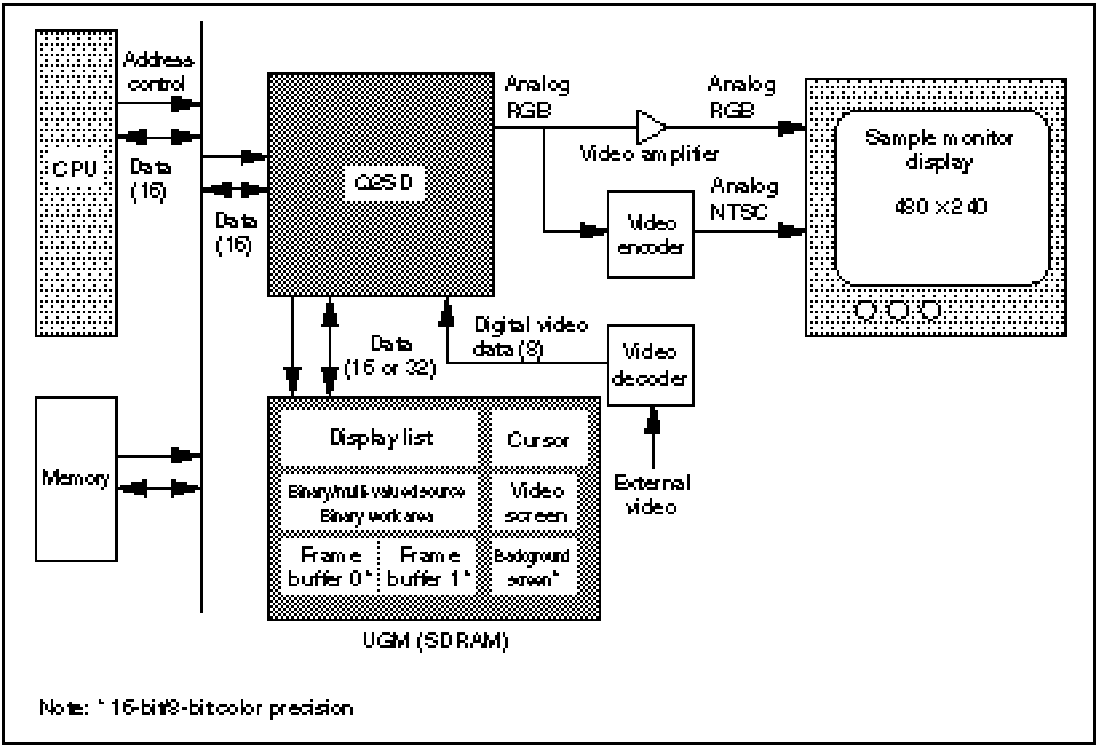


Figure 1.1 Sample System Configuration

1.2 Block Diagram

Figure 1.2 shows a block diagram of the Q2SD. The functions of the various blocks in figure 1.2 are as follows.

- Rendering unit

  Performs fetching and interpretation of the display list in the UGM, references the source data in the UGM, and outputs drawing data to the drawing-side frame buffer in the UGM.
- Rendering buffer unit

  Buffers data and addresses between the rendering unit and the UGM, and outputs them efficiently.
- CPU interface unit

  Performs control relating to connection to the CPU bus.
- Memory interface unit

  Performs control relating to connection to the UGM bus.
- Display unit

  Controls the control signals sent to the CRT device.

- Display buffer unit

  Reads data to be displayed on the CRT from the display-side frame buffer, and outputs the display data in accordance with the display timing.

- Color palette (6 bits per color)

  When using 8 bits/pixel, performs conversion to display data of 256 colors out of 262,144, based on the color conversion table.

- ΔYUV (YUV) → RGB conversion

  Converts input data ΔYUV (262,144 colors) or YUV (262,144 colors) to RGB data (65,536 colors), and stores it in the UGM.

- Video unit

  Fetches 4:2:2 YUV data and stores it in the UGM in YC or RGB format.

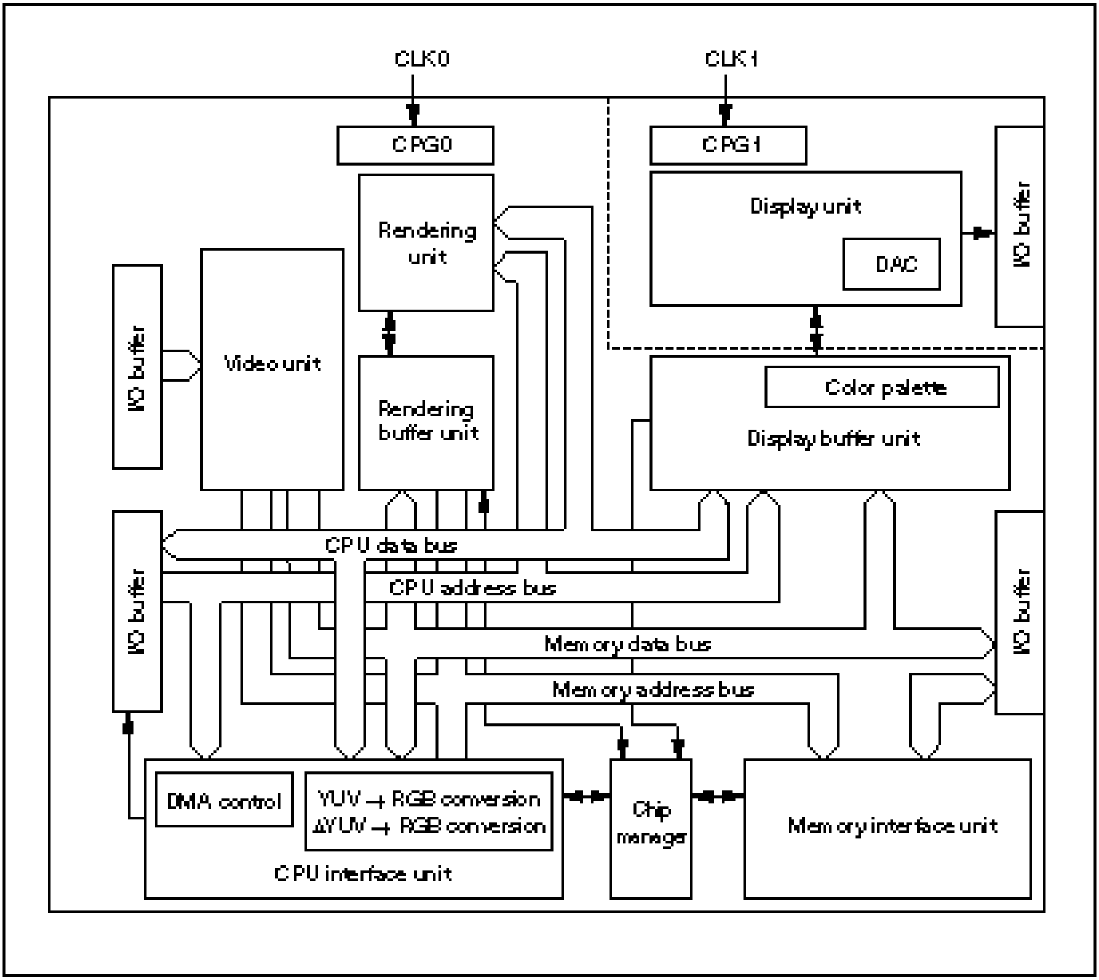


Figure 1.2 Internal Block Diagram

1.3 Concepts

1.3.1 Simplicity (Optimization of System Configuration)

Use of Unified Graphics Memory Architecture:

· Unified handling of image data (unified graphics memory (UGM) architecture)
  Data in various formats can be stored and managed in the same unified graphics memory (see figure 1.3).

· Minimum necessary UGM
  Minimum UGM configuration: One 16-bit-data-bus type 16-Mbit synchronous DRAM

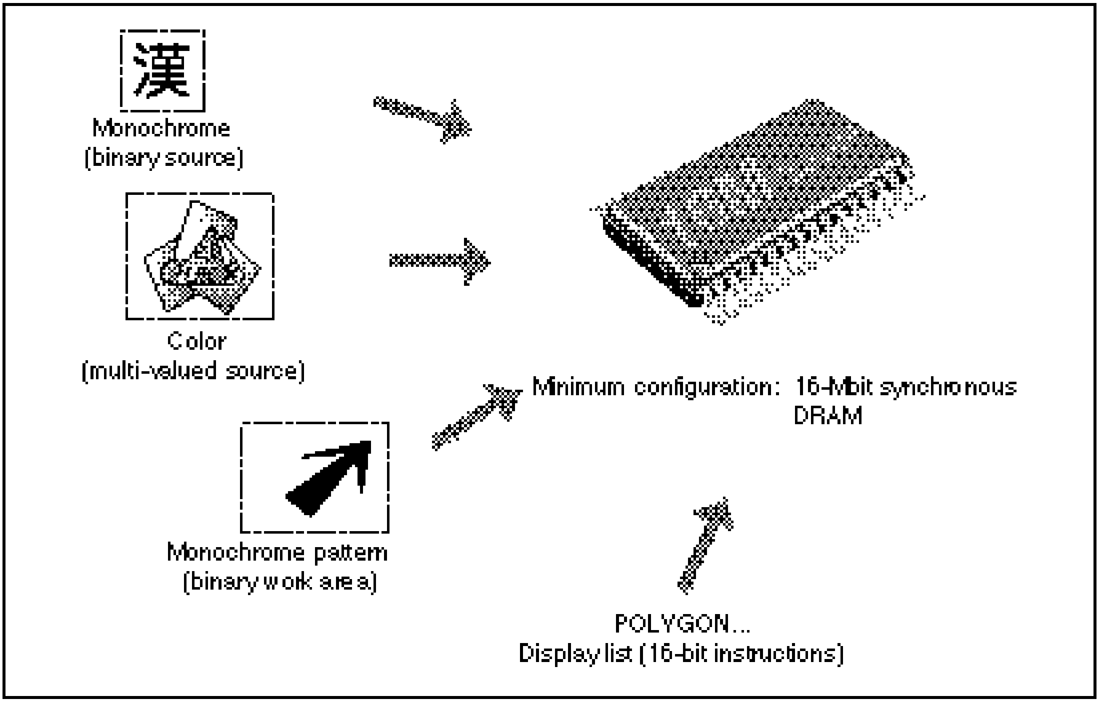


Figure 1.3 Reduced System Size Through Use of UGM Architecture

· Unified system bus interface

A CPU interface circuit is incorporated to provide a unified interface. This enables unified graphics memory to be allocated in the CPU's memory space (see figure 1.4).

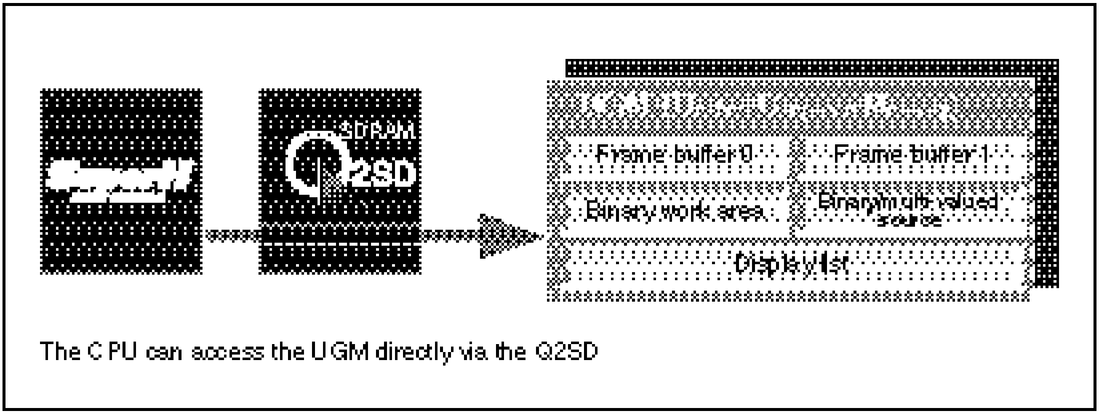


Figure 1.4 Unified System Bus Interface

1.3.2 Realtime Operation

Use of Double-Buffering Architecture: The use of a double-buffering architecture that allows switching between the drawing buffer and display buffer in frame or field units, together with the use of synchronous DRAM for the UGM, enables realtime operation by alternating display processing with high-speed drawing processing (see figure 1.5).

· Double-buffer control

Kinds of double-buffer control:

¾ Auto display change mode

Mode in which priority is given to a display frame change. Can be used when drawing ends during a frame interval.

¾ Auto rendering mode

Mode in which display switching is not performed until drawing ends. If drawing does not end within one frame, drawing is continued without interruption and a frame change is performed at the frame boundary after drawing is completed.

¾ Manual display change mode

Mode in which display frame changes and the start of drawing are controlled by software. When the display area change bit (DC bit) is set after drawing is completed, a frame change is performed at the next frame boundary.

Double-buffer switching timing:

¾ Non-interlace mode

Scanning system in which one frame is composed of one field. Double-buffer switching is performed in units of a frame.

¾ Interlace mode

Scanning system in which one frame is composed of two fields. Double-buffer switching is performed in units of a frame.

¾ Interlace sync & video mode

Scanning system in which one frame is composed of two fields. Double-buffer switching is performed in units of a field.

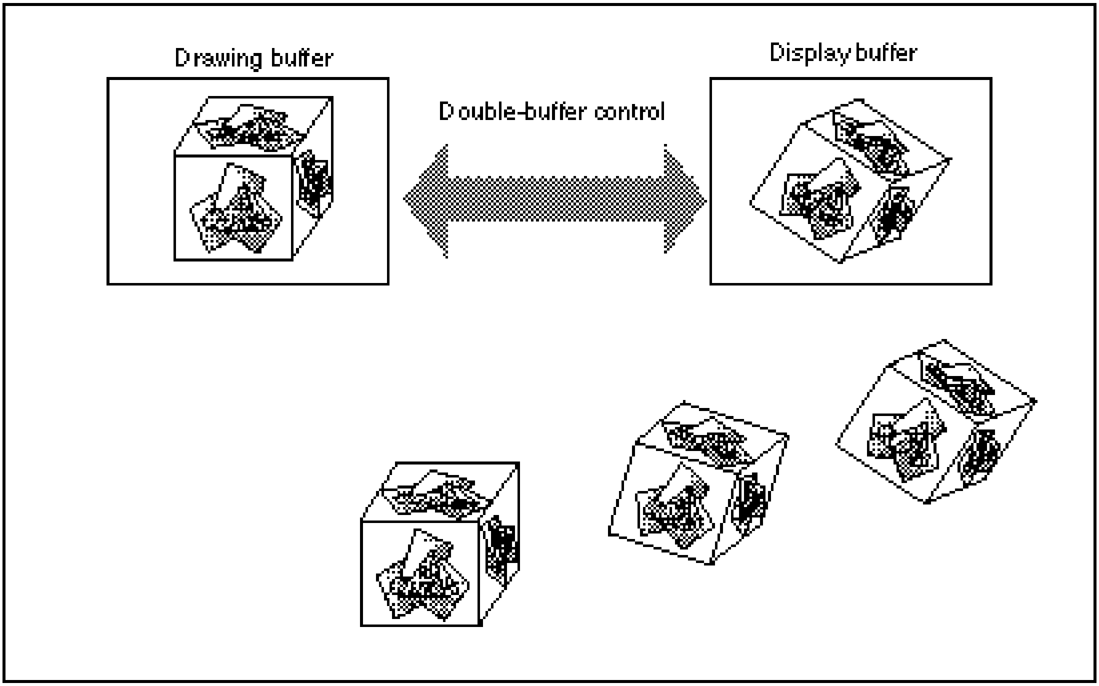


Figure 1.5 Double-Buffering Architecture

Support for Synchronous DRAM: Synchronous DRAM can be used for the UGM. This enables the Q2SD to use burst access to the UGM and perform high-speed drawing.

Use of Write-Only Drawing: Write-only drawing (a drawing method using only write operations) is used to improve drawing performance.

1.3.3 Upgradability

Algorithm Upgrading: In the Q2SD's drawing system, algorithms for coordinate conversion, etc., are executed by the CPU, using a systematized data base containing coordinates and other data, and the results are represented in graphical form. Thus, the graphics for a variety of shapes can be implemented simply by upgrading the algorithms, without having to modify the data base (see figure 1.6).

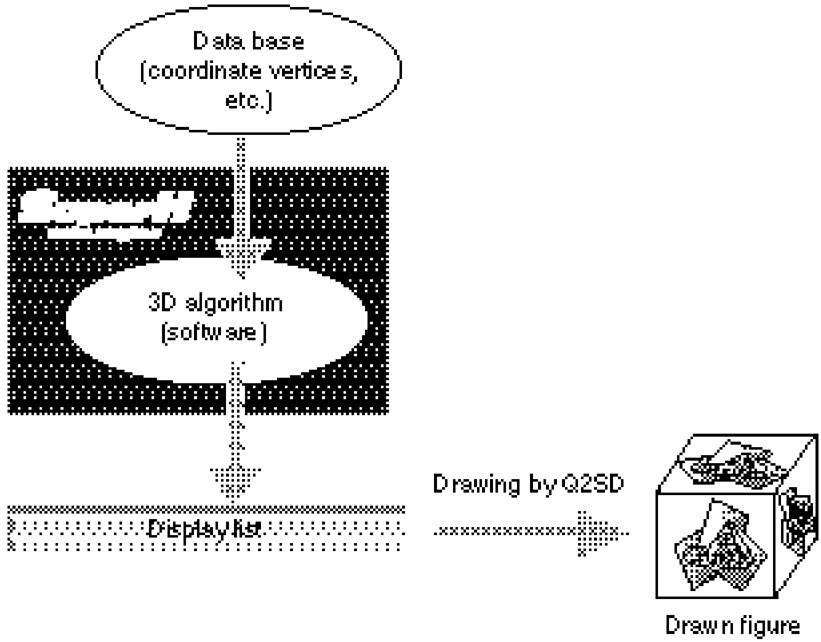


Figure 1.6 Data Flow when Using a 3D Algorithm

Drawing System Upgrading: The Q2SD has been developed as a member of the Q Series, enabling the user to select the most appropriate model from the series for a particular application. The user's drawing system can also be upgraded as necessary by changing the Q2SD or CPU combination.

Consistency of Application Interface: The Q2SD's carefully selected drawing commands are of four kinds: four-vertex surface drawing, line drawing, work surface drawing, and work line drawing. This makes it possible to reduce the parts dependent upon drawing commands within an application, and so achieve a more consistent interface between applications.

1.4 Summary of Functions

Table 1.1 summarizes the functions of the Q2SD.

Table 1.1 Summary of Q2SD Functions

Item		Function/Performance
Maximum clock frequency	Drawing system internal operation (operating frequency)	66 MHz × 1, 33 MHz × 2, 16.5 MHz × 4 (using multiplier)
	Display system internal operation	Operating frequency/2 (max. 33 MHz)
Drawing performance		Polygon drawing performance (20 × 25 pixels): 90,000/sec (2-screen composite mode: 60,000/sec)
		Line drawing performance (10 pixels): 1200,000/sec (2-screen composite mode: 400,000/sec)
Display functions	Sample screen sizes	320 × 240, 400 × 240, 480 × 240, 640 × 480, NTSC, PAL, etc.
	CRT scanning system	Non-interlace, interlace, interlace sync & video
	External synchronization	Master, TV synchronization
	Built-in color palette	Simultaneous display of 256 colors out of 260,000
	Cursors	Two cursors, 32 × 32 pixels, display color selectable from color palette
Video		8-bit multiplexed YUV 4:2:2 digital input
Drawing functions	Drawing commands	4-vertex surface drawing, line drawing, work surface drawing, work line drawing
	Color representation	Source: 1/8/16 bits/pixel; drawing: 8/16 bits/pixel; work: binary
	Register setting	Current pointer setting, local offset setting, clipping, specific address-mapped register setting
	Sequence control	Jump, subroutine, vertical retrace line interval wait

Table 1.1 Summary of Q2SD Functions (cont)

Item			Function/Performance
Interfaces	SH	Command/ data transfer	DMA transfer (single address, dual address), or performed by SuperH
		YUV → RGB conversion	16-bit input, 4:2:2 (8 bits each for Y, U, V) 16-bit output (R: 5, G: 6, B: 5 bits)
		ΔYUV → RGB conversion	8-bit input (4 bits each for d-Y, d-U, d-V) 16-bit output (R: 5, G: 6, B: 5 bits)
		Interrupt output	TV sync signal error flag, frame flag, DMA flag, command error flag, vertical blanking flag, trap flag, command suspend flag, drawing break flag
		Supported SuperH	Can be connected to 3.3-V-operation SuperH
	Unified graphics memory	32/16-bit-bus-width synchronous DRAM	Minimum 16 Mbits (choice of one 16-Mbit (×16) memory, two parallel 16-Mbit (×16) memories, one 64-Mbit (×16) memory, or one 64-Mbit (×32) memory)
	Display	Analog RGB output	6-bit resolution for each of R, G, and B (8-bit resolution for each of R, G, and B for video stored in UGM in YC format)
Process/package			0.35-micron CMOS/176-pin LQFP
Power supply voltage/temperature range			3.3 V ±0.3 V/0°C to 70°C (Details of a –40°C to 85°C special-specification model are also available from Hitachi sales representatives)

1.5 Basic Functions

1.5.1 Interface Functions

DMA Transfer Function: Data can be transferred between memory connected to the CPU bus and the graphics memory using the DMAC. DMA transfer can be used for display list, YUV data, and ΔYUV data transfer. In DMA transfer, the Q2SD controls graphics memory addresses with its internal address counter, enabling high-speed transfer in single address mode or dual address mode.

YUV → RGB Conversion: Data comprising 8 bits for each of Y, U, and V, in a 4:2:2 format, is converted to RGB data (R: 5 bits, G: 6 bits, B: 5 bits).

ΔYUV → RGB Conversion: Data comprising 4 bits for each of ΔY, U, and V is converted to RGB data (R: 5 bits, G: 6 bits, B: 5 bits).

Interrupt Output Function: Interrupt output to the CPU can be generated based on the vertical retrace line interval and by command. This feature is used for display list and source data transfer to the UGM, and blinking control.

Synchronous DRAM Support: 32/16-bit-bus-width synchronous DRAM can be used as the UGM.

Multiplication Function: The Q2SD allows duty free designation of the external input clock (CLK0).

Video Input: An 8-bit data stream with a YUV4:2:2 format is taken in and stored in the UGM in YC or RGB 16-bit format.

Analog RGB Output: The Q2SD performs 18-bit/pixel analog RGB output (6-bit resolution for each of R, G, and B).

1.5.2 Rendering Functions

Coordinate Systems: The Q2SD has four 2-dimensional coordinate systems (screen coordinates, rendering coordinates, multi-valued source coordinates, and work coordinates), and one 1-dimensional coordinate system (binary source coordinates).

Screen coordinates are display control coordinates. Screen coordinate X corresponds to the horizontal dimension of the display screen, and Y to the vertical dimension, and the origin is at the upper left of the display screen. The screen coordinate positive directions are right for the X-axis and down for the Y-axis. Either 16 bits (16 bits/pixel) or 8 bits (8 bits/pixel) can be selected as the data width of one screen coordinate.

Rendering coordinates are drawing control coordinates. Rendering coordinates are shifted horizontally and vertically with respect to screen coordinates by the offset amounts specified in drawing commands. Drawing commands perform drawing operations using these coordinates. However, drawing commands that specify clipping use screen coordinates. Either 16 bits (16 bits/pixel) or 8 bits (8 bits/pixel) can be selected as the data width of one rendering coordinate.

Multi-valued source coordinates are drawing control coordinates. When a drawing command is executed, these are the source (rectangle) coordinates specified by the command. Either 16 bits (16 bits/pixel) or 8 bits (8 bits/pixel) can be selected as the data width of one multi-valued source coordinate.

Binary source coordinates are drawing control coordinates. When a drawing command is executed, these are the source data (1-dimensional) coordinates specified by the command. The data width of one binary source coordinate is 1 bit (1-bit/pixel). For one binary source, one physical address (top-left) and the horizontal width and vertical height of the binary source are specified.

Work coordinates are drawing control coordinates that correspond one-to-one with the screen coordinates. When a drawing command is executed, these are the work coordinates specified by the command. The data width of one work coordinate is 1 bit.

The maximum screen coordinate values are X = 1023, Y = 511.

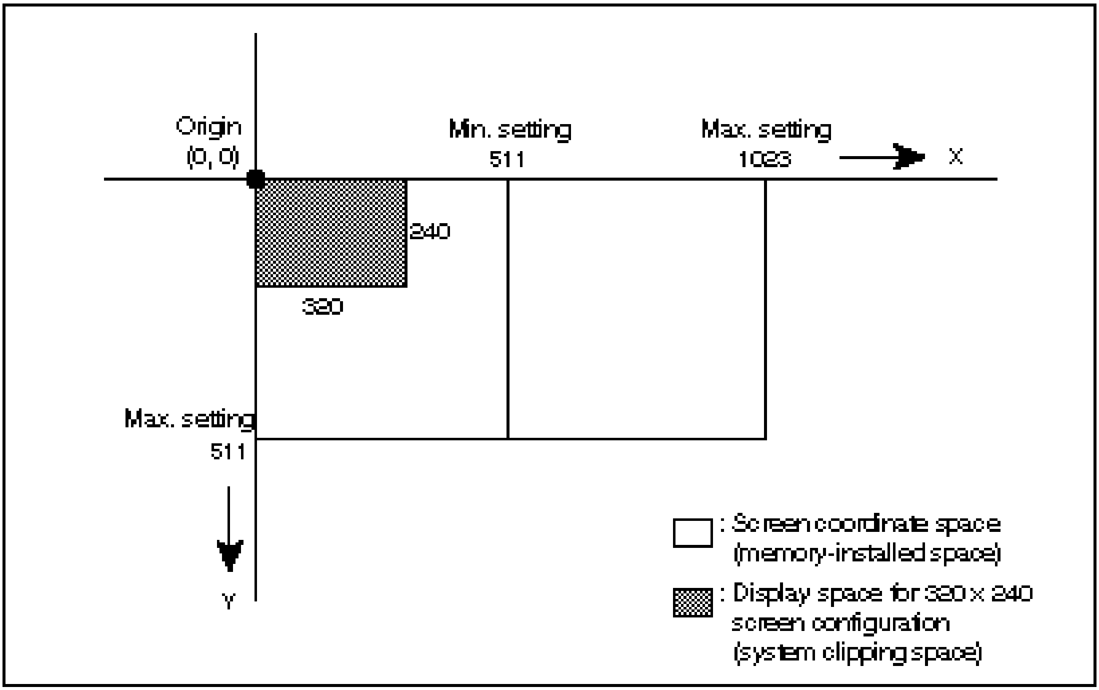


Figure 1.7 Screen Coordinates

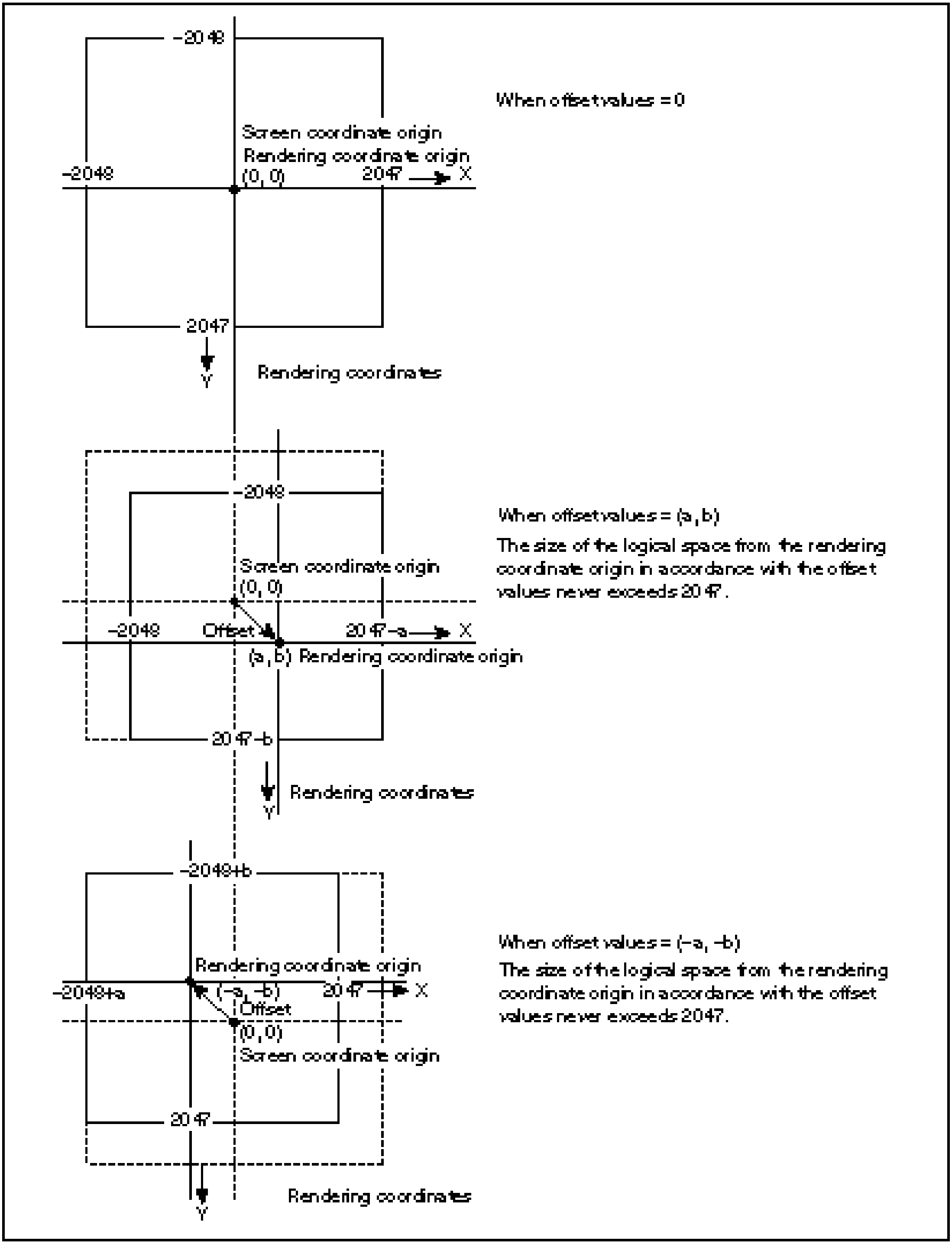


Figure 1.8 Rendering Coordinates

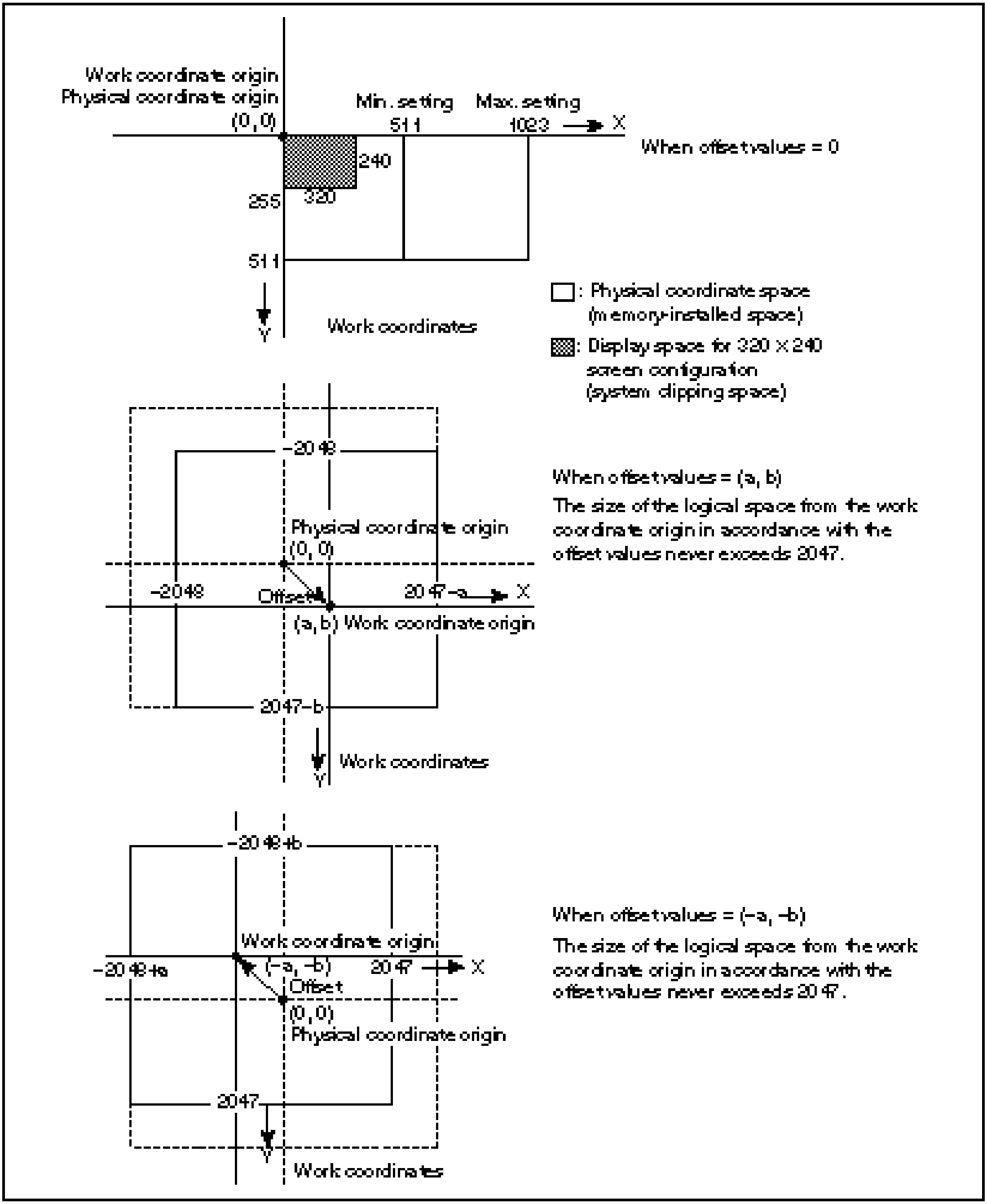


Figure 1.9 Work Coordinates

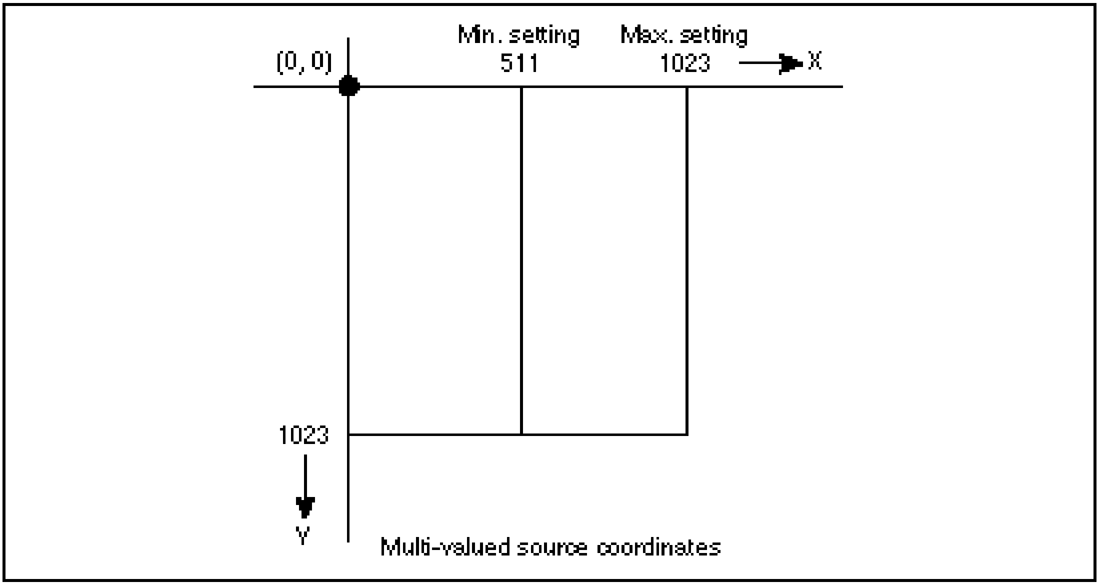


Figure 1.10 Multi-Valued Source Coordinates

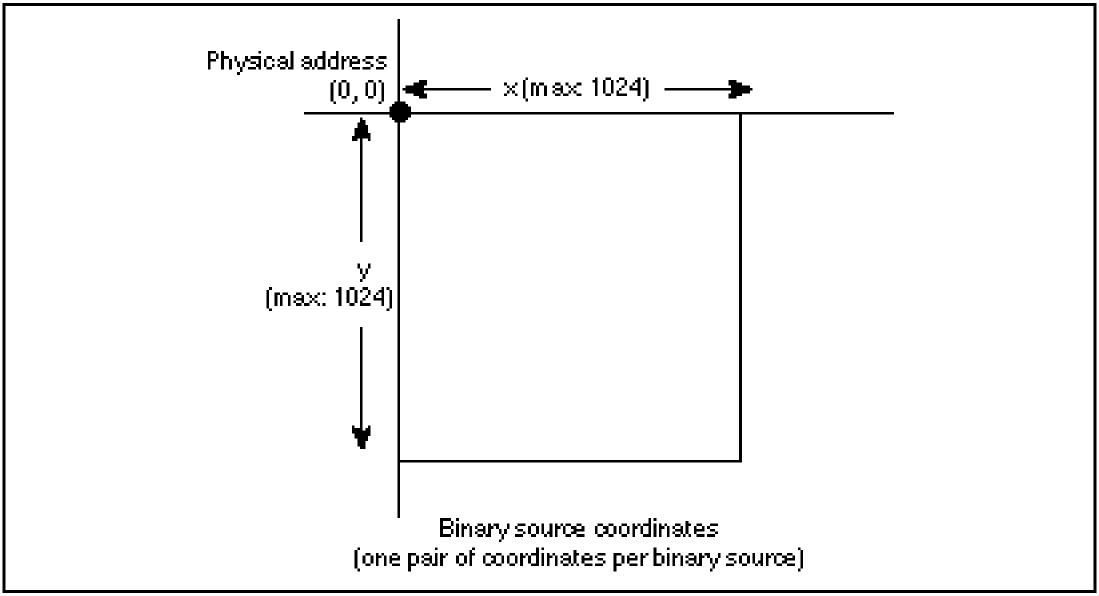


Figure 1.11 Binary Source Coordinates

Drawing Functions: Drawing is performed at rendering coordinates or work coordinates by means of drawing commands. Whether or not source referencing is possible, and the drawing destination (rendering or work coordinates), depend on the individual drawing command.

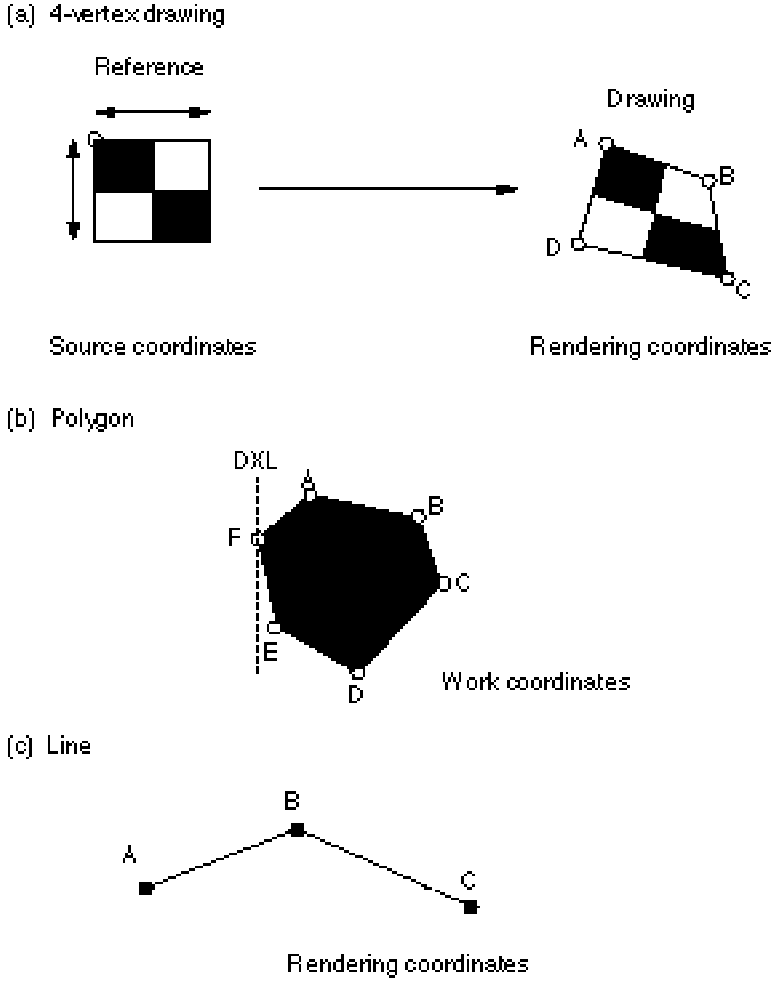


Figure 1.12 Drawing Functions

Jump: Changes the address specifying the display list (linked drawing command list) fetch destination (JUMP command).

Subroutines: Subroutines down to one nesting level can be used in display list control (GOSUB command).

Interrupts: An interrupt is sent to the CPU when the internal state of the chip changes.

Clipping: Two kinds of clipping can be specified: system clipping (SCLIP command) and user clipping (UCLIP command).

No Operation: No operation is performed. The next instruction is simply fetched, without any processing being executed (NOP3 command).

Drawing Suspension and Resumption: The Q2SD supports a drawing suspend/resume function, synchronized with the $\overline{VSYNC}$ signal between the CPU and Q2SD. This function is mainly used when alternately using frame buffers and the background screen to execute drawing.

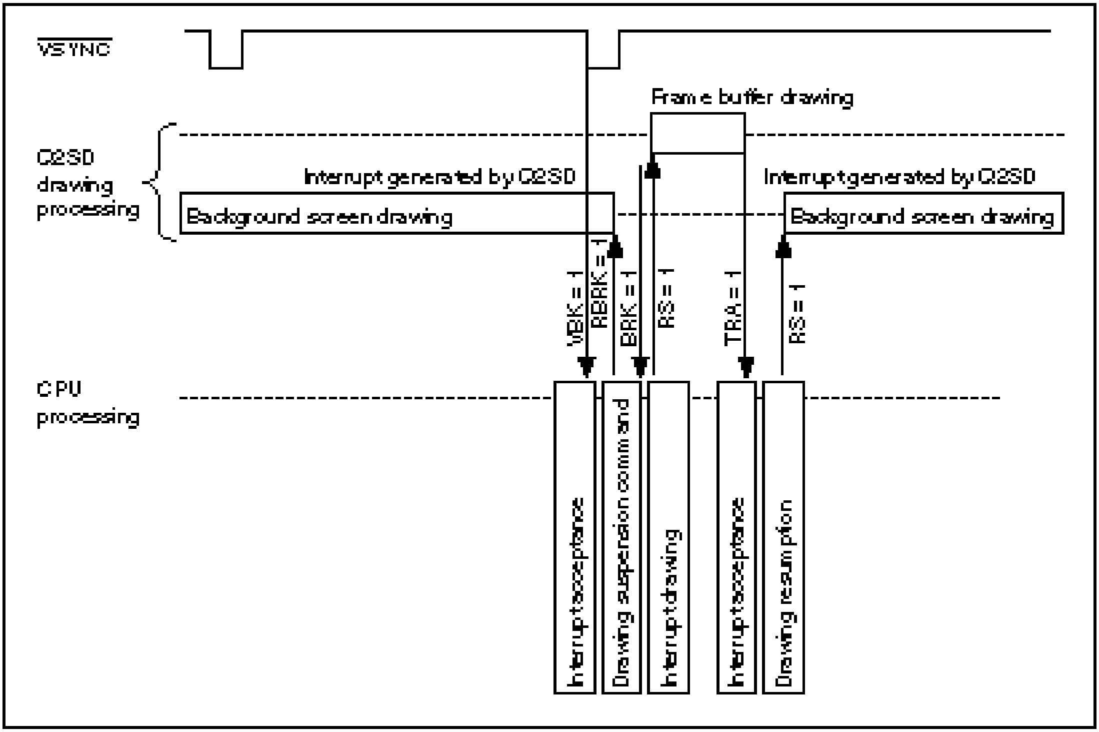


Figure 1.13 Example of Timing for Suspending and Resuming Background Screen Drawing

1.5.3 Display Functions

Display Size: Standard 480 × 240, display size settable by register

CRT Scan Modes: There are three scan modes:

- Non-interlace (vertical scan cycle examples: 1/60 sec, 1/30 sec)
- Interlace (vertical scan cycle example: 1/30 sec)
- Interlace sync & video (vertical scan cycle example: 1/30 sec)

External Synchronization Mode (TV Sync Mode): In TV sync mode, the Q2SD is synchronized and operated using the horizontal and vertical sync signals of a TV, video, or other external asynchronous system

In this mode, the TV, video, or other asynchronous system is treated as the master, and the Q2SD as the slave. The Q2SD can synchronize its display output with the external system.

Synchronization is performed every horizontal scan with the $\overline{\text{EXHSYNC}}$ input signal, and every vertical scan with the $\overline{\text{EXVSYNC}}$ input signal (see section 3.3.4, Display Functions).

Built-In Color Palette: The Q2SD has a built-in color palette that enables simultaneous display of 256 colors out of 262,144. The palette is mapped onto the Q2SD's register space, with 6 bits used for each of R, G, and B. The color palette is only valid in 8-bit/pixel mode.

2.1 Pin Arrangement and Functions

2.1.1 Overview of Pins

Figure 2.1 shows an overview of the Q2SD's pins. Unused input pins should be made inactive by pulling them up or down.

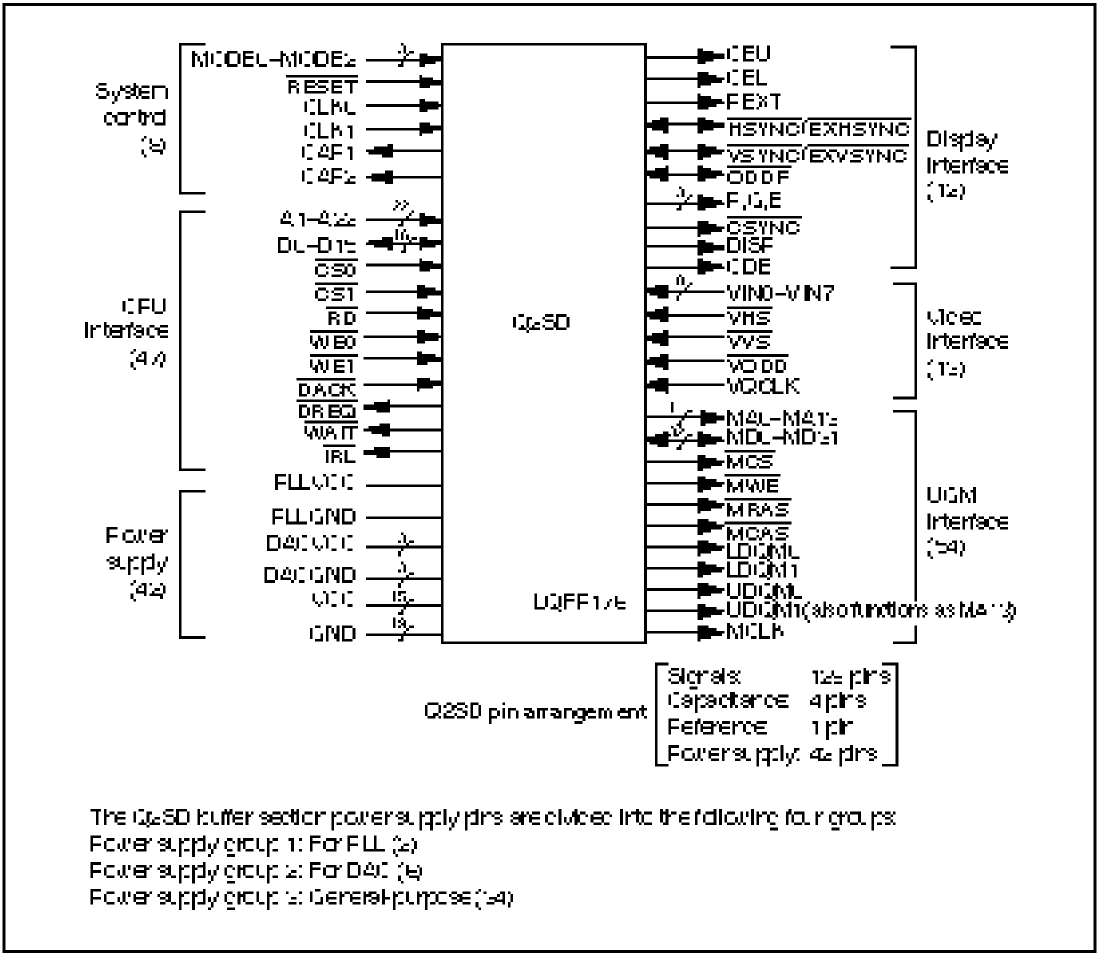


Figure 2.1 Overview of Q2SD Pins

2.1.2 Pin Arrangement

Figure 2.2 shows the pin arrangement of the Q2SD.

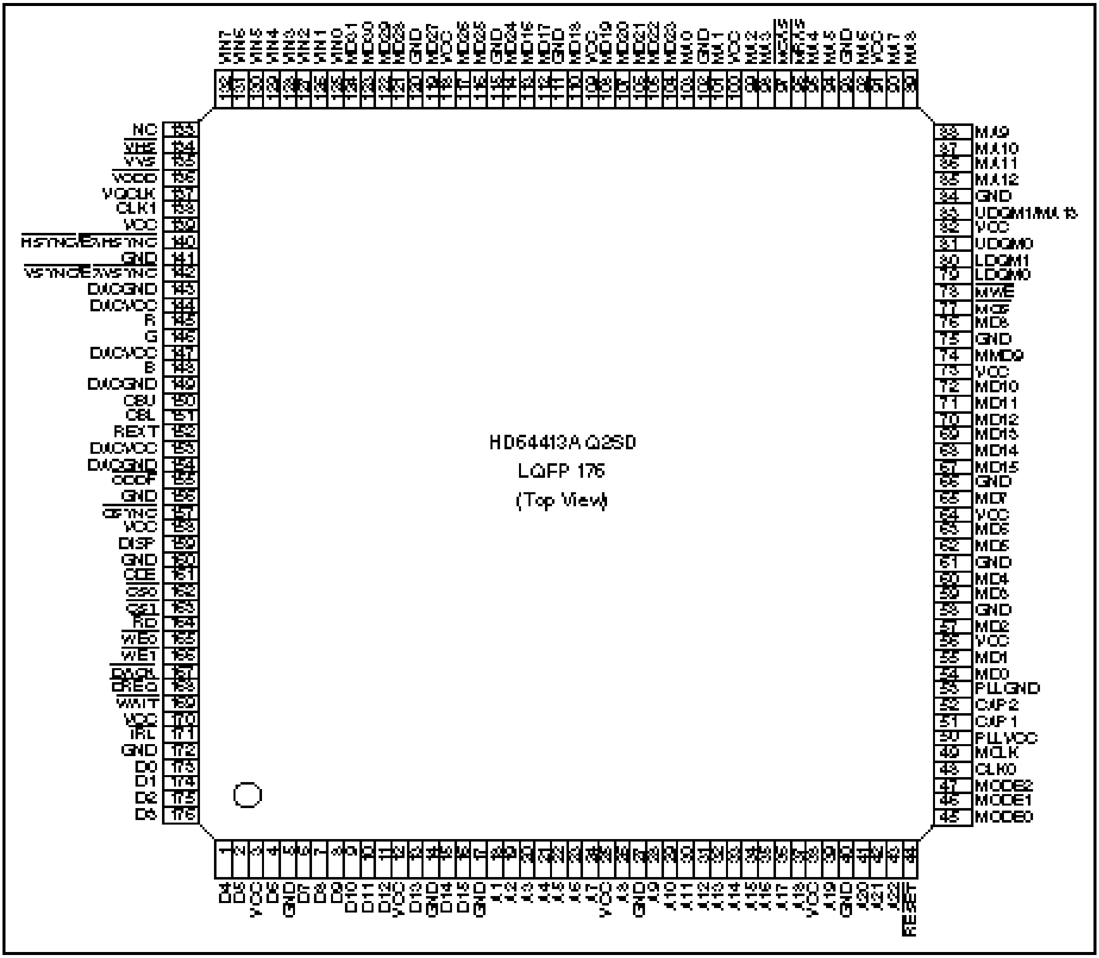


Figure 2.2 Pin Arrangement

2.1.3 Pin Functions

Table 2.1 summarizes the functions of the Q2SD's pins.

Table 2.1 Pin Functions

Type	Symbol	Pin No.	I/O	Function
System control	MODE0	45	Input	Operating mode pin 0
	MODE1	46	Input	Operating mode pin 1
	MODE2	47	Input	Operating mode pin 2
	CLK0	48	Input	Q2SD operating clock
	CLK1	138	Input	Display dot clock
	RESET	44	Input	Reset
	CAP1	51	Output	Multiplication circuit external capacitance pin
	CAP2	52	Output	Multiplication circuit external capacitance pin
CPU interface	A1	18	Input	CPU address 1
	A2	19	Input	CPU address 2
	A3	20	Input	CPU address 3
	A4	21	Input	CPU address 4
	A5	22	Input	CPU address 5
	A6	23	Input	CPU address 6
	A7	24	Input	CPU address 7
	A8	26	Input	CPU address 8
	A9	28	Input	CPU address 9
	A10	29	Input	CPU address 10
	A11	30	Input	CPU address 11
	A12	31	Input	CPU address 12
	A13	32	Input	CPU address 13
	A14	33	Input	CPU address 14
	A15	34	Input	CPU address 15
	A16	35	Input	CPU address 16
	A17	36	Input	CPU address 17
	A18	37	Input	CPU address 18
	A19	39	Input	CPU address 19
	A20	41	Input	CPU address 20

Table 2.1 Pin Functions (cont)

Type	Symbol	Pin No.	I/O	Function
CPU interface	A21	42	Input	CPU address 21
	A22	43	Input	CPU address 22
	D0	173	I/O	CPU data 0
	D1	174	I/O	CPU data 1
	D2	175	I/O	CPU data 2
	D3	176	I/O	CPU data 3
	D4	1	I/O	CPU data 4
	D5	2	I/O	CPU data 5
	D6	4	I/O	CPU data 6
	D7	6	I/O	CPU data 7
	D8	7	I/O	CPU data 8
	D9	8	I/O	CPU data 9
	D10	9	I/O	CPU data 10
	D11	10	I/O	CPU data 11
	D12	11	I/O	CPU data 12
	D13	13	I/O	CPU data 13
	D14	15	I/O	CPU data 14
	D15	16	I/O	CPU data 15
	$\overline{CS0}$	162	Input	Chip select 0 (UGM)
	$\overline{CS1}$	163	Input	Chip select 1 (internal registers)
	$\overline{RD}$	164	Input	Read strobe
	$\overline{WE0}$	165	Input	Write pulse 0 (lower)
	$\overline{WE1}$	166	Input	Write pulse 1 (upper)
	$\overline{DACK}$	167	Input	DMA acknowledge
	$\overline{DREQ}$	168	Output	DMA request
	$\overline{WAIT}$	169	Output	CPU wait
	$\overline{IRL}$	171	Output	Interrupt request
Display interface	CBU	150	Output	DAC external capacitance pin
	CBL	151	Output	DAC external capacitance pin
	REXT	152	Output	DAC external reference pin
	R	145	Output	Display data output R

Table 2.1 Pin Functions (cont)

Type	Symbol	Pin No.	I/O	Function
Display interface	G	146	Output	Display data output G
	B	148	Output	Display data output B
	$\overline{CSYNC}$	157	Output	Composite sync output signal
	$\overline{HSYNC}$/ $\overline{EXHSYNC}$	140	I/O	Horizontal sync output/external horizontal sync input
	$\overline{VSYNC}$/ $\overline{EXVSYNC}$	142	I/O	Vertical sync output/external vertical sync input
	DISP	159	Output	Signal indicating display interval (high during display interval)
	CDE	161	Output	Color detection (high in case of specific color output)
	$\overline{ODDF}$	155	I/O	Signal indicating odd field (low when odd)
Video interface	VIN0	125	Input	Video input data 0
	VIN1	126	Input	Video input data 1
	VIN2	127	Input	Video input data 2
	VIN3	128	Input	Video input data 3
	VIN4	129	Input	Video input data 4
	VIN5	130	Input	Video input data 5
	VIN6	131	Input	Video input data 6
	VIN7	132	Input	Video input data 7
	$\overline{VHS}$	134	Input	Video horizontal sync input
	$\overline{VVS}$	135	Input	Video vertical sync input
	$\overline{VODD}$	136	Input	Signal indicating video input odd field
	VQCLK	137	Input	Video input valid data incorporation clock
UGM interface	MA0	103	Output	Memory address 0
	MA1	101	Output	Memory address 1
	MA2	99	Output	Memory address 2
	MA3	98	Output	Memory address 3
	MA4	95	Output	Memory address 4
	MA5	94	Output	Memory address 5
	MA6	92	Output	Memory address 6
	MA7	90	Output	Memory address 7

Table 2.1 Pin Functions (cont)

Type	Symbol	Pin No.	I/O	Function
UGM interface	MA8	89	Output	Memory address 8
	MA9	88	Output	Memory address 9
	MA10	87	Output	Memory address 10
	MA11	86	Output	Memory address 11
	MA12	85	Output	Memory address 12
	MA13	83	Output	Memory address 13 (also functions as UDQM1)
	MD0	54	I/O	Memory data 0
	MD1	55	I/O	Memory data 1
	MD2	57	I/O	Memory data 2
	MD3	59	I/O	Memory data 3
	MD4	60	I/O	Memory data 4
	MD5	62	I/O	Memory data 5
	MD6	63	I/O	Memory data 6
	MD7	65	I/O	Memory data 7
	MD8	76	I/O	Memory data 8
	MD9	74	I/O	Memory data 9
	MD10	72	I/O	Memory data 10
	MD11	71	I/O	Memory data 11
	MD12	70	I/O	Memory data 12
	MD13	69	I/O	Memory data 13
	MD14	68	I/O	Memory data 14
	MD15	67	I/O	Memory data 15
	MD16	113	I/O	Memory data 16
	MD17	112	I/O	Memory data 17
	MD18	110	I/O	Memory data 18
	MD19	108	I/O	Memory data 19
	MD20	107	I/O	Memory data 20
	MD21	106	I/O	Memory data 21
	MD22	105	I/O	Memory data 22
	MD23	104	I/O	Memory data 23
	MD24	114	I/O	Memory data 24

Table 2.1 Pin Functions (cont)

Type	Symbol	Pin No.	I/O	Function
UGM interface	MD25	116	I/O	Memory data 25
	MD26	117	I/O	Memory data 26
	MD27	119	I/O	Memory data 27
	MD28	121	I/O	Memory data 28
	MD29	122	I/O	Memory data 29
	MD30	123	I/O	Memory data 30
	MD31	124	I/O	Memory data 31
	$\overline{MCS}$	77	Output	Memory chip select
	$\overline{MWE}$	78	Output	Memory write pulse
	$\overline{MRAS}$	96	Output	Row select signal
	$\overline{MCAS}$	97	Output	Column select signal
	LDQM0	79	Output	Lower word, lower byte I/O mask
	LDQM1	80	Output	Lower word, upper byte I/O mask
	UDQM0	81	Output	Upper word, lower byte I/O mask
	UDQM1	83	Output	Upper word, upper byte I/O mask (also functions as MA13)
	MCLK	49	Output	Memory clock
Power supply	VCC	3	Power supply	Buffer/internal VDD
	VCC	12	Power supply	Buffer/internal VDD
	VCC	25	Power supply	Buffer/internal VDD
	VCC	38	Power supply	Buffer/internal VDD
	VCC	56	Power supply	Buffer/internal VDD
	VCC	64	Power supply	Buffer/internal VDD
	VCC	73	Power supply	Buffer/internal VDD
	VCC	82	Power supply	Buffer/internal VDD
	VCC	91	Power supply	Buffer/internal VDD
	VCC	100	Power supply	Buffer/internal VDD
	VCC	109	Power supply	Buffer/internal VDD
	VCC	118	Power supply	Buffer/internal VDD
	VCC	139	Power supply	Buffer/internal VDD
	VCC	158	Power supply	Buffer/internal VDD
	VCC	170	Power supply	Buffer/internal VDD

Table 2.1 Pin Functions (cont)

Type	Symbol	Pin No.	I/O	Function
Power supply	GND	5	Ground	Buffer VSS
	GND	14	Ground	Buffer VSS
	GND	27	Ground	Buffer VSS
	GND	40	Ground	Buffer VSS
	GND	58	Ground	Buffer VSS
	GND	66	Ground	Buffer VSS
	GND	75	Ground	Buffer VSS
	GND	84	Ground	Buffer VSS
	GND	93	Ground	Buffer VSS
	GND	102	Ground	Buffer VSS
	GND	111	Ground	Buffer VSS
	GND	120	Ground	Buffer VSS
	GND	141	Ground	Buffer VSS
	GND	160	Ground	Buffer VSS
	GND	172	Ground	Buffer VSS
	GND	17	Ground	Internal VSS
	GND	61	Ground	Internal VSS
	GND	115	Ground	Internal VSS
	GND	156	Ground	Internal VSS
	PLL VCC	50	Power supply	Multiplication circuit VDD
	PLL GND	53	Ground	Multiplication circuit VSS
	DAC VCC	144	Power supply	DAC VDD
	DAC VCC	147	Power supply	DAC VDD
	DAC VCC	153	Power supply	DAC VDD
	DAC GND	143	Ground	DAC VSS
	DAC GND	149	Ground	DAC VSS
	DAC GND	154	Ground	DAC VSS
	NC	133		No-connection (leave open)

2.2 System Interface Pins

2.2.1 Operating Mode Pins

These pins determine the Q2SD's operating mode. The mode is fixed in a reset-startup.

1. MODE2 = L, MODE1 = L, MODE0 = L
   Normal operation state. Multiplication on. The external input clock is duty-free.
   The internal operating clock has the same frequency as the external input clock.

2. MODE2 = L, MODE1 = L, MODE0 = H
   Normal operation state. Multiplication on. The external input clock is duty-free.
   The internal operating clock has twice the frequency of the external input clock.

3. MODE2 = L, MODE1 = H, MODE0 = L
   Normal operation state. Multiplication on. The external input clock is duty-free.
   The internal operating clock has four times the frequency of the external input clock.

4. MODE2 = L, MODE1 = H, MODE0 = H: Setting prohibited

5. MODE2 = H, MODE1 = *, MODE0 = *: Setting prohibited

Notes: H: High level
L: Low level
*: Either high or low level

2.2.2 Clock Pins

The operating clock is input to CLK0, and the display clock to CLK1.

CAP1 and CAP2 are external capacitance pins for the multiplication circuit. Figure 2.3 shows a sample circuit.

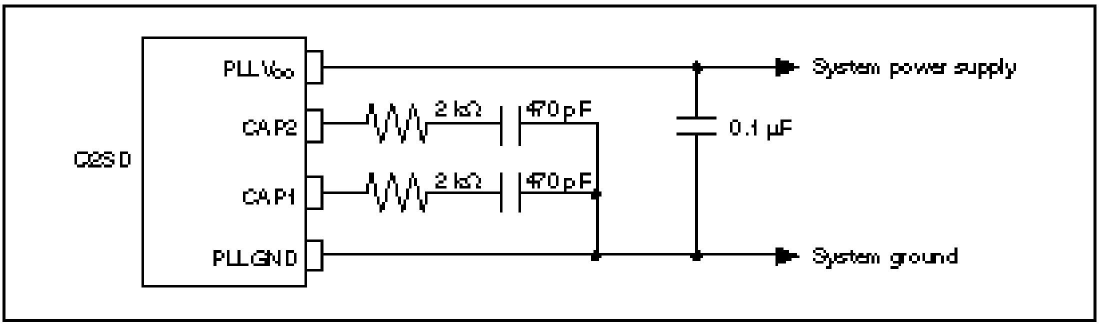


Figure 2.3 Example of Circuit for Connection to CAP1 and CAP2 Pins

2.2.3 Reset Pin

A hardware reset signal is input to this pin.

2.2.4 D/A Converter

The D/A converter converts display data to linear format.

Connect the specified resistances or capacitances to REXT, CBU, and CBL.

Connect resistive load RL to the R, G, and B output pins. If the current flowing in resistive load RL is designated Iout, then Vout = Iout × RL.

The following relationship also applies: REXT = 2.842/Iout × DACVcc.

Therefore, to obtain Vout = IVpp when RL = 330 Ω and DACVcc = 3.3 V, REXT = 3.1 kΩ.

The maximum output current is 3.0 mA.

The D/A converter has 8-bit resolution, but the dynamic settling error is determined by resistive load RL, output pin load C, and CLK1 frequency f.

For example, when RL = 330 Ω, C = 20 pF, and f = 33 MHz, the value of n when the following equation is satisfied is the D/A converter precision.

$$\exp\left(\frac{-1}{RL \cdot C \cdot f}\right) \leq \frac{1}{2^n} \qquad \text{(Where n is an integer)}$$

Since n is 6 in this case, the D/A converter has 6-bit precision. (The dynamic settling error is $1/2^6$ = 1.56% full-scale.)

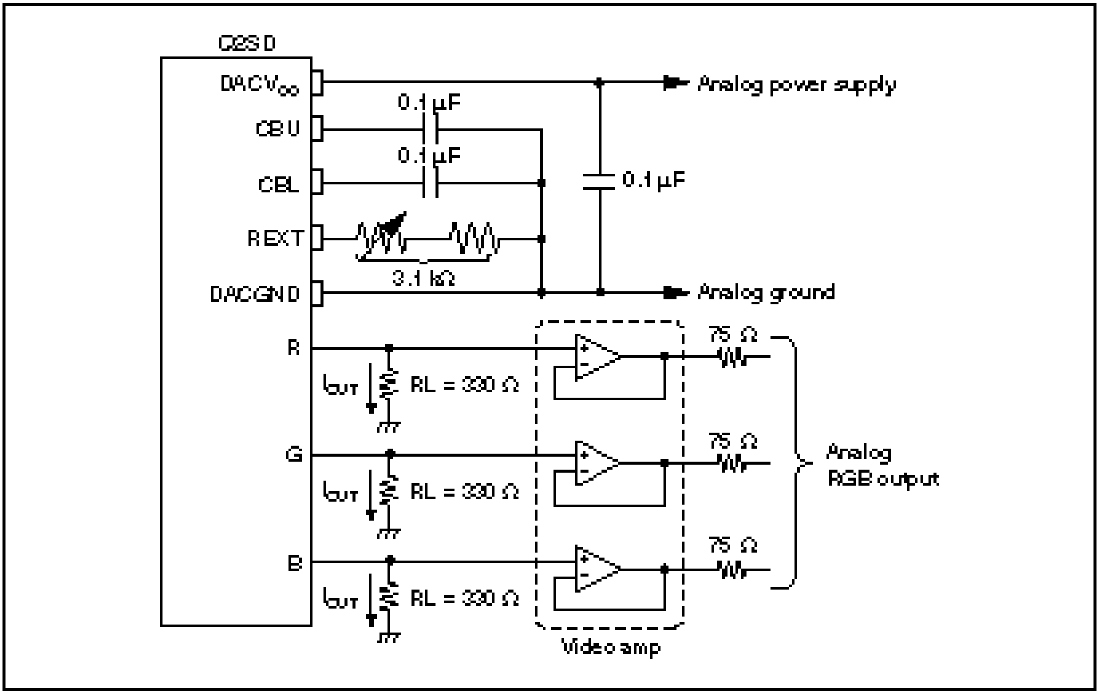


Figure 2.4 Example of Circuit for Connection to REXT, CBU, and CBL Pins

2.3 CPU Interface Pins

2.3.1 CPU Writes

The CPU can access the UGM or a Q2SD internal register. In a UGM access, a low-level signal is input to $\overline{CS0}$; in a Q2SD internal register access, a low-level signal is input to $\overline{CS1}$. $\overline{CS0}$ and $\overline{CS1}$ must not be driven low at the same time. The UGM or Q2SD internal register address is input to A22 to A1. The address is a byte address. Only word (2-byte) access can be used in the Q2SD for registers, while word access or byte access can be used for the UGM. In word access, input a low-level signal to both $\overline{WE0}$ and $\overline{WE1}$; in byte access, drive $\overline{WE0}$ low for an access to bits 7 to 0, or drive $\overline{WE1}$ low for an access to bits 15 to 8.

The Q2SD uses the $\overline{WAIT}$ signal to notify the CPU of a delay in CPU access due to an internal Q2SD operation. However, because of the high-level width specification for the $\overline{WE0}$ and $\overline{WE1}$ signals, the CPU external bus operating frequency should be set equal to or lower than the Q2SD's internal operating frequency. Following detection of a low level of $\overline{CS0}$ or $\overline{CS1}$ and a low level of $\overline{RD}$, $\overline{WE0}$, or $\overline{WE1}$, there is a maximum interval of 3 cycles, followed by an output buffer delay (max. 15 ns), before the Q2SD's $\overline{WAIT}$ signal is asserted. The number of software waits should be adjusted by software according to the frequency ratio between the CPU and Q2SD, and system specifications such as synchronous or asynchronous operation.

In some SuperH RISC engine family products, the $\overline{\text{CS}}$ pin is initially set as an input port. If this signal is connected directly to the $\overline{\text{CS0}}$ or $\overline{\text{CS1}}$ signal of the Q2SD, pull up the SuperH's $\overline{\text{CS}}$ pin externally to prevent the voltage level from becoming unstable in a reset.

When using a CPU that uses an $\overline{\text{RDY}}$ signal for interfacing, invert the Q2SD's $\overline{\text{WAIT}}$ signal and use it as the $\overline{\text{RDY}}$ signal.

The $\overline{\text{WAIT}}$ signal is output for a minimum of 1 tcyc0 when accessing the Q2SD.

2.3.2 CPU Reads

A read operation is basically the same as a write operation. Reads are performed in word units.

2.3.3 DMA Writes

The CPU can perform write DMA access, using cycle stealing, to the UGM or a Q2SD address-mapped register (the image data entry register (IDE)). To perform DMA access, DMA transfer start address, DMA transfer word count, and system control register DMA mode and DMA address mode settings must be made. After the DMA mode settings are made, the Q2SD dives the $\overline{\text{DREQ}}$ signal low as soon as its preparations are completed. When the DMA controller receives this signal, it drives the $\overline{\text{DACK}}$ signal low and begins DMA access. DMA access is performed in word units.

Use a DMA mode setting of 01 when performing DMA writes with a YUV mode (YUV2, YUV1, YUV0) setting of 000, and a DMA mode setting of 11 when performing DMA writes with a YUV mode setting other than 000. Other address-mapped registers cannot be accessed. The destination address (UGM address) is set as the DMA transfer start address (DMSARH, DMSARL), and the number of words set as the DMA transfer word count (DMAWRH, DMAWRL) are transferred.

When DMA address mode bits DAA1 and DAA0 in the system control register (SYSR) are is set to 00 or 01, transfer is performed using single address transfer timing.

When the DMA address mode (DAA1, DAA0) is set to 10, transfer is performed using dual address transfer timing. In this case, access to the Q2SD should be performed by driving $\overline{\text{DACK}}$ low. $\overline{\text{CS0}}$ is ignored. The DMA mode is set to 01 for UGM access, and to 11 for Q2SD address-mapped register (image data entry register (IDE)) access. Other address-mapped registers cannot be accessed. The destination address (UGM address) is set as the DMA transfer start address (DMSARH, DMSARL), and the number of words set as the DMA transfer word count (DMAWRH, DMAWRL) are transferred. Addresses input from off-chip are not used.

When making another DMA mode setting after DMA transfer ends, first check that the DMF bit is set to 1 in the status register.

In DMA transfer from synchronous DRAM to the Q2SD, the D15–D0 setup time (t_{WRDRS}) relative to the rise of the $\overline{RD}$ signal must be at least two Q2SD system operating clock cycles, and therefore the external bus operating frequency must be no higher than 1/2 the system operating clock frequency.

When using the DMAC, make the following DMAC settings.

· For DMA transfer in dual address mode
  ¾ $\overline{DACK}$ output in write cycle
  ¾ Active-low $\overline{DACK}$ output
  ¾ Fixed destination address (set any UGM address)
  ¾ Source address incremented
  ¾ External request, dual address mode
  ¾ $\overline{DREQ}$ falling-edge detection
  ¾ Cycle stealing
· For DMA transfer in single address mode
  ¾ $\overline{DACK}$ output in read cycle
  ¾ Active-low $\overline{DACK}$ output
  ¾ Fixed destination address
  ¾ Source address incremented
  ¾ External request, single address mode
  ¾ $\overline{DREQ}$ falling-edge detection
  ¾ Cycle stealing

The SuperH family includes models in which the initial DACK pin setting is active-high. In this case, leave the DACK pin at its initial setting (active-high) and use an external circuit to invert the DACK pin signal before connection to the Q2SD's $\overline{DACK}$ pin.

2.3.4 Interrupts

The Q2SD interrupts the CPU by means of internal sources. Interrupt sources are set in the interrupt enable register (IER).

2.4 Power Supply Pins

2.4.1 Normal Power Supply, DAC Power Supply, and PLL Power Supply

The normal power supply, DAC power supply, and PLL power supply are connected to 3.3 V.

2.5 Display Interface Pins

The signals output from the display interface pins are all synchronized with the display operating clock.

2.5.1 Display Signal Output

RGB analog display signals are output synchronized with the internal dot clock. The pixel data resolution is 6 bits for each of R, G, and B. Outside the display period, the image data (R, G, B) goes to the level corresponding to 0.

2.5.2 Video Encoder Interface

Outputs the composite sync signal ($\overline{\text{CSYNC}}$). In master mode, equalizing pulses can also be added to the composite sync signal.

2.5.3 CRT Interface

Outputs the horizontal sync signal and vertical sync signal, the DISP signal indicating the display interval, the CDE signal for color detection, and the $\overline{\text{ODDF}}$ signal that indicates whether the current field is even or odd for interlace control. When synchronization is coordinated with an external device (TV or video recorder), the horizontal sync, vertical sync, and $\overline{\text{ODDF}}$ signals are input. In a reset, the $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, and $\overline{\text{ODDF}}$ pins go to input mode, and therefore these pins must be fixed in a non-significant direction (pulled up).

2.6 UGM Interface Pins

2.6.1 UGM Access

The Q2SD allows synchronous DRAM to be used as the UGM, and has a direct interface for synchronous DRAM.

When connecting only one synchronous DRAM with a data bit width of 16, use pins MD0 to MD15, and leave pins MD16 to MD31 open.

The operating mode of the synchronous DRAM (write mode, $\overline{\text{CAS}}$ latency, burst type, and burst length) is set automatically by the Q2SD.

For refreshing, auto-refresh mode is used. The synchronous DRAM's CKE pin should be fixed high.

Synchronous DRAM precharging is carried out using the Precharge All Banks (PALL) command.

2.7 States

2.7.1 State Transitions

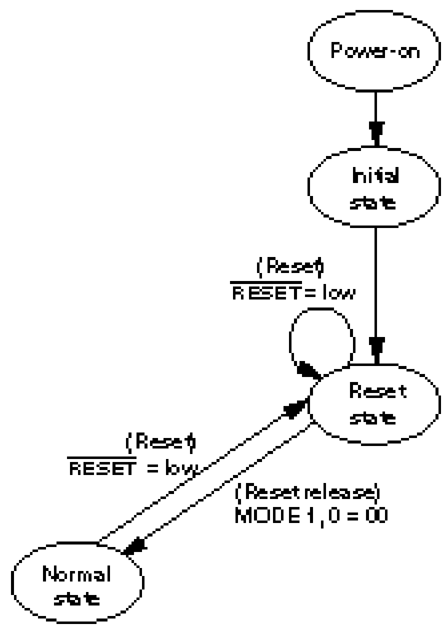


Figure 2.5 State Transition Diagram

2.7.2 Initial States (when Specified Power is Supplied)

Initial states are undefined.

Registers: Undefined
I/O pins: Undefined
Output pins: Low/high-level output

2.7.3 Reset State (when Low Level is Input at $\overline{\text{RESET}}$ Pin)

Pins: Table 2.2 shows the Q2SD pin states after a reset.

Table 2.2 Pin States After Reset

I/O Pins	Input state	D0–D15*, $\overline{\text{VSYNC}}$/$\overline{\text{EXVSYNC}}$, $\overline{\text{HSYNC}}$/$\overline{\text{EXHSYNC}}$, $\overline{\text{ODDF}}$
	Output state (low-level output)	MD0–MD31
Output Pins	Low-level output	DISP, CDE, R, G, B
	High-level output	$\overline{\text{DREQ}}$, $\overline{\text{IRL}}$, $\overline{\text{WAIT}}$
	Low/high-level output	$\overline{\text{CSYNC}}$, MA0–MA13, $\overline{\text{MWE}}$, $\overline{\text{MRAS}}$, $\overline{\text{MCAS}}$, LDQM0, LDQM1, UDQM0, UDQM1, MCLK

Note: * However, pins D0–D15 go to the output state when $\overline{\text{RD}}$ is a low-level input.

UGM Refreshing: UGM refreshing is not performed when the $\overline{\text{RESET}}$ pin is low.

2.7.4 Normal Operating State

In the normal operating state, the Q2SD executes drawing commands and performs display control.

Section 3 Unified Graphics Memory (UGM) and Display Functions

3.1 Clocks

There are two Q2SD clocks, CLK0 and CLK1. The clock used as the base for the system operating clock is input at the CLK0 pin, and the clock used as the display operating clock is input at the CLK1 pin.

The system operating clock is the base clock for performing drawing operations, and is also used as the base clock for UGM access. The Q2SD includes an operating clock multiplication circuit that enables a ×1, ×1/2, or ×1/4 multiple of the operating clock to be selected for input at the CLK0 pin.

The display operating clock is the base clock for display operations, and is used to control display data output and generate horizontal and vertical sync signals.

The relationship between the clocks and operating frequencies is summarized in table 3.1.

Table 3.1 Input Clocks and Operating Frequencies

Clock Input Pin	Clock Type	Operating Mode
CLK0	One of the clocks on the right is the system operating clock.	Clock with the CLK0 frequency, and duty adjusted to 50%
		Clock with twice the CLK0 frequency, and duty adjusted to 50%
		Clock with four times the CLK0 frequency, and duty adjusted to 50%
CLK1	The clock on the right is the display operating clock.	Clock with the CLK1 frequency

The system operating clock and display operating clock frequencies can be set to any values within the following range:

System operating clock ≥ 2 × display operating clock
(where display operating clock ≤ 33 MHz)

Drawing operations can therefore be performed at maximum speed without being influenced by the characteristics of the display device. When a SuperH that operates on synchronous input is used as the CPU, input a clock synchronized with the CPU's operating clock to the CLK0 pin to perform synchronous interfacing between the CPU and the Q2SD.

3.2 UGM (Unified Graphics Memory)

3.2.1 Overview

The memory connected to the Q2SD (graphics memory) is used for the following purposes.

1. Frame buffers, background screen

   Q2SD drawing area and display area.

2. Display list (command list)

   Area that stores the Q2SD drawing command list. The Q2SD fetches commands from this area while carrying out drawing operations.

3. Source areas, work areas, etc.

   Used as the source area that stores painting patterns and font data, the FTRAP command drawing area, and so on.

4. Video area

   Stores data taken from the video input data.

The UGM can be allocated to part of the CPU's main memory area, enabling it to be used as CPU work areas as well as for the above purposes. Figure 3.1 shows a sample system configuration using the UGM, and figure 3.2 shows an example of UGM mapping onto the CPU memory space.

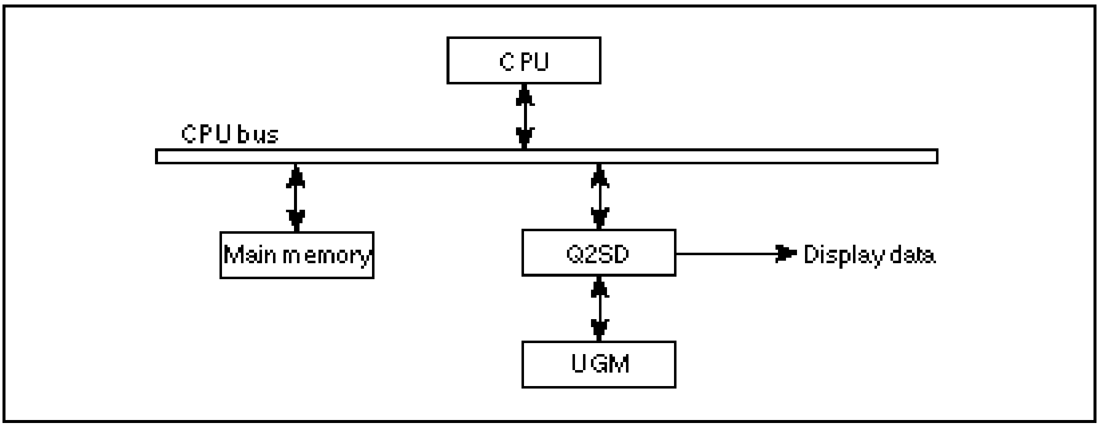


Figure 3.1 Example of System Configuration Using UGM

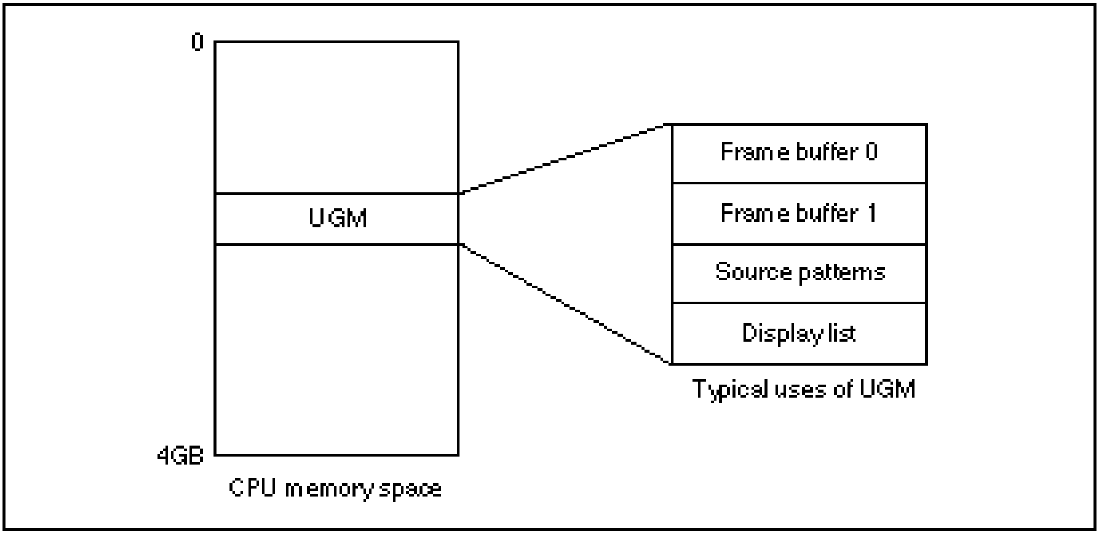


Figure 3.2 Example of UGM Mapping onto CPU Memory Space

3.2.2 Memory Access

The priority order for control of UGM access is as follows:

1. Refreshing
2. Display
3. Video incorporation
4. CPU
5. Other (command fetches, drawing, source referencing, etc.)

To enable these different kinds of processing to be performed in parallel, after performing access for a fixed period, the Q2SD passes the access right to another source. So if three sources are requesting access, for example, they will perform accesses alternately.

UGM Access by the CPU: The CPU can access the UGM in two ways, via CPU software or via DMA transfer by the DMAC. When the CPU accesses the UGM, the UGM address is input directly to Q2SD pins A1 to A22, and the $\overline{CS0}$ pin is driven low. A UGM address within the range specified by the memory mode register (MEMR) should therefore be input to Q2SD pins A1 to A22. When using a single 16-Mbit memory, for example, wire pins A21 and A22 so that they go low.

If a SuperH is used as the CPU, the UGM should be mapped onto “SuperH normal space.” Data transfer between the CPU and Q2SD is synchronized with the Q2SD’s system operating clock.

- Access by software

  In access by software, the UGM is accessed as part of the main memory.

  In a write operation, access is possible with a minimum number of wait cycles if there is empty space in the Q2SD's built-in 32-byte FIFO buffer.

  In a read operation, a number of wait cycles are inserted. The number of wait cycles varies greatly depending on the relationship between the system operating clock and the display operating clock, and the screen size.

- Access by DMA

  With a CPU that has a built-in DMAC, data in the memory connected to the CPU can be transferred to the UGM using the DMAC. DMA transfer can be used to transfer display list or YUV data.

  Single address mode or dual address mode can be used in DMA transfers, since graphics memory addresses are controlled by the Q2SD's built-in address counter. However, only cycle-steal mode can be used as the bus mode.

UGM Access by Q2SD: Synchronous DRAM can be connected directly to the Q2SD as the UGM. Use of this memory enables the Q2SD to perform memory access in one-cycle (operating clock) units.

Synchronous DRAMs that can be used for the UGM are those that have a power supply voltage of 3.3 V and meet the cycle specification of MCLK output by the Q2SD. The following memory configurations can be used:

- 64-Mbit capacity (1-Mbit × 16 × 4-bank configuration)
- 64-Mbit capacity (512-kbit × 32 × 4-bank configuration)
- 16-Mbit capacity (512-kbit × 16 × 2-bank configuration)

The type of memory is set in the memory mode register (MEMR).

3.2.3 Memory Map

The Q2SD performs UGM address control. The UGM includes the display list area, binary source area, work area, 8-bit/pixel source or 16-bit/pixel source area, 8-bit/pixel rendering or 16-bit/pixel rendering area, and video area. The UGM is configured in 512-byte units, and a different memory configuration is used for each area. The memory configuration for each of the areas is shown in figure 3.3.

Area settings are made according to the respective start addresses (see section 5.4, Memory Control Registers).

1. 1-bit/pixel (work, binary source, display list)

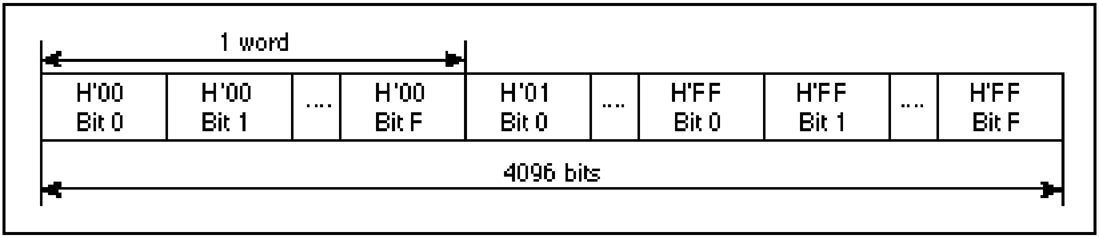


Figure 3.3 Configuration of One Memory Unit (512 Bytes) (1)

2. 8 bits/pixel (multi-valued source, multi-valued destination)

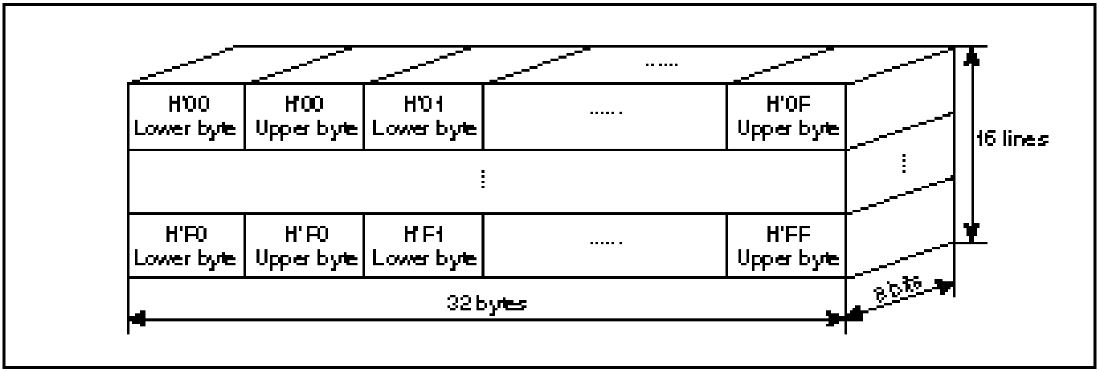
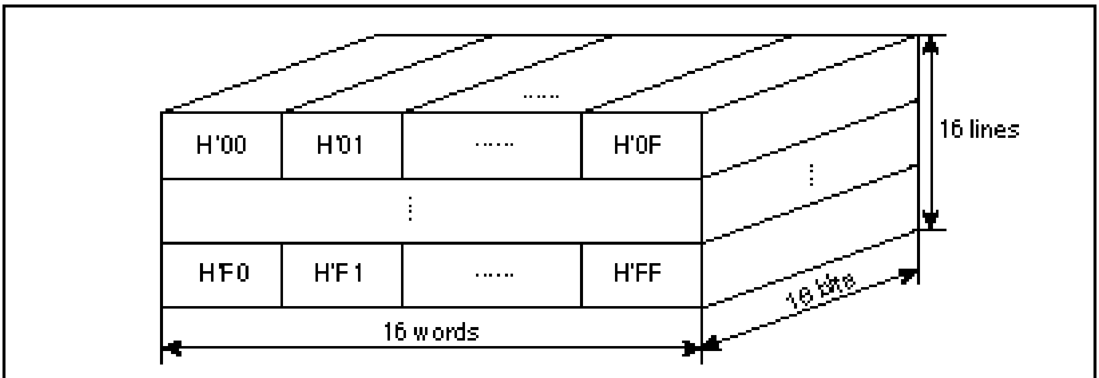


Figure 3.3 Configuration of One Memory Unit (512 Bytes) (2)

3. 16 bits/pixel (multi-valued source, multi-valued destination, video)



Note: In the video data arrangement, an 8-bit Y/8-bit Cr configuration alternates with an 8-bit Y/8-bit Cb configuration.

Figure 3.3 Configuration of One Memory Unit (512 Bytes) (3)

The UGM consists of addresses that are consecutive within one memory unit (linear addresses), as shown in figure 3.4 (a).

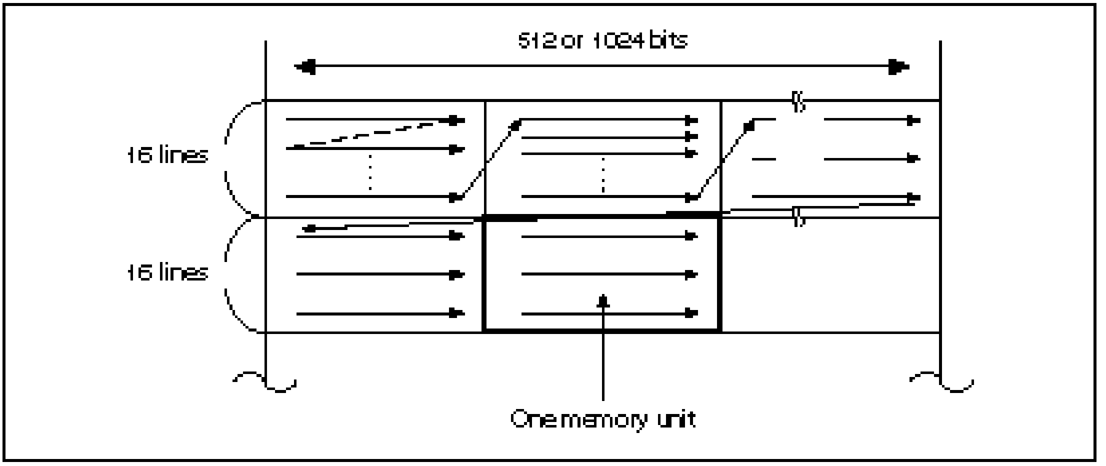


Figure 3.4 (a) UGM Address Transitions

Figure 3.4 (b) shows a memory map of the UGM. A combination of 8-bit/pixel and 16-bit/pixel areas can be used in the UGM, but area allocation must be carried out so that areas do not overlap. For this purpose, 8-bit/pixel and 16-bit/pixel areas should ideally be considered as shown in figure 3.4 (c) when performing area allocation. In terms of the number of Y-direction dots, there is a 2-to-1 relationship between the 8-bit/pixel and 16-bit/pixel memory maps.

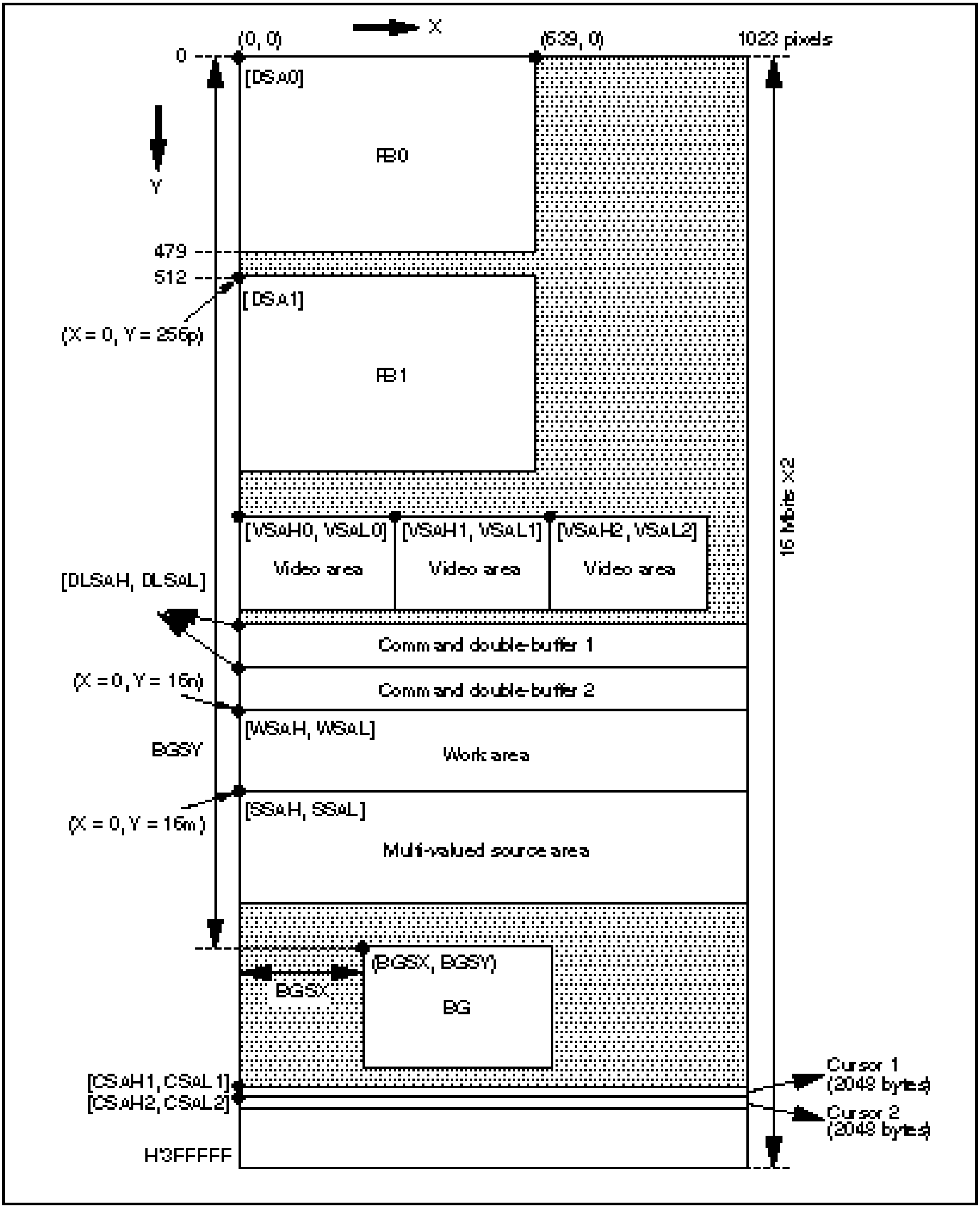


Figure 3.4 (b) Sample Memory Map
(Corresponding to 640 × 480 Screen Size, with 16 Bits/Pixel)

- [WSAH, WSAL]: Address corresponding to “positive multiple of 16 dots in Y-direction”
- [SSAH, SSAL]: Address corresponding to “X = 0 dots and positive multiple of 16 dots in Y-direction”
- [DSA0], [DSA1]: Address corresponding to “X = 0 dots and positive multiple of 256 dots in Y-direction”
- [DLSAH, DLSAL]: Arbitrary word (16-bit) address)
- [VSAHn, VSALn]: Address corresponding to “positive multiple of 32 dots in X-direction and positive multiple of 16 dots in Y-direction when UGM is viewed as 16 bits/pixel” (n = 0, 1, 2)

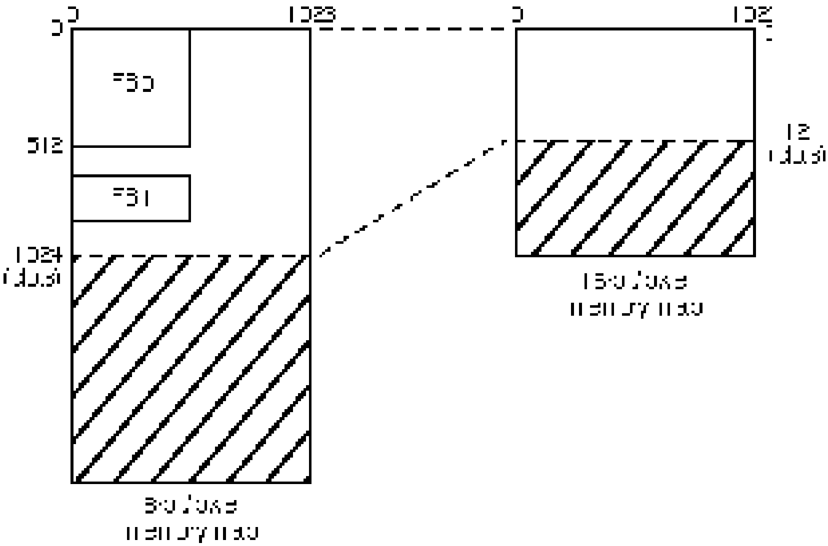


Figure 3.4 (c) Relationship between 8-Bit/Pixel and 16-Bit/Pixel Memory Maps

Figures 3.4 (d) and (e) show the correspondence between memory physical addresses (bytes) and the coordinates shown in the sample memory map in section 3.2, Memory Map. The X upper coordinate and X lower coordinate refer to the values when the X values in the sample memory map are divided into the respective bit widths. Similarly, the Y upper coordinate and Y lower coordinate are the values when the Y values are divided.

8 bits/pixel, MWX = 0 (512 pixels)

A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Y upper coordinate										X upper coordinate				Y lower coordinate				X lower coordinate				

8 bits/pixel, MWX = 1 (1024 pixels)

A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Y upper coordinate									X upper coordinate					Y lower coordinate				X lower coordinate				

16 bits/pixel, MWX = 0 (512 pixels)

A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Y upper coordinate									X upper coordinate					Y lower coordinate				X lower coordinate				0

16 bits/pixel, MWX = 1 (1024 pixels)

A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Y upper coordinate								X upper coordinate						Y lower coordinate				X lower coordinate				0

Upper line: Memory physical addresses (bytes) A22 to A1, A0
Lower line: Logical coordinates (X, Y)

Note: A0 is an LSI internal signal, indicating the least significant bit of the byte address. The least significant bit of the byte address is decoded and output at pins LDQM0 and LDQM1.

Figure 3.4 (d) Correspondence between Memory Physical Addresses (Bytes) and Rendering Coordinates and Multi-Valued Source Coordinates (16-Bit Bus)

8 bits/pixel, MWX = 0 (512 pixels)

A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Y upper coordinate										X upper coordinate				Y lower coordinate				X lower coordinate				

8 bits/pixel, MWX = 1 (1024 pixels)

A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Y upper coordinate									X upper coordinate					Y lower coordinate				X lower coordinate				

16 bits/pixel, MWX = 0 (512 pixels)

A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Y upper coordinate									X upper coordinate					Y lower coordinate				X lower coordinate				0

16 bits/pixel, MWX = 1 (1024 pixels)

A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Y upper coordinate								X upper coordinate						Y lower coordinate				X lower coordinate				0

Upper line: Memory physical addresses (bytes) A22 to A2, A1, A0
Lower line: Logical coordinates (X, Y)

Note: A0 is an LSI internal signal, indicating the least significant bit of the byte address. A1 is always output as 0 from the pin. It indicates the least significant bit of the word address. The least significant bits of the byte address and word address are decoded and output at pins LDQM0, LDQM1, UDQM0, and UDQM1.

Figure 3.4 (e) Correspondence between Memory Physical Addresses (Bytes) and Rendering Coordinates and Multi-Valued Source Coordinates (32-Bit Bus)

If a 1024-pixel memory width configuration is used when the horizontal screen size is 512 pixels or less (e.g. 320 × 240 equivalent), frame buffer F1 can be set from position X = 512 by setting the HDIS bit to 1 in display mode register 2. In this case, the same value is set in DSA0 and DSA1. When the HDIS bit is set to 1, use the following settings: GBM2 = 0, GBM1 = 0, RSAE = 0.

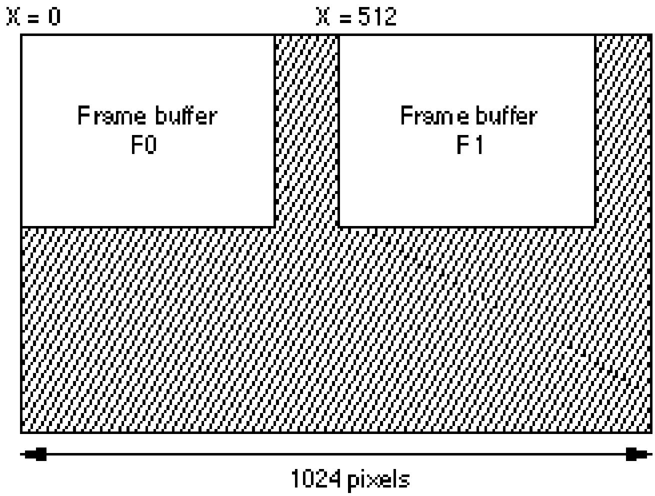


Figure 3.5 Example of Frame Buffer F1 Location from X = 512

3.3 Display and Display Control

3.3.1 Overview

The Q2SD has two screens, a drawing screen and a display screen, managed by means of rendering coordinates. Display is performed for both these screens in accordance with double-buffering control designated by the user.

The Q2SD also has display functions for controlling the display timing, allowing coordination with the display timing of the display device to which data is output from the Q2SD.

When 16-bit/pixel mode is set with the GBM bit in the Q2SD's rendering mode register (REMR), a function can be used that converts YUV or ΔYUV data color images to RGB data. When 8-bit/pixel mode is set, the color palette can be used, enabling 256 colors to be specified out of a total of 262,144.

3.3.2 Double-Buffering Control

The Q2SD uses double-buffering control to alternately switch the display and drawing areas located in the UGM. An area switching operation is called a frame change. There are three modes for double-buffering control: auto display change mode, auto rendering mode, and manual display change mode. In auto display change mode, a frame change is performed each time the Q2SD detects the frame change timing. In auto rendering mode, a frame change is performed once only when the Q2SD detects the frame change timing after drawing is completed. In manual display change mode, the Q2SD performs a frame change once only at the frame change timing following issuance by the CPU of a frame change directive to the Q2SD. These modes are specified by the double-buffering mode bits (DBM) in the system control register. The start of drawing is specified by the RS bit.

When double-buffering control is performed, frame changes are performed in frame units when the Q2SD is operating in non-interlace or interlace mode, and in field units when operating in interlace sync & video mode.

When the Q2SD is operated in interlace mode, the frame flag (FRM) in the status register is used for $\overline{\text{VSYNC}}$ synchronization pulse detection by the CPU. When the Q2SD is operated in non-interlace mode, synchronization pulses are detected using the vertical blanking flag (VBK). When the Q2SD is operating in interlace sync & video mode, since the first frame corresponds to the even field and the second frame to the odd field, synchronization pulses are detected using VBK or FRM.

The same results can also be achieved by using the VBKEM command. See the description of the VBKEM command for details.

Examples are given below for Q2SD non-interlace operation, with a description of the operation in each mode.

Auto Display Change Mode: In auto display change mode, display frame changes have priority. If drawing is in progress when the frame is changed, drawing is aborted midway through that display list . It is therefore essential for drawing to be finished before the arrival of a $\overline{\text{VSYNC}}$ synchronization pulse.

An outline of operation in this mode is shown in figure 3.6. Drawing cannot be started with the VBKEM command in this mode, so the VBK or FRM flag must be used.

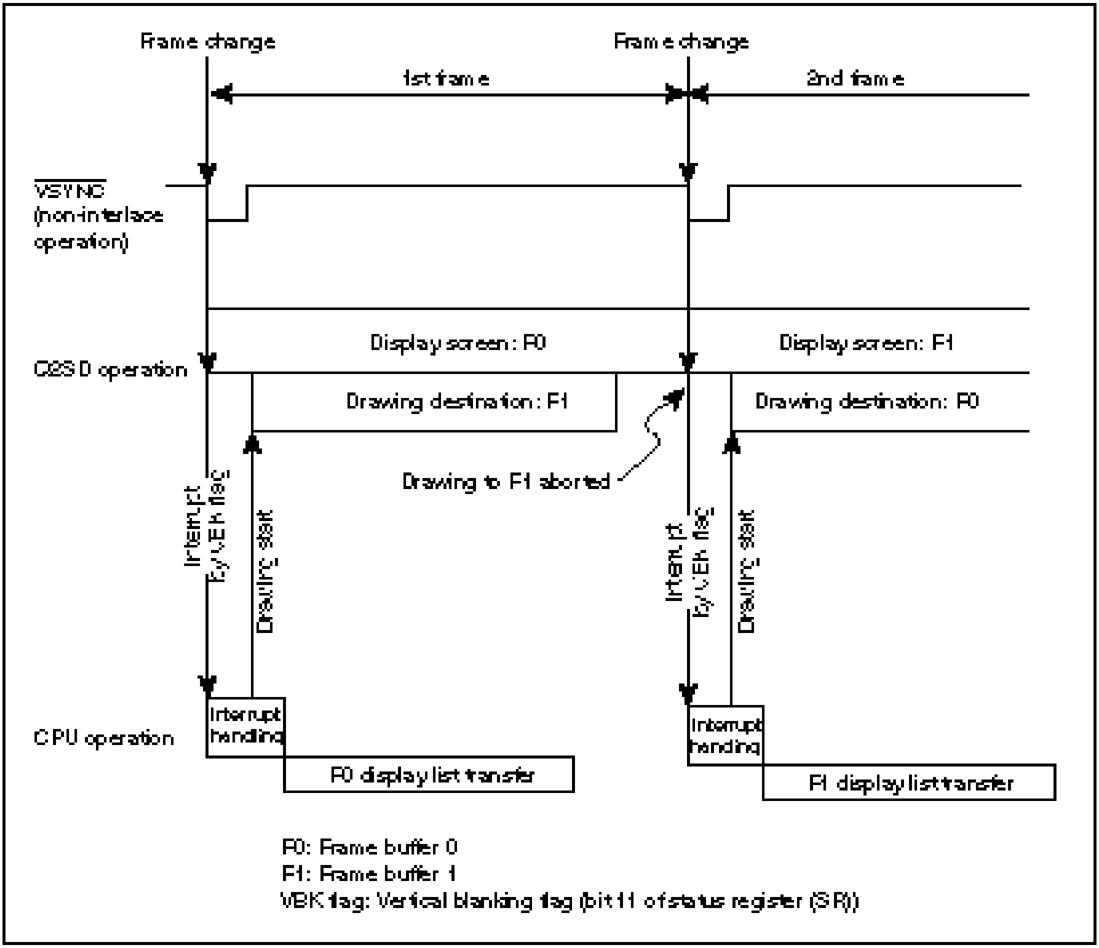


Figure 3.6 Operation in Auto Display Change Mode

Auto Rendering Mode: In auto rendering mode, display switching is not performed until execution of a TRAP command is completed. If drawing does not end within one frame, it is continued without interruption. An outline of operation in this mode is shown in figure 3.7.

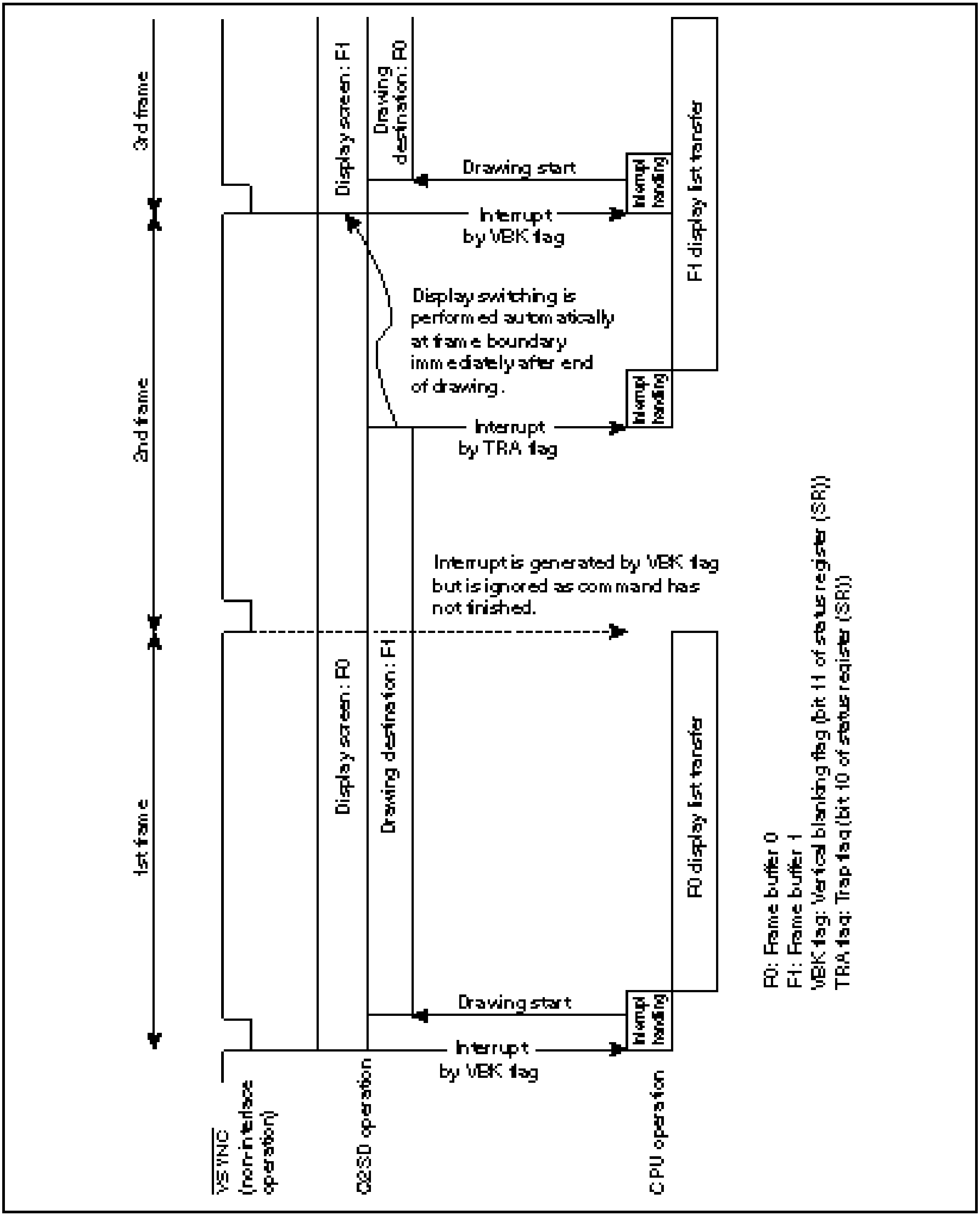


Figure 3.7 Operation in Auto Rendering Mode

Manual Display Change Mode: In manual display change mode, display frame changes and the start of drawing are controlled independently by software. Frame changes can be performed by software by switching between F0 and F1 according to the setting of the DC bit in SYSR, or by using the WPR command to set the F0 or F1 start address in the display start address register indicated by DBF in the status register. The start of drawing is controlled by the RS bit in the system control register. Interrupts by means of the VBKEM command or the TRA flag are used for the control timing. An outline of operation in this mode when using the DC bit is shown in figure 3.8 (a). When changing from this mode to another double-buffering control mode, first check that the DC bit has been set to 1 and has then returned to 0. If this is not done, a frame change will occur at a timing coordinated with VSYNC during display processing.

Confirm that the DC bit is cleared to 0 before setting it to 1.

Control by Means of VBKEM and WPR Commands: The VBKEM command holds fetching and execution of the display list waiting following this command. With the VBKEM command , the waiting state is cleared at the next VSYNC in non-interlace mode display or interlace sync & video mode display, and at the start of the next frame in interlace sync mode display. Use of this command allows drawing processing to be started without using a VBK or FRM interrupt. Control is carried out by a combination of the WPR command, which performs drawing-related register setting, and the VBKEM command, which ends in synchronization with VBK, as shown in figure 3.8 (b). The CPU only has to monitor drawing end interrupts; monitoring of VBK interrupts is no longer necessary.

This kind of double-buffering control can be used only in auto-rendering mode and manual display change mode.

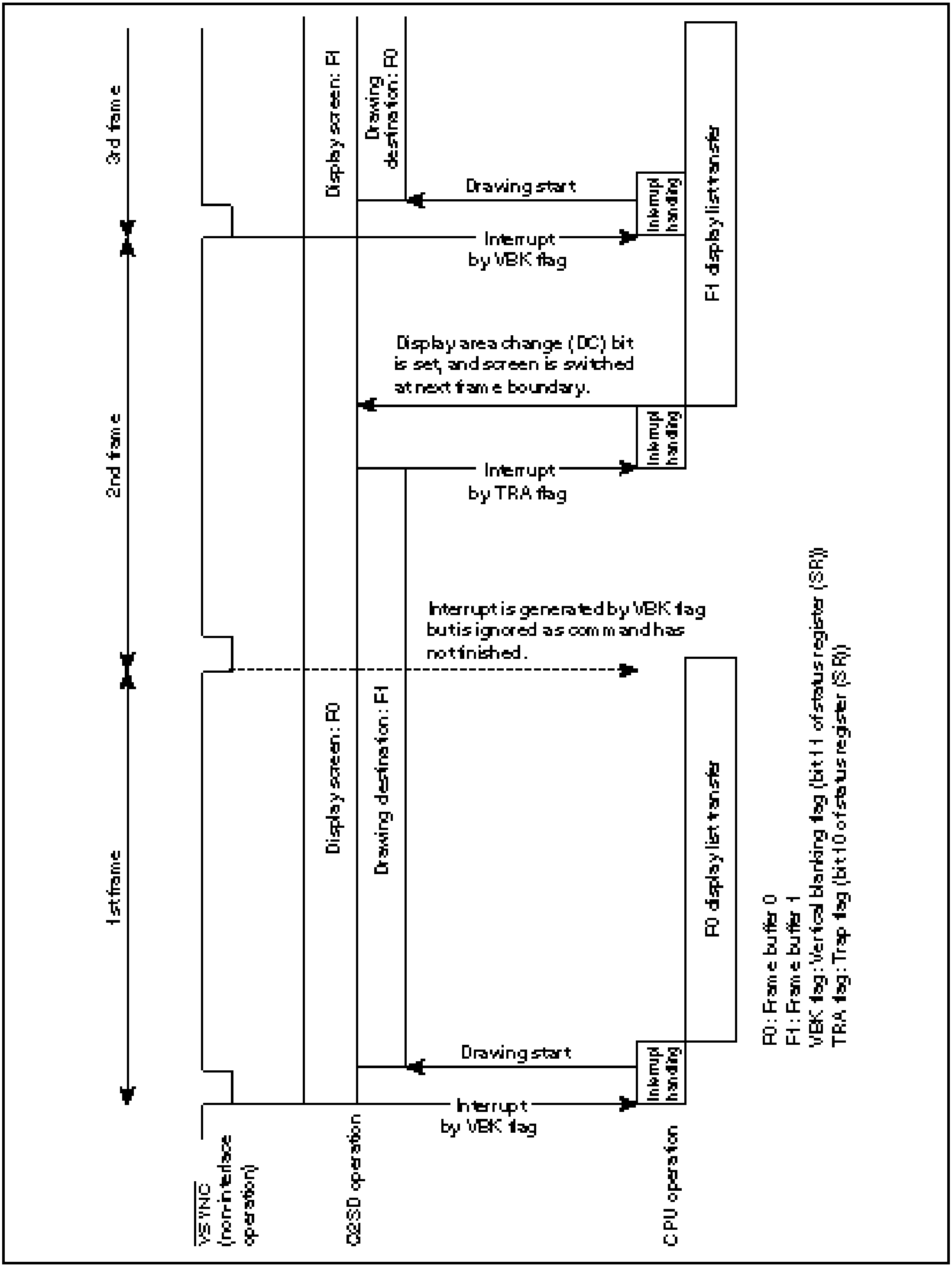


Figure 3.8 (a) Operation in Manual Display Change Mode

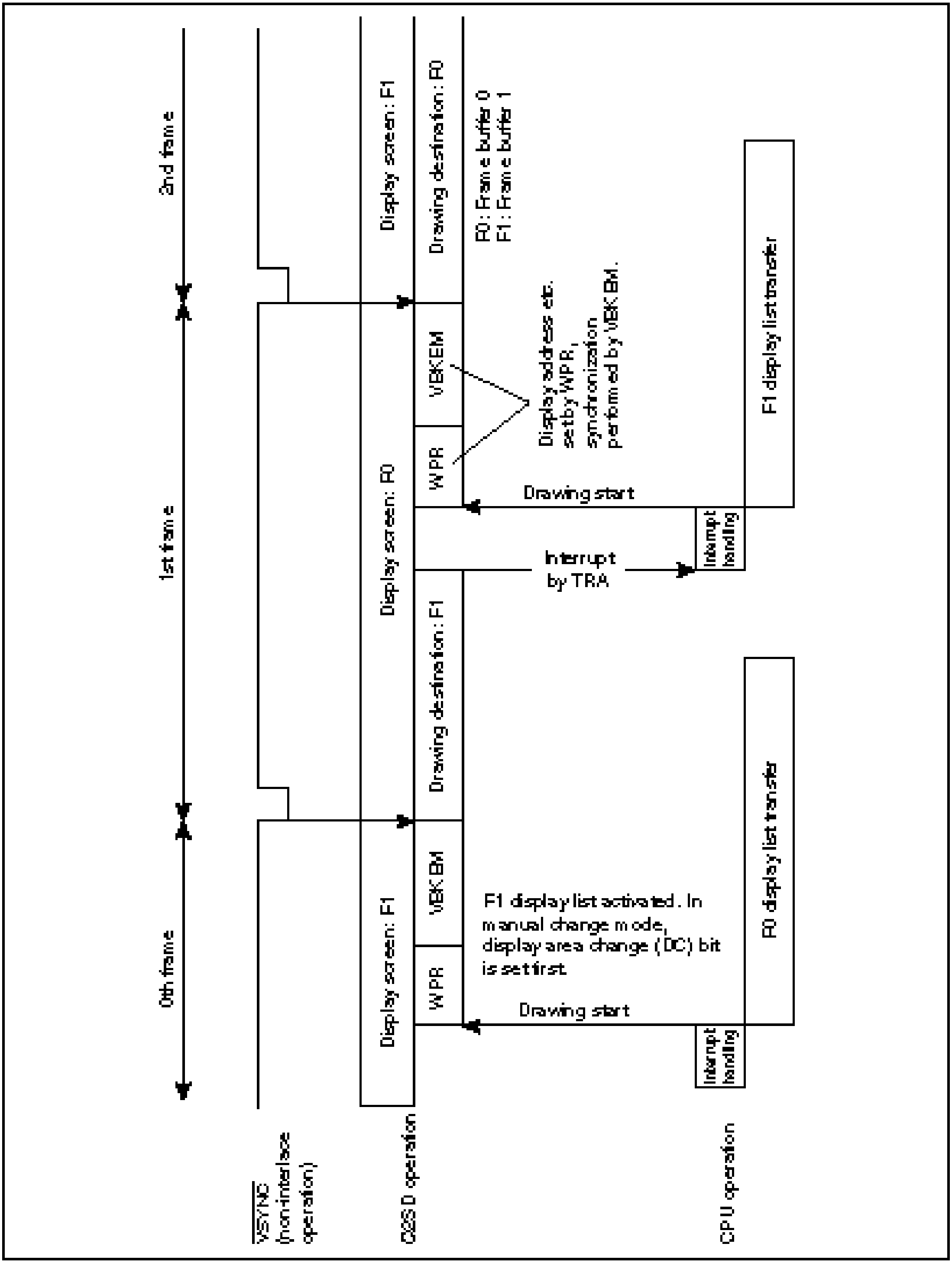
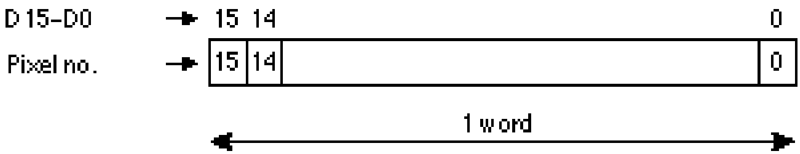


Figure 3.8 (b) Operation when Using VBKEM Command

3.3.3 Color Data Formats

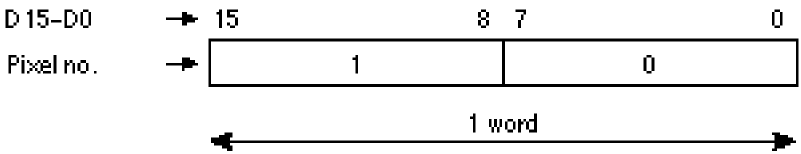
Input Color Data Configurations: Input color data configurations are shown below.

1. 1-bit/pixel data



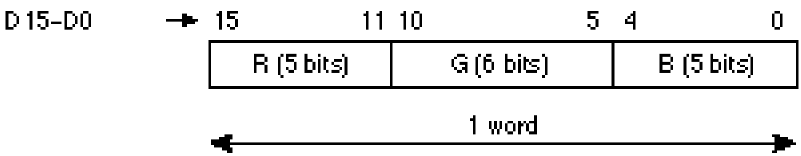
Note: The pixel number runs from 0 upward from the left to right side of the screen.

2. 8-bit/pixel data



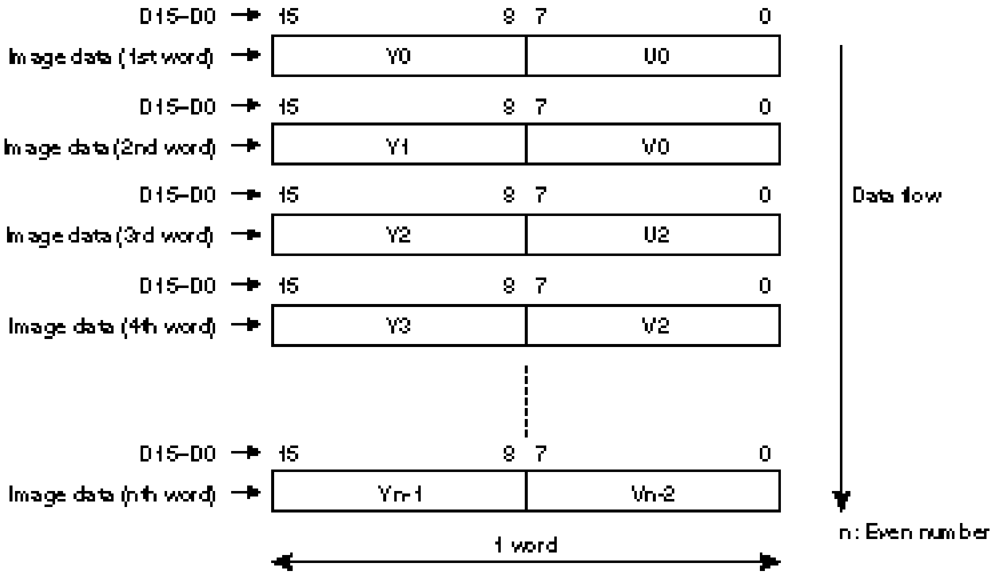
Note: Set the same values for D15–D8 and D7–D0.

3. RGB data (16-bit/pixel data)



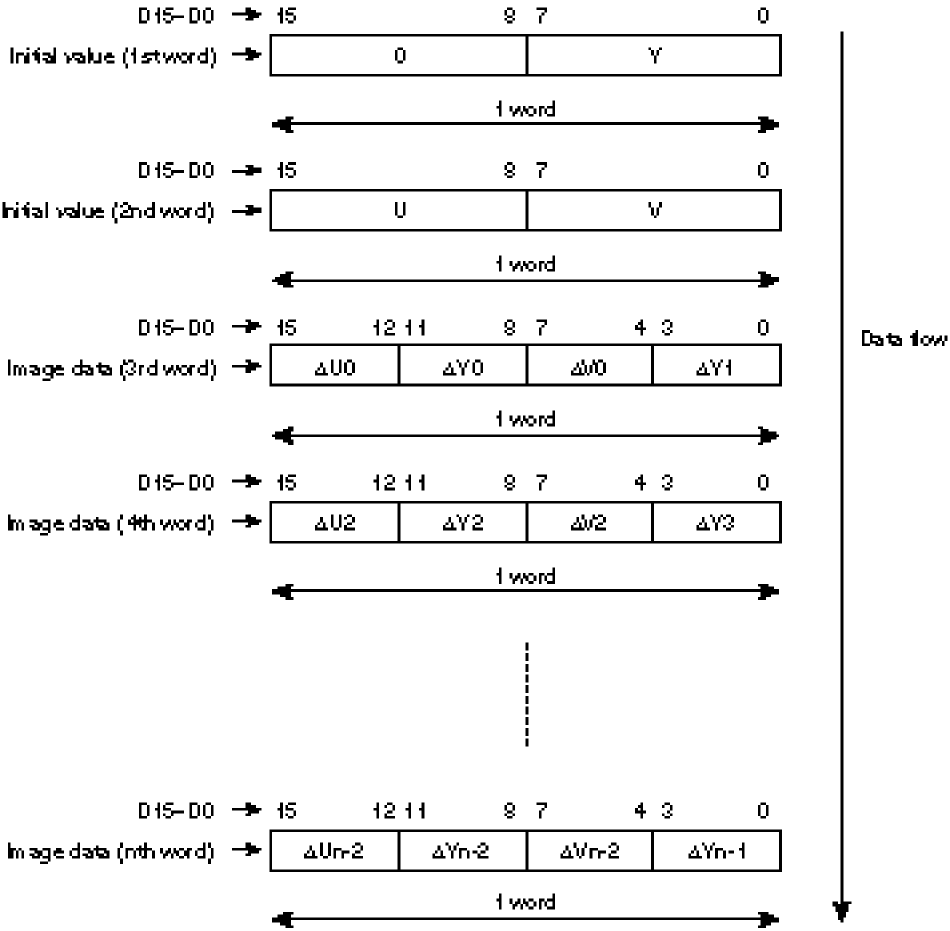
5. YUV data

YUV data uses a 4:2:2 format. The U and V data is horizontally reduced data.

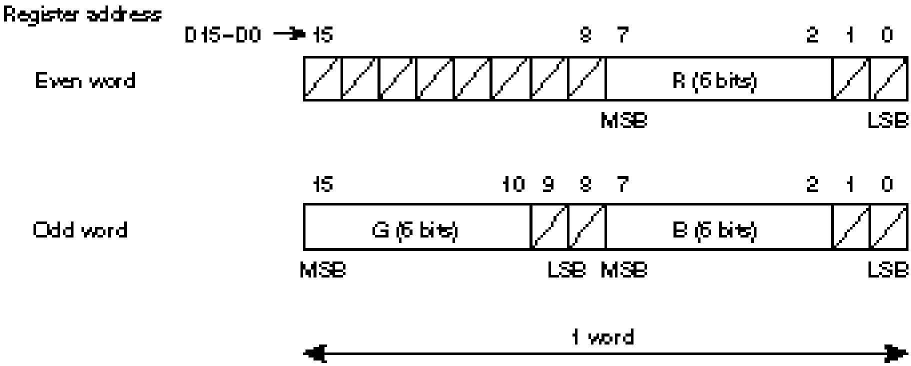


6. ΔYUV data

ΔYUV data uses a raster as the basic unit. The data configuration for one raster consists of the initial value in the first two words and compressed image data in the remaining words.

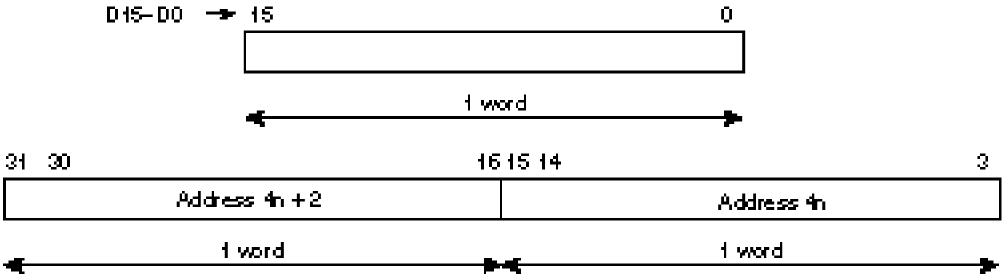


Color Palette Register Color Data Configuration: The color palette register color data configuration is shown below.

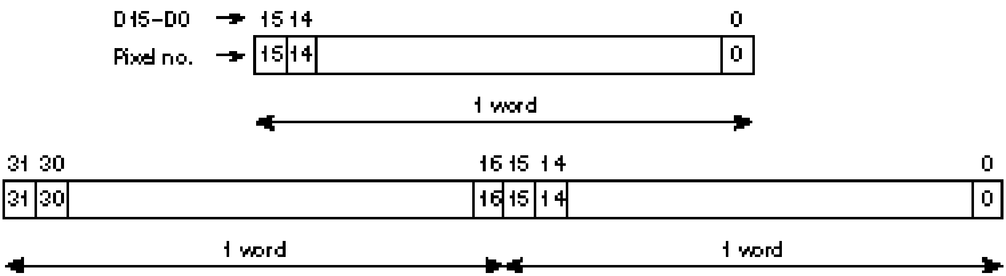


Configurations of Data in UGM: The UGM data configuration is shown below (first for a UGM 16-bit bus, then for a 32-bit bus).

1. 16-bit data

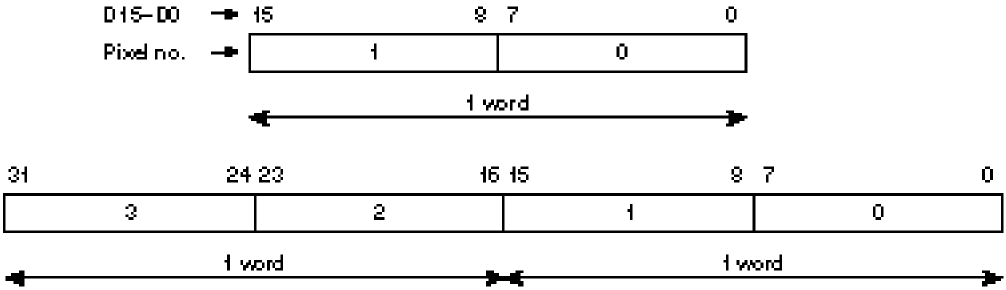


2. 1-bit/pixel data

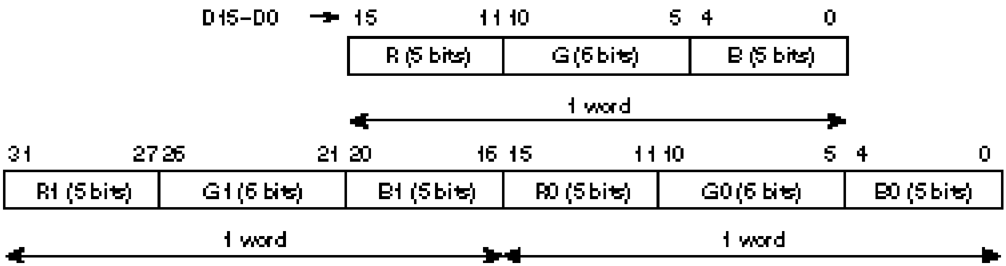


Note: The pixel number runs from 0 upward from the left to right side of the screen.

3. 8-bit/pixel data

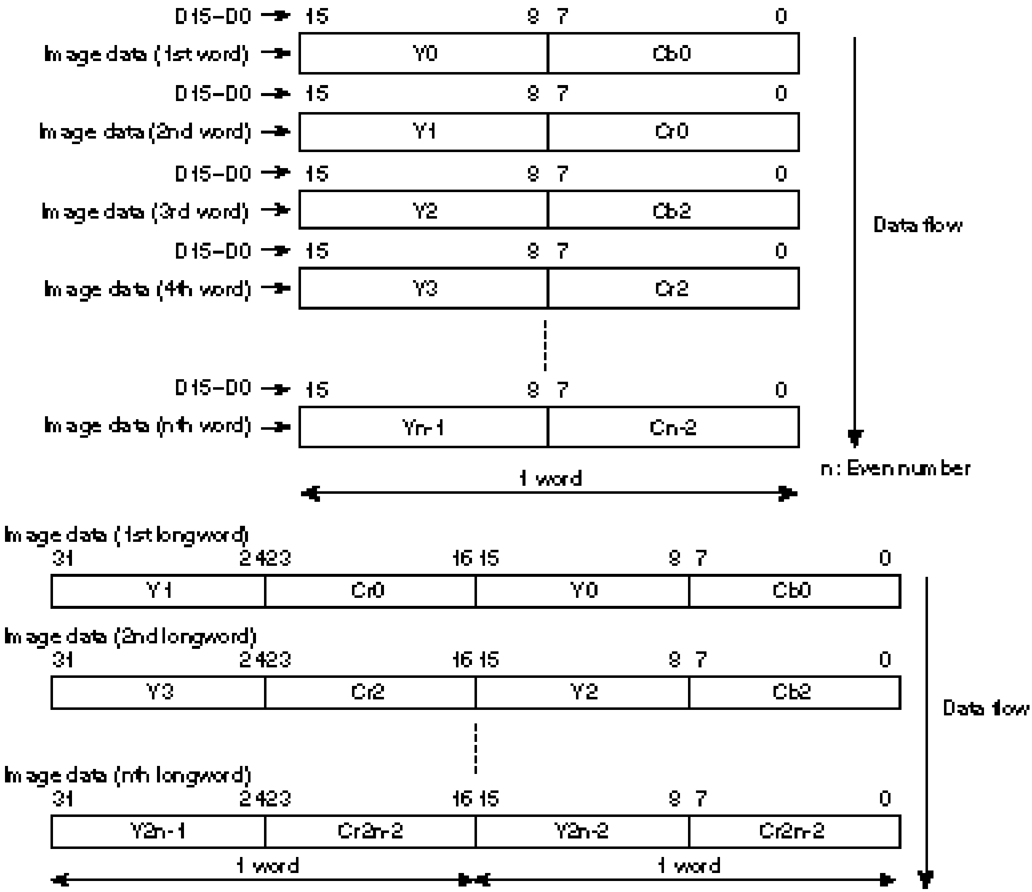


4. RGB data (16-bit/pixel data)



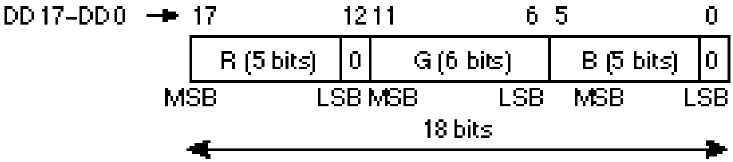
5. YC data

YC data uses a 4:2:2 format. Cr and Cb data is horizontally reduced data.

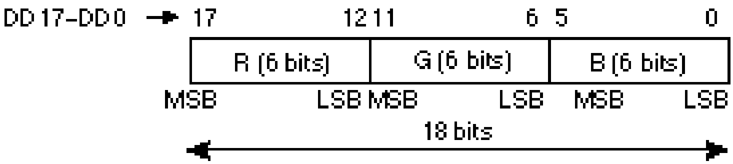


Output Color Data Configurations (Q2SD → On-Chip DAC): Output color data configurations are shown below.

1. RGB data
   a. When the frame buffer is 16 bits/pixel and the color palette is not used



   b. When the frame buffer is 8 bits/pixel and the color palette is used



DD17 to DD0 are internal signals. Q2SD analog output is the result of D/A conversion of the above data.

Color Data Format Conversion: The specifications of the function for converting ΔYUV or YUV data in main memory to RGB data are shown in figure 3.9.

The Q2SD converts ΔYUV or YUV data transferred from the SuperH to RGB data and stores it in the UGM. The converted RGB data can be used as source data for quadrilateral-drawing commands.

Also, RGB data on the SuperH side can be transferred to the UGM source area without being converted.

Q2SD registers that should be set by the SuperH are as follows. Make the register settings in the order shown in figure 3.10.

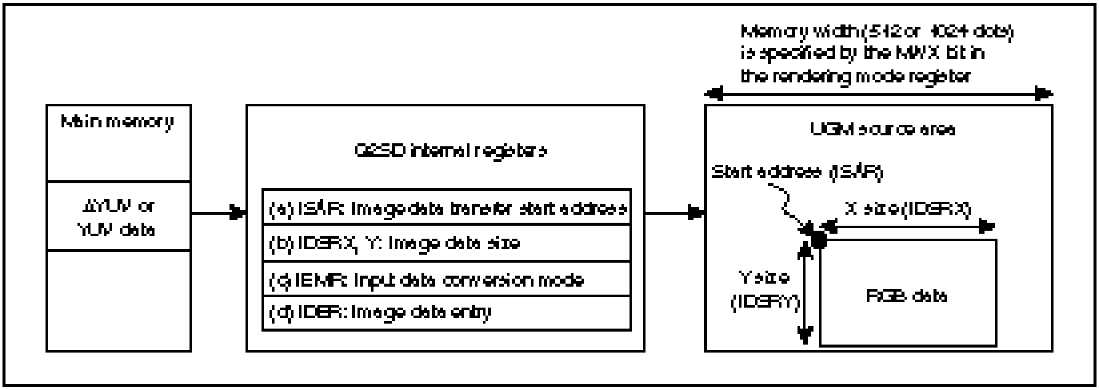


Figure 3.9 ΔYUV/YUV-to-RGB Conversion Function Specifications

Set the following:

(a) ISAR : image data transfer start address
(b) IDSRX, Y : image data size

↓

(c) Set IEMR (bits YUY2, 1, 0): input data conversion mode

The setting procedure is shown in the following table.

Values to Be Set in YUY2, YUY1, YUY0			Setting Procedure
YUY2	YUY1	YUY0	
0	0	1	Set (0, 0, 1) in (YUY2, 1, 0).
0	1	0	Set (0, 1, 0) in (YUY2, 1, 0).
0	1	1	Set (0, 0, 0) in (YUY2, 1, 0), then set (0, 1, 1) in (YUY2, 1, 0).
1	1	1	Set (1, 0, 0) in (YUY2, 1, 0), then set (1, 1, 1) in (YUY2, 1, 0).

↓

(d) Write to IDER : image data entry

Figure 3.10 Register Setting Procedure for ΔYUV/YUV-to-RGB Conversion

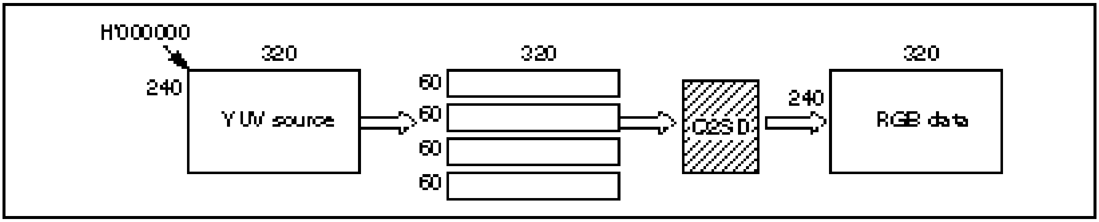
1. Sample settings for YUV-RGB and ΔYUV-RGB conversion by DMA transfer

   When performing YUV-RGB or ΔYUV-RGB conversion by DMA transfer, ensure that the number of pixels corresponding to DMA transfer word count registers H and L (DMAWRH, DMAWRL) is the same as the total number of pixels specified by image data size registers X and Y (IDSRX, IDSRY).

If these two values are not the same, DMA transfer will end at the smaller of the two values, and then bits YUV2, YUV1, and YUV0 will be cleared to 000, and bits DMA1 and DMA0 will be cleared to 00 again.

Therefore, if the total transfer word count of the YUV source is larger than the DMA transfer word count, DMAWR, the DMA setting must be divided into a number of stages. The YUV image data transfer start address, ISAR, must be set each time this conversion is performed.

An example of the settings for transferring 320 × 240 YUV source data by means of four DMA operations is shown below.



2. Sample settings for YUV-RGB conversion

Conditions:	• YUV source size:	320 × 240 dots
	• Number of setting stages:	4
	• UGM transfer destination address:	H'000000
	• YUV mode:	YUV-RGB conversion

· 1st time

(1) Image data transfer start address setting
ISAR = H'000000

(2) Image data transfer size register settings*1
IDSRX = 320
IDSRY = 60

(3) DMA transfer word count setting*2
DMAWR = 19200

(4) YUV mode setting
IEMR = H'01

(5) DMA mode setting
DMA in SYSR = H'11

(6) Wait until the DMF bit in the status register (SR) changes to 1.

· 2nd time onward

(7) Image data transfer start address re-setting*3
ISAR = current ISAR + transfer word count (Y) = H'C180

Notes: 1. Where IDSRX and IDSRY satisfy the following conditions:

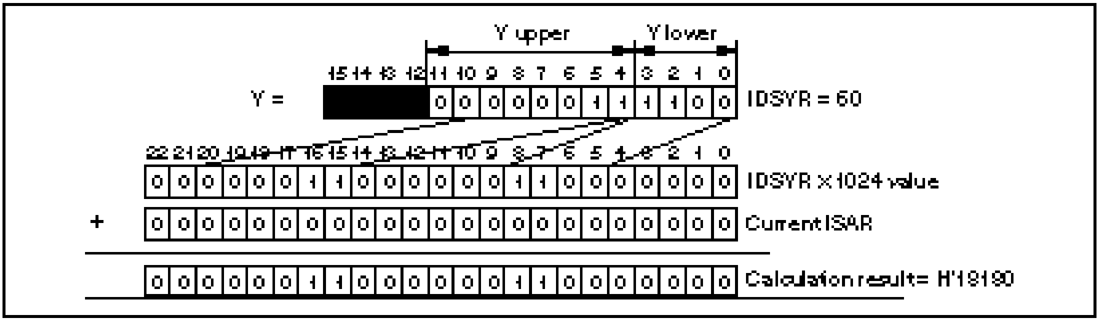
- The transfer unit is a line.
- One transfer is within the DMAWR range.

2. Set the transfer word count corresponding to IDSXR/IDSYR.

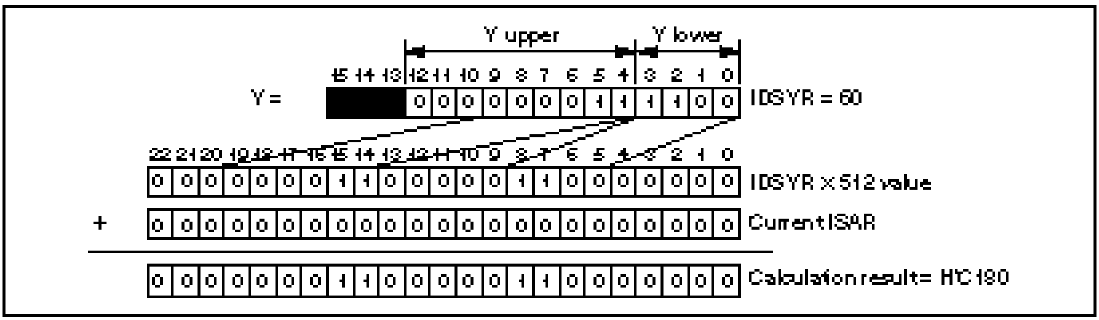
3. In the Q2SD, the frame buffer area address allocation is as shown in section 3.2.3, Memory Map, in the Target Specification. Therefore, set the drawing data transfer start address in ISAR with reference to the relationship between memory physical addresses and coordinates shown in figure 3.4 (d) or 3.4 (e).

   In this setting example, the start position of the second image data transfer is at the [X = 0, Y = 60] dot position. This position is divided into the upper and lower coordinates of X and Y, respectively, and the value assigned in figure 3.4 (d) or 3.4 (e) is the value set in ISAR the second time.

Example: Method of calculating second ISAR, with memory width of 512 (from figure 3.4 (d))



Example: Method of calculating second ISAR, with memory width of 1024 (from figure 3.4 (d))



(8) Image data transfer size register settings*4

IDSRX = 320

IDSRY = 60

(9) DMA transfer word count setting*5

DMAWR = 19200

(10) YUV mode setting

IEMR = H'01

(11) DMA mode setting

DMA in SYSR = H'11

Steps (6) to (11) are then repeated until the end of the YUV transfer source. Settings for ΔYUV-RGB conversion are also made as shown in the above example.

Notes: 4. Same setting conditions as for (2).

5. Same setting conditions as for (3).

3.3.4 Display Functions

The Q2SD has functions for outputting image data, drawn in the UGM, in synchronization with externally or internally generated display timing.

Registers and Display Screen: In the Q2SD, horizontal and vertical display timing for the display screen is set in the display control registers (see section 5.5, Display Control Registers).

The display control register settings depend on the scanning and synchronization systems used. The calculations shown in table 3.2 should therefore be carried out before making the display control register settings.

Figure 3.11 shows the display timing in non-interlace mode. The display screen is defined by the variables shown in table 3.3. Set the number of rasters within one $\overline{VSYNC}$ cycle for each of vc, vsw, ys, and yw, regardless of the display mode register scan mode.

For the dot clock frequency, use the value obtained by dividing the number of pixels to be displayed in the xw interval by the duration of the xw interval. Input the dot clock to the CLK1 pin.

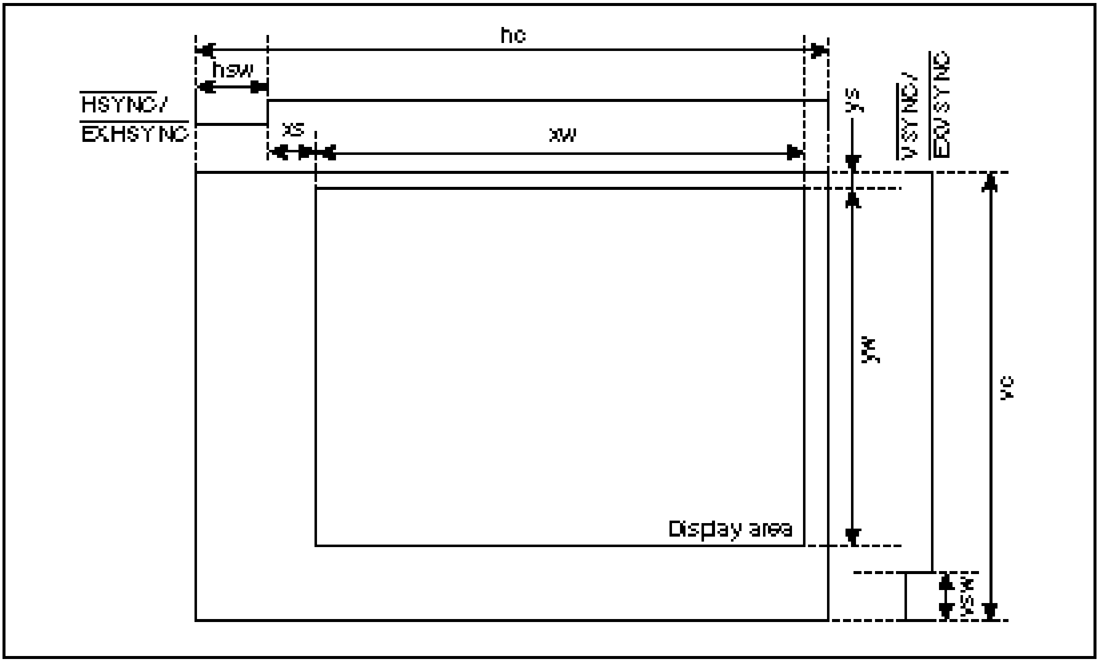


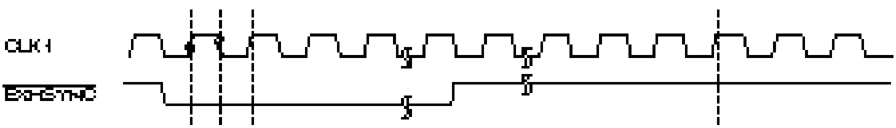
Figure 3.11 Display Timing

Table 3.2 Register Settings

Register No. (Address)	Register Name		Bit Name	Operating Mode	
				Master Mode	**TV Sync Mode**
008	Display size register X (DSRX)		DSX	xw[*5]	xw[*5]
009	Display size register Y (DSRY)		DSY	yw	yw
013	Display window	Horizontal display start position register (DSWR-HDS)	HDS	hsw + xs – 11[*3]	hsw + xs – 14[*2,*3]
014		Horizontal display end position register (DSWR-HDE)	HDE	hsw + xs – 11 + xw	hsw + xs – 14 + xw[*2]
015		Vertical display start position register (DSWR-VDS)	VDS	ys – 2[*4]	ys – 2[*4]
016		Vertical display end position register (DSWR-VDE)	VDE	ys – 2 + yw	ys – 2 + yw
017	Horizontal sync pulse width register (HSWR)		HSW	hsw – 1	hsw – 1
018	Horizontal scan cycle register (HCR)		HC	hc – 1	hc
019	Vertical sync position register (VSPR)		VSP	vc – vsw – 1	vc – vsw – 1
01A	Vertical scan cycle register (VCR)		VC	vc – 1	vc + 2

Notes: 1. In all scanning modes the settings of the VDS, VDE, VSP, and VC bits are made for a one-field unit.

2. The HDS and HDE specifications are the values from the fourth rise of CLK1 after the low level of $\overline{EXHSYNC}$ is detected at the rise of CLK1.



3. The setting for the lower limit of the HDS bits is as follows: when MCLK = 2 × CLK1, HDS ≥ 64 × (CLK1/MCLK); when MCLK > 2 × CLK1, HDS ≥ (64 + 80) × (CLK1/MCLK).

The unit for MCLK and CLK1 is MHz. When MCLK = 2 × CLK1, use a clock with which MCLK and CLK1 are synchronized. With a multiplication factor of N, MCLK is N × CLK0.

4. In interlace and interlace sync & video modes, the setting is: VDS ≥ 1.
5. Use a value of 4 or more for DSX.

   If Cursor 1 Horizontal Display Start Position (HCS1) and Cursor 2 Horizontal Display Start Position (HCS2) in the cursor registers are DSX, DSX-1, DSX-2, DSX-3, DSX-4, DSX-5, then set DSX = XW+6.

Table 3.3 Variables Defined by Display Screen

Variable	Description	Unit
hc	Horizontal scan cycle	Dot clock
hsw	Horizontal sync pulse width	Dot clock
xs	Interval between HSYNC rise and display screen horizontal display start position	Dot clock
xw	Display screen display width per raster	Dot clock
vc	Vertical scan cycle	Raster lines
vsw	Vertical sync pulse width	Raster lines
ys	Interval between VSYNC rise and display screen vertical display start position	Raster lines
yw	Display screen vertical display interval	Raster lines

Screen Display: In the Q2SD, the DEN (display enable) bit in the system control register (SYSR) can be used to select whether or not display data is to be output to the screen. When display data is not output, the display off output register (DOOR) settings are displayed.

The frame flag (FRM) and vertical blanking flag (VBK) in the status register (SR) indicate the detected position of the fall of the vertical sync signal ($\overline{\text{VSYNC}}$) determined by the set value (VSP) in the vertical sync position register (VSPR), regardless of the synchronization method.

Scanning Systems: The Q2SD allows selection of non-interlace mode, interlace mode, or interlace sync & video mode as the scanning system. The mode setting is made in the SCM (scan mode) bits in the display mode register (DSMR). In non-interlace mode, one frame is composed of one field. In interlace mode, one frame is composed of two fields, even and odd, in which the same data is displayed. In interlace sync & video mode, also, one frame is composed of two fields, even and odd, but in this mode different data is displayed in these two fields. When the ODEV bit is cleared to 0 in display mode register 2 (DSMR2), the $\overline{\text{ODDF}}$ pin signal functions as follows. In master mode, the Q2SD outputs a high-level signal from the $\overline{\text{ODDF}}$ pin during even field display, and a low-level signal during odd field display. In TV sync mode, a high-level signal is input at the $\overline{\text{ODDF}}$ pin to display the even field, and a low-level signal to display the odd field. When the

ODEV bit is set to 1 in DSMR2, the polarity of the $\overline{ODDF}$ pin is the opposite of that described above. Figure 3.12 shows examples of raster scan control display.

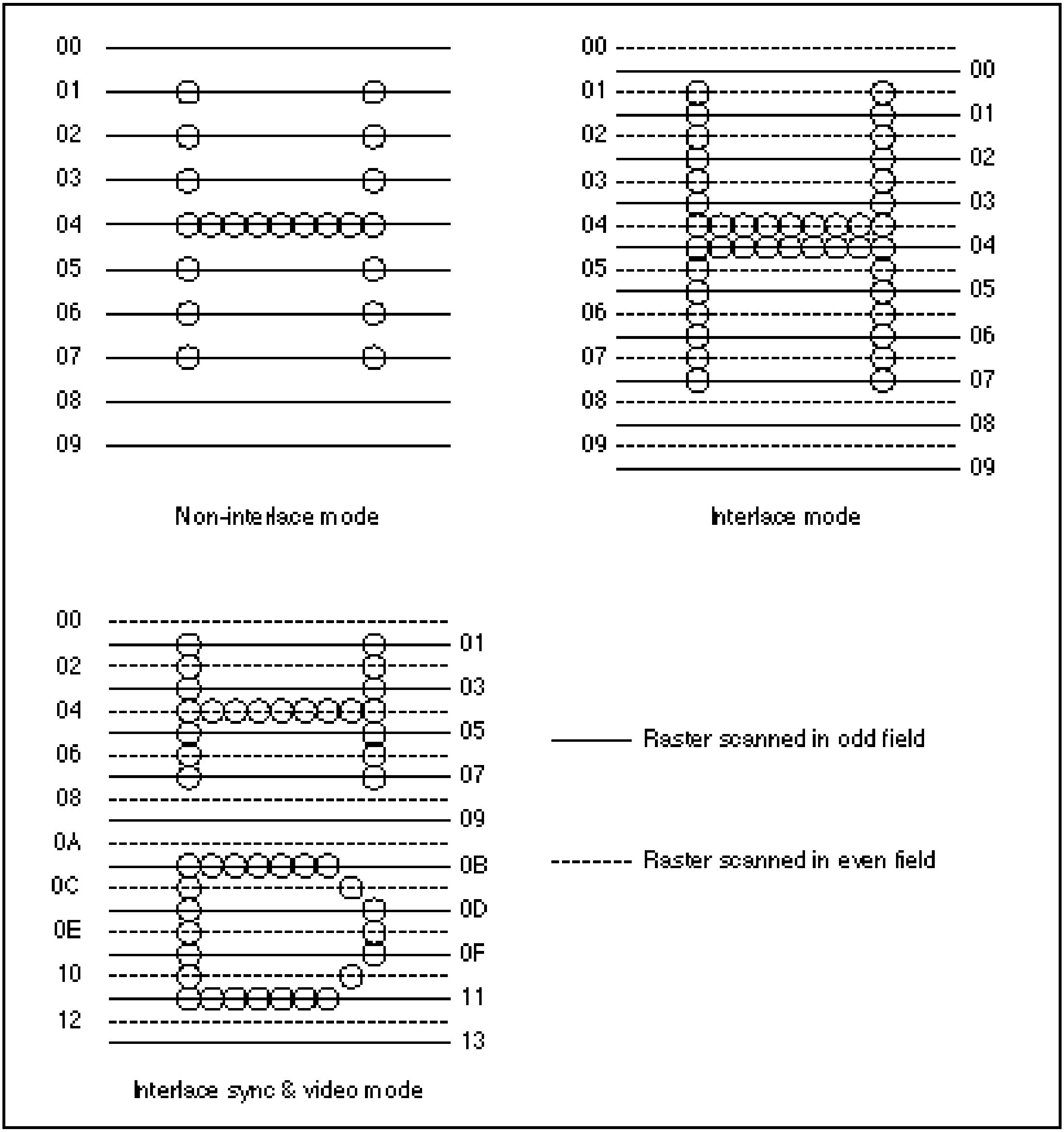


Figure 3.12   Examples of Raster Scan Control Display

Synchronization Systems: The Q2SD is provided with a TV sync function in addition to master mode to simplify synchronization with an external device.

The TVM (TV sync mode) bits in the display register (DSMR) are used to select master mode or TV sync mode.

- Internal Synchronization Mode (Master Mode)

  Setting the horizontal and vertical sync signal ($\overline{HSYNC}$ and $\overline{VSYNC}$) cycles and pulse widths in the display control register outputs the corresponding waveforms, and display data is output in synchronization with these signals.

  In interlace mode and interlace sync & video mode, a signal indicating odd field or even field is output at the $\overline{ODDF}$ pin.

- External Synchronization Mode (TV Sync Mode)

  In TV sync mode, display data is output in synchronization with vertical and horizontal sync signals ($\overline{EXHSYNC}$ and $\overline{EXVSYNC}$) input from an external source. The Q2SD outputs display data on the basis of the fall of the $\overline{EXHSYNC}$ signal and the rise of the $\overline{EXVSYNC}$ signal.

  In this mode, the horizontal sync signal, vertical sync signal, and clock from the sync signal generator should be input at the $\overline{EXHSYNC}$, $\overline{EXVSYNC}$, and CLK1 pins, respectively. The $\overline{CYSINC}$ pin outputs a high-level signal. Signals without equalizing pulses should be used for $\overline{EXHSYNC}$ and $\overline{EXVSYNC}$.

  In interlace mode and interlace sync & video mode, a signal indicating odd field or even field should be input at the $\overline{ODDF}$ pin.

  When the Q2SD is operated in TV sync mode, display control register HSWR, HCR, VSPR, and VCR settings are essential.

  In non-interlace mode, the $\overline{ODDF}$ pin should be fixed high or low to prevent an unstable input level at this pin.

  The Q2SD performs UGM refreshing based on $\overline{EXHSYNC}$ and $\overline{EXVSYNC}$. Therefore, $\overline{EXHSYNC}$ and $\overline{EXVSYNC}$ must be input to enable UGM refreshing to be carried out.

  The signal flow in TV sync mode is shown in figure 3.13.

  In this mode, the CDE pin can be controlled by the Q2SD by comparing the colors displayed by the Q2SD with the colors set in color detection registers H and L (CDERH, CDERL), and master R/G/B output and slave R/G/B output can be switched in pixel units by external circuitry.

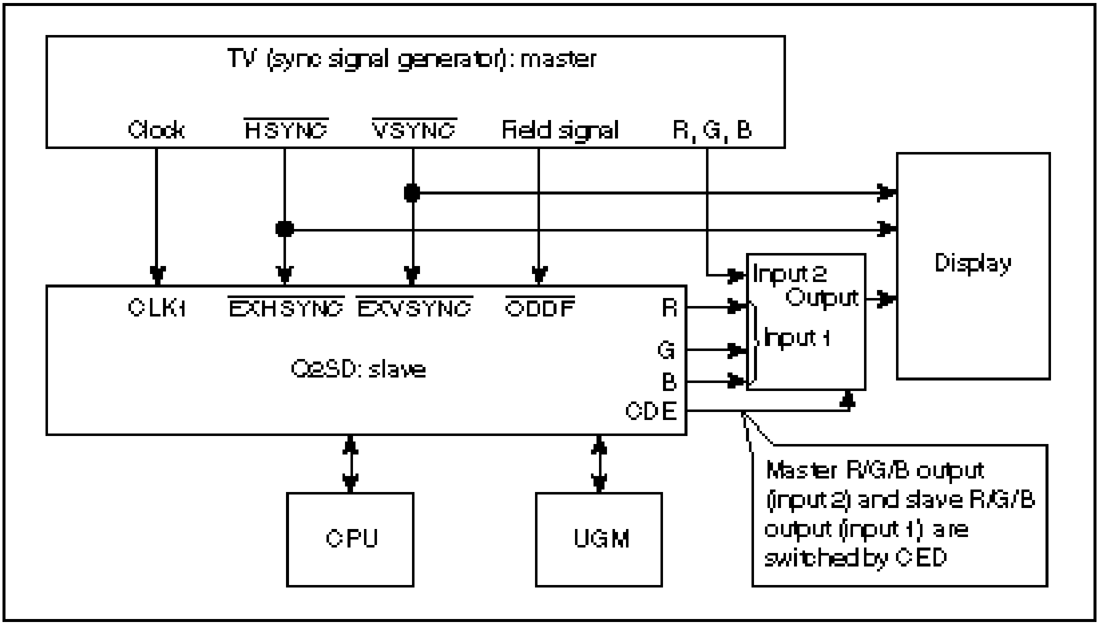


Figure 3.13 Signal Flow in TV Sync Mode

· TV Sync Mode Change Procedure

When B'01 is set in the TV sync mode (TVM) bits in the display mode register (DSMR) and a transition is made to synchronization system switching mode, set the display reset bit (DRES) to 1 and clear the display enable bit (DEN) to 0 in the system control register before making the transition to synchronization system switching mode.

This procedure provides for the HD64413A to perform UGM refreshing in synchronization system switching mode. This procedure must only be carried out when the Q2SD is not performing drawing.

The procedure is shown below. Steps 1 to 3 must be carried out in that order.

1. Set BG = 0, VWE = 0, CE1 = 0, and CE2 = 0.
2. Set DRES = 1 and DEN = 0.
3. Set TVM1 = 0 and TVM0 = 1.

The procedure for switching from synchronization system switching mode to TV sync mode is shown in 4 to 7 below.

4. Input the clock to CLK1. When TVM1 = 1 and TVM0 = 0, also input signals to the $\overline{\text{EXHSYNC}}$, $\overline{\text{EXVSYN}}$C, and $\overline{\text{ODDF}}$ pins.
5. If the display size is to be changed, set values in the Q2SD's address-mapped registers.
6. Set TVM1 = 0 and TVM0 = 0, or TVM1 = 1 and TVM0 = 0, to enable clock input from the CLK1 pin. If necessary, also set BG = 1, VWE = 1, CE1 = 1, and CE2 = 1.
7. Set DRES = 0 and DEN = 1. When an internal update is performed, the Q2SD begins display.

Refresh Control: The number of refresh cycles for the UGM connected to the Q2SD is set in bits REF3 to REF0 (refresh cycle count) in the display mode register (DSMR).

Bit 3: REF3	Bit 2: REF2	Bit 1: REF1	Bit 0: REF0	Operation
0	0	0	0	Refresh timing is not output.
*	*	*	*	Refresh timing is set to any value from 1 to 15 cycles, and output.

The setting made in bits REF3 to REF0 is the number of refreshes per raster.

For example, if the refreshing specification of the memory used is 1/60 sec for one field at 4096 cycles/64 ms, the necessary number of cycles in one field is 1067. The number of refresh cycles (times/raster) should be set so that the number of cycles required for one field is the number of lines.

The number of refresh cycles should therefore be set so that the following expression is satisfied:

$$1067 \leq \text{number of lines} \times \text{number of refresh cycles}$$

The Q2SD supports CAS-before-RAS refresh mode.

The number of refreshes set in bits REF3 to REF0 are executed from the fall of the DISP signal.

Table 3.4 shows sample settings.

Table 3.4 Sample Estimations of Number of Refresh Cycles

Display Screen Size	Frame Rate	Number of Rasters	Number of Refreshes Required Per Raster	REF Set Value
320 × 240	1/60 sec	525/2 lines	(1/60) (2/525) (4096/0.064) = 4.06	5
480 × 240	1/60 sec	525/2 lines	(1/60) (2/525) (4096/0.064) = 4.06	5
640 × 480	1/60 sec	525/line	(1/60) (1/525) (4096/0.064) = 2.03	3

Superimposed Display: The Q2SD is provided with functions for performing superimposed display. The screen types and their features are described below.

- Superimposed screen types
  - ¾ Frame screen (FB0 or FB1)
  - ¾ Video window
  - ¾ Background screen
  - ¾ Cursors

The frame screens, video windows, and background screens that can actually be superimposed depend on the UGM bus width, the Q2SD operating frequency, and the display operating clock frequency. See appendix E.

- Priority order of superimposed screens

  Screens are displayed in the priority order shown below. With the cursors, display can be performed according to the priority order set in the window priority bits (PRI) in display mode register 2 (DSMR2).

  Frame screen > video window > background screen (in front-to-rear order)

- Features of each screen
  - ¾ Frame screen (FG)

    If the data for a frame screen pixel is 0, a low-priority screen such as the video window is displayed through that pixel.
  - ¾ Video window (VW)

    In the video window, all display data incorporated in the video is displayed.Therefore, the video window is displayed as a rectangle, and is not transparent to a low-display-priority screen such as a background screen. When VIE = 0, this window can also be used as an independent window for displaying the video area defined by the video area start address registers (VSAROH, VSAROL).
  - ¾ Background screen (BG)

    The display start position can be set in background coordinate display start registers X and Y (BGSX, BGSY) in pixel units from address UGM0. The background screen is suitable for performing scroll display. This screen can only be used when the frame screen is set to 8-bit/pixel mode with bits GBM2 to GBM0 in the rendering mode register (REMR). When displaying the background screen, ensure that the frame screen and background screen locations in the UGM do not overlap.
  - ¾ Cursors

    Two 32 × 32-pixel cursors with a hardware blink function can be displayed. If the cursor pixel data is 0, a low-priority screen is displayed through that pixel.

· Display on/off control

The bits that control whether or not each screen is displayed are shown below. With the frame screen and background screen, set either or both to be displayed. When the frame screen is set to 16-bit/pixel mode with bits GBM2 to GBM0, the Q2SD's internal display data increases and other screens cannot be displayed. Therefore, to disable display of the video window, background screen, and cursors, the bits controlling whether or not each screen is to be displayed should be cleared to 0. In this case, also, clear the VIE bit to 0 in the video incorporation mode register (VIMR) to disable video incorporation.

¾ Frame screen: Can be set with the FBD bit in display mode register 2 (DSMR2).

¾ Video window: Can be set with the VWE bit in display mode register 2 (DSMR2).

¾ Background screen: Can be set with the BG bit in the display mode register (DSMR).

¾ Cursors: Can be set with bits CE1 and CE2 in display mode register 2 (DSMR2).

Register updating for each screen should be carried out in the register update interval shown in section 5.2, Register Updating. The display contents differ according to the setting of the background screen wraparound mode (WRAP) bit.

Table 3.5 Background Screen Related Register Settings

Register		Field			
Address	**Name**	**Bit No.**	**Name**	**Set Value**	**Notes**
H'005	DSMR	10	BG	1/0	Combination on/off
		11	WRAP	1/0	Wraparound on/off
H'006	REMR	2–0	GBM	000–111	8 or 16 bits/pixel
H'026	BGSRX	9–0	BGSX	BG starting point X coordinate	Coordinate origin is start of UGM
H'027	BGSRY	13–0	BGSY	BG starting point Y coordinate	

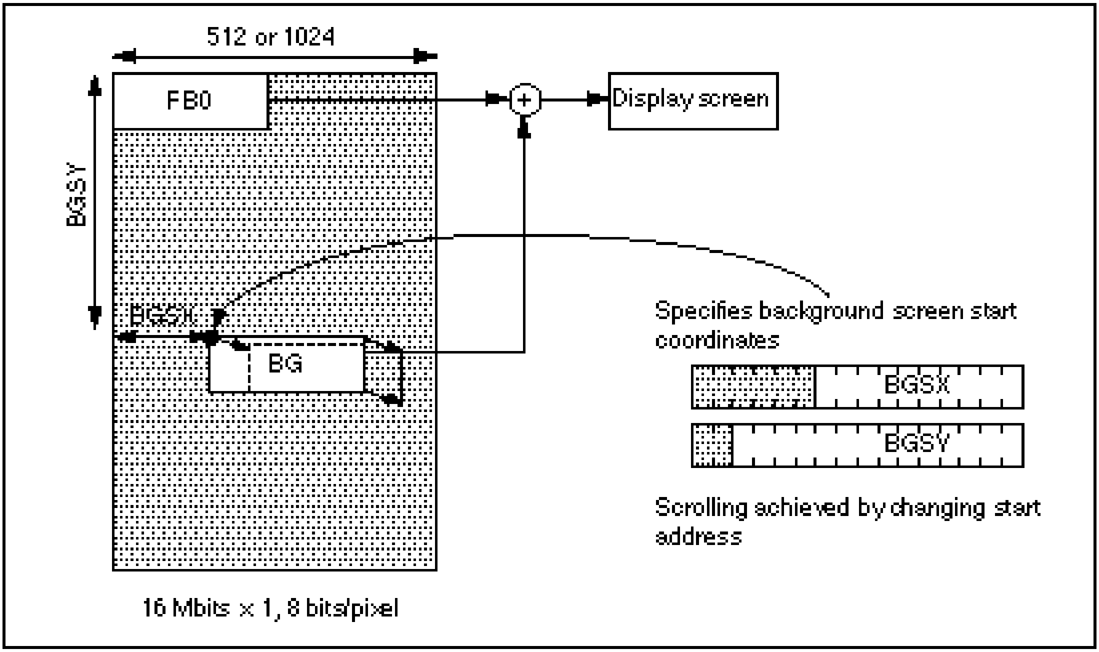


Figure 3.14   Example of Background Screen Simple Scroll (WRAP = 0)

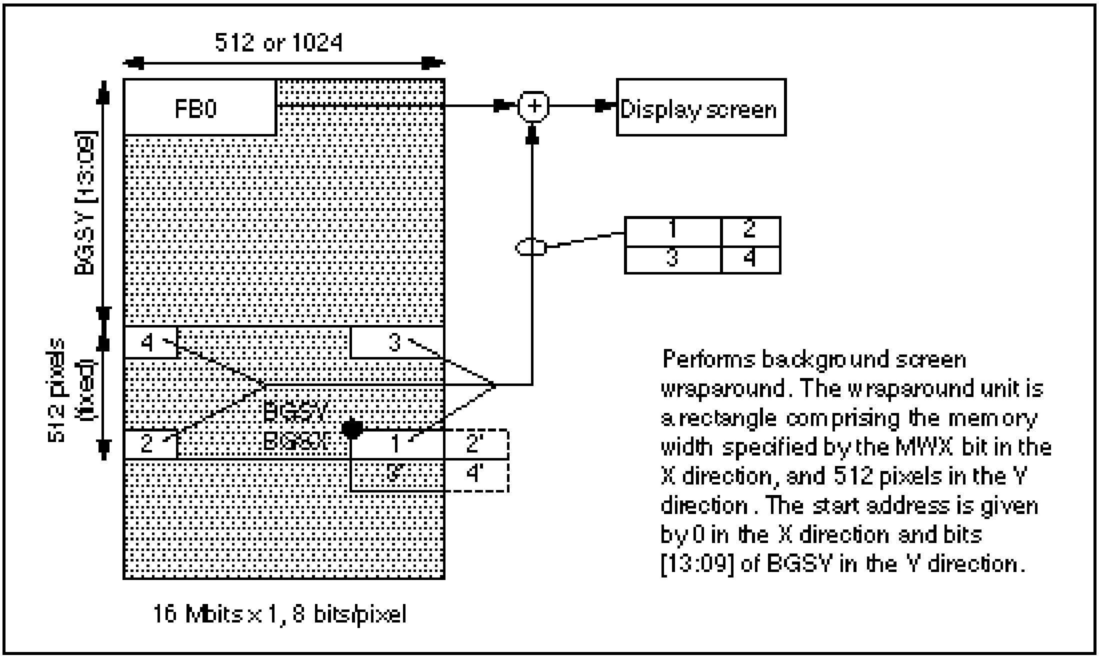


Figure 3.15   Example of Background Screen Wraparound Scroll (WRAP = 1)

Display Timing: The relationship between the display control register settings and the display signals is shown in figure 3.16.

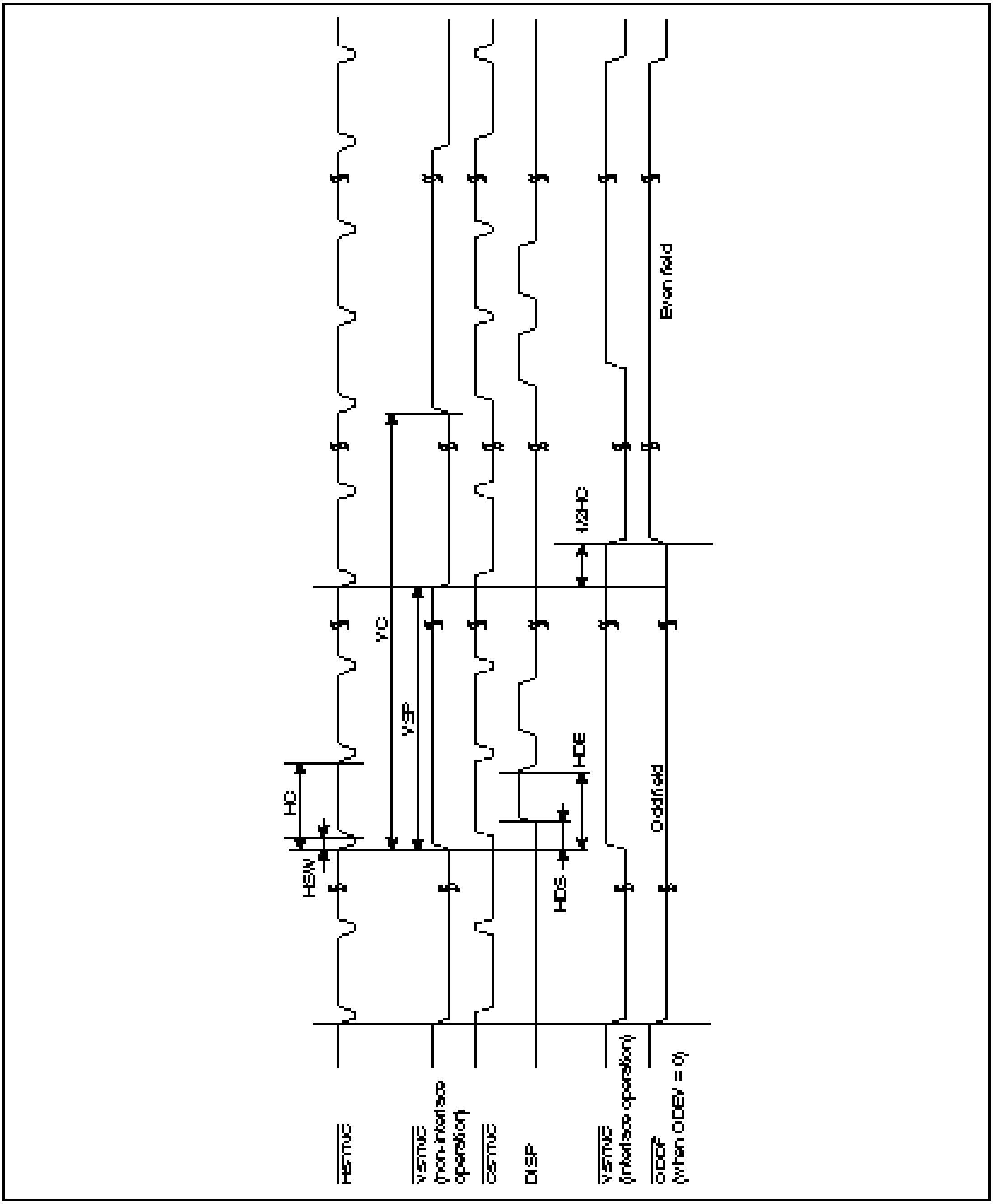


Figure 3.16 Display Timing

Video Incorporation and Video Display: The Q2SD can incorporate a YUV 4:2:2 8-bit data stream obtained by digital encoding of NTSC signals. The signals needed for incorporation are VIN0 to VIN7, $\overline{VHS}$, $\overline{VVS}$, $\overline{VODD}$, and VQCLK.

Video incorporation is performed at the rising edge of the VQCLK signal. The 8-bit data stream corresponding to the number of pixels set in the VSIZEX field in the video window size register (VSIZER) is incorporated for each VHS signal and transferred to one of three video storage areas determined by video area start address registers 0—2H/L (VSAR0—2H/L). These areas are used sequentially in frame units. The video window status bits (VID0, VID1) are valid when 0 is set in the video incorporation enable bit (VIE) and indicate the most recent video area in which video incorporation has been completed. The size of the video storage areas is determined by VSIZEX and VSIZEY. Use a frequency not exceeding 1/2 the system operating clock frequency for VQCLK (the system operating clock should be in the range 64 to 66 MHz). A number of VQCLK cycles equal to twice the number of luminous pixels are necessary per VHS. $\overline{VVS}$, $\overline{VHS}$, $\overline{VODD}$, and VQCLK are accepted following hardware reset release, and video incorporation is started by setting VIE to 1, having the first VVS signal sync signal input, then having the first VHS signal sync signal input.

As the video storage area incorporation line number is incremented each time a VHS signal sync signal is input, VQCLK must not be input during the VHS signal sync signal period.

For video incorporation, select a UGM bus width of 32 bits by setting MES1 and MES0 in the memory mode register (MEMR).

The relationship between video input signals is shown in figure 3.17.

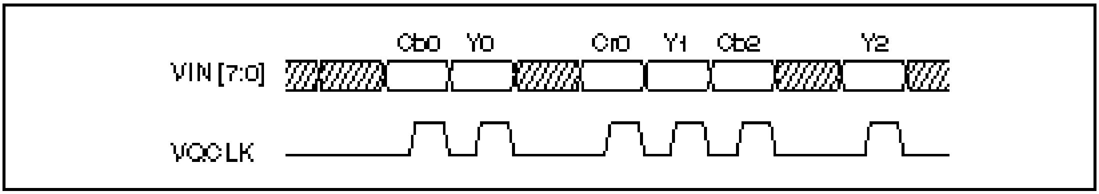


Figure 3.17 Video Incorporation Signals

For VSIZEX and VSIZEY, set the values (with fractions truncated) obtained by multiplying the number of effective pixels in the horizontal and vertical directions output from the digital encoder by the video incorporation reduction (thinning-out) ratio specified by the video incorporation reduction ratio bits (VSIZ4 to VSIZ0).

When handling interlace video input, field handling can be specified. When ODEN1, ODEN0 = 0, 1, a one-frame screen is created by combining even and odd fields. Motion interpolation is not performed. In the case of moving pictures with violent motion, the screen may be difficult to see as a still picture. This mode is suitable for interlace display under conditions in which the frame rate and the number of scanning lines in the vertical direction are both the same as for the input video. Note that even and odd lines are reversed between the original signal and the UGM.

Therefore, incorporation begins with an odd field (VINM = 0) when an even field is displayed first within a frame (ODEV = 1), and with an even field (VINM = 1) when an odd field is displayed first within a frame (ODEV = 0).

Data stored in a video storage area is displayed when video window enable (VWE) is set to 1 in display mode register 2 (DSMR2). The display start position at this time is set in the video display position register (VPR). Therefore, before VWE is set to 1, the initial value must first be set in the video display position register. The display size is set by VSIZEX and VSIZEY, and display is performed as an independent window (video window).

When ODEN1, ODEN0 = 1, 0, or 1, 1, a one-field image is treated as a one-field image. At this time, the number of vertical scanning lines is halved. Original-size display is not possible. To preserve the vertical/horizontal ratio, the horizontal multiplication factor should be adjusted. This mode is used for non-interlace (SCM1, 0 = 0:0) display.

The figure below shows the relationship between the various parameters in video incorporation.

The video display area must be set so that it does not extend beyond the frame buffer display area.

The video window is the same size as the video storage area.

Set the value of VACTIVE according to the setting of ODEN1 and ODEN0 in the video incorporation mode register (VIMR).

When performing video incorporation, input the video stream data to the VIN pin, without having scaling processing (thinning-out processing) performed by the video stream decoder.

1. When ODEN1 = 0 and ODEN0 = 1

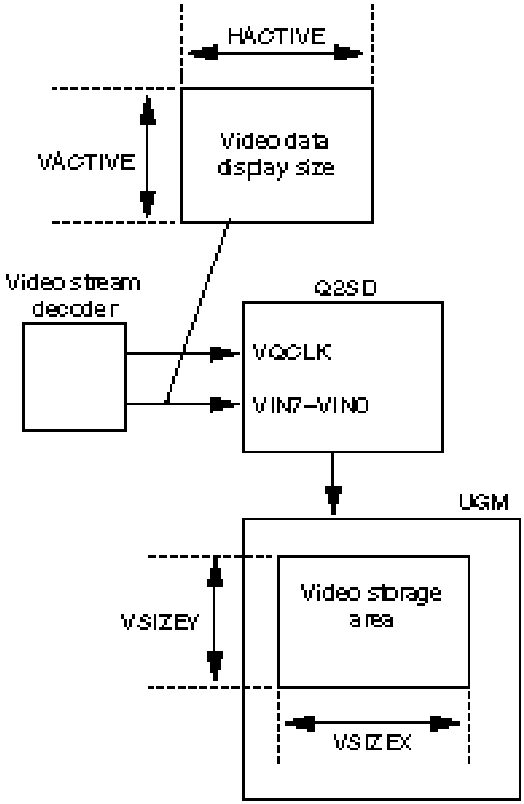
   Make the value of VACTIVE the total number of effective display lines in the vertical direction in two VVS intervals.

   For example, with 240 effective display lines in the vertical direction in one VVS interval, the setting should be:

   VACTIVE = 240 × 2 = 480

2. For settings other than ODEN1 = 0, ODEN0 = 1

   Make the value of VACTIVE the number of effective display lines in the vertical direction in one VVS interval.



vsizx: Horizontal reduction (thinning-out) ratio set by video incorporation reduction ratio (1/1, 1/2, 1/3, 1/4, or 1/5)
vsizy: Vertical reduction (thinning-out) ratio set by video incorporation reduction ratio (1/1, 1/2, 1/3, or 1/4)

HACTIVE (x vsizx pixels) ≥ VSIZEX
VACTIVE (x vsizy pixels) ≥ VSIZEY

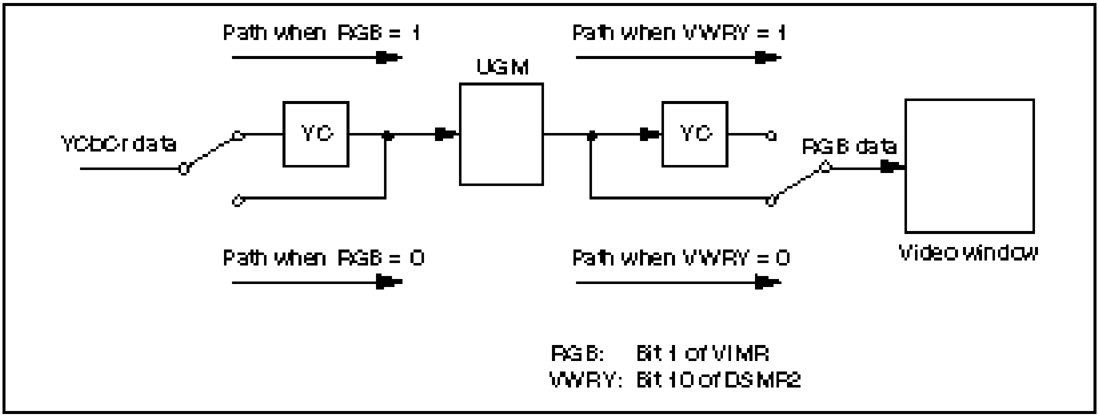
$$\text{VQCLK high-level width (sec.)} \geq \frac{2}{\text{MCLK}}$$

MCLK = CLK0 × N (Hz)

CLK0: Frequency (Hz) of clock input to CLK0 pin
N: Multiplication factor determined by pins MODE2 to MODE0

Flow of Data Used in Video Window: The YCbCr data captured from pins VIN0 to VIN7 undergoes the transitions shown in the figure below and is converted to RGB data. In order to make these data transitions, the setting in 1 or 2 below must be made.

1. When RGB = 1, set VWRY = 0
2. When RGB = 0, set VWRY = 1



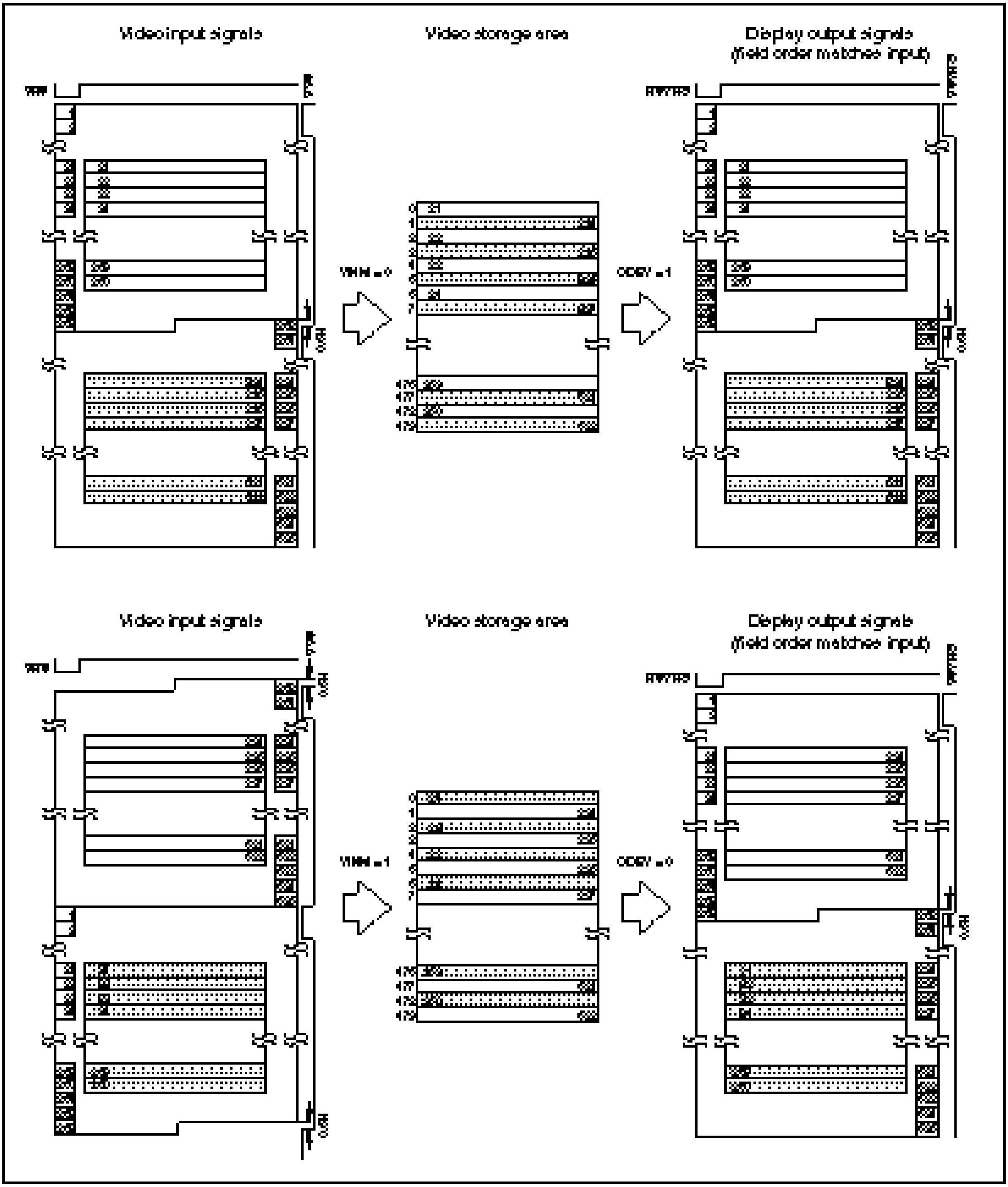


Figure 3.18 Interlace Video Input Field Handling Specification

$\overline{\text{CSYNC}}$ Generation Method: When performing display is master mode, the Q2SD outputs a composite sync signal. The signal waveform is based on the fall of $\overline{\text{VSYNC}}$. The low-level width of equalizing pulses and separation pulses can be set in the equalizing pulse width register (EQWR) and the separation pulse width register (SPWR), respectively.

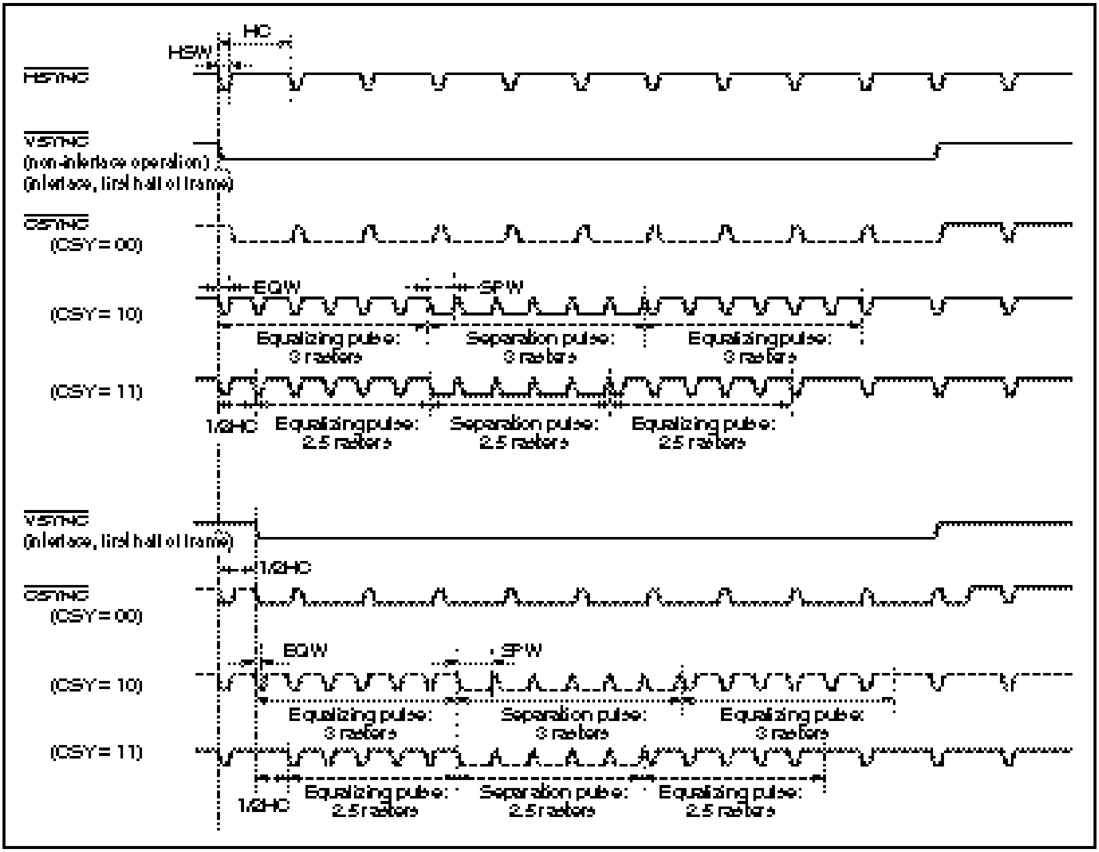


Figure 3.19 $\overline{\text{CSYNC}}$ Output Waveform

Section 4 Display List

4.1 Overview

The Q2SD performs drawing on the basis of a group of drawing commands located in the UGM. This group of drawing commands is called a display list. Drawing commands comprise four-vertex surface drawing and line drawing commands which draw at rendering coordinates, and work surface drawing and work line drawing commands which draw at work coordinates. There are also parameter register setting, sequence control, and drawing end commands.

Line drawing, trapezoid fill, and current pointer setting commands include absolute coordinate and relative coordinate specification commands.

Table 4.1 lists the drawing commands.

Table 4.1 Drawing Commands

Type	Command Name	Function
Four-vertex surface drawing	POLYGON4 Quadrilateral paint	Draws quadrilateral with four coordinates as vertices. Painting can be performed with source tiling and specified color.
	POLYGON4A	Four-vertex surface drawing with multi-valued source as transfer source
	POLYGON4B	Four-vertex surface drawing with binary source as transfer source
	POLYGON4C	Four-vertex surface drawing using specified color
Line drawing	LINE Polygonal line	Draws solid polygonal line from start coordinates through nodal coordinates.
	LINE	Polygonal line drawing (absolute coordinate specification)
	RLINE	Polygonal line drawing (relative coordinate specification)
	PLINE Polygonal line with line-type specification	Draws polygonal line with line type (pattern) from start coordinates through nodal coordinates.
	PLINE	Pattern-reference polygonal line drawing (absolute coordinate specification)
	RPLINE	Pattern-reference polygonal line drawing (relative coordinate specification)

Table 4.1 Drawing Commands (cont)

Type	Command Name		Function
Work surface drawing	FTRAP Trapezoid paint		Performs binary EOR painting of trapezoid with left side parallel to Y-axis.
		FTRAP	Binary EOR trapezoid fill (absolute coordinate specification)
		RFTRAP	Binary EOR trapezoid fill (relative coordinate specification)
	CLRW Rectangle zero-clear		Performs zero-painting of rectangle with diagonal designated by two coordinate points.
Work line drawing	LINEW Polygonal line		Draws solid polygonal line from start coordinates through nodal coordinates.
		LINEW	Binary polygonal line drawing (absolute coordinate specification)
		RLINEW	Binary polygonal line drawing (relative coordinate specification)
Register setting	MOVE		Current pointer setting (absolute coordinate specification)
	RMOVE		Current pointer setting (relative coordinate specification)
	LCOFS		Local offset value setting (absolute coordinate specification)
	RLCOFS		Local offset value setting (relative coordinate specification)
	SCLIP		Sets rectangle with diagonal designated by origin and specified coordinate point as clipping area.
	UCLIP		Sets rectangle with diagonal designated by two coordinate points as clipping area.
	WPR		Sets a specific address-mapped register.
Sequence control	JUMP		Command sequence jump (branch)
	GOSUB		Subroutine call (branch)
	RET		Subroutine return
	NOP3		No operation: no processing executed.
	VBKEM		Waits until vertical retrace line interval.
Drawing end	TRAP		Ends drawing processing and generates CPU interrupt.

The following items (basic functions) are available for drawing command parameter specifications. The items that can be specified depend on the command.

- Rendering coordinate system

  The position of all coordinate system origins, excluding binary source coordinates, can be assigned to the pixel position at which x = 0 and y is a multiple of 128, counting from the start of the unified graphics memory (UGM) in pixel units.

¾ Rendering coordinates (2-dimensional coordinate system)

These are the coordinates at which the Q2SD performs drawing. As the size for drawing in the UGM, a 512-pixel × 512-pixel or 1024-pixel × 512-pixel coordinate system can be selected according to the size of the UGM.

¾ Multi-valued source coordinates (2-dimensional coordinate system)

These are the coordinates for natural image and other color map data. A maximum of 1024 × 1024 size positive coordinates can be used. The size of the coordinates that can be used is determined by the size of the UGM. Also, the maximum number of colors that can be handled with multi-valued source coordinates is normally the same as for rendering coordinates. Multi-valued source coordinates can be superimposed on rendering coordinates.

¾ Work coordinates (2-dimensional coordinate system)

These are the coordinates for managing graphics used when rendering attribute work specification is performed. Work coordinates are managed by the Q2SD so that there is a one-to-one correspondence for each rendering coordinate pixel. Clipping processing is also handled in the same way as for rendering coordinates.

¾ Binary source coordinates (1-dimensional coordinate system)

These are coordinates for storing character patterns and line patterns. Character patterns and line patterns are stored in order from any address in the UGM, and pattern sizes are managed with a 2-dimensional coordinate system using command parameters TDX and TDY.

· Rendering reference data

¾ In drawing that references the transfer source, the referenced data format may be multi-valued source data or binary source data, defined as individual multi-valued source coordinates and binary source coordinates.

¾ In drawing that does not reference the transfer source, specified color data may be referenced.

¾ With a POLYGON4 type command, work data may be referenced.

· Rendering attributes

¾ Twelve kinds of attribute specifications can be made: work (WORK), clipping (CLIP), transparent (TRNS), source style (STYL), net drawing (NET), source half (HALF), even/odd select (EOS), bold line drawing (FWUL, W2UL, FWDR, W2DR), source linear address (LNi), 4-pixel-unit processing (FST), source coordinate relative address (REL), and edge (EDG). The attributes that can be specified depend on the command.

4.2 Command Fetching

The Q2SD carries out drawing operations while performing fetches from the display list stored in the UGM. The display list consist of a number of linked Q2SD drawing commands.

The Q2SD performs sequential fetches in low-to-high address order, starting at the address set in the display list start address register (DLSAR). The fetch address can be changed midway, using a JUMP or GOSUB command. Q2SD fetching can be terminated by placing a TRAP command at the end of the display list.

The Q2SD has a dedicated command buffer, and an equivalent area of the UGM is accessed at one time. When processing of the commands in this buffer is completed, another command fetch is performed.

If the commands include a JUMP, GOSUB, or other command that changes the flow, the Q2SD starts fetching again from the new address indicated by that command.

Figure 4.1 shows an example of the display list.

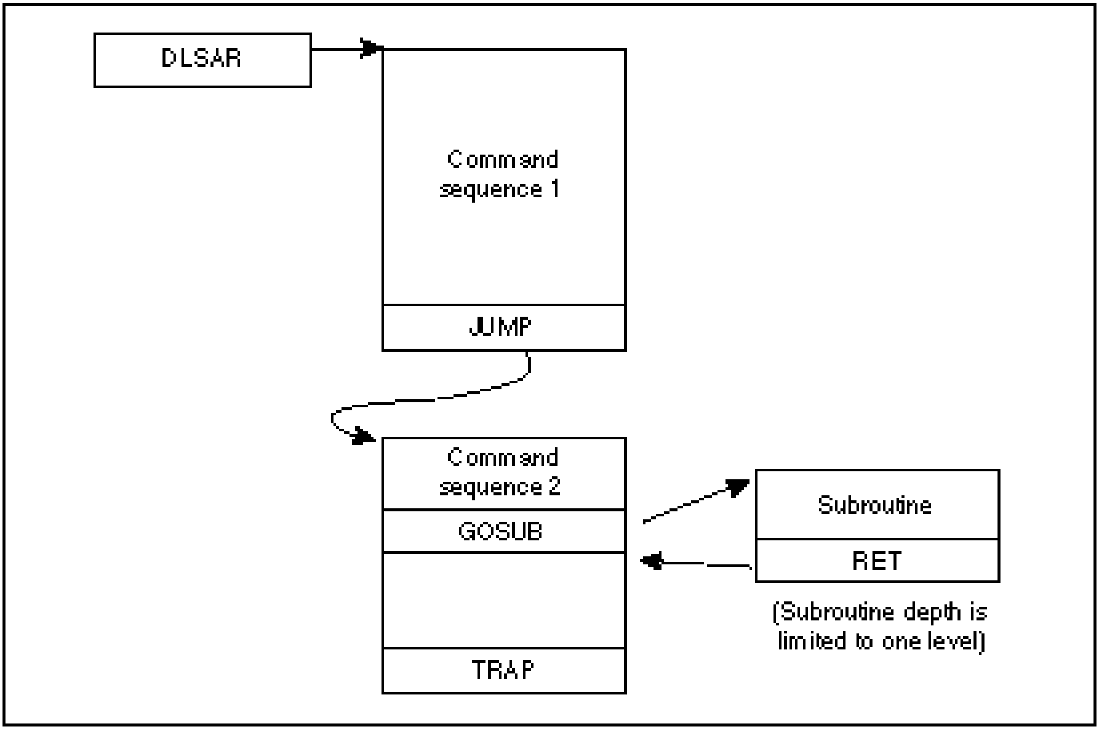


Figure 4.1 Example of Display List

The Q2SD is provided with a drawing suspension facility to support execution control. This allows prioritized parallel execution of a number of drawing processes. An outline of the operation of this facility is given below.

Suspension Processing:

1. Set BRCL to 1 in the status clear register (SRCR), clear the BRK bit to 0 in the status register (SR), and set the drawing suspension directive bit (Rendering Break: RBRK) to 1 in the system control register (SYSR).
2. Next, monitor the BRK bit and TRA bit.
3. When BRK is observed to be set to 1, this means that the currently executing drawing command processing has ended and the drawing unit has halted (drawing has been suspended) at the point at which the next drawing command was fetched. Information required for software processing in anticipation of resumption processing should be read from the address-mapped registers and saved in memory. At this time, the RBRK bit is cleared to 0.

   When TRA is observed to be set to 1, this means that a TRAP command has been executed and Q2SD drawing processing has ended. Therefore, ensure that no subsequent resumption processing is carried out. If drawing is to be performed after suspension processing, wait until the TRA flag is observed to be set to 1.

Resumption Processing:

1. The parameters saved immediately after suspension are restored. Some are written directly to the registers, and some are set by command. The former include the subroutine return address (which can also be set with the WPR command), and the latter, clip area, local offset, current pointer, and execution restart addresses. Of the latter, the execution restart address is restored by setting the command status register value at the time of the suspension as the jump destination of a JUMP command. For the other parameters in the latter group, settings should be made to provide for recovery by means of the appropriate command before execution of this JUMP command.
2. After performing a write for the purpose of subroutine return address restoration, and creating a command list to restore the other parameters, drawing can be resumed by setting the address of this command list in DLSAR and implementing a rendering start.

4.3 Basic Functions

4.3.1 Rendering Coordinate Systems

The Q2SD controls three 2-dimensional coordinate systems, for rendering coordinates, 8-bit/pixel or 16-bit/pixel (multi-valued) source coordinates, and work coordinates, and one 1-dimensional coordinate system, for 1-bit/pixel (binary) source coordinates.

Rendering Coordinates: This is the coordinate system used for drawing processing; it has a fixed size as shown in figure 4.2. The correspondence to the frame buffers is also fixed, but depends on the installed memory capacity and screen size. Make the appropriate selection with the mode selection register. In an area other than one containing a frame buffer, although drawing operations are performed, nothing is written. The bit configuration of these coordinates is the drawing bit configuration indicated by the combination of the graphic bit mode 2 to 0 bits (GBM2 to GBM0) in the rendering mode register (REMR). When drawing is performed using the LCOFS command, coordinates after addition of offset values XO and YO set by the LCOFS command must be within the range shown in the following expressions.

(When bold line attribute is specified)

$$-2045 \le X + XO \le 2044$$
$$-2045 \le Y + YO \le 2044$$

(When bold line attribute is not specified)

$$-2048 \le X + XO \le 2047$$
$$-2048 \le Y + YO \le 2047$$

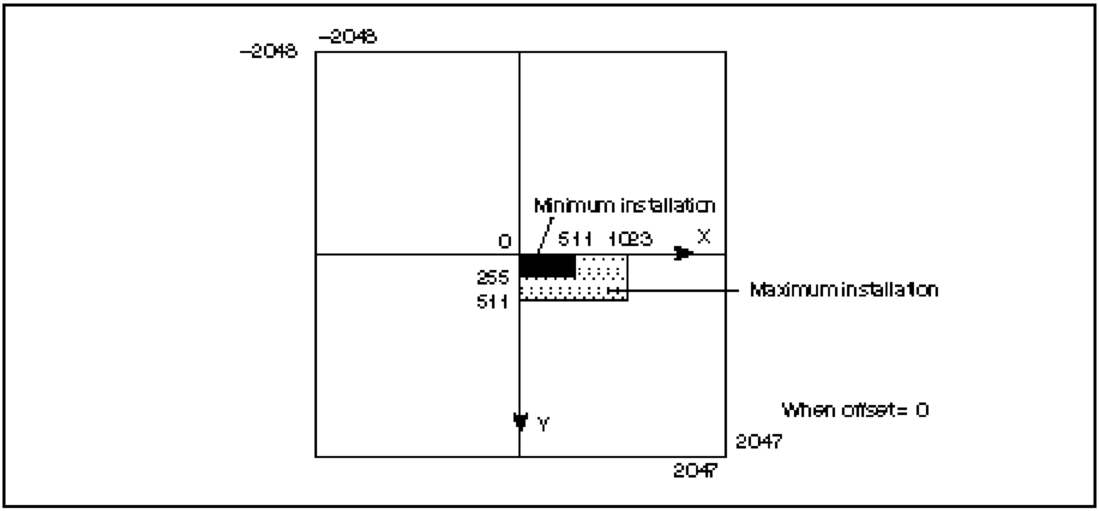


Figure 4.2 Rendering Coordinates

Multi-Valued Source Coordinates: The Q2SD can use two kinds of multi-valued source coordinates according to the value of linear attribute LNi. When LNi = 0, the coordinate origin is specified by the multi-valued source area start address. Figure 4.3 shows the multi-valued source coordinates when LNi = 0. As shown in this figure, the maximum coordinate system size is represented by 1024 × 1024 positive coordinates, but the size depends on the installed memory capacity, screen size, and multi-valued source area start address. Depending on the multi-valued source start address, this coordinate system may entirely or partially overlap another coordinate system.

When LNi = 0, multi-valued source coordinates are configured based on the memory unit shown in section 3.2.3, Memory Map.

When LNi = 1, it is possible to use multi-valued source arranged in linear fashion in the UGM. The size of the multi-valued source in this case is determined by the TDX and TDY parameters of the POLYGON4A command. Figure 4.4 shows the multi-valued source coordinates when LNi = 1. When this coordinate system is used, address conversion must be carried out as shown in the figures 3.4 (d) and (e) in section 3.2.3, Memory Map.

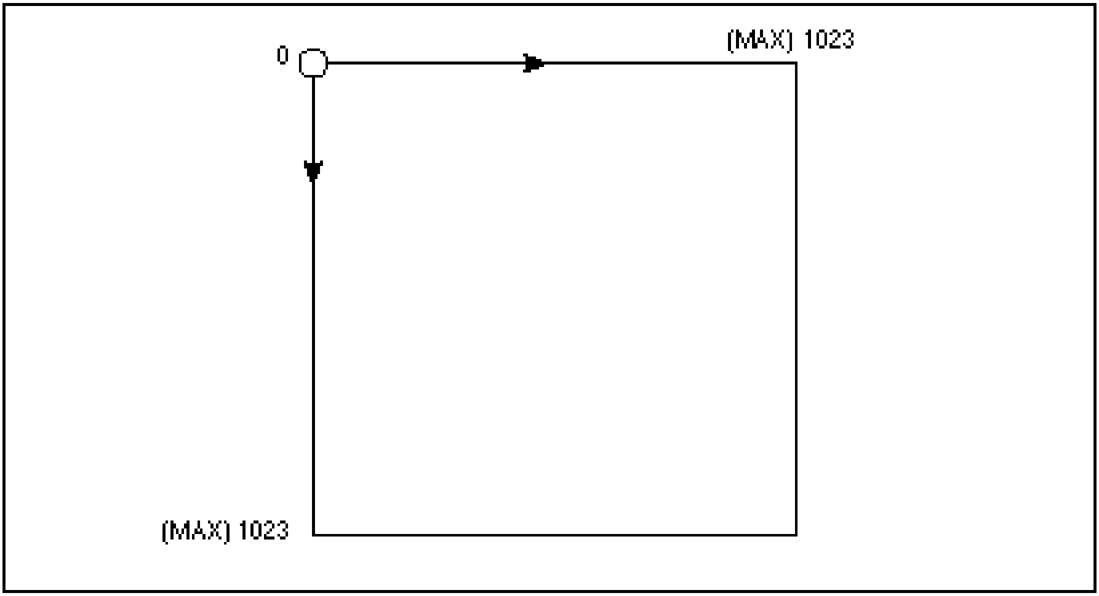


Figure 4.3 Multi-Valued Source Coordinates (LNi = 0)

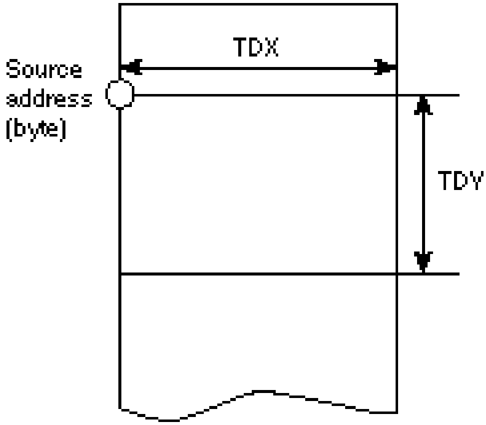


Figure 4.4 Multi-Valued Source Coordinates with LNi = 1 Specified (Linear Address)

Binary Source Coordinates: The binary (1-bit/pixel) source coordinate system is mapped directly onto 1-dimensional memory space. Any area and location can be used, and can be intermixed with the display list space. However, the start address of a source figure is always a byte address. The size of the figure is specified by POLYGON4B command parameters TDX and TDY.

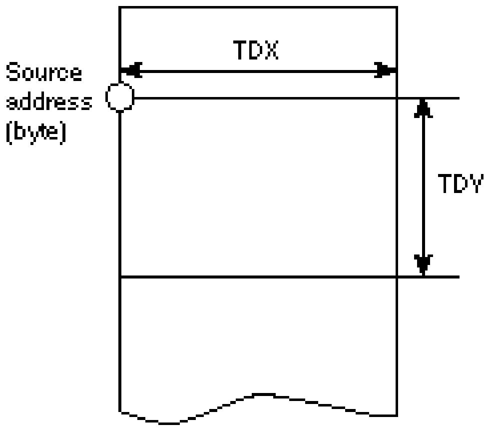


Figure 4.5 Binary Source Coordinates

Binary Work Coordinate System: The work coordinate system corresponds on a one-to-one basis to the rendering coordinate system, as shown in figure 4.6. Therefore, clipping is also handled in the same way as for the rendering coordinate system.

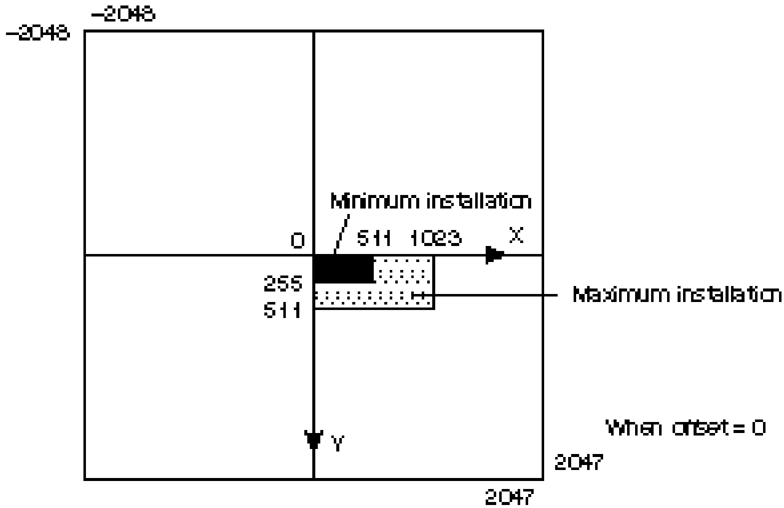


Figure 4.6 Work Coordinate System

Relationship between Binary Work Coordinates and Addresses: Work coordinates are linear coordinates that start from the work area start address. Work coordinates comprise 2-dimensional coordinates reflected at each pixel (512 or 1024 pixels) specified by the MWX bit in the rendering mode register (REMR).

The memory capacity required for the binary work area is (the number of pixels specified by the MWX bit) × (SCLIP command YMAX + 1)/8 [bytes]. In general, one less than the number of display lines in the vertical direction should be set as YMAX in the SCLIP command.

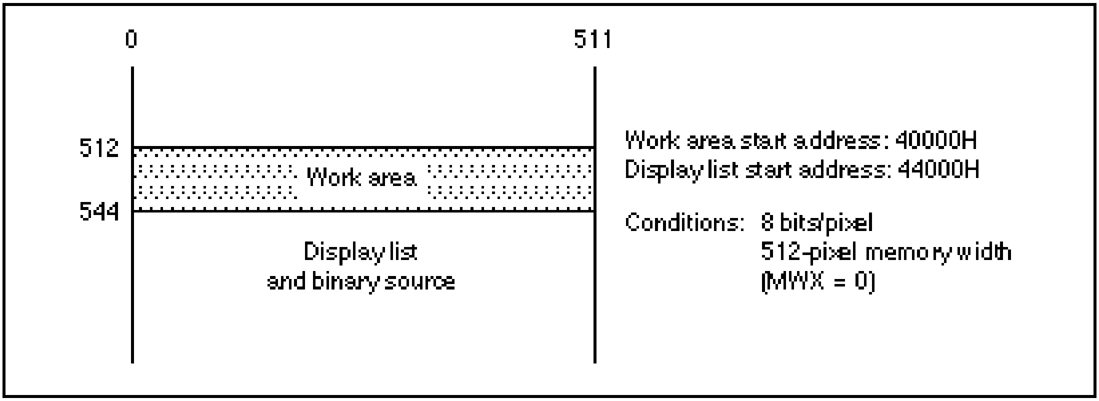


Figure 4.7 Example of Relationship between Work Coordinates and Physical Addresses

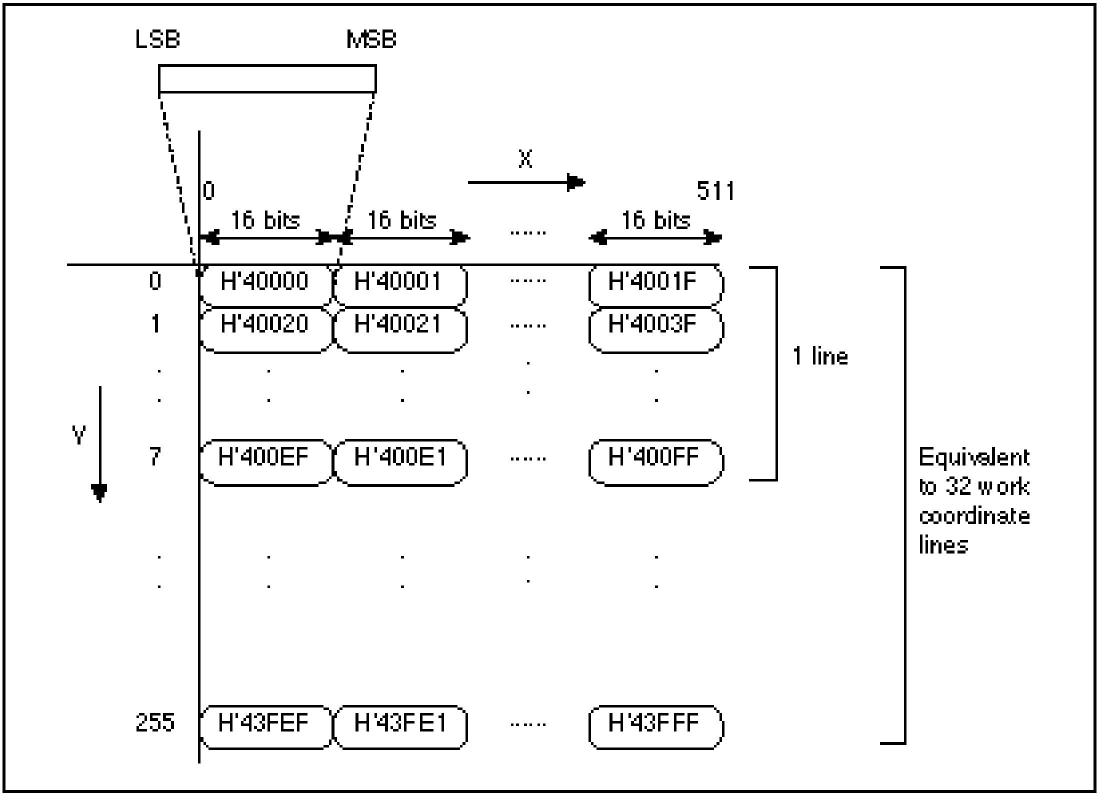


Figure 4.8 Relationship between Work Coordinates and Addresses

4.3.2 Source Data

Q2SD drawing operations can be broadly divided into those that reference the source data and those that do not. Drawing commands that reference the source data are POLYGON4A, POLYGON4B, PLINE, and RPLINE. Drawing commands that do not reference the source data are POLYGON4C, LINE, RLINE, FTRAP, RFTRAP, CLRW, LINEW, and RLINEW.

With drawing operations that reference the source data, there are two reference data formats: multi-valued source data and binary source data.

Of the commands that do not reference source data, POLYGON4C, LINE, RLINE, LINEW, and RLINEW reference the specified color data belonging to the command.

With POLYGON4 commands, it is possible to reference a combination of multi-valued source data and binary source data, binary source data and binary work data, or specified color data and binary work data (see figure 4.9).

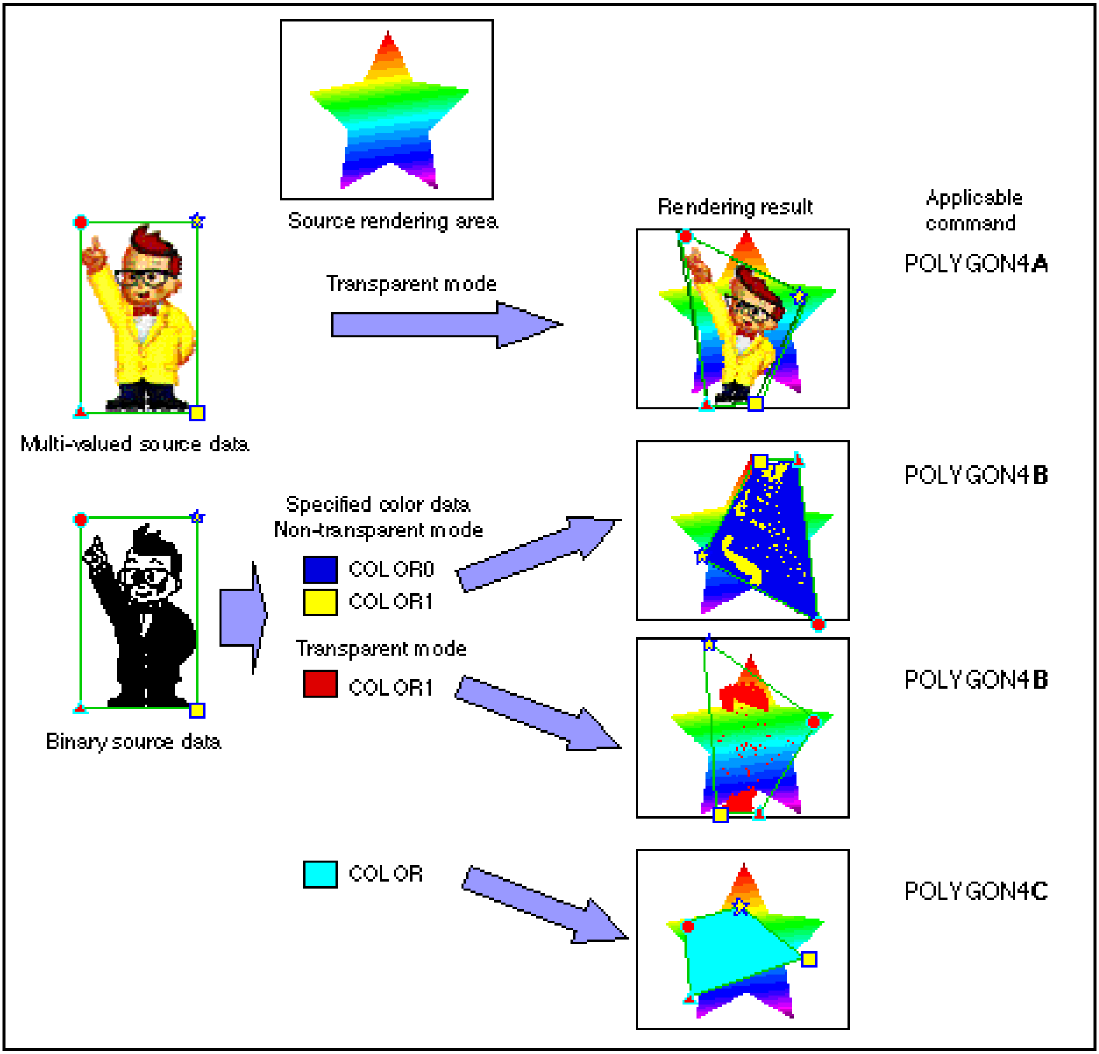


Figure 4.9 Example of POLYGON4 Transfer Data Combinations

Multi-Valued Source Data: Multi-valued source data is defined as multi-valued source coordinates (2-dimensional coordinates).

However, the horizontal width (TDX) is specified as a value of 8 pixels or more. The configuration of multi-valued source data is shown in figure 4.10.

A linear arrangement (LNi = 1) is also possible, in which case a multiple of 8 pixels should be set as the TDX value.

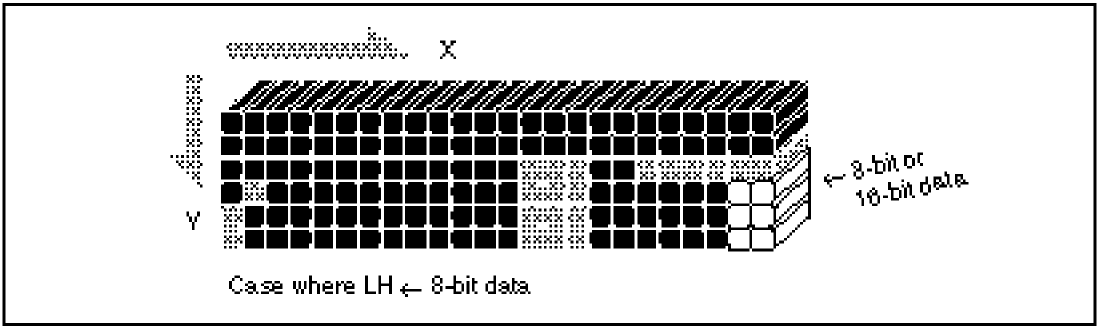


Figure 4.10 Multi-Valued Source Data Configuration

Binary Source Data: Binary source data is arranged in linear fashion in the binary source area in the UGM, and is managed as 2-dimensional coordinates (binary source coordinates) by TDX and TDY in the POLYGON4B command. The left-hand screen pixel must be located at the LSB of the binary source data when the binary source data area is viewed from the Q2SD.

However, the horizontal width (TDX) is specified as a multiple of 8 pixels. An example of binary source data is shown in figure 4.11.

A binary source is used for the definition of character data and line-type data. When drawing, 0s are converted to COLOR0 data, and 1s to COLOR1 data (in transparent mode, only 1s are converted to COLOR1 data for drawing).

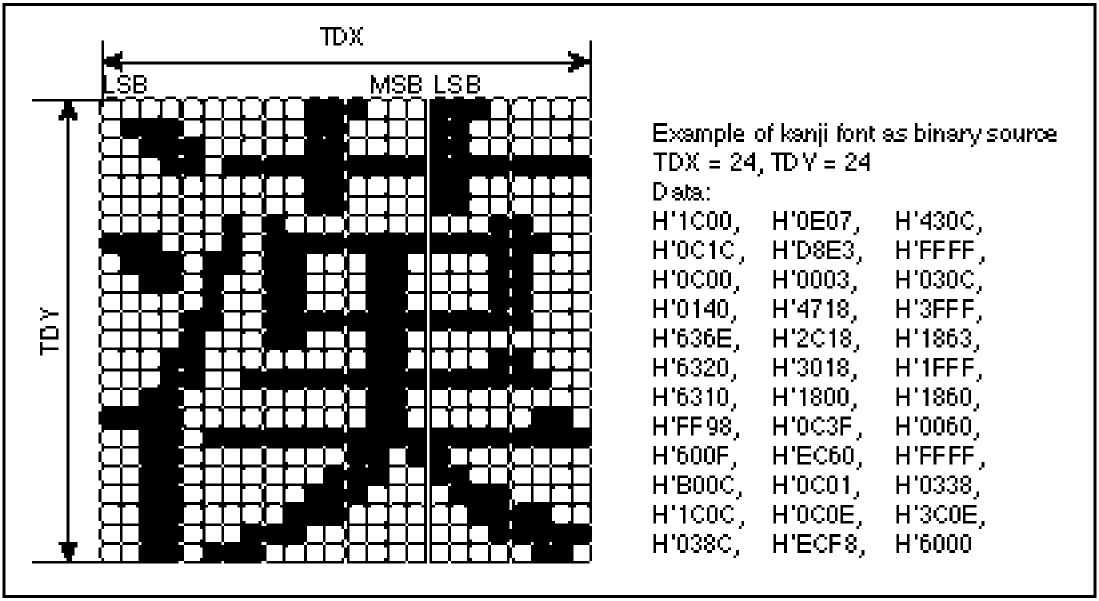


Figure 4.11 Example of Kanji Font as Binary Source (TDX = 24, TDY = 24)

Binary Work Data: Binary work data is defined as work coordinates (2-dimensional coordinates). Work data is used to implement polygon painting. Polygon outline data is created with the FTRAP command, etc., and the created figure data is used to delineate the rendering figure. If, for example, the POLYGON4C command is used jointly for work, the work area polygon can be drawn in the rendering area with the specified color value. The configuration of binary work data is shown in figure 4.12.

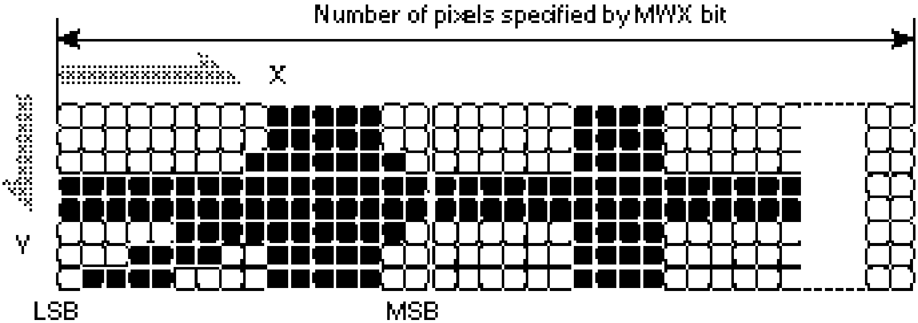


Figure 4.12 Binary Work Data Configuration

Specified Color Data: Specified color data is defined directly by drawing parameter color specifications (COLOR, COLOR0, COLOR1, LINE COLOR0, and LINE COLOR1). When the Q2SD is used for 8-bit/pixel operation, the same color palette number is defined in the upper 8 bits and lower 8 bits in the drawing parameter color specification. When the Q2SD is used for 16-bit/pixel operation, the R, G, and B values are defined directly by the drawing parameter color specification.

However, with LINEW and RLINEW, the value to be drawn at work coordinates is defined by the rendering attribute EOS bit.

Q2SD Internal Buffers: The Q2SD has three internal buffers—a command buffer, source buffer, and work buffer—as shown in figure 4.13.

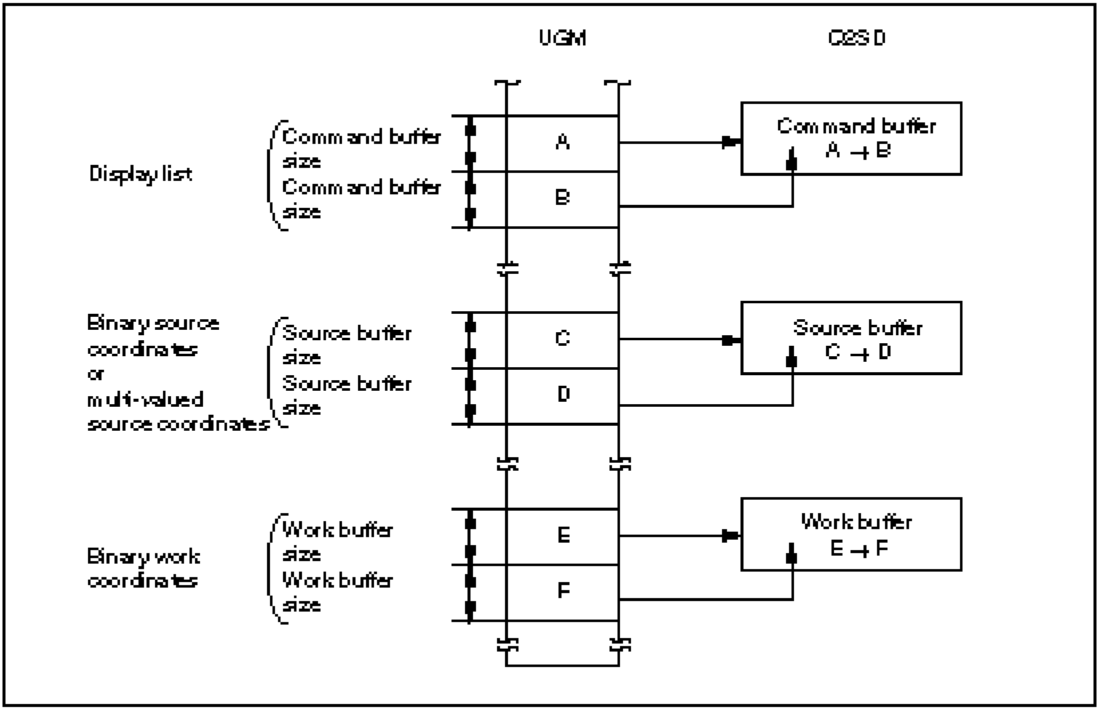


Figure 4.13 Updating of Q2SD's Internal Buffers

These buffers are used by the Q2SD to temporarily store data held in the UGM. The Q2SD uses the data stored in these buffers when executing drawing. The functions of these buffers are as follows:

1. Command buffer (32 bytes × 2)

   Used by the Q2SD to store a display list held in the UGM. The buffer size is 64 bytes.

2. Source buffer (32 bytes × 2)

   Used by the Q2SD to store a binary source or multi-valued source held in the UGM. The buffer size is 64 bytes.

3. Work buffer (16 bytes)

   Used by the Q2SD when performing drawing at binary work coordinates in the UGM. The buffer size is 16 bytes.

When buffer contents are not updated, (when the same address is referenced by data of or below the capacity of the buffer, or a reference ends at a location at or below the capacity of the buffer from the previous reference start location), the previous buffer contents will be used even though the data in the UGM is rewritten. To intentionally update buffer contents, the address of a location exceeding the buffer capacity should be referenced.

4.3.3 Rendering Attributes

With the Q2SD, 12 rendering attributes can be specified. The rendering attributes are embedded in the commands, and can be specified on an individual command basis. Figure 4.14 shows the bit arrangement for rendering attributes.

Bits 15–11	Bits 10–0
CODE	DRAW MODE

Command	10	9	8	7	6	5	4	3	2	1	0
POLYGON4A		TRNS	STYL	CLIP	0	NET	EOS	FST	LNI	COOF	WORK
POLYGON4A		TRNS	STYL	CLIP	REL	NET	EOS	0	1	COOF	WORK
POLYGON4B		TRNS	STYL	CLIP	REL	NET	EOS			0	WORK
POLYGON4B		TRNS	0	CLIP	REL	NET	EOS			HALF	WORK
POLYGON4C				CLIP		NET	EOS	FST			WORK
FTRAP, RFTRAP				CLIP			EOS	EDG			
LINEW, RLINEW				CLIP			EOS				
LINE, RLINE				CLIP		NET	EOS	FWUL	W2UL	FWDR	W2DR
PLINE, RPLINE		TRNS	1	CLIP		NET	EOS	EDG2		EDG1	1
JUMP, GOSUB					REL						
CLRW				CLIP							
(Commands other than the above)											

Note: Shaded areas should be cleared to 0.
FWUL, W2UL, FWDR, W2DR: Bold line drawing bits
REL: Relative address specification
EDG: Edge drawing bit

Figure 4.14 Rendering Attribute Bit Arrangement

Transparency Specification (TRNS): When color expansion of binary source data is performed, transparency or non-transparency can be selected on an individual drawing command basis with the TRNS bit. When transparency is selected, a 0 in the binary source data is transparent and a 1 has the value of the COLOR1 parameter. When non-transparency is selected, a binary data 0 has the value of the COLOR0 parameter, and a 1 has the value of the COLOR1 parameter. With multi-valued source data, all-0 data becomes a transparent color, and those pixels are not drawn. The transparency specification can be used with the POLYGON4A, POLYGON4B, PLINE, and RPLINE commands; in other commands, the TRNS bit should be cleared to 0.

Source Style Specification (STYL): When drawing a rectangle, the STYL bit can be used to select, on an individual drawing command basis, whether the source data is to be enlarged or reduced, or referenced repeatedly. If no style specification is made, the source data is enlarged or reduced in proportion to the size of the rendering area. When a style specification is made, the source data is referenced repeatedly in proportion to the size of the rendering area. This attribute is therefore used when drawing repeated patterns such as hatch patterns. The source style specification can be used with the POLYGON4A, POLYGON4B, PLINE, and RPLINE commands; in other commands, the STYL bit should be cleared to 0. When a source style specification is used, do not make a source half specification.

An example of a source style specification is shown in figure 4.15.

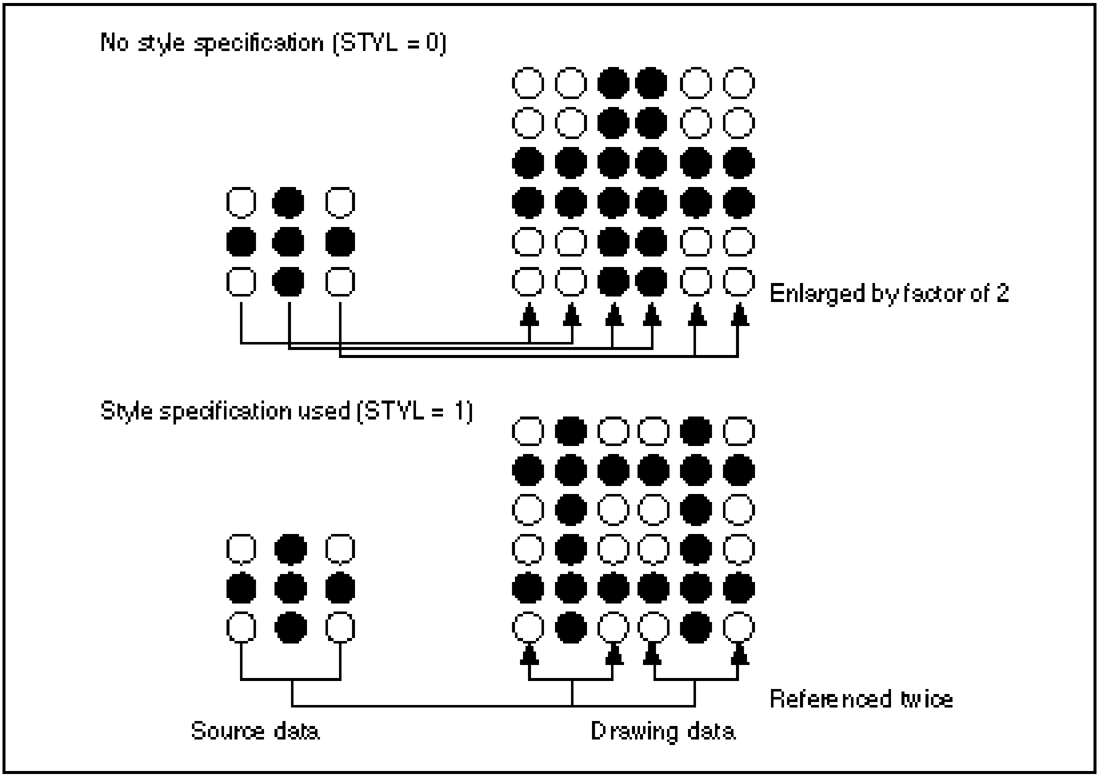


Figure 4.15 Example of Source Style Specification

Clipping Specification (CLIP): The Q2SD can perform clipping area management. There are two kinds of clipping area: a system clipping area designated by the SCLIP command, and a user clipping area designated by the UCLIP command.

The system clipping area has a fixed drawing range. The system clipping area is always valid, regardless of attribute specifications.

A user clipping area can be designated as desired within the system clipping area. Whether or not clipping is performed in that area can be selected on an individual command basis with the rendering attribute CLIP bit. The boundary is drawn.

Clipping is set with screen coordinates.

An example of a clipping specification is shown in figure 4.16.

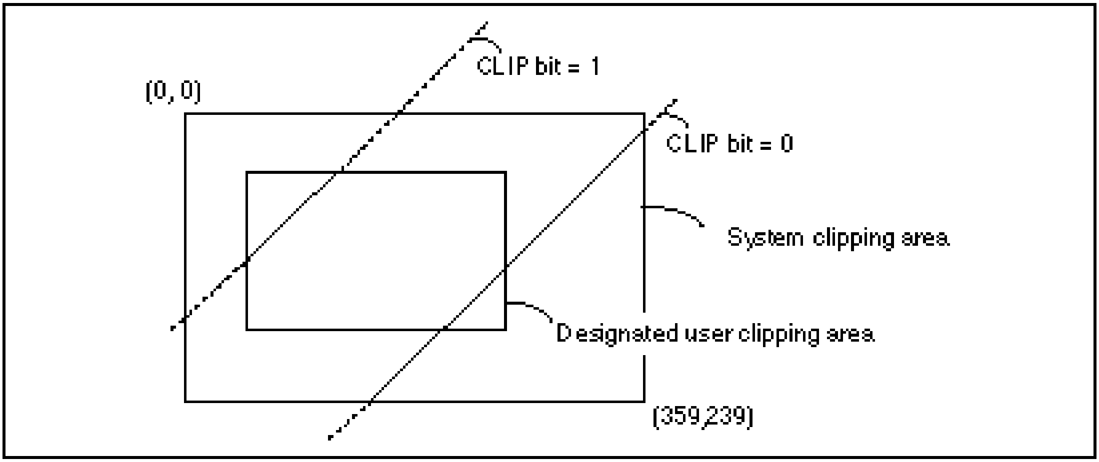


Figure 4.16 Example of Clipping Specification
[Specified system clipping area is (0, 0) to (359, 239)]

Net Drawing Specification (NET): The NET bit can be used to select, on an individual drawing command basis, whether or not net drawing is to be performed. Net drawing is a function for drawing only pixels at coordinates for which the condition “rendering coordinates X + Y = EOS (0: even number, 1: odd number)” is true. For example, if EOS = 0, drawing will only be performed at coordinates Y = 0, X = 0, 2, 4, 6, 8, ..., Y = 1, X = 1, 3, 5, 7, 9, ...

This function enables the drawn figure and ground to be mutually semi-superimposed.

The net drawing specification can be used with the POLYGON4 commands, and the LINE, RLINE, PLINE, and RPLINE commands; in other commands, the NET bit should be cleared to 0.

Even/Odd Select Specification (EOS): Even pixels are selected when EOS = 0, and odd pixels when EOS = 1.

The even/odd select specification is used together with the net specification or source half specification.

With the LINEW and RLINEW commands, drawing is performed at the work coordinates with 0 when EOS = 0, and with 1 when EOS = 1.

Examples of even/odd select specifications are shown in figure 4.17.

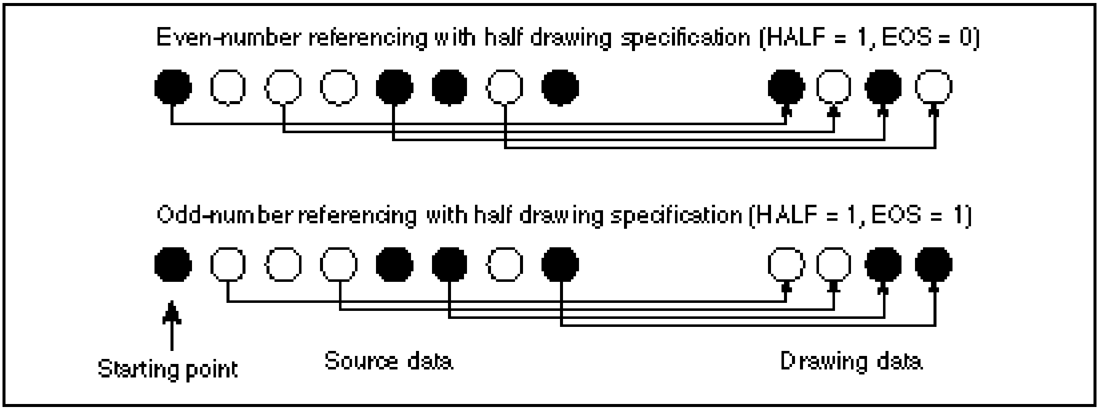


Figure 4.17 Examples of Even/Odd Select Specifications

Source Half Drawing Specification (HALF): The HALF bit can be used to select whether all or only half of the source data is to be referenced. When the source half drawing specification is selected, only EOS (0: even number, 1: odd number) data is referenced from the source starting point. Thus only half of the source data in the horizontal direction is referenced.

The source half drawing specification can only be used with the POLYGON4B (binary source) command; in other commands, the HALF bit should be cleared to 0. When a source half specification is used, do not make a source style specification.

Work Specification (WORK): When drawing is performed at rendering coordinates with POLYGON4 commands, the WORK bit can be used to select, on an individual drawing command basis, whether or not binary work data is to be referenced.

When binary work data referencing is selected, drawing is performed if the work data for the pixel corresponding to the rendering coordinates is 1, but not if the work data is 0. The same shape as that drawn at work coordinates can thus be drawn at rendering coordinates. Drawing at work coordinates can be performed either by means of the FTRAP command or else by the SuperH. Ensure that UGM drawing access by command and UGM drawing access by the SuperH are not performed simultaneously. The work specification can be used with the POLYGON4A, POLYGON4B, and POLYGON4C commands; in other commands, the WORK bit should be cleared to 0.

With the PLINE and RPLINE commands, this attribute is specified but work references are not performed.

Bold Line Drawing Specification: Taking individual line segments of a polygonal line specified by parameters as reference lines, this specification makes the reference lines bold lines in the upper-left direction and lower-right direction, independently. Whether or not this attribute is enabled is specified by the FWUL bit and FWDR bit, while the width of a bold lines can be selected from line widths 1 to 5 by a combination of bits W2UL and W2DR. The FWUL bit enables bold-line implementation in the upper-left direction, while the FWDR bit enables bold-line implementation in the lower-right direction. The W2UL bit is valid when FWUL = 1, and the W2DR bit when FWDR = 1.

This function is valid for each segment of a polygonal line. Using the segment line main scanning axes, lines with the same slope in the up (left) and down (right) directions, and of the same length, are drawn repeatedly. Therefore, the shape of the segment linkage parts is not considered. This function can be used with the LINE and RLINE commands; in other commands, the FWUL, W2UL, FWDR, and W2DR bits should all be cleared to 0.

When performing bold line drawing, set the vertex coordinates so that the entire bold line area does not extend beyond the drawing area (both x and y in the range –2045 to 2044).

Table 4.2 Bold Line Drawing Settings

FWUL	W2UL	FWDR	W2DR	Line Width (Direction, Magnification)
0	0	0	0	1 (no magnification)
			1	1 (no magnification)
		1	0	2 (lower right 1)
			1	3 (lower right 2)
	1	0	0	1 (no magnification)
			1	1 (no magnification)
		1	0	2 (lower right 1)
			1	3 (lower right 2)
1	0	0	0	2 (upper left 1)
			1	2 (upper left 1)
		1	0	3 (upper left 1, lower right 1)
			1	4 (upper left 1, lower right 2)
	1	0	0	3 (upper left 2)
			1	3 (upper left 2)
		1	0	4 (upper left 2, lower right 1)
			1	5 (upper left 2, lower right 2)

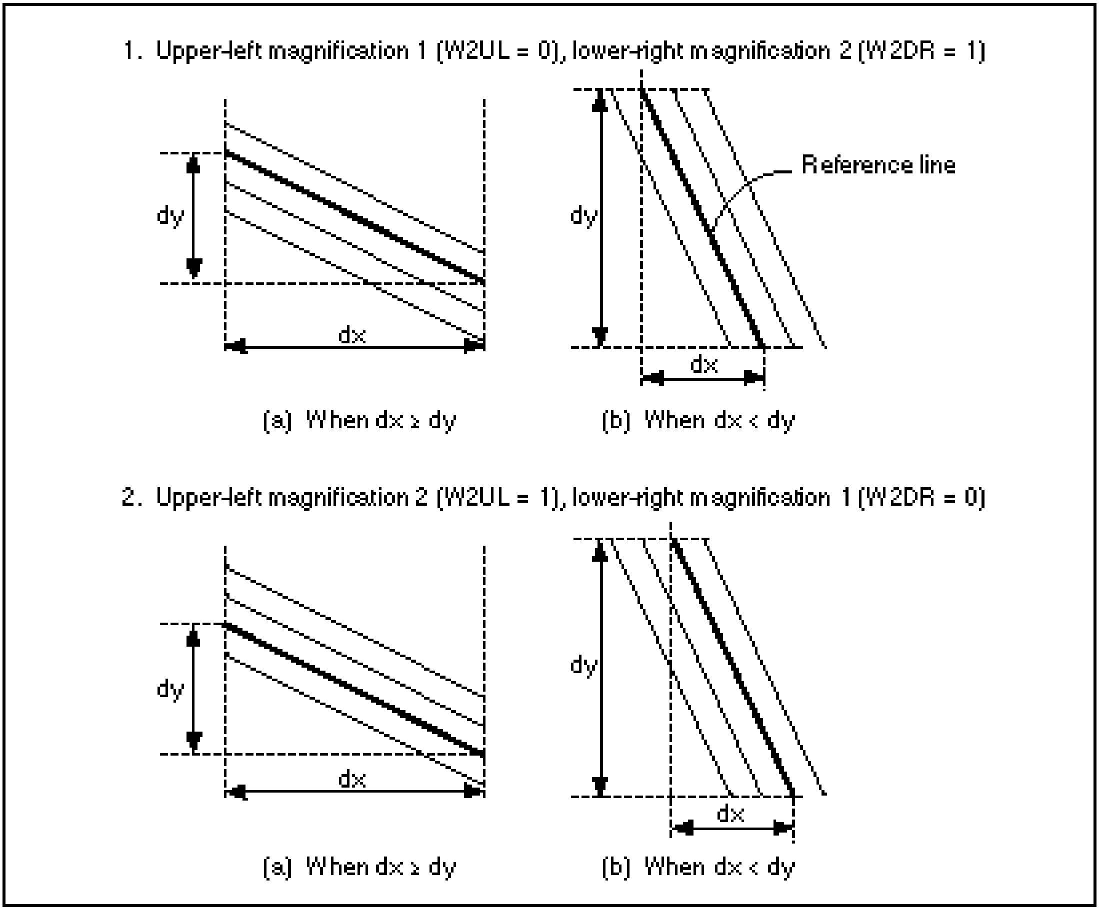


Figure 4.18 Examples of Bold Line Drawing (Line Width 4 Drawing) (FWUL = 1, FWDR = 1)

Source Address Linear Specification (LNi): Use of a 2-dimensional virtual address or a linear address as the source address can be selected, on an individual drawing command basis, by means of the LNi bit. To use a linear address, set this bit to 1.

This function can be used with the POLYGON4A command; in other commands, the LNi bit should be cleared to 0. For details of command operation, see section 4.4.1, POLYGON4A.

4-Pixel-Unit Processing (FST): Whether or not 4-pixel unit processing is performed can be specified for individual drawing commands by means of the FST bit. To perform 4-pixel unit processing, set the FST bit to 1. In this case, no other rendering attributes except CLIP can be used. This function can be used with the POLYGON4A and POLYGON4C commands; in other commands, the FST bit should be cleared to 0.

When using this attribute, set the command parameters as indicated in the individual command descriptions.

Source Coordinate Relative Address Specification (REL): Setting the REL bit to 1 in POLYGON4A, POLYGON4B, JUMP, and GOSUB commands enables source referencing and branching to be performed at an address relative to (before or after) the command code. The source address must be a linear address. Also, for reasons relating to referencing of a multi-valued source arranged in linear fashion, the LNi bit must be set to 1 when using POLYGON4A; operation cannot be guaranteed if the LNi bit is 0.

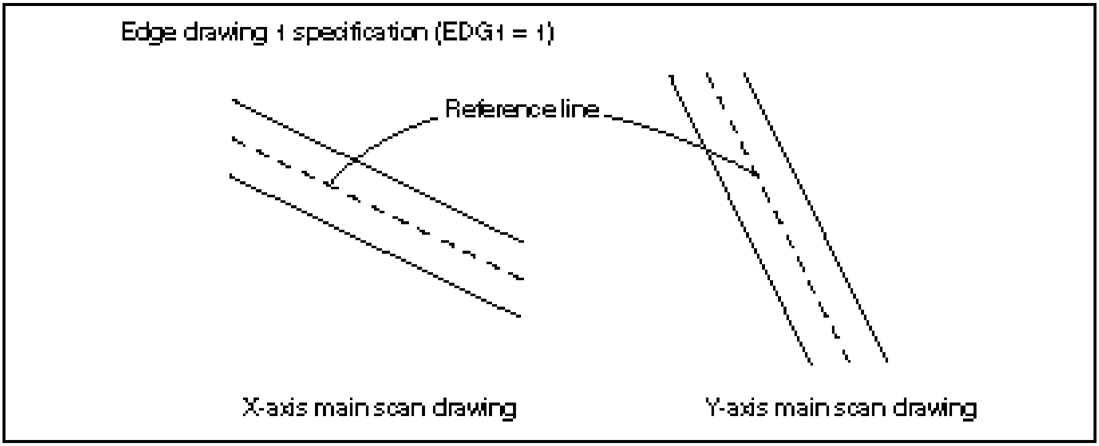
The command code address is the relative address origin.

Edge Drawing (EDG): With the FTRAP and RFTRAP commands, setting the EDG bit to 1 enables edge lines to be drawn after completion of trapezoid painting. Whether edge line drawing is performed with 0 or with 1 is specified by the EOS bit.

Line Drawing Edge Specification (EDG1, EDG2): Whether or not edge drawing is performed for a polygonal line with line type can be specified for individual drawing commands by means of the EDG1 bit.

This function is valid for each segment of a polygonal line. Using the segment line main scanning axes, solid lines with the same slope and of the same length, are drawn either vertically or horizontally. Therefore, the shape of the polygonal line linkage parts is not considered. The solid edge lines have the value of COLOR1.

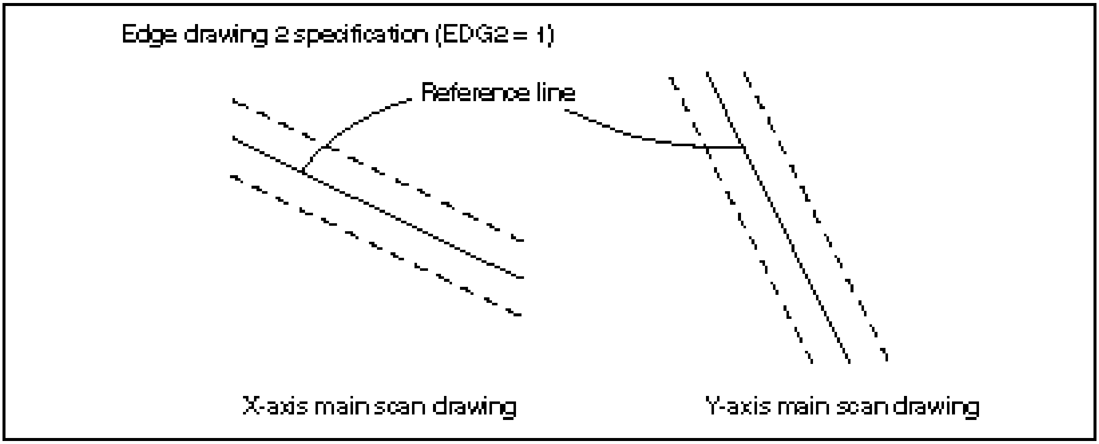
This function can be used with the PLINE and RPLINE commands; in other commands, the EDG1 bit should be cleared to 0. A source size of 8 or 16 can be used. Set 8 or 16 for source size parameter TDX.



Whether or not edge drawing is performed for a polygonal line with line type can be specified for individual drawing commands by means of the EDG2 bit.

This function is valid for each segment of a polygonal line. Here, each segment of the polygonal line specified by the parameter is considered as a reference line. This function is implemented for each segment of a polygonal line, using the following procedure. First, the reference line is drawn as a line with line type. Next, using the segment line main scanning axes, solid lines with the same slope and of the same length, are drawn either vertically or horizontally. Finally, the reference line is drawn as a solid line. Therefore, the shape of the polygonal line linkage parts is not considered. The solid line drawn last has the value of COLOR1.

This function can be used with the PLINE and RPLINE commands; in other commands, the EDG2 bit should be cleared to 0.



Do not set both EDG1 and EDG2 to 1 at the same time.

Color Offset (COOF): This function can be used with the POLYGON4A command. In 16-bit/pixel drawing, if the rendering attribute COOF bit is set to 1, the result of adding the value in the COLOR register to the value of the multi-valued source data is drawn. The operation is performed by saturation processing. In 8-bit/pixel drawing, the COOF bit must be cleared to 0.

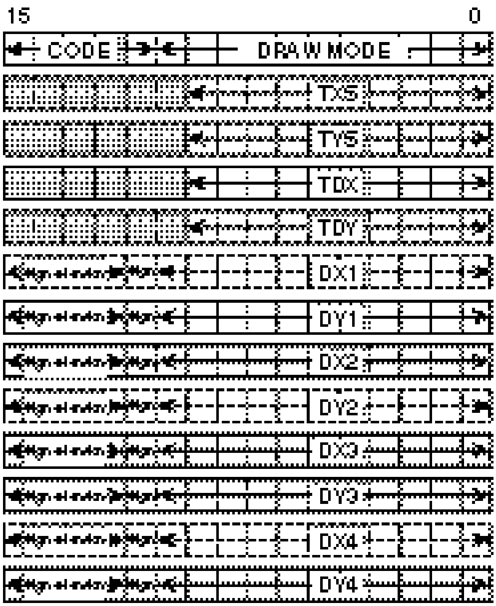
4.4 Drawing Commands

4.4.1 POLYGON4A

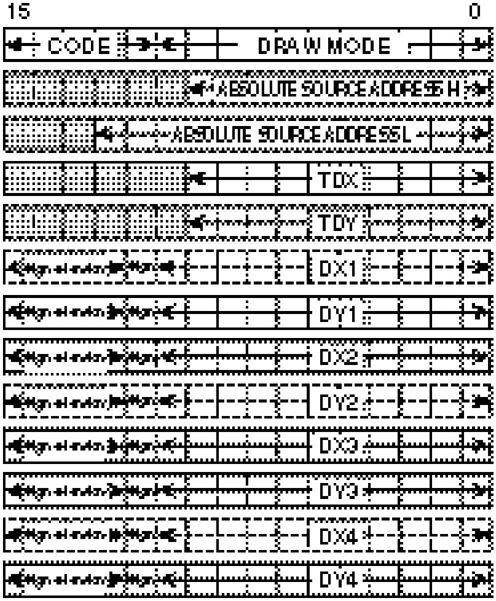
Function

Performs any four-vertex drawing at rendering coordinates while referencing a multi-valued (8- or 16-bit/pixel) source.

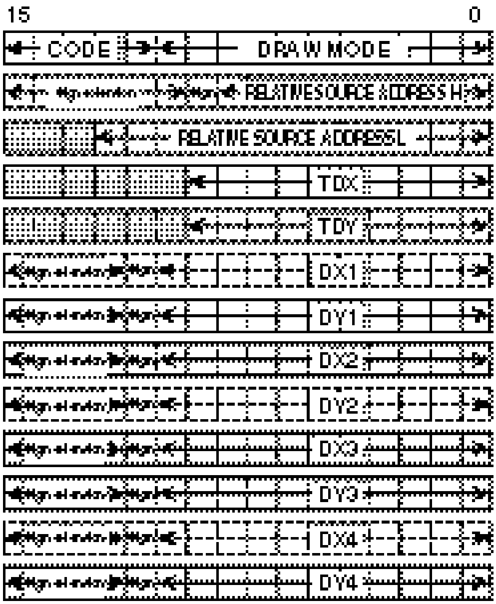
Command Format LNi = 0



LNi = 1, REL = 0



LNi = 1, REL = 1



1. Code

   B'00000

2. Rendering Attributes

Reference Data				Drawing Destination	
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work
O		A		O	

DRAW MODE										
Reserved	TRNS	STYL	CLIP	REL	NET	EOS	FST	LNi	COOF	WORK
Fixed at 0	*	*	O	Z	*	*	O	*	O	*

O: Can be used

V: Can be used (specified color is binary EOS bit value)

A: Referenced depending on mode (valid when WORK = 1)

*: Referenced depending on mode (clear to 0 when FST = 1)

Z: Referenced depending on mode (clear to 0 when LNi = 1)

Blank: Cannot be used (clear to 0)

3. Command Parameters

   TXS, TYS: Source starting point

   ABSOLUTE/RELATIVE SOURCE ADDRESS H: Source start upper address (byte address)

   ABSOLUTE/RELATIVE SOURCE ADDRESS L: Source start lower address (byte address)

   TDX, TDY: Source size

   DXn, DYn (n = 1 to 4): Absolute values, rendering coordinates, negative numbers expressed as two's complement

Description

Transfers multi-valued (8- or 16-bit/pixel) source data to any quadrilateral rendering coordinates. The source is always scanned horizontally, but diagonal scanning may be used in the drawing, depending on the shape. In diagonally-scanned drawing, double-writing occurs to fill in gaps.

When LNi = 1, set a multiple of 8 pixels as the TDX value.

When LNi = 0, set 8 pixels or more as the TDX value.

If the TDX setting is less than 8 pixels, multi-valued source references will not be performed normally.

1. When repeated source referencing is selected as a rendering attribute (STYL = 1), the source is not enlarged or reduced, but is referenced repeatedly.
2. When work referencing is selected as a rendering attribute (WORK = 1), only places where the work coordinate pixel is 1 are drawn at rendering coordinates while referencing work coordinates for the same coordinates as the rendering coordinates.
3. When LNi = 0, make TXS and TYS settings in pixel units.
4. When LNi = 1, the linear address space in the UGM can be used for multi-valued source coordinates. See section 4.3.1 for a description of multi-valued source coordinates.

   When LNi = 1, set the upper bits of the source address in SOURCE ADDRESS H, and the lower bits in SOURCE ADDRESS L. When REL = 0, the source address can be specified as an absolute address. When REL = 1, the source address can be specified as a relative address with respect to the UGM address at which the POLYGON4A command code is located. Absolute addresses and relative addresses must be even numbers. If a relative address is negative, its two's complement should be used.

   In 16-bit/pixel drawing, if the rendering attribute COOF bit is set to 1, the result of adding the value in the COLOR register to the value of the multi-valued source data is drawn. The operation is performed by saturation processing. In 8-bit/pixel drawing, the COOF bit must be cleared to 0.

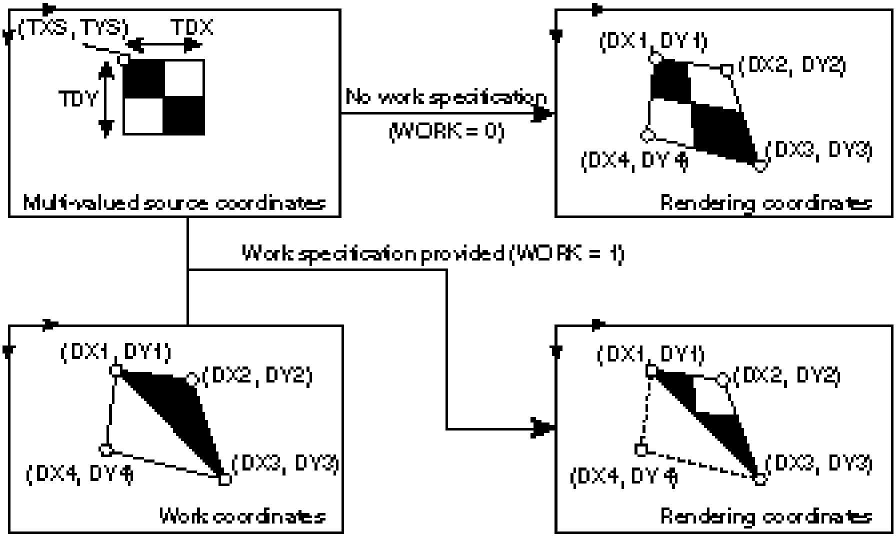
Note on FST Mode

When the register attribute FST bit is set to 1, processing is carried out in 4-pixel units. However, operation will be executed normally only if all the following conditions are satisfied; in other cases, operation cannot be guaranteed. Evaluation of these conditions is not performed internally.

- Make settings so that the source and destination are rectangles of the same size, with DX1 = DX4 = 4j – 4, DX2 = DX3 = 4k – 1, DY1 = DY2, DY3 = DY4, DX2 – DX1 = 32n – 1 (where j, k, and n are natural numbers).
- When FST = 1, no other rendering attributes except CLIP can be used.

- When this command is used with FST = 1, first use the MOVE, RMOVE, LCOFS, or RLCOFS command to change the clipping range and local offset values to the values given in the descriptions of the individual commands.
- Set a multiple of 4 for TXS and TYS.
- Operation is valid in 8-bit/pixel and 16-bit/pixel modes.
- The local offset values set by the LCOFS and RLCOFS commands must be non-negative.

Example

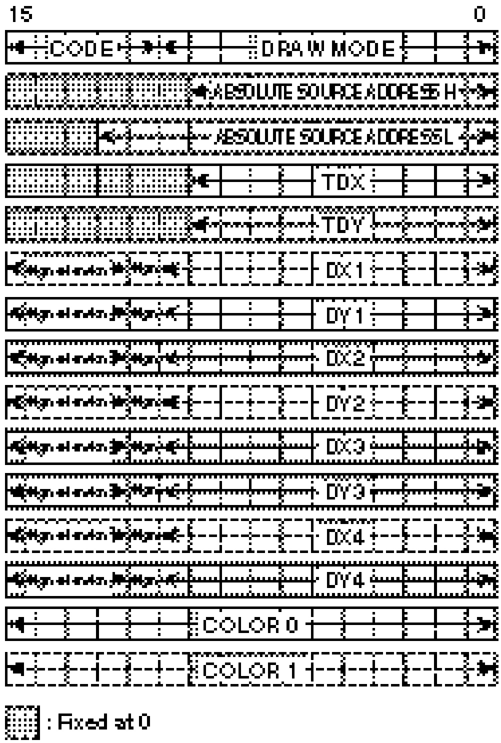


4.4.2 POLYGON4B

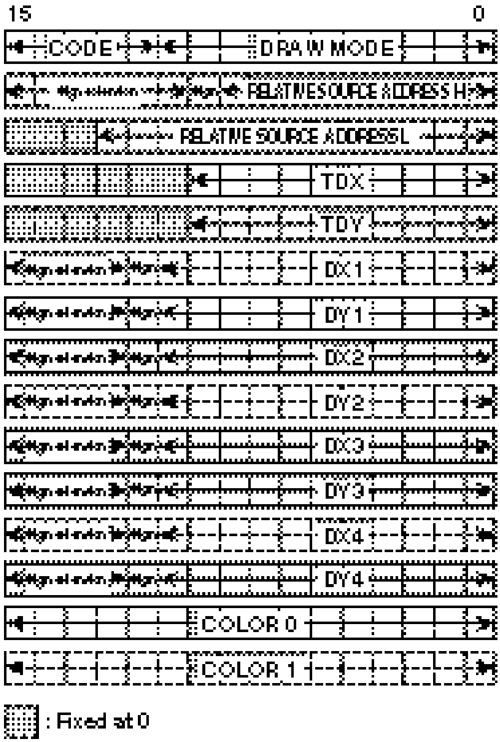
Function

Performs any four-vertex drawing at rendering coordinates while referencing a binary (1-bit/pixel) source.

Command Format REL = 0



REL = 1



15
0
CODE
DRAW MODE
RELATIVE SOURCE ADDRESS H
RELATIVE SOURCE ADDRESS L
TDX
TDY
DX 1
DY 1
DX 2
DY 2
DX 3
DY 3
DX 4
DY 4
COLOR 0
COLOR 1
: Fixed at 0

1. Code

   B'00001

2. Rendering Attributes

Reference Data				Drawing Destination	
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work
	O	A		O	

DRAW MODE										
Reserved	TRNS	STYL	CLIP	REL	NET	EOS	Reserved	Reserved	HALF	WORK
Fixed at 0	O	O*	O	O	O	O	Fixed at 0	Fixed at 0	O*	O

O: Can be used
V: Can be used (specified color is binary EOS bit value)
A: Referenced depending on mode (valid when WORK = 1)
*: Referenced depending on mode (clear to 0 when FST = 1)
Z: Referenced depending on mode (clear to 0 when LNi = 1)
Blank: Cannot be used (clear to 0)

Note: * The STYL bit and HALF bit cannot both be set to 1 at the same time.

3. Command Parameters

   ABSOLUTE/RELATIVE SOURCE ADDRESS H: 1-bit/pixel source start upper address (byte address)

   ABSOLUTE/RELATIVE SOURCE ADDRESS L: 1-bit/pixel source start lower address (byte address)

   TDX, TDY: Source size

   DXn, DYn (n = 1 to 4): Absolute values, rendering coordinates, negative numbers expressed as two's complement

   COLOR0, COLOR1: 8- or 16-bit/pixel color specifications

Description

Draws binary (1-bit/pixel) source data in any quadrilateral rendering area, using the colors specified by parameters COLOR0 and COLOR1. For the COLOR0 and COLOR1 data formats, see section 3.3.3, Color Data Format Input Color Data Configuration. The source is always scanned horizontally, but diagonal scanning may be used in the drawing, depending on the shape. In diagonally-scanned drawing, double-writing occurs to fill in gaps.

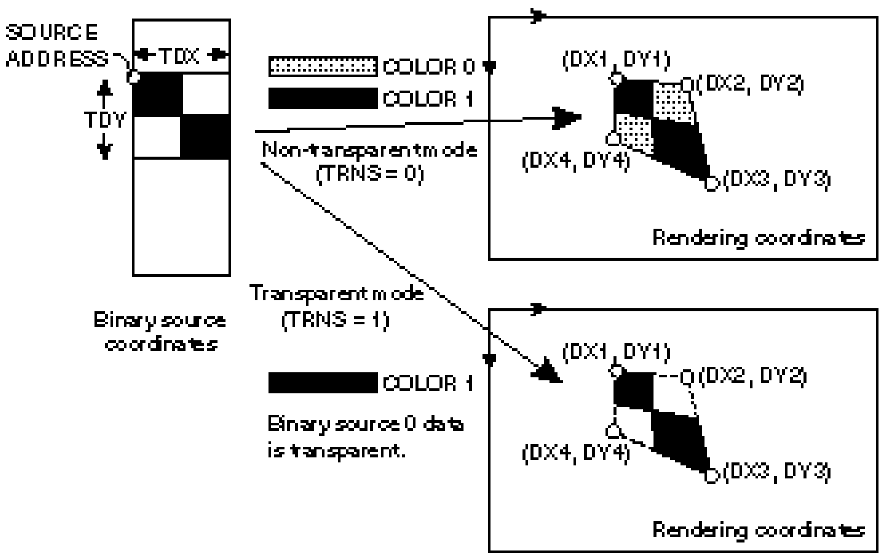
A multiple of 8 pixels must be set as the TDX value.

Binary source data is located in an area in the UGM. When REL = 0, the source address can be specified as an absolute address. When REL = 1, the source address can be specified as a relative address with respect to the UGM address at which the POLYGON4B command code is located.

Absolute addresses and relative addresses must be even numbers. If a relative address is negative, its two's complement should be used.

1. When repeated source referencing is selected as a rendering attribute (STYL = 1), the source is not enlarged or reduced, but is referenced repeatedly.
2. When work referencing is selected as a rendering attribute (WORK = 1), only places where the work coordinate pixel is 1 are drawn at rendering coordinates while referencing work coordinates for the same coordinates as the rendering coordinates.

Example

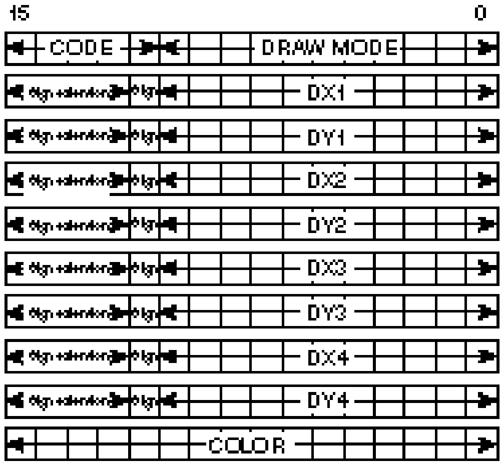


4.4.3 POLYGON4C

Function

Performs any four-vertex drawing at rendering coordinates with a monochrome specification.

Command Format



1. Code

   B'00010

2. Rendering Attributes

Reference Data				Drawing Destination	
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work
		A	O	O	

DRAW MODE										
Reserved			CLIP	Reserved	NET	EOS	FST	Reserved		WORK
Fixed at 0	Fixed at 0	Fixed at 0	O	Fixed at 0	*	*	O	Fixed at 0	Fixed at 0	*

O: Can be used

V: Can be used (specified color is binary EOS bit value)

A: Referenced depending on mode (valid when WORK = 1)

*: Referenced depending on mode (clear to 0 when FST = 1)

Z: Referenced depending on mode (clear to 0 when LNi = 1)

Blank: Cannot be used (clear to 0)

3. Command Parameters

   DXn, DYn (n = 1 to 4): Absolute values, rendering coordinates, negative numbers expressed as two's complement

   COLOR: 8- or 16-bit/pixel color specification

Description

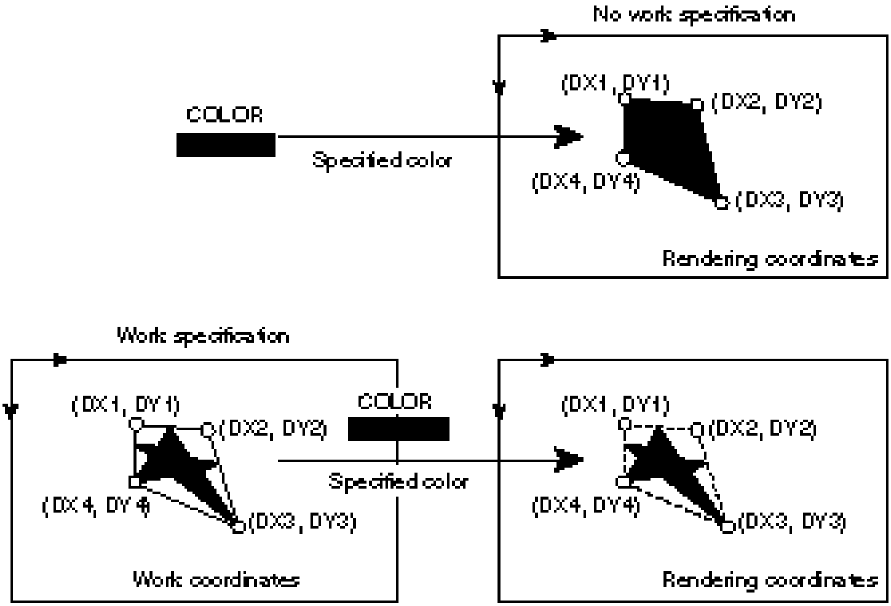
Draws any quadrilateral in the rendering area in the single color specified by the COLOR parameter. For the COLOR data format, see section 3.3.3, Color Data Format Input Color Data Format Configuration.

When work referencing is selected as a rendering attribute (WORK = 1), only places where the work coordinate pixel is 1 are drawn at rendering coordinates while referencing work coordinates for the same coordinates as the rendering coordinates.

When the register attribute FST bit is set to 1, processing is carried out in 4-pixel units. However, operation will be executed normally only if all the following conditions are satisfied; in other cases, operation cannot be guaranteed. Evaluation of these conditions is not performed internally.

- Make settings so that the source and destination are rectangles of the same size, with DX1 = DX4 = 4j – 4, DX2 = DX3 = 4k – 1, DY1 = DY2, DY3 = DY4, DX2 – DX1 = 32n – 1 (where j, k, and n are natural numbers).
- When FST = 1, no other rendering attributes except CLIP can be used.
- When this command is used with FST = 1, first use the MOVE, RMOVE, LCOFS, or RLCOFS command to change the clipping range and local offset values to the values given in the descriptions of the individual commands.
- Operation is valid in 8-bit/pixel and 16-bit/pixel modes. In 8-bit/pixel mode, set the same 8-bit data for the upper and lower color attribute values.
- The local offset values set by the LCOFS and RLCOFS commands must be non-negative.

Example



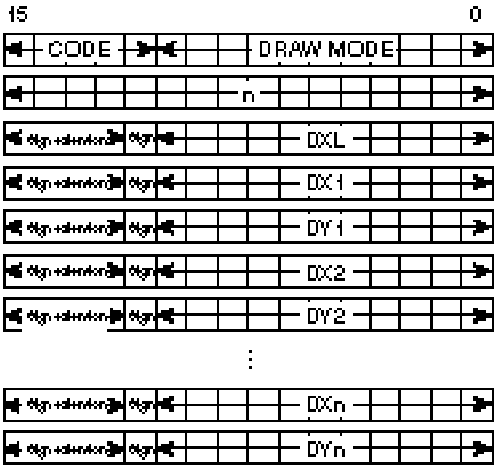
No work specification
COLOR
Specified color
(DX1, DY1)
(DX2, DY2)
(DX4, DY4)
(DX3, DY3)
Rendering coordinates
Work specification
(DX1, DY1)
(DX2, DY2)
(DX4, DY4)
(DX3, DY3)
Work coordinates
COLOR
Specified color
(DX1, DY1)
(DX2, DY2)
(DX4, DY4)
(DX3, DY3)
Rendering coordinates

4.4.4 FTRAP

Function

Draws a polygon at work coordinates.

Command Format



1. Code
   B'01000

2. Rendering Attributes

Reference Data				Drawing Destination	
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work
					O

HITACHI

DRAW MODE											
Reserved			CLIP	Reserved		EOS	EDG	Reserved			
Fixed at 0	Fixed at 0	Fixed at 0	O	Fixed at 0	Fixed at 0	B	O	Fixed at 0	Fixed at 0	Fixed at 0	

O: Can be used

V: Can be used (specified color is binary EOS bit value)

A: Referenced depending on mode (valid when WORK = 1)

B: Referenced depending on mode (valid when EDG = 1)

*: Referenced depending on mode (clear to 0 when FST = 1)

Z: Referenced depending on mode (clear to 0 when LNi = 1)

Blank: Cannot be used (clear to 0)

3. Command Parameters

   n (n = 2 to 65,535): Number of vertices

   DXL: Left-hand side coordinate

   DXn (n = 2 to 65,535): Absolute value, work coordinate, negative number expressed as two's complement

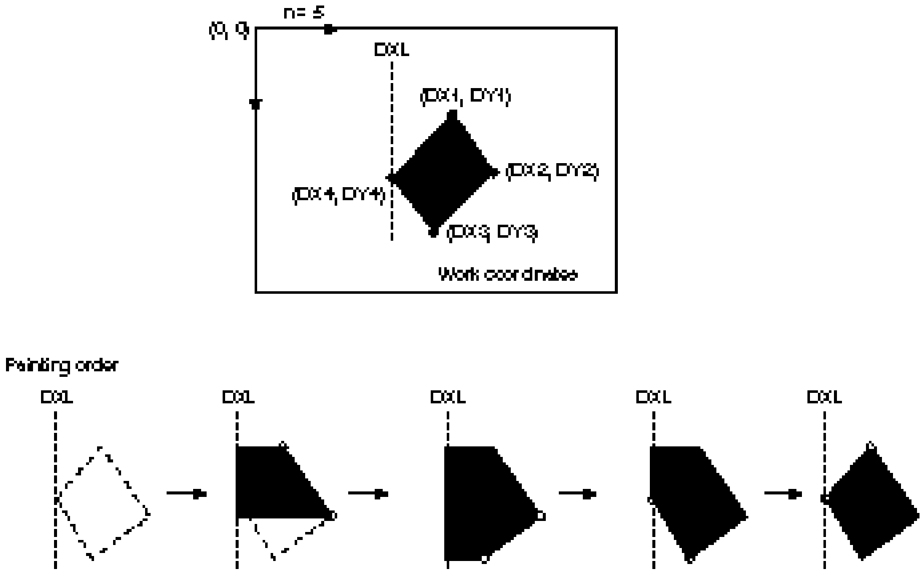
   DYn (n = 2 to 65,535): Absolute value, work coordinate, negative number expressed as two's complement

Description

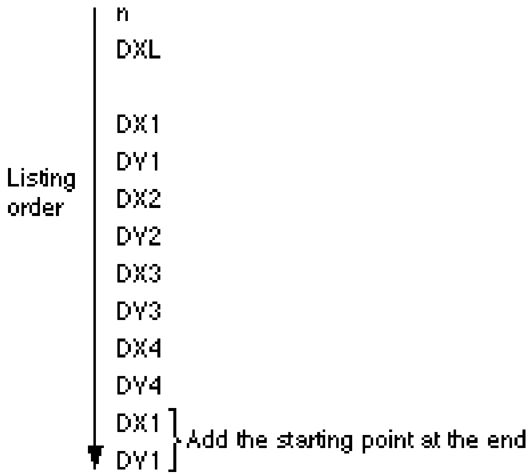
Draws a polygon with n-1 vertices at work coordinates. Paints n-1 trapezoids at work coordinates using binary EOR, with X = DXL as the left-hand side, and line segments (DX1, DY1) – (DX2, DY2), (DX2, DY2) – (DX3, DY3), ..., (DXn-1, DYn-1) – (DXn, DYn) as the right-hand sides, and with top and bottom bases parallel to the X-axis. Bottom base drawing is not performed. Set the minimum value of DX1 to DXn as DXL.

If the draw mode EDG bit is set to 1, an edge line is drawn after the paint operation. The line drawing data is selected with the EOS bit. When setting the EDG bit to 1, set (DXN, DYN) = (DX1, DY1) to give a closed figure.

Example



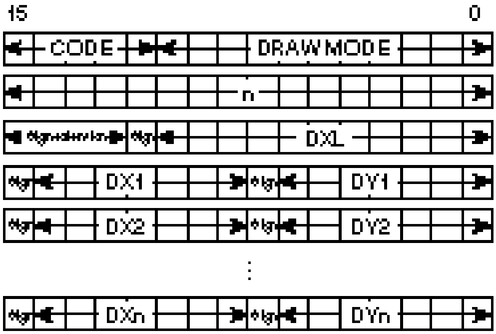
Order of Listing FTRAP Parameters



4.4.5 RFTRAP

Draws a polygon at work coordinates.

Command Format



1. Code
   B'01001

2. Rendering Attributes

Reference Data				Drawing Destination	
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work
					O

DRAW MODE										
Reserved			CLIP	Reserved		EOS	EDG	Reserved		
Fixed at 0	Fixed at 0	Fixed at 0	O	Fixed at 0	Fixed at 0	B	O	Fixed at 0	Fixed at 0	Fixed at 0

O: Can be used
V: Can be used (specified color is binary EOS bit value)
A: Referenced depending on mode (valid when WORK = 1)
B: Referenced depending on mode (valid when EDG = 1)
*: Referenced depending on mode (clear to 0 when FST = 1)
Z: Referenced depending on mode (clear to 0 when LNi = 1)
Blank: Cannot be used (clear to 0)

3. Command Parameters
   n (n = 1 to 65,535): Number of vertices

DXL: Left-hand side coordinate, work coordinate, negative number expressed as two's complement

DXn, DYn (n = 1 to 65,535): Relative values, work coordinates, negative numbers expressed as two's complement

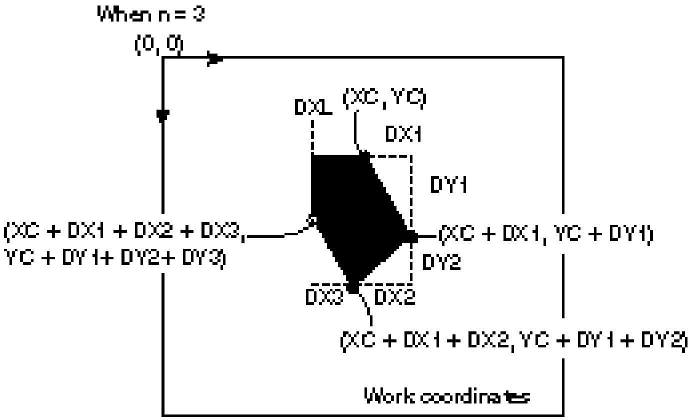
Description

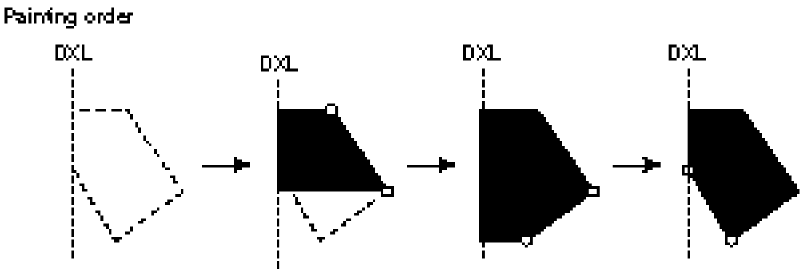
Paints n trapezoids at work coordinates using binary EOR, with X = DXL as the left-hand side, and line segments specified by the relative shift (DX, DY) from the current pointer values (XC, YC) ((XC, YC) – (XC + DX1, YC + DY1), (XC + DX1, YC + DY1) – (XC + DX1 + DX2, YC + DY1 + DY2), ..., (XC + ... + DXn – 1, YC + ... + DYn – 1) – (XC + ... + DXn –1 + DXn, YC + ... + DYn – 1 + DYn)) as the right-hand sides, and with top and bottom bases parallel to the X-axis. Bottom base drawing is not performed.

The final coordinate point is stored as the current pointer values (XC, YC).

If the draw mode EDG bit is set to 1, an edge line is drawn after the paint operation. The line drawing data is selected with the EOS bit. When setting the EDG bit to 1, set (DX1 + DX2 + ... + DXn = 0, DY1 + DY2 + ... + DYn = 0) to give a closed figure.

Example


When n = 3
(0, 0)
DXL
(XC, YC)
DX1
DY1
(XC + DX1 + DX2 + DX3,
YC + DY1+ DY2+ DY3)
(XC + DX1, YC + DY1)
DY2
DX3
DX2
(XC + DX1 + DX2, YC + DY1 + DY2)
Work coordinates

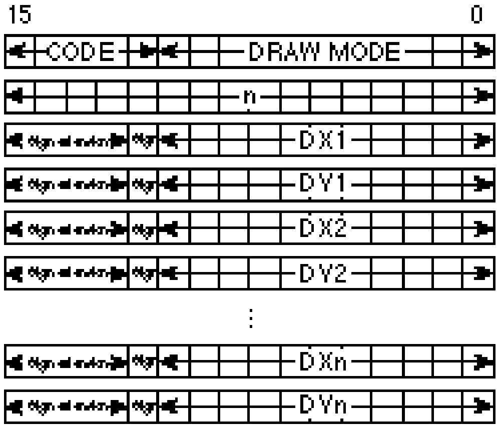

Painting order
DXL
DXL
DXL
DXL

4.4.6 LINEW

Function

Draws a 1-bit-wide solid line at work coordinates.

Command Format



1. Code
   B'01010

2. Rendering Attributes

Reference Data				Drawing Destination	
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work
			V		O

DRAW MODE										
Reserved			CLIP	Reserved		EOS	Reserved			
Fixed at 0	Fixed at 0	Fixed at 0	O	Fixed at 0	Fixed at 0	O	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0

O: Can be used
V: Can be used (specified color is binary EOS bit value)
A: Referenced depending on mode (valid when WORK = 1)
*: Referenced depending on mode (clear to 0 when FST = 1)
Z: Referenced depending on mode (clear to 0 when LNi = 1)
Blank: Cannot be used (clear to 0)

3. Command Parameters

n (n = 2 to 65,535): Number of vertices

DXn (n = 2 to 65,535): Absolute value, work coordinate, negative number expressed as two's complement

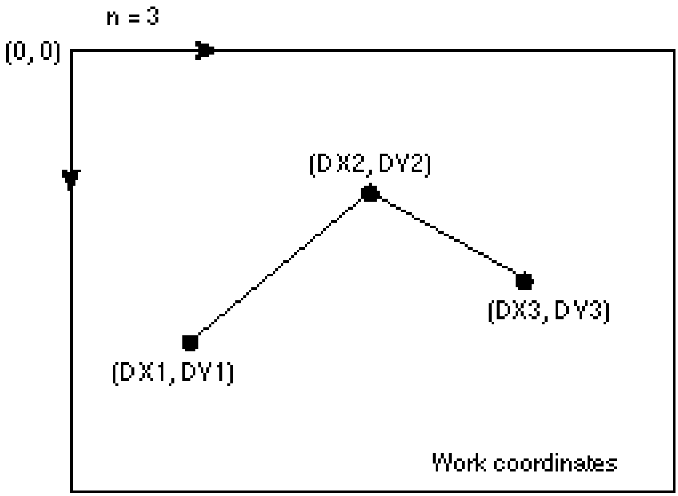
DYn (n = 2 to 65,535): Absolute value, work coordinate, negative number expressed as two's complement

Description

Performs binary drawing at work coordinates of a polygonal line from vertex 1 (DX1, DY1), through vertex 2 (DX2, DY2), ..., vertex n – 1 (DXn – 1, DYn – 1), to vertex n (DXn, DYn). 0 drawing or 1 drawing is selected with the drawing mode EOS bit. Drawing is performed at work coordinates with 0 when EOS = 0, and at work coordinates with 1 when EOS = 1. (Used for border drawing at work coordinates for a polygonal painted figure.)

Note: 8-point drawing is used.

Example

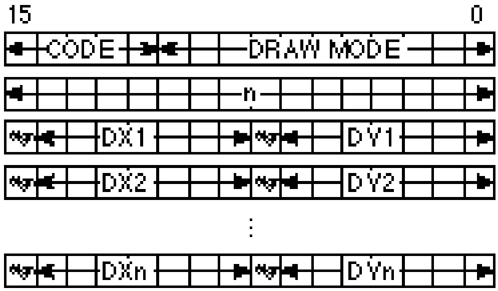


4.4.7 RLINEW

Function

Draws a 1-bit-wide solid line at work coordinates.

Command Format



1. Code
   B'01011

2. Rendering Attributes

Reference Data				Drawing Destination	
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work
			V		O

DRAW MODE										
Reserved			CLIP	Reserved		EOS	Reserved			
Fixed at 0	Fixed at 0	Fixed at 0	O	Fixed at 0	Fixed at 0	O	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0

O: Can be used
V: Can be used (specified color is binary EOS bit value)
A: Referenced depending on mode (valid when WORK = 1)
*: Referenced depending on mode (clear to 0 when FST = 1)
Z: Referenced depending on mode (clear to 0 when LNi = 1)
Blank: Cannot be used (clear to 0)

3. Command Parameters
   n (n = 1 to 65,535): Number of vertices

DXn, DYn (n = 1 to 65,535): Relative values, work coordinates, negative numbers expressed as two's complement

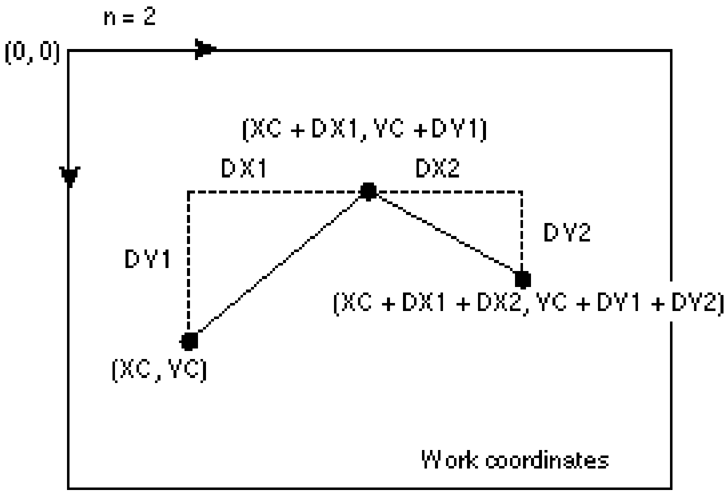
Description

Performs binary drawing at work coordinates of a polygonal line comprising line segments (XC, YC) – (XC + DX1, YC + DY1), (XC + DX1, YC + DY1) – (XC + DX1 + DX2, YC + DY1 + DY2), ..., (XC + ... + DXn – 1, YC + ... + DYn – 1) – (XC + ... + DXn –1 + DXn, YC + ... + DYn – 1 + DYn) to the coordinates specified by the relative shift (DX, DY) from the current pointer values (XC, YC). 0 drawing or 1 drawing is selected with the drawing mode EOS bit. Drawing is performed at work coordinates with 0 when EOS = 0, and at work coordinates with 1 when EOS = 1.

The final coordinate point is stored as the current pointer values (XC, YC). (Used for border drawing at work coordinates for a polygonal painted figure.)

Note: 8-point drawing is used.

Example

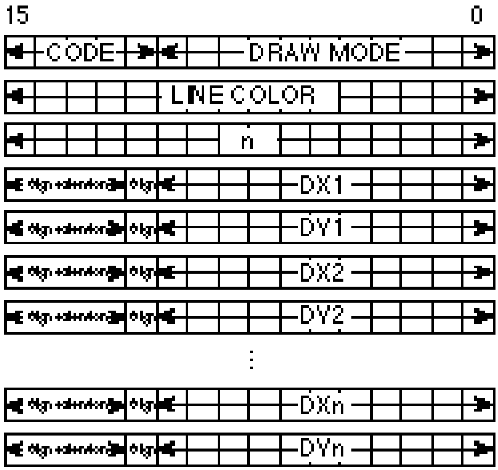


4.4.8 LINE

Function

Draws a solid line 1 to 5 bits in width at rendering coordinates.

Command Format



1. Code
   B'01100

2. Rendering Attributes

Reference Data				Drawing Destination	
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work
			O	O	

DRAW MODE											
Reserved			CLIP	Reserved	NET	EOS	FWUL	W2UL	FWDR	W2DR
Fixed at 0	Fixed at 0	Fixed at 0	O	Fixed at 0	O	O	0000–1111			

O: Can be used

V: Can be used (specified color is binary EOS bit value)

A: Referenced depending on mode (valid when WORK = 1)

*: Referenced depending on mode (clear to 0 when FST = 1)

Z: Referenced depending on mode (clear to 0 when LNi = 1)

Blank: Cannot be used (clear to 0)

3. Command Parameters

   LINE COLOR: 8- or 16-bit/pixel color specification

   n (n = 2 to 65,535): Number of vertices

   DXn (n = 2 to 65,535): Absolute values, rendering coordinates, negative numbers expressed as two's complement

   DYn (n = 2 to 65,535): Absolute values, rendering coordinates, negative numbers expressed as two's complement

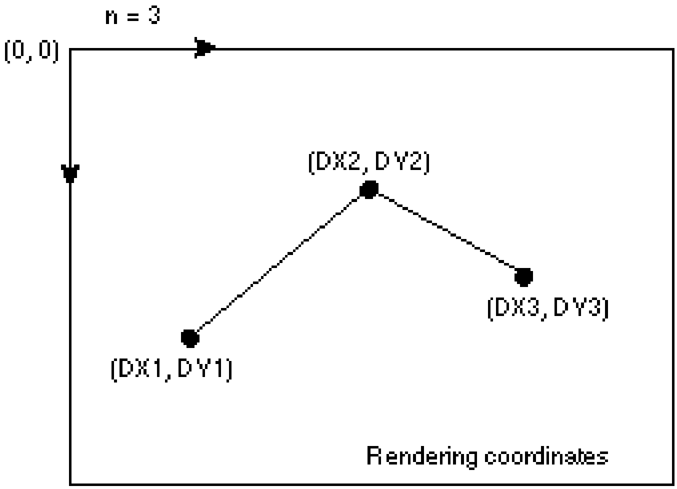
Description

Draws a polygonal line at rendering coordinates from vertex 1 (DX1, DY1), through vertex 2 (DX2, DY2), ..., vertex n – 1 (DXn – 1, DYn – 1), to vertex n (DXn, DYn), using the single color specified by parameter LINE COLOR.

For the LINE COLOR data format, see section 3.3.3, Color Data Format Input Color Data Format Configuration.

Note: 8-point drawing is used.

Example

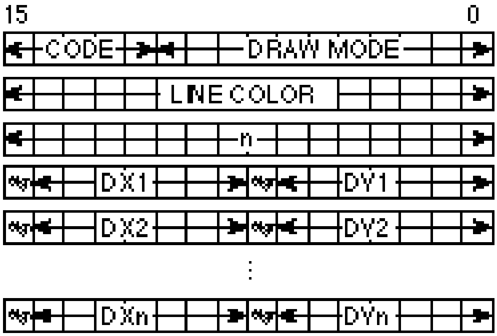


4.4.9 RLINE

Function

Draws a solid line 1 to 5 bits in width at rendering coordinates.

Command Format



1. Code
   B'01101

2. Rendering Attributes

Reference Data				Drawing Destination	
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work
			O	O	

DRAW MODE										
Reserved			CLIP	Reserved	NET	EOS	FWUL	W2UL	FWDR	W2DR
Fixed at 0	Fixed at 0	Fixed at 0	O	Fixed at 0	O	O	0000–1111			

O: Can be used
V: Can be used (specified color is binary EOS bit value)
A: Referenced depending on mode (valid when WORK = 1)
*: Referenced depending on mode (clear to 0 when FST = 1)
Z: Referenced depending on mode (clear to 0 when LNi = 1)
Blank: Cannot be used (clear to 0)

3. Command Parameters
   LINE COLOR: 8- or 16-bit/pixel color specification

n (n = 1 to 65,535): Number of vertices

DXn, DYn (n = 1 to 65,535): Relative values, rendering coordinates, negative numbers expressed as two's complement

Description

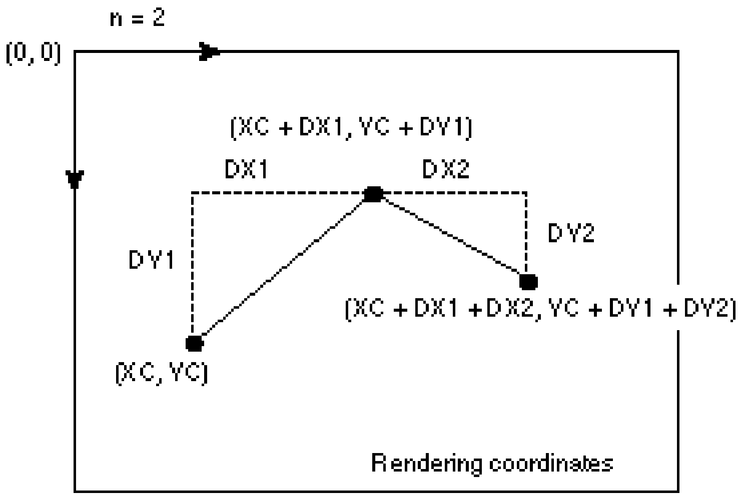
Draws, at rendering coordinates, a polygonal line comprising line segments (XC, YC) – (XC + DX1, YC + DY1), (XC + DX1, YC + DY1) – (XC + DX1 + DX2, YC + DY1 + DY2), ..., (XC + ... + DXn – 1, YC + ... + DYn – 1) – (XC + ... + DXn – 1 + DXn, YC + ... + DYn – 1 + DYn) to the coordinates specified by the relative shift (DX, DY) from the current pointer values (XC, YC), using the single color specified by parameter LINE COLOR.

For the LINE COLOR data format, see section 3.3.3, Color Data Format Input Color Data Format Configuration.

The final coordinate point is stored as the current pointer values (XC, YC).

Note: 8-point drawing is used.

Example



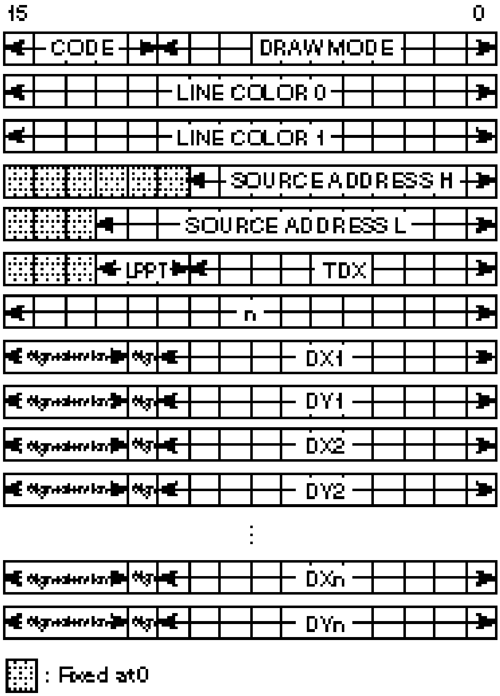
HITACHI

4.4.10 PLINE

Function

Draws a polygonal line at rendering coordinates while referencing a binary source.

Command Format



1. Code

   B'01110

2. Rendering Attributes

Reference Data				Drawing Destination	
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work
	O			O	

DRAW MODE										
Reserved	TRNS	Reserved	CLIP	Reserved	NET	EOS	EDG2	Reserved	EDG1	Reserved
Fixed at 0	O	Fixed at 1	O	Fixed at 0	O	O	O	Fixed at 0	O	Fixed at 1

O: Can be used

V: Can be used (specified color is binary EOS bit value)

A: Referenced depending on mode (valid when WORK = 1)

*: Referenced depending on mode (clear to 0 when FST = 1)

Z: Referenced depending on mode (clear to 0 when LNi = 1)

Blank: Cannot be used (clear to 0)

3. Command Parameters

   LINE COLOR0: 8- or 16-bit/pixel color specification

   LINE COLOR1: 8- or 16-bit/pixel color specification

   SOURCE ADDRESS H: 1-bit/pixel source start upper address (byte address)

   SOURCE ADDRESS L: 1-bit/pixel source start lower address (byte address)

   TDX: Source size

   LPPT: Line pattern pointer

   n (n = 2 to 65,535): Number of vertices

   DXn (n = 2 to 65,535): Absolute values, rendering coordinates, negative numbers expressed as two's complement

   DYn (n = 2 to 65,535): Absolute values, rendering coordinates, negative numbers expressed as two's complement

Description

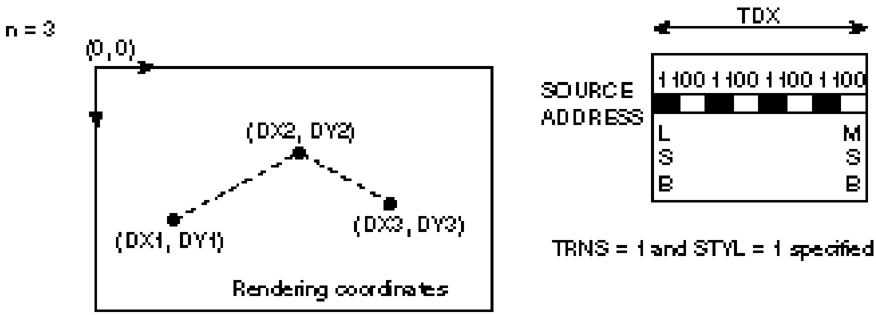
Draws a polygonal line from vertex 1 (DX1, DY1), through vertex 2 (DX2, DY2), ..., vertex n – 1 (DXn – 1, DYn – 1), to vertex n (DXn, DYn).

A multiple of 8 pixels must be set for the TDX value.

The reference start position of the binary source data can be adjusted by setting a value between 0 and 7 in the line pattern pointer. For example, if 0 is set, referencing starts at the beginning of the source data, while if 5 is set, referencing starts 5 pixels from the beginning of the source data. When STYL = 1, pattern repetition starts at the pixel after [source start position + TDX + LPPT – 1]. The source start address must be an even number.

Note: 4-point drawing is used.

Example

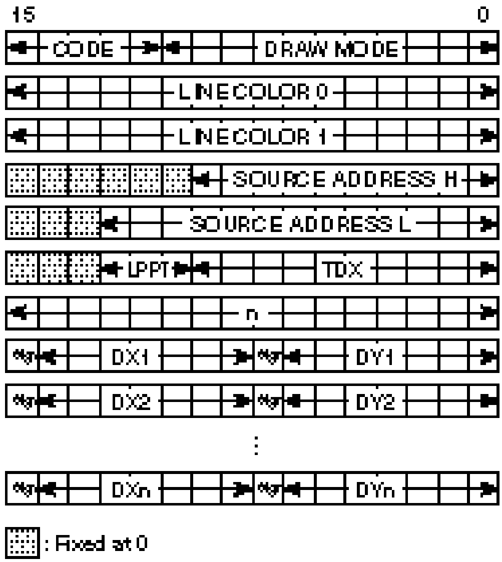


4.4.11 RPLINE

Function

Draws a polygonal line at rendering coordinates while referencing a binary source.

Command Format



1. Code

   B'01111

2. Rendering Attributes

Reference Data				Drawing Destination	
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work
	O			O	

DRAW MODE										
Reserved	TRNS	Reserved	CLIP	Reserved	NET	EOS	EDG2	Reserved	EDG1	Reserved
Fixed at 0	O	Fixed at 1	O	Fixed at 0	O	O	O	Fixed at 0	O	Fixed at 1

O: Can be used

V: Can be used (specified color is binary EOS bit value)

A: Referenced depending on mode (valid when WORK = 1)

*: Referenced depending on mode (clear to 0 when FST = 1)

Z: Referenced depending on mode (clear to 0 when LNi = 1)

Blank: Cannot be used (clear to 0)

3. Command Parameters

   LINE COLOR0: 8- or 16-bit/pixel color specification

   LINE COLOR1: 8- or 16-bit/pixel color specification

   SOURCE ADDRESS H: 1-bit/pixel source start upper address (byte address)

   SOURCE ADDRESS L: 1-bit/pixel source start lower address (byte address)

   LPPT: Line pattern pointer

   TDX: Source size

   n (n = 1 to 65,535): Number of vertices

   DXn, DYn (n = 1 to 65,535): Relative values, rendering coordinates, negative numbers expressed as two's complement

Description

Draws a polygonal line comprising line segments (XC, YC) – (XC + DX1, YC + DY1), (XC + DX1, YC + DY1) – (XC + DX1 + DX2, YC + DY1 + DY2), ..., (XC + ... + DXn – 1, YC + ... + DYn – 1) – (XC + ... + DXn –1 + DXn, YC + ... + DYn – 1 + DYn) to the coordinates specified by the relative shift (DX, DY) from the current pointer values (XC, YC).

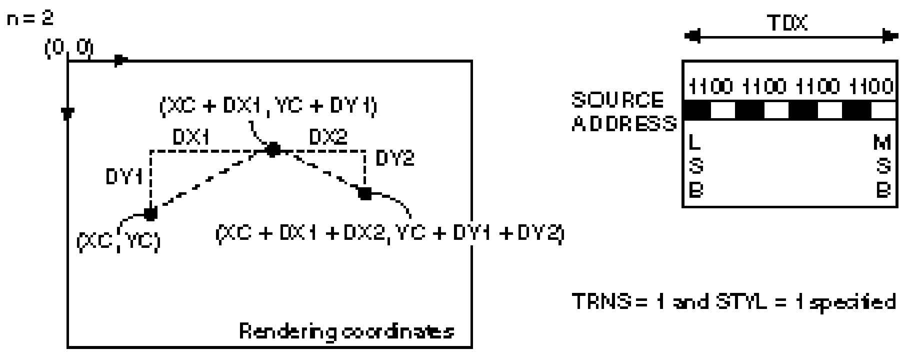
The final coordinate point is stored as the current pointer values (XC, YC).

A multiple of 8 pixels must be set for the TDX value.

The reference start position of the binary source data can be adjusted by setting a value between 0 and 7 in the line pattern pointer. For example, if 0 is set, referencing starts at the beginning of the source data, while if 5 is set, referencing starts 5 pixels from the beginning of the source data. When STYL = 1, pattern repetition starts at the pixel after [source start position + TDX + LPPT – 1]. The source start address must be an even number.

Note: 4-point drawing is used.

Example

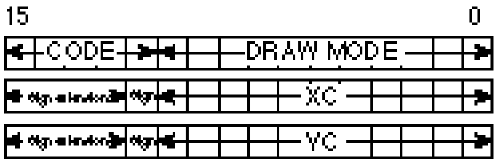


4.4.12 MOVE

Function

Sets the current pointer.

Command Format



1. Code

   B'10000

2. Rendering Attributes

Reference Data				Drawing Destination	
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work

DRAW MODE										
Reserved										
Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0

O: Can be used

V: Can be used (specified color is binary EOS bit value)

A: Referenced depending on mode (valid when WORK = 1)

*: Referenced depending on mode (clear to 0 when FST = 1)

Z: Referenced depending on mode (clear to 0 when LNi = 1)

Blank: Cannot be used (clear to 0)

3. Command Parameters

   XC: Absolute value, rendering coordinate, work coordinate, negative number expressed as two's complement

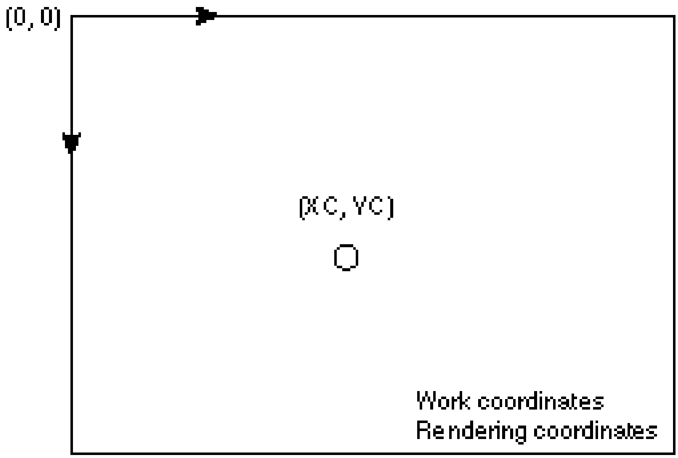
   YC: Absolute value, rendering coordinate, work coordinate, negative number expressed as two's complement

Description

Sets the values obtained by adding the local offset values to XC and YC in the current pointers. XC and YC are set as absolute coordinates. The current pointers are used by relative drawing commands only.

After issuing a MOVE command, use relative drawing commands in succession. If an absolute drawing command is used during this sequence, the current pointers will be used as registers for internal computation, and the current pointer values will be lost. A MOVE command must be therefore be issued before using relative drawing commands again.

Example

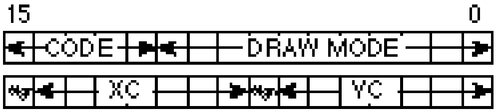


4.4.13 RMOVE

Function

Sets the current pointer.

Command Format



1. Code

   B'10001

2. Rendering Attributes

Reference Data				Drawing Destination	
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work

DRAW MODE										
Reserved										
Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0

O: Can be used
V: Can be used (specified color is binary EOS bit value)
A: Referenced depending on mode (valid when WORK = 1)
*: Referenced depending on mode (clear to 0 when FST = 1)
Z: Referenced depending on mode (clear to 0 when LNi = 1)
Blank: Cannot be used (clear to 0)

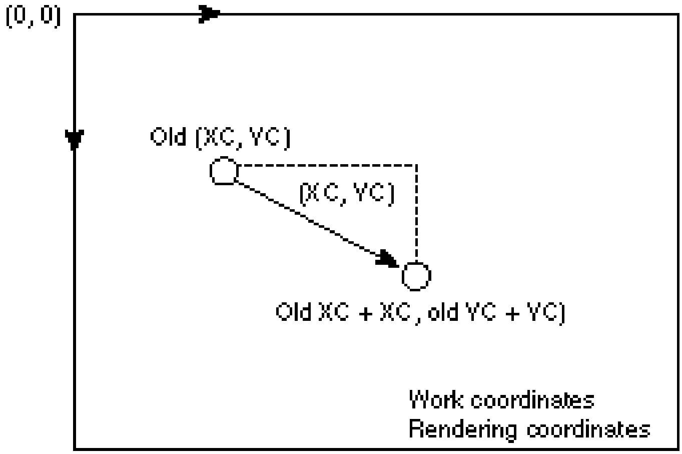
3. Command Parameters

   XC, YC: Relative values, rendering coordinates, work coordinates, negative numbers expressed as two's complement

Description

Adds XC and YC to the current pointers.

Example

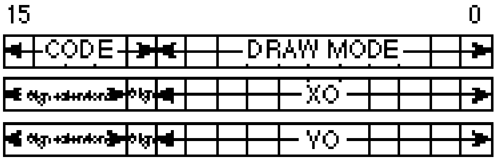


4.4.14 LCOFS

Function

Sets the local offset.

Command Format



1. Code
   B'10010

2. Rendering Attributes

Reference Data				Drawing Destination	
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work

DRAW MODE										
Reserved										
Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0

O: Can be used
V: Can be used (specified color is binary EOS bit value)
A: Referenced depending on mode (valid when WORK = 1)
*: Referenced depending on mode (clear to 0 when FST = 1)
Z: Referenced depending on mode (clear to 0 when LNi = 1)
Blank: Cannot be used (clear to 0)

3. Command Parameters
   XO, YO: Local offset value absolute specifications, rendering coordinates, work coordinates, negative numbers expressed as two's complement

Description

Sets the local offset with absolute coordinates. After these settings are made, these offset values are added in all subsequent coordinate specifications.

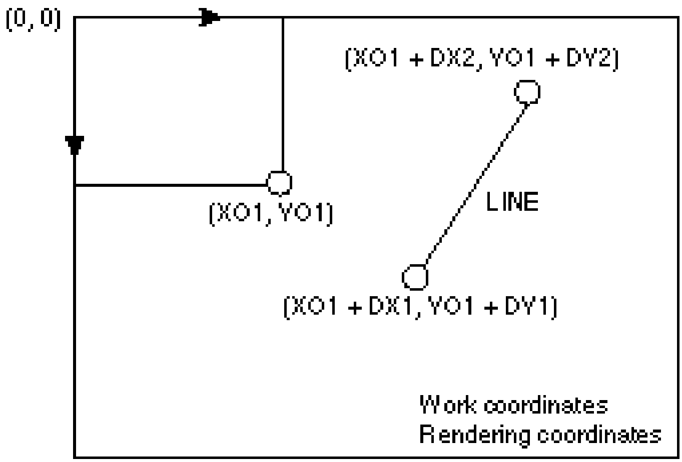
These settings must be made at the start of the display list (the initial values are undefined).

To reflect the local offset values in the current pointers, issue a MOVE command after the LCOFS command.

When using a command that employs the FST specification, a multiple of 4 must be set for the XO value.

Use non-negative values for both XO and YO.

Example

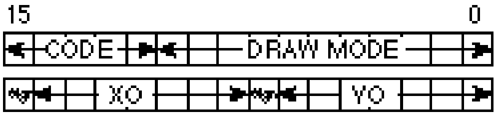


4.4.15 RLCOFS

Function

Sets the local offset.

Command Format



1. Code
   B'10011

2. Rendering Attributes

Reference Data				Drawing Destination	
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work

DRAW MODE										
Reserved										
Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0

O: Can be used
V: Can be used (specified color is binary EOS bit value)
A: Referenced depending on mode (valid when WORK = 1)
*: Referenced depending on mode (clear to 0 when FST = 1)
Z: Referenced depending on mode (clear to 0 when LNi = 1)
Blank: Cannot be used (clear to 0)

3. Command Parameters
   XO, YO: Local offset value relative specifications, rendering coordinates, work coordinates, negative numbers expressed as two's complement

Description

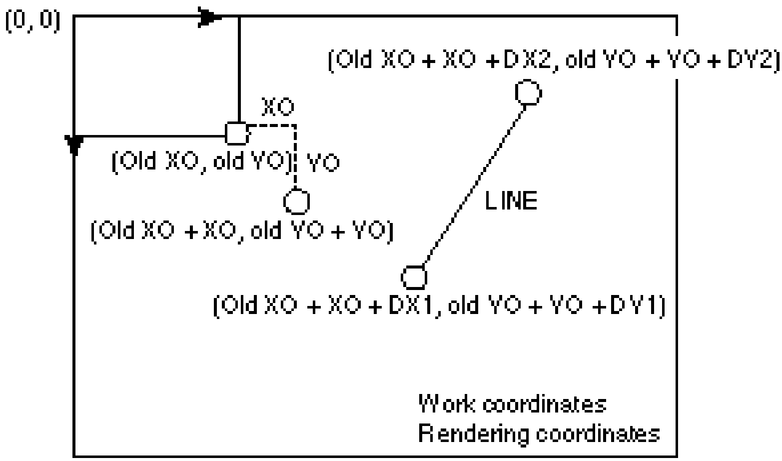
Adds XO and YO to the local offset. After these settings are made, these offset values are added in all subsequent coordinate specifications.

To reflect the local offset values in the current pointers, issue a MOVE command after setting the local offset with the LCOFS or RLCOFS command.

When using a command that employs the FST specification, the value obtained by adding XO to the local offset must be a multiple of 4.

The local offset values set by XO and YO must be non-negative.

Example

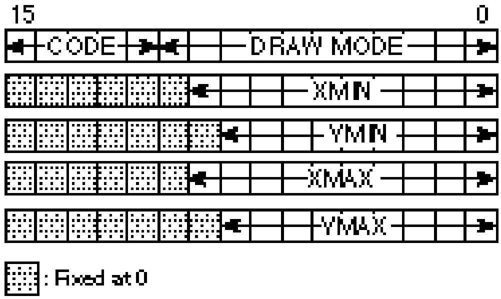


4.4.16 UCLIP

Function

Sets the user clipping area.

Command Format



1. Code
   B'10101

2. Rendering Attributes

Reference Data				Drawing Destination	
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work

DRAW MODE										
Reserved										
Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0

O: Can be used
V: Can be used (specified color is binary EOS bit value)
A: Referenced depending on mode (valid when WORK = 1)
*: Referenced depending on mode (clear to 0 when FST = 1)
Z: Referenced depending on mode (clear to 0 when LNi = 1)
Blank: Cannot be used (clear to 0)

3. Command Parameters
   XMIN, XMAX: Left and right X coordinate values, rendering coordinates, work coordinates

YMIN, YMAX: Upper and lower Y coordinate values, rendering coordinates, work coordinates

Description

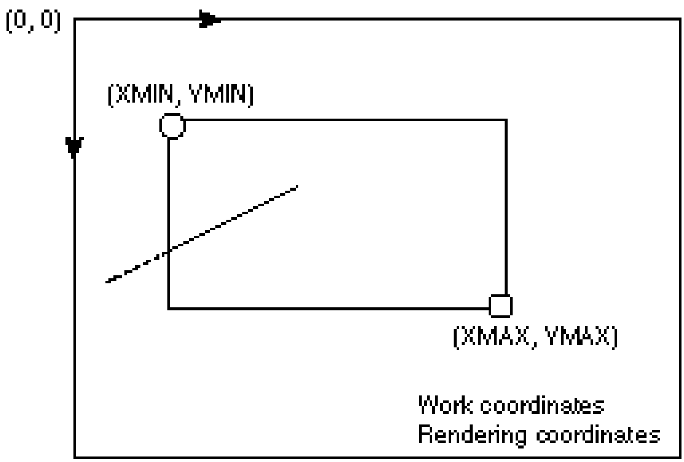
Designates the area specified by upper-left coordinates (XMIN, YMIN) and lower-right coordinates (XMAX, YMAX) in the rendering coordinate and work coordinate systems as a user clipping area. The local offset values specified by the LCOFS or RLCOFS command are not added to the coordinates set by this command.

When making these settings, ensure that XMIN < XMAX and YMIN < YMAX, and that the system clipping area is not exceeded.

This setting is valid when CLIP = 1.

When using a command that employs the FST specification, set a multiple of 4 as the XMIN value, and a multiple of 4 – 1 as the XMAX value.

Example

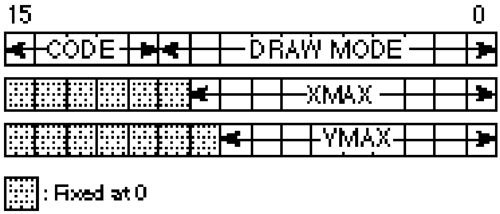


4.4.17 SCLIP

Function

Sets the system clipping area.

Command Format



1. Code
   B'10111

2. Rendering Attributes

Reference Data				Drawing Destination	
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work

DRAW MODE										
Reserved										
Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0

O: Can be used
V: Can be used (specified color is binary EOS bit value)
A: Referenced depending on mode (valid when WORK = 1)
*: Referenced depending on mode (clear to 0 when FST = 1)
Z: Referenced depending on mode (clear to 0 when LNi = 1)
Blank: Cannot be used (clear to 0)

3. Command Parameters
   XMAX: Left and right X coordinate values, rendering coordinates, work coordinates
   YMAX: Upper and lower Y coordinate values, rendering coordinates, work coordinates

Description

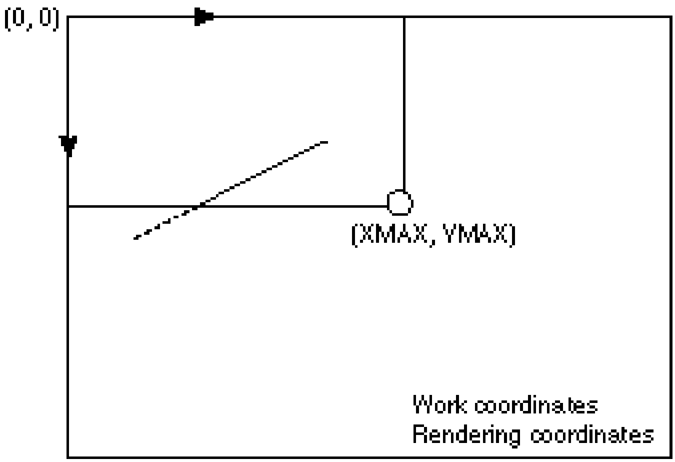
Designates the area specified by upper-left coordinates (0, 0) and lower-right coordinates (XMAX, YMAX) in the rendering coordinate and work coordinate systems as the system clipping area. The local offset values specified by the LCOFS or RLCOFS command are not added to the coordinates set by this command.

Set the maximum drawing range values for XMAX and YMAX. After powering on, the initial values of the clipping range are undefined. The clipping range must therefore be set with the SCLIP command at the start of the first display list executed.

For the set values given by this command, screen coordinates must be set as reference coordinates.

When using a command that employs the FST specification, set a multiple of 4 – 1 as the XMAX value.

Example

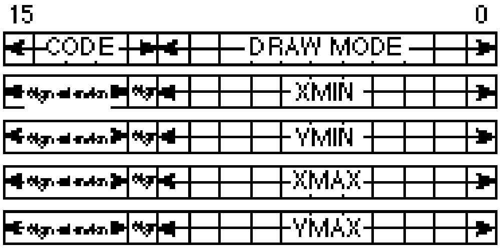


4.4.18 CLRW

Function

Zeroizes the work coordinates.

Command Format



1. Code
   B'10100

2. Rendering Attributes

Reference Data				Drawing Destination	
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work
					O

DRAW MODE										
Reserved			CLIP	Reserved						
Fixed at 0	Fixed at 0	Fixed at 0	O	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0

O: Can be used
V: Can be used (specified color is binary EOS bit value)
A: Referenced depending on mode (valid when WORK = 1)
*: Referenced depending on mode (clear to 0 when FST = 1)
Z: Referenced depending on mode (clear to 0 when LNi = 1)
Blank: Cannot be used (clear to 0)

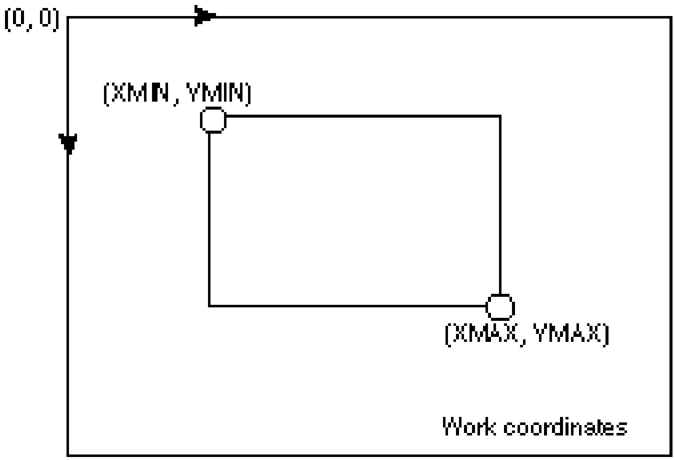
3. Command Parameters
   XMIN, XMAX: Left and right X coordinate values, work coordinates, negative numbers expressed as two's complement

YMIN, YMAX: Upper and lower Y coordinate values, work coordinates, negative numbers expressed as two's complement

Description

Zero-clears the area specified by upper-left coordinates (XMIN, YMIN) and lower-right coordinates (XMAX, YMAX) in the work coordinate system.

Example

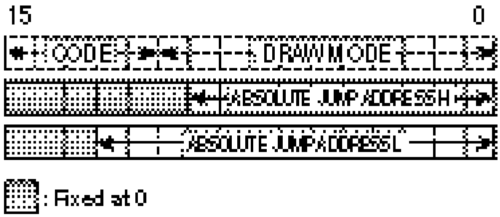


4.4.19 JUMP

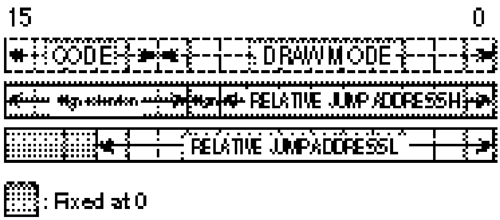
Function

Changes the display list fetch destination.

Command Format **REL = 0**



REL = 1



1. Code
   B'11000

2. Rendering Attributes

Reference Data				Drawing Destination	
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work

DRAW MODE											
Reserved				REL	Reserved						
Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	O	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0

O: Can be used
V: Can be used (specified color is binary EOS bit value)
A: Referenced depending on mode (valid when WORK = 1)
*: Referenced depending on mode (clear to 0 when FST = 1)
Z: Referenced depending on mode (clear to 0 when LNi = 1)
Blank: Cannot be used (clear to 0)

3. Command Parameters

ABSOLUTE/RELATIVE JUMP ADDRESS H: Absolute/relative jump destination upper address (byte address)

ABSOLUTE/RELATIVE JUMP ADDRESS L: Absolute/relative jump destination lower address (byte address)

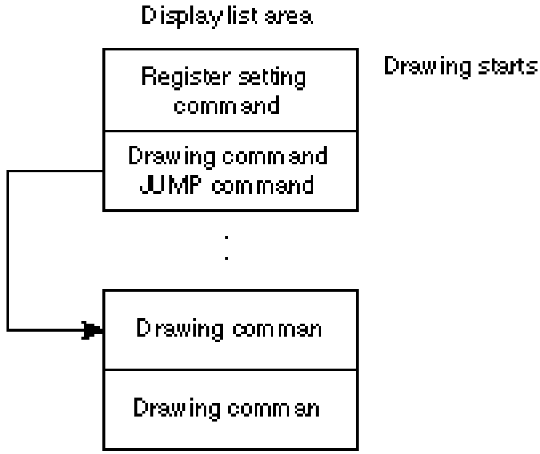
Description

Changes the display list fetch destination to the specified address.

When REL = 0, the jump destination address can be specified as an absolute address. When REL = 1, the source address can be specified as a relative address with respect to the UGM address at which the command code is located.

Absolute addresses and relative addresses must be even numbers. If a relative address is negative, its two's complement should be used.

Example

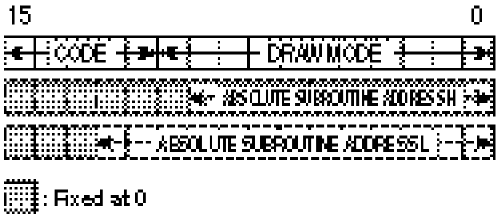

Display list area
Register setting command
Drawing command
JUMP command
Drawing starts
Drawing comman
Drawing comman

4.4.20 GOSUB

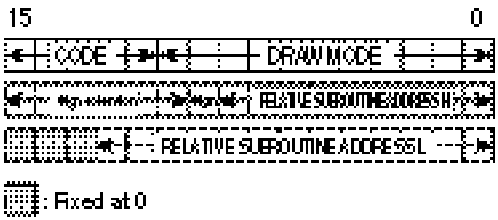
Function

Makes a subroutine call for the display list.

Command Format **REL = 0**



REL = 1



1. Code
   B'11001

2. Rendering Attributes

Reference Data				Drawing Destination	
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work

HITACHI

DRAW MODE										
Reserved				REL	Reserved					
Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	O	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0

O: Can be used

V: Can be used (specified color is binary EOS bit value)

A: Referenced depending on mode (valid when WORK = 1)

*: Referenced depending on mode (clear to 0 when FST = 1)

Z: Referenced depending on mode (clear to 0 when LNi = 1)

Blank: Cannot be used (clear to 0)

3. Command Parameters

   ABSOLUTE/RELATIVE SUBROUTINE ADDRESS H: Absolute/relative subroutine upper address (byte address)

   ABSOLUTE/RELATIVE SUBROUTINE ADDRESS L: Absolute/relative subroutine lower address (byte address)

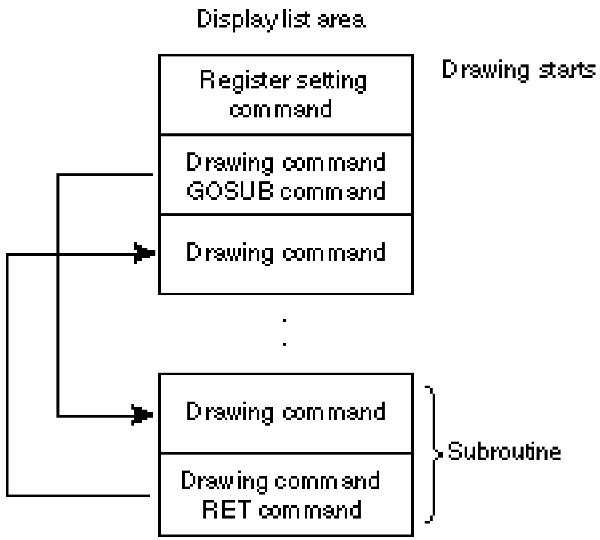
Description

Changes the display list fetch destination to the specified subroutine address. The fetch address is restored by an RET instruction. As only one level of nesting is permitted, it will not be possible to return if a subroutine call is issued within the subroutine.

When REL = 0, the subroutine destination address can be specified as an absolute address. When REL = 1, the address can be specified as a relative address with respect to the UGM address at which the command code is located.

Absolute addresses and relative addresses must be even numbers. If a relative address is negative, its two's complement should be used.

Example

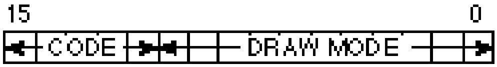

Display list area
Register setting command
Drawing starts
Drawing command
GOSUB command
Drawing command
Drawing command
Drawing command
RET command
Subroutine

4.4.21 RET

Function

Returns from a subroutine call made by the GOSUB command.

Command Format



1. Code
   B'11011

2. Rendering Attributes

Reference Data				Drawing Destination	
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work

DRAW MODE										
Reserved										
Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0

O: Can be used
V: Can be used (specified color is binary EOS bit value)
A: Referenced depending on mode (valid when WORK = 1)
*: Referenced depending on mode (clear to 0 when FST = 1)
Z: Referenced depending on mode (clear to 0 when LNi = 1)
Blank: Cannot be used (clear to 0)

Description

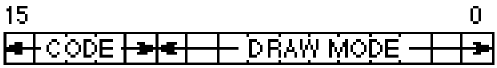
Restores the display list fetch destination to the address following the source of the subroutine call.

4.4.22 TRAP

Function

Informs the Q2SD of the end of the display list.

Command Format



1. Code
   B'11111

2. Rendering Attributes

Reference Data				Drawing Destination	
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work

DRAW MODE										
Reserved										
Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0

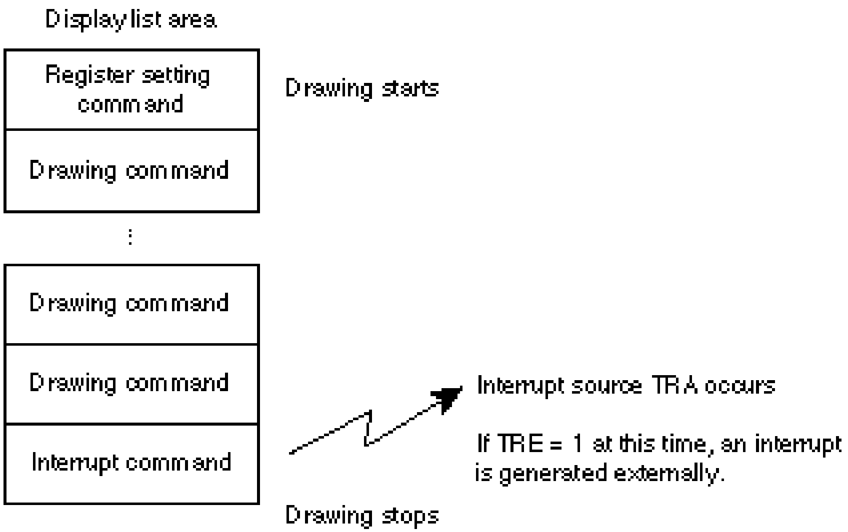
O: Can be used
V: Can be used (specified color is binary EOS bit value)
A: Referenced depending on mode (valid when WORK = 1)
*: Referenced depending on mode (clear to 0 when FST = 1)
Z: Referenced depending on mode (clear to 0 when LNi = 1)
Blank: Cannot be used (clear to 0)

Description

Halts the drawing operation and sets TRA to 1 in the status register (SR). If TRE is set to 1 in the interrupt enable register (IER), an interrupt is sent to the SuperH.

This command must be placed at the end of the display list.

Example

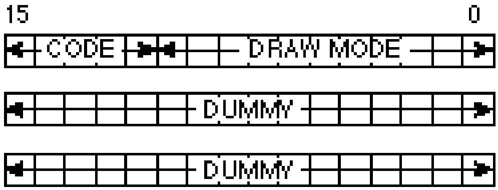

Display list area
Register setting command
Drawing command
Drawing command
Drawing command
Interrupt command
Drawing starts
Interrupt source TRA occurs
If TRE = 1 at this time, an interrupt is generated externally.
Drawing stops

4.4.23 NOP3

Function

Executes no operation.

Command Format



1. Code
   B'11110

2. Rendering Attributes

Reference Data				Drawing Destination	
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work

DRAW MODE										
Reserved										
Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0

O: Can be used
V: Can be used (specified color is binary EOS bit value)
A: Referenced depending on mode (valid when WORK = 1)
*: Referenced depending on mode (clear to 0 when FST = 1)
Z: Referenced depending on mode (clear to 0 when LNi = 1)
Blank: Cannot be used (clear to 0)

Description

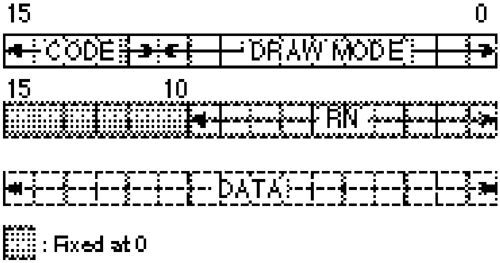
The NOP3 command does not perform any operation. This command, which consists of three words including the command code, simply fetches the next instruction without executing any processing.

4.4.24 WPR

Function

Sets a value in a specific address-mapped register.

Command Format



1. Code
   B'10110

2. Rendering Attributes

Reference Data				Drawing Destination	
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work

DRAW MODE										
Reserved										
Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0

O: Can be used
V: Can be used (specified color is binary EOS bit value)
A: Referenced depending on mode (valid when WORK = 1)
*: Referenced depending on mode (clear to 0 when FST = 1)
Z: Referenced depending on mode (clear to 0 when LNi = 1)
Blank: Cannot be used (clear to 0)

3. Command Parameters
   RN: Register number
   DATA: Data

Description

Writes data to the Q2SD's address-mapped registers. The register number is set in RN, and the write data in DATA.

When a write is performed to an address-mapped register with this command, select the location to ensure that the currently executing drawing processing is not adversely affected.

Also ensure that there is no conflict with access by the SuperH.

This command is intended primarily for performing the operations shown in (a) to (e), and the registers that can be written to are limited to those listed below. If a write is performed to another register, subsequent operation cannot be guaranteed.

Register No.	Name
00A:	DSA0
00B:	DSA1
00E:	SSAR
00F:	WSAR
04C:	RSAR
006:	REMR
04A:	RTNH
04B:	RTNL
04D:	COLOR

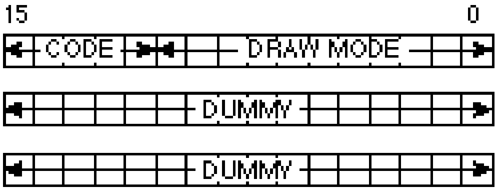
(a) Change of display start address or drawing start address (RN = 00A, 00B, 04C)
(b) Change of multi-valued source or work start address (RN = 00E, 00F)
(c) Change of graphic bit mode (RN = 006)
(d) Return address setting when performing resumption processing after drawing suspension (RN = 04A, 04B)
(e) Change of drawing color offset value when performing drawing processing (RN = 04D)

4.4.25 VBKEM

Function

Performs synchronization with the frame change timing.

Command Format



1. Code
   B'11010

2. Rendering Attributes

Reference Data				Drawing Destination	
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work

DRAW MODE										
Reserved										
Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0	Fixed at 0

O: Can be used
V: Can be used (specified color is binary EOS bit value)
A: Referenced depending on mode (valid when WORK = 1)
*: Referenced depending on mode (clear to 0 when FST = 1)
Z: Referenced depending on mode (clear to 0 when LNi = 1)
Blank: Cannot be used (clear to 0)

Description

When this command is executed, the drawing operation is kept waiting until the timing for a frame change. As soon as the frame change timing has elapsed, control passes to the next command. The frame change timing is every VBK in non-interlace and interlace & video modes, and every FRM in interlace mode.

Do not use this command in auto display charge mode.

Section 5 Registers

5.1 Overview

The Q2SD has address-mapped registers mapped onto the CPU address space (H'000 to H'2FF). These registers are divided into six groups—interface control registers, memory control registers, display control registers, rendering control registers, input data control registers, and color palette registers. Word access is used on all of these registers. The address specification is made by inputting the address from pins A10 to A1 while the $\overline{CS1}$ pin is in the 0 state.

Addresses A10–A1 = H'04E to H'0FF are reserved, and must not be read or written to. Reading or writing to these addresses may result in the loss of address-mapped register values, and unpredictable operation by the Q2SD.

To facilitate management of UGM access rights, initial values must be set in the address-mapped registers by the SuperH before it accesses the UGM.

The setting procedure is shown in 1 to 3 below.

1. Set initial values in the system control register. Set SRES = 0, DRES = 1, and DEN = 0.
2. Set initial values in registers 002 to 025 and 02B.
3. Set SRES = 0 and DRES = 0.

Also, since video control related registers (video area start address register 0–2H/L (VSAR0–2H/L), video window size register X and Y (VSIZERX, VSIZERY), and video incorporation mode register (VIMR) are externally updated for video incorporation operations, they should only be rewritten when the VIE bit is cleared to 0 in the video incorporation mode register. The same also applies when updating bits other than VIE in the video incorporation mode register. The procedure is shown below.

1. Clear the VIE bit to 0 in the video incorporation mode register. Set bits other than VIE to the values to which they are set at that time.
2. Make address register 0–2H/L (VSAR0–2H/L), video window size register X and Y (VSIZERX, VSIZERY), and video incorporation mode register (VIMR) settings after the elapse of one $\overline{VVS}$ cycle. Changes to bits other than the VIE bit in the video incorporation mode register should also be made here.
3. Set the VIE bit to 1 in the video input mode register. Set bits other than VIE to the values to which they are set at that time.

Table 5.1 Registers

1. Interface Control Registers

Register Address CS	Register Address A [10:1]	R/W	Register Name	Abbreviation	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	—	—	—	—	—															
0	000	R/W	System control	SYSR	SRES	DRES	DEN			RBRK	GO	RS	DAM		DMA		DAA			
	001	R	Status	SR	TVR	FRM	DMF	CER	VBK	TRA	CSF	DBF	BRK	FEMP			Q			
	002	W	Status register clear	SRCR	TVCL	FRCL	DMCL	CECL	VBCL	TRCL	CSCL		BRCL							
	003	R/W	Interrupt enable	IER	TVE	FRE	DME	CEE	VBE	TRE	CSE		BRE							
	004	R/W	Memory mode	MEMR											MES					MWT
	005	R/W	Display mode	DSMR	FLT				WRAP	BS			TVM		SCM		RSF			
	006	R/W	Rendering mode	REMR	MODE									MWX				GBM		
	007	R/W	Input data conversion mode	IEMR												YUV	MDTP	DTP	YUV	

2. Memory Control Registers

Register Address CS	Register Address A [10:1]	R/W	Register Name	Abbreviation	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	008	R/W	Display size X	DSR							DSX									
	009	R/W	Display size Y									DSY								
	00A	R/W	Display start address 0	DSAR										DSA0						
	00B	R/W	Display start address 1											DSA1						
	00C	R/W	Display list start address H	DLSAR										DLSAH						
	00D	R/W	Display list start address L		DLSAL															
	00E	R/W	Multi-valued source area start address	SSAR	SSAL									SSAH						
	00F	R/W	Work area start address	WSAR	WSAL									WSAH						
	010	R/W	DMA transfer start address H	DMASR										DMASH						
	011	R/W	DMA transfer start address L		DMASL															
	012	R/W	DMA transfer word count L	DMAWR	DMAWL															

3. Display Control Registers

Register Address CS	Register Address A [10:1]	R/W	Register Name	Abbreviation	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	013	R/W	Display window: Horizontal display start position	DSWR								HDS								
	014	R/W	Display window: Horizontal display end position								HDE									
	015	R/W	Display window: Vertical display start position									VDS								
	016	R/W	Display window: Vertical display end position								VDE									
	017	R/W	Horizontal sync pulse width	HSWR										HSW						
	018	R/W	Horizontal scan cycle	HCR						HC										
	019	R/W	Vertical sync position	VSPR							VSP									
	01A	R/W	Vertical scan cycle	VCR							VC									
	01B	R/W	Display off output H	DOOR									DOR							
	01C	R/W	Display off output L		DOG								DOB							
	01D	R/W	Color detection H	CDER									CDR							
	01E	R/W	Color detection L		CDG								CDB							

4. Rendering Control Registers

Register Address CS	Register Address A [10:1]	R/W	Register Name	Abbreviation	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	01F	R	Command status H	CSTR										CSTH						
	020	R	Command status L		CSTL															

Table 5.1 Registers (cont)

5. Input Data Control Registers

Register Address CS	A [10:1]	R/W	Register Name		Abbreviation	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	021	R/W	Image data transfer start address	H	IDAR										IDAH						
	022	R/W		L		IDAL															
	023	R/W	Image data size	X	IDSR						IDSX										
	024	R/W		Y								IDSY									
	025	W	Image data entry		IDER	IDE															

6. Memory Control Registers (2)

Register Address CS	A [10:1]	R/W	Register Name		Abbreviation	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	026	R/W	Background start coordinate	X	BGSR							BGSX									
	027	R/W		Y				BGSY													
	028	R/W	DMA transfer word count	H	DMAWR														DMAWH		

7. Display Control Registers

Register Address CS	A [10:1]	R/W	Register Name	Abbreviation	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	029	R/W	Equalizing pulse width	EQWR										EQW						
	02A	R/W	Separation width	SPWR							SPW									
	02B	R/W	Display mode register 2	DSMR2				CDED	FRIS	VWTY	HDI6	CDEV	CSY		PRI		PED	OE2	OE1	VWE
	02C	R/W	Video display start position	VPR							HVP									
	02D	R/W										VVP								
	030	R/W	Reserved	—																
	031	R/W	Video area start address	VSAR0										VSAH0						
	032	R/W			VSAL0															
	033	R/W		VSAR1										VSAH1						
	034	R/W			VSAL1															
	035	R/W		VSAR2										VSAH2						
	036	R/W			VSAL2															
	037	R/W	Video window size	VWSZR							VWSZX									
	038	R/W										VWSZY								
	039	R/W	Video incorporation mode	VIMR	VID						VIZ2					VINM	CDEN		RGB	VIE
	03A	R/W	Cursor	CSR	BLINKA						HCS1									
	03B	R/W			BLINKB							VCS1								
	03C	R/W									HCS2									
	03D	R/W										VCS2								
	03E	R/W	Cursor 1 start address	CSAR1	CSARL1									CSARH1						
	03F	R/W	Cursor 2 start address	CSAR2	CSARL2									CSARH2						

Table 5.1 Registers (cont)

8. Rendering Control Registers (2)

CST	A [10:1]	R/W	Register Name		Abbreviation	Data (bits 15–0)
0	040	R	Current pointer	X	CURR	15–14: —; 13–0: XC
	041	R		Y		15–14: —; 13–0: YC
	042	R	Local offset	X	LCOR	15–14: —; 13–0: XO
	043	R		Y		15–14: —; 13–0: YO
	044	R	User clipping area	XMIN	UCLR	15–14: —; 13–0: UXMIN
	045	R		YMIN		15–14: —; 13–0: UYMIN
	046	R		XMAX		15–14: —; 13–0: UXMAX
	047	R		YMAX		15–14: —; 13–0: UYMAX
	048	R	System clipping area	XMAX	SCLR	15–14: —; 13–0: SXMAX
	049	R		YMAX		15–14: —; 13–0: SYMAX
	04A	R/W	Return address	H	RTNR	15–7: —; 6–0: RTNH
	04B	R/W		L		15–1: RTNL; 0: —
	04C	R/W	Rendering start address		RSAR	15–7: —; 6–0: RSA
	04D	R/W	Color offset		OCLCR	15–11: COOFR; 10–5: COOFG; 4–0: COOFB

9. Reserved

CST	A [10:1]	R/W	Register Name	Abbreviation	Data
0	04E–0FF		—	RSAR	Reserved

10. Color Palette

CST	A [10:1]	R/W	Register Name		Abbreviation	Data (bits 15–0)
0	100	R/W	Color palette	000H	CP000R	15–8: —; 7–2: R000; 1–0: —
	101	R/W		000L		15–10: G000; 9–8: —; 7–2: B000; 1–0: —
	102	R/W		001H	CP001R	15–8: —; 7–2: R001; 1–0: —
	103	R/W		001L		15–10: G001; 9–8: —; 7–2: B001; 1–0: —
	104	R/W		002H	CP002R	15–8: —; 7–2: R002; 1–0: —
	105	R/W		002L		15–10: G002; 9–8: —; 7–2: B002; 1–0: —
	⋮	⋮				⋮
	2FE	R/W		255H	CP255R	15–8: —; 7–2: R255; 1–0: —
	2FF	R/W		255L		15–10: G255; 9–8: —; 7–2: B255; 1–0: —

5.2 Register Updating

External Updating: In external updating, values set in address-mapped registers by the SuperH become effective after the end of the SuperH access. Making use of the fact that the VBK flag and FRM flag in the status register (SR) are set to 1 at the start of vertical blanking makes it possible for display control related registers, such as the color palette registers, for which the set values are updated externally to be rewritten without causing display flicker.

Internal Updating: In internal updating, values set in address-mapped registers become effective when Q2SD internal updating is performed. In the case of registers with an internal update function, therefore, display flicker can be prevented even if the SuperH modifies address-mapped registers relating to display operations without being aware of the display timing.

Internal updating is carried out while the DRES bit is set to 1 in the system control register (SYSR) and at the beginning of each frame. Internal updating is also performed at the beginning of each field for WRAP, BG , and, in interlace sync & video mode, BGSX and BGSY. The update is performed at the falling edge of $\overline{\text{VSYNC}}$ when the TV sync mode setting in the display mode register (DSMR) is TVM1 = 0, TVM0 = 0 (master mode), and on detection of the fall of $\overline{\text{EXVSYNC}}$ when TVM1 = 1 and TVM0 = 0 (TV mode). Internal updating is not performed when TVM1 = 0 and TVM0 = 1.

The address-mapped registers provided with an internal update function are shown in tables 5-1 (a) to (c). The initial values of these registers should be set while the DRES bit is set to 1. However, internal updating is used for display start address registers 0, display start address register 1, and the GBM bits in the rendering mode register in display operations. In drawing operations, external updating is used.

Internal updating is used for the video area start address, video area start coordinates, and video display size in display operations. In video incorporation operations, external updating is used.

Table 5.2 Registers with Internal Update Function

(a) Interface Control Registers

Address A[10:1]	Name	Abbreviation	Bits with Internal Update Function
000	System control register	SYSR	DEN (bit 13)
005	Display mode register	DSMR	WRAP (bit 11) BG (bit 10)
006	Rendering mode register	REMR	GBM (bits 2–0)
02B	Display mode register 2	DSMD2	All bits

(b) Memory Control Registers

Address A[10:1]	Name	Abbreviation	Bits with Internal Update Function
008	Display size register X	DSX	All bits
009	Display size register Y	DSY	All bits
00A	Display start address register 0	DSA0	All bits
00B	Display start address register 1	DSA1	All bits
026	Background start coordinate register X	BGSX	All bits
027	Background start coordinate register Y	BGSY	All bits

(c) Display Control Registers

Address A[10:1]	Name	Abbreviation	Bits with Internal Update Function
013	Display window register (horizontal display start position)	HDS	All bits
014	Display window register (horizontal display end position)	HDE	All bits
015	Display window register (vertical display start position)	VDS	All bits
016	Display window register (vertical display end position)	VDE	All bits
017	Horizontal sync pulse width register	HSW	All bits
018	Horizontal scan cycle register	HC	All bits
019	Vertical sync position register	VSP	All bits

(c) Display Control Registers (cont)

Address A[10:1]	Name	Abbreviation	Bits with Internal Update Function
01A	Vertical scan cycle register	VC	All bits
01D	Color detection register H	CDR	All bits
01E	Color detection register L	CDG, CDB	All bits
02C	Video display position register (horizontal display start position)	HVP	All bits
02D	Video display position register (vertical display end position)	VVP	All bits
031	Video area start address register 0H	VSA0H	All bits
032	Video area start address register 0L	VSA0L	All bits
033	Video area start address register 1H	VSA1H	All bits
034	Video area start address register 1L	VSA1L	All bits
035	Video area start address register 2H	VSA2H	All bits
036	Video area start address register 2L	VSA2L	All bits
037	Video window size register X	VSIZEX	All bits
038	Video window size register Y	VSIZEY	All bits
03A	Cursor register (horizontal start position 1)	BLINKA, HCS1	All bits
03B	Cursor register (vertical start position 1)	BLINKB, VCS1	All bits
03C	Cursor register (horizontal start position 2)	HCS2	All bits
03D	Cursor register (vertical start position 2)	VCS2	All bits
03E	Cursor area start address register 1	CSARL1, CASRHI	All bits
03F	Cursor area start address register 2	CSARL2, CASRH2	All bits

5.3 Interface Control Registers

The interface control registers are registers related to overall Q2SD control, mapped onto addresses (A10–A1) H'000 to H'007.

5.3.1 System Control Register (SYSR)

Register Address: H'000

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYSR	SRES	DRES	DEN	—	—	RBRK	DC	RS	DBM1	DBM0	DMA1	DMA0	DAA1	DAA0	—	—
Initial value:	1	1	0	—	—	0	0	0	*	*	0	0	0	0	—	—
R/W:	R/W	R/W	R/W	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	—	—

Note: * Value is retained.

The system control register (SYSR) is a 16-bit readable/writable register that specifies Q2SD system operation.

The SYSR is initialized as follows in a reset:

- Bits SRES and DRES are set to 1.
- Bits DEN, RBRK, DC, RS, DMA1, DMA0, DAA1, and DAA0 are cleared to 0.
- Bits DBM1 and DBM0 retain their values.

Bit 15—Software Reset (SRES): Controls execution and suspension of command processing.

Bit 15: SRES	Description
0	Command processing execution is enabled.
1	SRES is set to 1 when a hardware reset is performed. (Initial value) Clear to 0 in initialization. When this bit is set to 1 by software, a reset is performed for drawing operations only. In this case, the bit must be set to 1 for at least 16 system operating clock cycles. When SRES is set to 1, the command error flag (CER), trap flag (TRA), command suspend flag (CSF), rendering break bit (RBRK), and drawing break flag (BRK) are cleared to 0.

Bit 14—Display Reset (DRES)

Bit 13—Display Enable (DEN): These bits control starting and stopping of display synchronous operation.

Bit 14: DRES	Bit 13: DEN	Description
0	0	Display operation is started. The DRES bit cannot be cleared to 0 while the $\overline{\text{RESET}}$ pin is low. When using the Q2SD from the initial state, make all control register settings before clearing the DRES bit to 0. When the DEN bit is 0, display data has the value set in display off output registers H and L (DOORH, L).
	1	Display operation is started. The DRES bit cannot be cleared to 0 while the $\overline{\text{RESET}}$ pin is low. When using the Q2SD from the initial state, make all control register settings, clear the DRES bit to 0, and then set the DEN bit to 1. Display data has the value stored in the UGM from the next frame.
1	0	Display synchronous operation is started.(Initial value) The Q2SD only performs UGM refresh operations, regardless of the setting of TVM1 and TVM0 in the display mode register. With these settings, the Q2SD operates as shown below. When switching from DRES, DEN = 01 to DRES, DEN = 10, the setting DRES, DEN = 11 occurs temporarily for reasons relating to internal updating, but this does not affect operation. 1. Drawing is not performed even if the RS bit is set to 1 in SYSR. 2. Display data is all-0 output. 3. The VBK flag is cleared to 0 in SR. 4. Except during video incorporation (VIE = 1), waits are output continuously when UGM access is performed by the CPU or DMA controller.
	1	Setting prohibited

Bits 12 and 11—Reserved: Only 0 should be written to these bits.

Bit 10—Rendering Break (RBRK): Controls rendering (drawing) breaks. This bit should only be set when the BRK bit is cleared to 0.

Bit 10: RBRK	Description
0	The TRA bit in the status register (SR) is set to 1 by TRAP command execution, and drawing is terminated. (Initial value)
1	The currently executing command ends while the Q2SD is performing drawing, and when the next command is fetched the BRK bit in the status register (SR) is set to 1 and drawing enters the terminated state. The BRK bit does not change if this bit is set to 1 while the Q2SD is not performing drawing. After the break, the start address of the next command is placed in the command status register (CSTR). This bit is cleared to 0 only when a drawing break is effected.

Bit 9—Display Area Change (DC): Controls frame buffer switching in manual display change mode.

Bit 9: DC	Description
0	Switching of the frame buffer for display is not performed in manual display change mode. When the DC bit is 0, it can be set to 1. (Initial value)
1	Switching of the frame buffer for display is performed in manual display change mode. This bit can be set to 1 set only when it is 0. Switching is performed in frame units in non-interlace and interlace modes, and in field units in interlace sync & video mode. This bit is cleared to 0 after frame buffer switching, and so should not be cleared to 0 by the SuperH.

Bit 8—Rendering Start (RS): Specifies the start of rendering.

Bit 8: RS	Description
0	Rendering is not started. (Initial value)
1	Rendering is started. This bit is cleared to 0 after rendering starts. When this bit is set to 1, all the data held in the FIFO in the CPU interface unit is stored in the UGM. All the data held in the FIFO is also stored in the UGM when the SuperH does not access the UGM for 32 tcyc0 or longer, and when the SuperH reads the UGM.

Bits 7 and 6—Double-Buffer Mode 1 and 0 (DBM1, DBM0): These bits select double-buffer control.

Bit 7: DBM1	Bit 6: DBM0	Description
0	0	Auto display change mode is set.
	1	Auto rendering mode is set.
1	0	Manual display change mode is set.
	1	Setting prohibited

Bits 5 and 4—DMA Mode (DMA1, DMA0): These bits specify DMA transfer. Use the DMA flag (DMF) in the status register (SR) to check for the beginning and end of DMA mode.

Bit 5: DMA1	Bit 4: DMA0	Description
0	0	Normal mode is set. If DMA transfer is in progress at this time, the transfer data is not guaranteed. (Initial value)
	1	The mode for DMA transfer to memory (UGM) corresponding to $\overline{CS0}$ is set. When the remaining DMA transfer count reaches 0, this bit is automatically cleared and normal mode is entered. The initial value of the remaining DMA transfer count is determined by the setting in the DMA transfer word count register (DMAWR). The remaining DMA transfer count is an internal value in the LSI, and is decremented by 1 each time a word is processed. Do not perform UGM access by the CPU in this mode. If normal mode (DMA1 = 0, DMA0 =0) is set by the SuperH in this mode, DMA transfer will be aborted. As the value of the transfer data at the time of the abort is undefined, if an abort is performed, DMA transfer must be started over again from the beginning.
1	0	Setting prohibited
	1	The mode for DMA transfer to the register [image data entry register (IDER)] corresponding to $\overline{CS1}$ is set. In this mode, register address incrementing is not performed and all writes are to IDER. When the remaining DMA transfer count reaches 0, this bit is automatically cleared and normal mode is entered. The initial value of the remaining DMA transfer count is determined by the setting in the DMA transfer word count register (DMAWR). The remaining DMA transfer count is an LSI internal value, and is decremented by 1 each time a word is processed. Do not perform UGM access by the CPU in this mode. If normal mode (DMA1 = 0, DMA0 =0) is set by the SuperH in this mode, DMA transfer will be aborted. As the value of the transfer data at the time of the abort is undefined, if an abort is performed, DMA transfer must be started over again from the beginning.

Bits 3 and 2—DMA Address Mode (DAA1, DAA0): Sets the address mode for DMA transfer.

Bit 3: DAA1	Bit 2: DAA0	Description
0	0	Single address mode, data is latched at the rising edge of the $\overline{RD}$ signal or the $\overline{DACK}$ signal, whichever comes first. (Initial value)
	1	Single address mode, with data latched at the rise of the $\overline{DACK}$ signal. The $\overline{RD}$ signal is ignored.
1	0	Dual address mode
	1	Setting prohibited

Bit 1—Reserved: Only 0 should be written to this bit.

5.3.2 Status Register (SR)

Register Address: H'001

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SR	TVR	FRM	DMF	CER	VBK	TRA	CSF	DBF	BRK	FEMP	—	—	Q3	Q2	Q1	Q0
Initial value:	0	0	0	0	0	0	0	*	0	0	—	—	0	1	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	—	—	R	R	R	R

Note: * Value is retained.

The status register (SR) is a 16-bit read-only register used to read the internal status of the Q2SD from outside.

The SR is initialized as follows in a reset:

- The DBF flag retains its value.
- The Q flags are set to 0100.
- The FEMP flag is set to 1.
- All other flags are cleared to 0.

Bit 15—TV Sync Signal Error Flag (TVR): Flag that indicates that $\overline{\text{EXVSYNC}}$ has been detected within the vertical cycle.

Bit 15: TVR	Description
0	The rise of $\overline{\text{EXVSYNC}}$ has been detected each time within the vertical cycle determined by the vertical scan cycle register (VCR) setting after the TVR flag has been cleared by the DRES bit in SYSR or the TVCL bit in SRCR. (Initial value)
1	In TV sync mode (bits TVM1 and TVM0 = 10 in DSMR), a rise of $\overline{\text{EXVSYNC}}$ has not been detected within the vertical cycle determined by the VCR set value. The TVR flag retains its state until cleared by a reset or by software.

Bit 14—Frame Flag (FRM): Flag that indicates the vertical blanking interval after frame display.

Bit 14: FRM	Description
0	Indicates the interval from FRM flag clearing by the DRES bit in SYSR or the FRCL bit in SRCR until the end of the next display in non-interlace mode, or until the end of the next even field display in interlace mode or interlace sync & video mode. (Initial value)
1	Indicates the interval from the first even field vertical blanking interval after FRM flag clearing by the DRES bit in SYSR or the FRCL bit in SRCR until the FRM flag is cleared again (switched in frame units).

Bit 13—DMA Flag (DMF): Flag that indicates that DMA transfer mode has been initiated and transfer has been completed.

Bit 13: DMF	Description
0	DMA transfer mode has not been initiated at all since DMF flag clearing by the DMCL bit in SRCR, or the next DMA transfer mode (bits DMA1 and DMA0 = 01 or 11 in SYSR) has been initiated and the remaining transfer count has not yet reached 0. (Initial value)
1	DMA transfer mode has been initiated and the transfer word count has reached 0. The DMF flag retains its state until cleared by a reset or by software.

Bit 12—Command Error Flag (CER): Flag that indicates that an illegal command has been fetched.

Bit 12: CER	Description
0	Normal state. An illegal command has not been fetched since CER flag clearing by the SRES bit in SYSR or the CECL bit in SRCR. An illegal command is one in which the upper 5 bits of the command code are undefined. The Q2SD does not check the legality of the rendering attributes in the lower 11 bits. (Initial value)
1	Drawing operation halt state. Drawing operation remains halted because an illegal command was fetched after CER flag clearing by the SRES bit in SYSR or the CECL bit in SRCR. The CER flag retains its state until cleared by a reset or by software.

Bit 11—Vertical Blanking Flag (VBK): Flag that indicates the vertical blanking interval.

Bit 11: VBK	Description
0	Indicates the interval from VBK flag clearing by the DRES bit in SYSR or the VBCL bit in SRCR until the end of the next display. (Initial value)
1	Indicates the interval from the first vertical blanking interval after VBK flag clearing by the DRES bit in SYSR or the VBCL bit in SRCR until the VBK flag is cleared again (switched in field units).

Bit 10—Trap Flag (TRA): Flag that indicates the end of command execution.

Bit 10: TRA	Description
0	Indicates the interval from TRA flag clearing by the SRES bit in SYSR or the TRCL bit in SRCR until the end of execution of the next command. (Initial value)
1	Command execution has ended, or the current command is not being executed. The TRA flag retains its state until cleared by a reset or by software.

Bit 9—Command Suspend Flag (CSF): Flag that indicates that command execution has been suspended due to a frame change in auto display change mode or manual display change mode.

Bit 9: CSF	Description
0	Normal operation (Initial value)
1	A rendering end interrupt has not been generated in the interval from CSF flag clearing by the SRES bit in SYSR or the CSCL bit in SRCR until the next frame change. The CSF flag retains its state until cleared by a reset or by software.

Bit 8—Display Buffer Frame (DBF): Flag that indicates the display start address register used as the display start address by the Q2SD.

Bit 8: DBF	Description
0	Address indicated by DSAR0 is being used as display start address.
1	Address indicated by DSAR1 is being used as display start address.

Bit 7—Drawing Break Flag (BRK): Flag that indicates a drawing break.

Bit 7: BRK	Description
0	Indicates the interval until the next drawing break occurs after the BRK flag is cleared by the SRES bit in SYSR or the BRCL bit in SRCR. (Initial value)
1	Indicates that a command is not currently being executed due to a drawing break directive. The BRK flag retains its state until cleared by a reset or by software.

Bit 6—FIFO Empty Flag (FEMP): Transfer data from the CPU to the UGM is temporarily stored in a FIFO. These transfers include UGM writes and data transfers via IDR. This flag indicates whether there is UGM storage data in the FIFO.

Bit 6: FEMP	Description
0	There is UGM storage data in the FIFO.
1	There is no UGM storage data in the FIFO. (Initial value)

Bits 5 to 4—Reserved: These bits always read 0.

Bits 3 to 0—Q Flags (Q3 to Q0): Flags used for Q2SD Series product identification. In the Q2SD, these flags read 0100.

Bit 3: Q3	Bit 2: Q2	Bit 1: Q1	Bit 0: Q0	Description
0	0	1	0	HD64411 (Q2)
0	0	1	1	HD64412 (Q2i)
0	1	0	0	HD64413A (Q2SD)

5.3.3 Status Register Clear Register (SRCR)

Register Address: H'002

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SRCR	TVCL	FRCL	DMCL	VBCL	TRCL	CSCL	—	BRCL	—	—	—	—	—	—	—	—
Initial value:	*	*	*	*	*	*	—	*	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	—	R/W	—	—	—	—	—	—	—	—

Note: * Value is retained.

The status register clear register (SRCR) is a 16-bit write-only register that clears the corresponding flags in the status register (SR). Writing 1 to one of bits 15 to 9 or 7 in the SRCR register will clear the corresponding flag in SR to 0. When SR clearing is completed, the value of the SRCR register is cleared to all-0 internally (a read will return 0).

Bit	Bit Name	Abbreviation	Description
15	TV sync signal error flag clear	TVCL	Writing 1 to the TCVL bit clears the TVR flag to 0 in SR.
14	Frame buffer clear	FRCL	Writing 1 to the FRCL bit clears the FRM flag to 0 in SR.
13	DMA flag clear	DMCL	Writing 1 to the DMCL bit clears the DMF flag to 0 in SR.
12	Command error flag clear	CECL	Writing 1 to the CECL bit clears the CER flag to 0 in SR.
11	Vertical blanking flag clear	VBCL	Writing 1 to the VBCL bit clears the VBK flag to 0 in SR.
10	Trap flag clear	TRCL	Writing 1 to the TRCL bit clears the TRA flag to 0 in SR.
9	Command suspend flag clear	CSCL	Writing 1 to the CSCL bit clears the CSF flag to 0 in SR.
7	Drawing break flag clear	BRCL	Writing 1 to the BRCL bit clears the BRK flag to 0 in SR.
8, 6–0	Reserved	—	Only 0 should be written to these bits.

5.3.4 Interrupt Enable Register (IER)

Register Address: H'003

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IER	TVE	FRE	DME	CEE	VBE	TRE	CSE	—	BRE	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	—	0	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	—	R/W	—	—	—	—	—	—	—

The interrupt enable register (IER) is a 16-bit readable/writable register that enables or disables interrupts by the corresponding flags in the status register (SR). When a bit in SR is set to 1 and the bit at the corresponding bit position in the IER register is also 1, $\overline{IRL}$ is driven low and an interrupt request is sent to the CPU.

The interrupt generation condition is as follows.

Interrupt generation condition = $\overline{IRL} = \overline{a+b+c+d+e+f+g}$

a = TVR TVE
b = FRM FRE
c = DMF DME
d = CER CEE
e = VBK VBE
f = TRA TRE
g = CSF CSE
h = BRK BRE

Bit 15—TV Sync Signal Error Flag Enable (TVE): Enables or disables interrupts initiated by the TVR flag in SR.

Bit 15: TVE	Description
0	Interrupts initiated by the TVR flag in SR are disabled. (Initial value)
1	Interrupts initiated by the TVR flag in SR are enabled. When TVR TVE = 1, an $\overline{IRL}$ interrupt request is sent to the CPU.

Bit 14—Frame Flag Enable (FRE): Enables or disables interrupts initiated by the FRM flag in SR.

Bit 14: FRE	Description
0	Interrupts initiated by the FRM flag in SR are disabled. (Initial value)
1	Interrupts initiated by the FRM flag in SR are enabled. When FRM FRE = 1, an $\overline{\text{IRL}}$ interrupt request is sent to the CPU.

Bit 13—DMA Flag Enable (DME): Enables or disables interrupts initiated by the DMF flag in SR.

Bit 13: DME	Description
0	Interrupts initiated by the DMF flag in SR are disabled. (Initial value)
1	Interrupts initiated by the DMF flag in SR are enabled. When DMF DME = 1, an $\overline{\text{IRL}}$ interrupt request is sent to the CPU.

Bit 12—Command Error Flag Enable (CEE): Enables or disables interrupts initiated by the CER flag in SR.

Bit 12: CEE	Description
0	Interrupts initiated by the CER flag in SR are disabled. (Initial value)
1	Interrupts initiated by the CER flag in SR are enabled. When CER CEE = 1, an $\overline{\text{IRL}}$ interrupt request is sent to the CPU.

Bit 11—Vertical Blanking Flag Enable (VBE): Enables or disables interrupts initiated by the VBK flag in SR.

Bit 11: VBE	Description
0	nterrupts initiated by the VBK flag in SR are disabled. (Initial value)
1	Interrupts initiated by the VBK flag in SR are enabled. When VBK VBE = 1, an $\overline{\text{IRL}}$ interrupt request is sent to the CPU.

Bit 10—Trap Flag Enable (TRE): Enables or disables interrupts initiated by the TRA flag in SR.

Bit 10: TRE	Description
0	Interrupts initiated by the TRA flag in SR are disabled. (Initial value)
1	Interrupts initiated by the TRA flag in SR are enabled. When TRA TRE = 1, an IRL interrupt request is sent to the CPU.

Bit 9—Command Suspend Flag Enable (CSE): Enables or disables interrupts initiated by the CSF flag in SR.

Bit 9: CSE	Description
0	Interrupts initiated by the CSF flag in SR are disabled. (Initial value)
1	Interrupts initiated by the CSF flag in SR are enabled. When CSF CSE = 1, an IRL interrupt request is sent to the CPU.

Bit 7—Drawing Break Flag Enable (BRE): Enables or disables interrupts initiated by the BRK flag in SR.

Bit 7: BRE	Description
0	Interrupts initiated by the BRK flag in SR are disabled. (Initial value)
1	Interrupts initiated by the BRK flag in SR are enabled. When BRK BRE = 1, an IRL interrupt request is sent to the CPU.

Bits 8 and 6 to 0—Reserved: Only 0 should be written to these bits.

5.3.5 Memory Mode Register (MEMR)

Register Address: H'004

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MEMR	—	—	—	—	—	—	—	—	—	—	MES1	MES0	—	—	—	MAT
Initial value:	—	—	—	—	—	—	—	—	—	—	0	0	—	—	—	0
R/W:	—	—	—	—	—	—	—	—	—	—	R/W	R/W	—	—	—	R/W

Note: * Value is retained.

The memory mode register (MEMR) is a 16-bit readable/writable register that specifies the size of UGM used and the memory access timing.

If the value of this register is modified during a memory access, operation will be temporarily unstable.

The MEMR bits MES1, MES0, and MAT are initialized to 0 by a reset.

Bits 15 to 6—Reserved: Only 0 should be written to these bits.

Bits 5 and 4—Memory Size (MES1, MES0): These bits select the size and quantity of memories used for the UGM.

Bit 5: MES1	Bit 4: MES0	Description
0	0	One 16-Mbit (×16) memory, 16-bit bus
	1	Two 16-Mbit (×16) memories, 32-bit bus
1	0	One 64-Mbit (×16) memory, 16-bit bus
	1	One 64-Mbit (×32) memory, 32-bit bus

Bits 3 to 1—Reserved: Only 0 should be written to these bits.

Bit 0—Memory Access Timing (MAT): Sets the UGM access timing.

	UGM Access Timing			
Bit 0: MAT	APL (Active Precharge Latency)	PI (Precharge Latency)	PCL (RAS-CAS Latency)	WPL (Write Precharge Latency)
0	5	3	3	2
1	5	2	2	**2**

5.3.6 Display Mode Register (DSMR)

Register Address: H'005

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DSMR	FLT	—	—	—	WRAP	BG	—	—	TVM1	TVM0	SCM1	SCM0	REF3	REF2	REF1	REF0
Initial value:	0	—	—	—	0	0	—	—	1	0	*	*	1	0	0	0
R/W:	R/W	—	—	—	R/W	R/W	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: * Value is retained.

The display mode register (DSMR) is a 16-bit readable/writable register that specifies Q2SD display operations.

If the value of this register is modified during a display operation, operation will be temporarily unstable.

The DSMR is initialized as follows in a reset:

Bits WRAP and BG are initialized to 0, bits TVM1 and TVM0 to 10, and bits REF3 to REF0 to 1000.

The SCM1 and SCM0 bits retain their values.

Bit 15—Filter Mode (FLT)

Bit 15: FLT	Description
0	FG and BG pixel data is output for display as the respective screens.
1	FG and BG pixel data is averaged and output for display as the FG screen. Set GBM = 001/101, VWE = 0, PRI = 00, FBD = 0, SCM = 11. FG transparent color determination is not performed. Transparent color determination (CDE) is performed on the result. Set the BG start position one line below the FG start position. The average is found by right-shifting the result of addition of each part in 16-bit format (5:6:5). A fraction of a shift is ignored.

Bits 14 to 12—Reserved: Only 0 should be written to these bits.

Bit 11—Background Screen Wraparound Mode Configuration (WRAP)

Bit 11: WRAP	Description
0	Background screen wraparound is not performed. Display contents are not guaranteed if the display area extends beyond the memory installation space. (Initial value)
1	Background screen wraparound is performed. The wraparound units are the number of pixels specified by the MWX bit in the rendering mode register (REMR) in the X direction, and 512 pixels in the Y direction. The start coordinates of this area are indicated by bits 13 to 9 of background start address register BGSY.

Bit 10—Background Screen Combination (BG)

Bit 10: BG	Description
0	Background screen combination is not performed. (Initial value)
1	Background screen combination is performed.

Bits 9 and 8—Reserved: Only 0 should be written to these bits.

Bits 7 and 6—TV Sync Mode (TVM1, TVM0): These bits specify TV sync mode, in which synchronous operation is performed by means of $\overline{\mathrm{EXHSYNC}}$ and $\overline{\mathrm{EXVSYNC}}$ input from an external source, or master mode, in which $\overline{\mathrm{HSYNC}}$ and $\overline{\mathrm{VSYNC}}$ are output.

Bit 7: TVM1	Bit 6: TVM0	Description
0	0	Master mode is set. The Q2SD outputs $\overline{\mathrm{HSYNC}}$, $\overline{\mathrm{VSYNC}}$, and $\overline{\mathrm{ODDF}}$ signals. In this mode, when CSY1 = 1 in display mode register 2 (DSMR2), set initial values in the equalizing pulse width register (EQWR) and separation width register (SPWR).
	1	Synchronization system switching mode is set. Switching is performed from TV sync mode to master mode, or vice versa, via this mode. In this mode, display operations are forcibly halted and the DISP pin output goes low. The clock supply to the CLK1 pin can also be stopped (input invalidated) (fixed high within the chip). The $\overline{\mathrm{HSYNC}}$, $\overline{\mathrm{VSYNC}}$, and $\overline{\mathrm{ODDF}}$ pins are inputs.
1	0	TV sync mode is set. $\overline{\mathrm{EXHSYNC}}$, $\overline{\mathrm{EXVSYNC}}$, and $\overline{\mathrm{ODDF}}$ signals are input to the Q2SD. CSYNC output is fixed high. In this mode, clear both CSY1 and CSY0 to 0 in display mode register 2 (DSMR2). (Initial value)
	1	Setting prohibited

Bits 5 and 4—Scan Mode (SCM1, SCM0): These bits specify the display output scan mode and the unit of display switching.

Bit 5: SCM1	Bit 4: SCM0	Description
0	0	Non-interlace mode: Frame buffer switching can be performed in 1-VC units.
	1	Setting prohibited
1	0	Interlace mode: Frame buffer switching can be performed in 2-VC units.
	1	Interlace sync & video mode: Frame buffer switching can be performed in 1-VC units.

Bits 3 to 0—Refresh Cycles (REF3 to REF0): These bits specify the number of cycles for which refreshing is performed within one raster in the display screen area.

Bit 3: REF3	Bit 2: REF2	Bit 1: REF1	Bit 0: REF0	Description
0	0	0	0	Refresh timing is not output
			1	Number of refresh cycles = 1
		1	0	Number of refresh cycles = 2
			1	Number of refresh cycles = 3
	1	0	0	Number of refresh cycles = 4
			1	Number of refresh cycles = 5
		1	0	Number of refresh cycles = 6
			1	Number of refresh cycles = 7
1	0	0	0	Number of refresh cycles = 8 (Initial value)
			1	Number of refresh cycles = 9
		1	0	Number of refresh cycles = 10
			1	Number of refresh cycles = 11
	1	0	0	Number of refresh cycles = 12
			1	Number of refresh cycles = 13
		1	0	Number of refresh cycles = 14
			1	Number of refresh cycles = 15

5.3.7 Display Mode Register 2 (DSMR2)

Register Address: H'02B

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DSMR2	—	—	—	CDED	PRI2	VWRY	HDIS	ODEV	CSY1	CSY0	PRI	—	FBD	CE2	CE1	VWE
Initial value:	—	—	—	0	0	0	0	0	*	*	0	—	0	0	0	0
R/W:	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	—	R/W	R/W	R/W	R/W

Note: * Value is retained.

The display mode register 2 (DSMR2) is a 16-bit readable/writable register that specifies Q2SD display operations. If the value of this register is modified during a display operation, operation will be temporarily unstable.

In a reset, bits CSY1 and CYS0 retain their values, and the other bits are cleared to 0.

Bits 15 to 13—Reserved: Only 0 should be written to these bits.

Bit 12—CDE Disable (CDED): Controls CDE pin output. In TV sync mode (TVM1 = 1, TVM0 = 0), the CDE pin is used to switch between external sync signal generation circuit video output and Q2SD analog R/G/B output.

Bit 12: CDED	Description
0	CDE pin output is enabled. (Initial value)
1	CDE pin output is disabled.

Bits 11 and 5—Window Priority (PRI2, PRI): These bits set the screen display priority.

Bit 11: PRI2	Bit 5: PRI	Description
0	0	Screen priority order is: cursor 1, cursor 2, foreground, video, background. (Initial value)
	1	Setting prohibited
1	0	Screen priority order is: cursor 1, foreground, video, cursor 2, background.
	1	Screen priority order is: foreground, video, cursor 1, cursor 2, background.

Bit 10—Video Window RGB/YC Mode (VWRY): Selects whether the data displayed in the video window is stored in the UGM in RGB format or YC format.

Bit 10: VWRY	Description
0	Video window displays RGB data in the UGM as RGB data. (Initial value)
1	Video window displays YC data in the UGM as RGB data.

Bit 9—[Mode in which Foreground Screen 1 Starts at x = 512 in Case of 1024-Pixel Memory Width] (HDIS): When HDIS = 1, use is possible when GBM = 000 or 001 and RSAE = 0.

Bit 9: HDIS	Description
0	Foreground screen 1 starts at x = 0. (Initial value)
1	Foreground screen 1 starts at x = 512.

Bit 8—$\overline{ODDF}$ Signal Polarity Select (ODEV): Selects the polarity of the $\overline{ODDF}$ signal.

Bit 8: ODEV	Description
0	$\overline{ODDF}$ goes low in first-half field in same frame of interlace display. (Initial value)
1	$\overline{ODDF}$ goes high in first-half field in same frame of interlace display.

Bits 7 and 6—$\overline{CSYNC}$ Mode (CSY1, CSY0): These bits select the $\overline{CSYNC}$ signal output mode in master mode (TVM1 = 0, TVM0 = 0).

When CSY1 = 1, values must be set in the equalizing pulse width register (EQWR) and separation width register (SPWR).

Bit 7: CSY1	Bit 6: CSY0	Description
0	0	Waveform determined by exclusive logical OR of $\overline{VSYNC}$ and $\overline{HSYNC}$ is output as $\overline{CSYNC}$. In TV sync mode (TVM1 = 1, TVM0 = 0), this mode should be selected.
	1	Setting prohibited
1	0	Equalizing pulses are output in 3-raster period from fall of $\overline{VSYNC}$, separation in next 3-raster period, equalizing pulses in next 3-raster period, and $\overline{HSYNC}$ waveform in other periods.
	1	Equalizing pulses are output in 2.5-raster period starting 0.5 raster after fall of $\overline{VSYNC}$, separation in next 2.5-raster period, equalizing pulses in next 2.5-raster period, and $\overline{HSYNC}$ waveform in other periods.

Bit 4—Reserved: Only 0 should be written to this bit.

Bit 3—Foreground Disable (FBD): Selects display or non-display of the foreground screen.

Bit 3: FBD	Description	
0	Foreground screen is displayed.	(Initial value)
1	Foreground screen is not displayed.	

Bit 2—Cursor 2 Enable (CE2): Selects display or non-display of cursor 2.

Bit 2: CE2	Description	
0	Cursor 2 is not displayed.	(Initial value)
1	Cursor 2 is displayed. Cursor blinking is always performed. To give the appearance of a non-blinking cursor, make the same setting for cursor blink shapes A and B stored in the cursor area. In Q2SD cursor blinking, cursor blink shapes A and B are displayed alternately. To provide a period in which the cursor is not displayed, make one entire waveform a transparent color.	

Bit 1—Cursor 1 Enable (CE1): Selects display or non-display of cursor 1.

Bit 1: CE1	Description	
0	Cursor 1 is not displayed.	(Initial value)
1	Cursor 1 is displayed. Cursor blinking is always performed. To give the appearance of a non-blinking cursor, make the same setting for cursor blink shapes A and B stored in the cursor area. In Q2SD cursor blinking, cursor blink shapes A and B are displayed alternately. To provide a period in which the cursor is not displayed, make one entire waveform a transparent color.	

Bit 0—Video Window Enable (VWE): Selects display or non-display of the video window.

Bit 0: VWE	Description	
0	Video window is not displayed.	(Initial value)
1	Video window is displayed. The display contents are not guaranteed if this bit is set before VID changes after VIE is set to 1.	

5.3.8 Rendering Mode Register (REMR)

Register Address: H'006

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REMR	RSAE	—	—	—	—	—	—	—	—	MWX	—	—	—	GBM2	GBM1	GBM0
Initial value:	0	—	—	—	—	—	—	—	—	*	—	—	—	*	*	*
R/W:	R/W	—	—	—	—	—	—	—	—	R/W	—	—	—	R/W	R/W	R/W

Note: * Value is retained.

The rendering mode register (REMR) is a 16-bit readable/writable register that specifies Q2SD rendering operations.

If the value of this register is modified during a drawing operation, operation will be temporarily unstable. The exception is modification by a WPR command from the display list, in which case the following conditions must be satisfied:

- Changing the MWX setting is prohibited.
- For the GBM bits, only the drawing bit configuration can be changed; changing the display bits is prohibited.
- RSAE can be changed, on condition that the change agrees with the GBM setting.

In a reset, the RSAE bit in the REMR register is cleared to 0, while the MWX and GBM bits retain their values.

Bit 15—Drawing Start Address Enable (RSAE): Allows the drawing area to be set separately from the display area. The start address of a drawing area separate from the display area is set in the drawing start address register (RSAR).

Bit 15: RSAE	Description
0	Value in display start address register (DSAR) is used for drawing area. When this setting is made, the GBM setting must be 000 or 001. (Initial value)
1	Value in rendering start address register (RSAR) is used for drawing area.

Bits 14 to 7—Reserved: Only 0 should be written to these bits.

Bit 6—Memory Width (MWX): Specifies the X-direction logical coordinate space of the UGM connected to the Q2SD.

Bit 6: MWX	Description
0	X-direction logical coordinate space is 512 pixels
1	X-direction logical coordinate space is 1024 pixels

Bits 5 to 3—Reserved: Only 0 should be written to these bits.

Bits 2 to 0—Graphic Bit Mode 2 to 0 (GBM2 to GBM0): These bits specify the bit configuration of the rendering data and display data handled by the Q2SD.

Note that the setting of these bits may be linked to the RSAE bit setting.

			Description			
Bit 2: GBM2	Bit 1: GBM1	Bit 0: GBM0	FG Bit Configuration	BG Bit Configuration	Rendering Bit Configuration	RSAE Bit Setting
0	0	0	8 bits/pixel	8 bits/pixel	8 bits/pixel	0 or 1
		1	16 bits/pixel	16 bits/pixel	16 bits/pixel	0 or 1
	1	0	8 bits/pixel	16 bits/pixel	8 bits/pixel	0 or 1
		1	16 bits/pixel	8 bits/pixel	16 bits/pixel	0 or 1
1	0	0	8 bits/pixel	8 bits/pixel	16 bits/pixel	Must be 1
		1	16 bits/pixel	16 bits/pixel	8 bits/pixel	Must be 1
	1	0	8 bits/pixel	16 bits/pixel	16 bits/pixel	Must be 1
		1	16 bits/pixel	8 bits/pixel	8 bits/pixel	Must be 1

5.3.9 Input Data Conversion Mode Register (IEMR)

Register Address: H'007

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IEMR	—	—	—	—	—	—	—	—	—	—	—	YUV2	MDTP	DTP	YUV1	YUV0
Initial value:	—	—	—	—	—	—	—	—	—	—	—	0	0	0	0	0
R/W:	—	—	—	—	—	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W

The input data conversion mode register (IEMR) is a 16-bit readable/writable register that specifies the conversion format for input data from the SuperH.

If the value of this register is modified during a data conversion, operation will be temporarily unstable.

In a reset, all IEMR bits are cleared to 0.

Bits 15 to 5—Reserved: Only 0 should be written to these bits.

Bits 4, 1, and 0—YUV Mode (YUV2, YUV1, YUV0): These bits specify whether data input in YUV or ΔYUV format is to be converted to RGB format before being stored in the UGM.

Bit 4: YUV2	Bit 1: YUV1	Bit 0: YUV0	Description
0	0	0	Normal mode is set. Data transfer via IDER is not performed. Also used when setting YUV2, 1, 0 to (0, 1, 1). (Initial value)
		1	YUV-RGB conversion is performed. When the total number of data conversion pixels reaches 0, these bits are automatically cleared and normal mode is entered. The total number of data conversion pixels is the product of the IDSX and IDSY set values in the image data size register (IDSR). The total number of data conversion pixels is decremented by 1 in the LSI each time a pixel is processed. Do not perform VGM access using the $\overline{CS0}$ pin in this mode.
	1	0	ΔYUV-RGB conversion is performed. When the total number of data conversion pixels reaches 0, these bits are automatically cleared and normal mode is entered. The total number of data conversion pixels is the product of the IDSX and IDSY set values in the image data size register (IDSR). The total number of data conversion pixels is decremented by 1 in the LSI each time a pixel is processed. Do not perform VGM access using the $\overline{CS0}$ pin in this mode.
		1	16-bit/pixel data is simply transferred, without conversion. When the total number of data conversion pixels reaches 0, these bits are automatically cleared and normal mode is entered. The total number of data conversion pixels is the product of the IDSX and IDSY set values in the image data size register (IDSR). The total number of data conversion pixels is decremented by 1 in the LSI each time a pixel is processed. Do not perform VGM access using the $\overline{CS0}$ pin in this mode.
1	0	0	Used when setting YUV2, 1, 0 to (1, 1, 1).
		1	Setting prohibited
	1	0	Setting prohibited
		1	8-bit/pixel data is simply transferred, without conversion. When the total number of data conversion pixels reaches 0, these bits are automatically cleared and normal mode is entered. The total number of data conversion pixels is the product of the IDSX and IDSY set values in the image data size register (IDSR). Set the number of transfer words (1/2 the number of pixels) as the IDSX value. The total number of data conversion pixels is decremented by 1 in the LSI each time a pixel is processed. Do not perform VGM access using the $\overline{CS0}$ pin in this mode.

Bit 3—Memory Data Type Mode (MDTP): Specifies whether byte-unit swapping is to be performed in a word access UGM memory write transfer from the SuperH. This bit is valid when bits YUV2 to YUV0 are set to 000, and bits DMA1 and DMA0 are set to either 00 or 01.

This bit is invalid for register writes from the SuperH, and also for UGM memory read operations by the SuperH.

Bit 3: MDTP	Description
0	Byte-unit swapping is not performed in a word access UGM memory write transfer from the SuperH. (Initial value)
1	In a word access UGM memory write transfer from the SuperH, the upper and lower bytes are swapped within the same word (16 bits).

Bit 2—Data Type Mode (DTP): Specifies whether byte-unit swapping is to be performed in a transfer. This bit is valid for data transfers via the image entry data register (IDER). This bit is valid when bits YUV2 to YUV0 are set to 001, 010, 011, or 111, and bits DMA1 and DMA0 are set to either 00 or 11.

Bit 2: DTP	Description
0	Byte-unit swapping is not performed in a transfer via IDER. (Initial value)
1	In a transfer via IDER, the upper and lower bytes are swapped within the same word (16 bits).

5.4 Memory Control Registers

The memory control registers are registers related to the UGM (unified graphics memory) configuration, mapped onto addresses (A10–A1) H'008 to H'012 and H'04C.

5.4.1 Display Size Registers (DSR)

Register Address: H'008

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	DSX									
Initial value:	—	—	—	—	—	—	*	*	*	*	*	*	*	*	*	*
R/W:	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Register Address: H'009

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	DSY								
Initial value:	—	—	—	—	—	—	—	*	*	*	*	*	*	*	*	*
R/W:	—	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: * Value is retained.

The display size registers (DSR) are two 16-bit readable/writable registers that specify the size of the display screen. The number of dots in the horizontal direction is set in DSX, and the number of dots in the vertical direction in DSY.

Write 0 to bits that are not used for the DSX and DSY fields (a read will return an undefined value).

The DSX and DSY fields in the DSR registers retain their values in a reset.

5.4.2 Display Address Registers (DSAR)

Register Address: H'00A

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	DSA0 (address A22–A16 setting)						
Initial value:	—	—	—	—	—	—	—	—	—	*	*	*	*	*	*	*
R/W:	—	—	—	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Register Address: H'00B

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	DSA1 (address A22–A16 setting)						
Initial value:	—	—	—	—	—	—	—	—	—	*	*	*	*	*	*	*
R/W:	—	—	—	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: * Value is retained.

The display address registers (DSAR) are two 16-bit readable/writable registers that specify the memory areas to be used as UGM frame buffers.

Only the upper 7 bits (A22 to A16) of the start physical address of frame buffer 0 (FB0) are set in the DSA0 field in DSAR, and only the upper 7 bits (A22 to A16) of the start physical address of frame buffer 1 (FB1) are set in the DSA1 field in DSAR.

The display address register whose contents are actually valid as the display start address is the register indicated by the DBF bit in the status register (SR). The display address register whose contents are not valid as the display start address indicates the rendering coordinate origin when RASE = 0 in the rendering mode register (REMR). When these registers are modified, the new set value becomes valid when an internal update is performed in the case of the display address register whose contents are valid as the display start address, and when an external update (rewrite) is performed in the case of the display address register that indicates the rendering coordinate origin.

Write 0 to bits that are not used for the DSA0 and DSA1 fields.

The DSA0 and DSA1 fields in the DSAR registers retain their values in a reset.

5.4.3 Display List Start Address Registers (DLSAR)

Register Address: H'00C to H'00D

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	DLSAH (address A22–A16 setting)						
Initial value:	—	—	—	—	—	—	—	—	—	*	*	*	*	*	*	*
R/W:	—	—	—	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DLSAL (address A15–A5 setting)											—	—	—	—	—
Initial value:	*	*	*	*	*	*	*	*	*	*	*	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	—	—	—	—	—

Note: * Value is retained.

The display list start address registers (DLSAR) are 16-bit readable/writable registers that specify the memory area to be used as the display list.

The DLSAH and DLSAL fields in DLSAR contain a total of 18 bits, and only the upper bits (A22 to A5) of the start physical address of the display list are set in these fields.

Write 0 to bits that are not used for the DLSAH and DLSAL fields (a read will return an undefined value).

The DLSAH and DLSA fields in the DLSAR registers retain their values in a reset.

5.4.4 Multi-Valued Source Area Start Address Register (SSAR)

Register Address: H'00E

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SSAL (address A15–A13 setting)			—	—	—	—	—	—	SSAH (address A22–A17 setting)						
Initial value:	*	*	*	—	—	—	—	—	—	*	*	*	*	*	*	*
R/W:	R/W	R/W	R/W	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: * Value is retained.

The multi-valued source area start address register (SSAR) is a 16-bit readable/writable register that specifies the memory area to be used as the multi-valued source area. The upper bits (A22 to A16) of the start physical address of the source area are set in the SSAH field, and the lower bits (A15 to A13) in the SSAL field.

The settable bit range depends on the highest color representation mode and maximum memory width used in each of the display, drawing, and video areas. In 8-bit/pixel mode with a 512-pixel memory width, all bits can be set. In 8-bit/pixel mode with a 1024-pixel memory width, or 16-bit/pixel mode with a 512-pixel memory width, bit 13 should be cleared to 0. In 16-bit/pixel mode with a 1024-pixel memory width, bits 14 and 13 should be cleared to 0.

Bits 12 to 7 of SSAR are reserved. Only 0 should be written to these bits (a read will return an undefined value).

The SSAH and SSAL fields in the SSAR register retain their values in a reset.

5.4.5 Work Area Start Address Register (WSAR)

Register Address: H'00F

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WSAL (address A15–A13 setting)			—	—	—	—	—	—	WSAH (address A22–A16 setting)						
Initial value:	*	*	*	—	—	—	—	—	—	*	*	*	*	*	*	*
R/W:	R/W	R/W	R/W	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: * Value is retained.

The work area start address register (WSAR) is a 16-bit readable/writable register that specifies the memory area to be used as the work area. The upper bits (A22 to A16) of the start physical address of the work area are set in the WSAH field, and the lower bits (A15 to A13) in the WSAL field.

The settable bit range depends on the highest color representation mode and maximum memory width used in each of the display, drawing, and video areas. In 8-bit/pixel mode with a 512-pixel memory width, all bits can be set. In 8-bit/pixel mode with a 1024-pixel memory width, or 16-bit/pixel mode with a 512-pixel memory width, bit 13 should be cleared to 0. In 16-bit/pixel mode with a 1024-pixel memory width, bits 14 and 13 should be cleared to 0.

Bits 12 to 7 of WSAR are reserved. Only 0 should be written to these bits (a read will return an undefined value).

The WSAH and WSAL fields in the WSAR register retain their values in a reset.

5.4.6 DMA Transfer Start Address Registers (DMASR)

Register Address: H'010 to H'011

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	DMASH (address A22–A16 setting)						
Initial value:	—	—	—	—	—	—	—	—	—	0	0	0	0	0	0	0
R/W:	—	—	—	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DMASL (address A15–A1 setting)															—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	—

The DMA transfer start address registers (DMASR) are 16-bit readable/writable registers that specify the start address of the transfer destination UGM in a DMA transfer.

The upper bits (A22 to A16) of the start address are set in the DMASH field in DMASR, and the lower bits (A15 to A1) in the DMASL field in DMASR.

If the value of these registers is modified during a series of DMA operations from the time bits DMA1 and DMA0 in the system control register (SYSR) are set to 01 by the CPU until they are cleared automatically by the Q2SD, operation will be unstable.

When bits DMA1 and DMA0 are set to 11, the value in these registers is not referenced. Transfer data passes via the image data entry register (IDER), is converted, and stored sequentially starting at the data transfer start address indicated by the image data transfer start address register (ISAR).

The address (A22 to A1) indicated by the DMASH and DMASL fields is a word address.

Write 0 to bits that are not used for the DMASH and DMASL fields (a read will return an undefined value).

The values of the DMASH and DMASL fields in the DMASR registers are initialized to all-0 by a reset.

These registers are not incremented when DMA transfer is performed.

5.4.7 DMA Transfer Word Count Registers (DMAWR)

Register Address: H'028

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	DMAWH		
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	0	0	0
R/W:	—	—	—	—	—	—	—	—	—	—	—	—	—	R/W	R/W	R/W

Register Address: H'012

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DMAWL															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The DMA transfer word count registers (DMAWR) are two 16-bit readable/writable registers that specify the number of words (1 word = 16 bits) to be transferred in DMA transfer.

If the value of these registers is modified during a series of DMA operations from the time bits DMA1 and DMA0 in the system control register (SYSR) are set to 01 or 11 by the CPU until they are cleared automatically by the Q2SD, operation will be unstable.

When bits DMA1 and DMA0 are set to 11, the value in these registers is not referenced. Transfer data passes via the image data entry register (IDER), is converted, and stored sequentially starting at the data transfer start address indicated by the image data transfer start address register (ISAR).

Write 0 to bits that are not used for the DMAWH and DMAWL fields (a read will return an undefined value).

The values of the DMAWH and DMAWL fields in the DMAWR registers are initialized to all-0 by a reset.

These registers are not decremented when DMA transfer is performed.

5.4.8 Rendering Start Address Register (RSAR)

Register Address: H'04C

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	RSA (address A22–A16 setting)						
Initial value:	—	—	—	—	—	—	—	—	—	*	*	*	*	*	*	*
R/W:	—	—	—	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: * Value is retained.

The rendering start address register (RSAR) is a 16-bit readable/writable register that specifies the start address of the rendering area that is valid when the RSAE bit is set to 1 in the rendering mode register (REMR).

Only the upper 7 bits (A22 to A16) of the start physical address of the rendering area are set in the RSA field.

Bits 15 to 7 of RSAR are reserved. Only 0 should be written to these bits (a read will return an undefined value).

The RSA field in the RSAR register retains its value in a reset.

5.5 Display Control Registers

The display control registers are used to set the display timing, and are mapped onto addresses (A10–A1) H'013 to H'01E and H'02B to H'03F.

5.5.1 Display Window Registers (DSWR)

Register Address: H'013

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	HDS								
Initial value:	—	—	—	—	—	—	—	*	*	*	*	*	*	*	*	*
R/W:	—	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Register Address: H'014

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	HDE									
Initial value:	—	—	—	—	—	—	*	*	*	*	*	*	*	*	*	*
R/W:	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Register Address: H'015

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	VDS								
Initial value:	—	—	—	—	—	—	—	*	*	*	*	*	*	*	*	*
R/W:	—	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Register Address: H'015

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	VDE									
Initial value:	—	—	—	—	—	—	*	*	*	*	*	*	*	*	*	*
R/W:	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: * Value is retained.

The display window registers (DSWR) are 16-bit readable/writable registers that specify the horizontal and vertical output timing for the display screen.

1. Horizontal Display Start Position (HDS Fields)
   Field that specifies the horizontal display start position in dot-clock units.
2. Horizontal Display End Position (HDE Fields)
   Field that specifies the horizontal display end position in dot-clock units.
3. Vertical Display Start Position (VDS Fields)
   Field that specifies the vertical display start position in raster-line units.
4. Vertical Display End Position (VDE Fields)
   Field that specifies the vertical display end position in raster-line units.

Write 0 to bits that are not used for the HDS, HDE, VDS, and VDE fields (a read will return an undefined value).

The HDS, HDE, VDS, and VDE fields in the DSWR registers retain their values in a reset.

5.5.2 Horizontal Sync Pulse Width Register (HSWR)

Register Address: H'017

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	HSW						
Initial value:	—	—	—	—	—	—	—	—	—	*	*	*	*	*	*	*
R/W:	—	—	—	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: * Value is retained.

The horizontal sync pulse width register (HSWR) is a 16-bit readable/writable register that specifies the horizontal signal low-level pulse width in dot-clock units.

Bits 15 to 17 of HSWR are reserved. Only 0 should be written to these bits (a read will return an undefined value).

The HSW bits in the HSWR register retain their values in a reset.

5.5.3 Horizontal Scan Cycle Register (HCR)

Register Address: H'018

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	HC										
Initial value:	—	—	—	—	—	*	*	*	*	*	*	*	*	*	*	*
R/W:	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: * Value is retained.

The horizontal scan cycle register (HCR) is a 16-bit readable/writable register that specifies the horizontal scan cycle in dot-clock units. In TV sync mode (bits TVM1 and TVM0 set to 10 in DSMR), this register setting must be made so that the $\overline{\text{HSYNC}}$ cycle specified by this register is the same as or greater than the $\overline{\text{EXHSYNC}}$ cycle.

Bits 15 to 11 of HCR are reserved. Only 0 should be written to these bits (a read will return an undefined value).

The HC bits in the HCR register retain their values in a reset.

5.5.4 Vertical Start Position Register (VSPR)

Register Address: H'019

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	VSP									
Initial value:	—	—	—	—	—	—	*	*	*	*	*	*	*	*	*	*
R/W:	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: * Value is retained.

The vertical start position register (VSPR) is a 16-bit readable/writable register that specifies the vertical sync signal start position in raster-line units. In TV sync mode (bits TVM1 and TVM0 set to 10 in DSMR), this register setting must be made so that the $\overline{\text{VSYNC}}$ fall setting position specified by this register is the same as or later than the fall of $\overline{\text{EXVSYNC}}$.

Bits 15 to 10 of VSPR are reserved. Only 0 should be written to these bits (a read will return an undefined value).

The VSP bits in the VSPR register retain their values in a reset.

5.5.5 Vertical Scan Cycle Register (VCR)

Register Address: H'01A

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	VC									
Initial value:	—	—	—	—	—	—	*	*	*	*	*	*	*	*	*	*
R/W:	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: * Value is retained.

The vertical scan cycle register (VCR) is a 16-bit readable/writable register that specifies the vertical scan interval, including the vertical retrace line interval, in raster-line units. In TV sync mode (TVM1 = 1, TVM0 = 0 in DSMR), set this register so that the $\overline{VSYNC}$ rise position set with this register is the same as, or later than, the rise of $\overline{EXVSYNC}$. If a rise of $\overline{EXVSYNC}$ is not detected within the vertical scan interval set in this register, the TVR flag in the status register (SR) will be set to 1.

Bits 15 to 10 of VCR are reserved. Only 0 should be written to these bits (a read will return an undefined value).

The VC bits in the VCR register retain their values in a reset.

5.5.6 Display Off Output Registers (DOOR)

Register Address: H'01B to H'01C

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	DOR						—	—
Initial value:	—	—	—	—	—	—	—	—	*	*	*	*	*	*	—	—
R/W:	—	—	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	—	—

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DOG						—	—	DOB						—	—
Initial value:	*	*	*	*	*	*	—	—	*	*	*	*	*	*	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	—	—	R/W	R/W	R/W	R/W	R/W	R/W	—	—

Note: * Value is retained.

The display off output registers (DOOR) are 16-bit readable/writable registers that specify the display data to be output when display is off. A 6-bit setting is made for each of the RGB components, in the DOR fields, DOG fields, and DOB fields.

Write 0 to bits that are not used for the DOR, DOG, and DOB fields.

The DOR, DOG, and DOB fields in the DOOR registers retain their values in a reset.

5.5.7 Color Detection Registers (CDER)

Register Address: H'01D to H'01E

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	CDR						—	—
Initial value:	—	—	—	—	—	—	—	—	*	*	*	*	*	*	—	—
R/W:	—	—	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	—	—

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CDG						—	—	CDB						—	—
Initial value:	*	*	*	*	*	*	—	—	*	*	*	*	*	*	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	—	—	R/W	R/W	R/W	R/W	R/W	R/W	—	—

Note: * Value is retained.

The color detection registers (CDER) are 16-bit readable/writable registers. When the output color data (DD17 to DD0) matches the values set in these registers, 1 is output from the CDE pin. For details of the output color data format, see (4) Output Color Data Configuration in section 3.3.3, Color Data Formats. The CDR bits (bits 7 to 2) in these registers are compared with DD17 to DD12, the CDG bits (bits 15 to 10) with DD11 to DD6, and the CDB bits (bits 7 to 2) with DD5 to DD0. As the display data is all-0 outside the display interval, if an all-0 setting is made in CDER, 1 will be output from the CDE pin outside the display interval.

Write 0 to bits that are not used for the CDR, CDB, and CDG fields.

The CDR, CDG, and CDB fields in the CDER registers retain their values in a reset.

5.5.8 Equalizing Pulse Width Register (EQWR)

Register Address: H'029

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	EQW						
Initial value:	—	—	—	—	—	—	—	—	—	*	*	*	*	*	*	*
R/W:	—	—	—	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: * Value is retained.

The equalizing pulse width register (EQWR) is a 16-bit readable/writable register that specifies the low-level pulse width of $\overline{\text{CSYNC}}$ signal equalizing pulses in dot-clock units. Equalizing pulses are generated at the start and in the middle of each raster.

This register is valid when CYS1 is set to 1 in display mode register 2 (DSMR2).

Bits 15 to 7 of EQWR are reserved. Only 0 should be written to these bits (a read will return an undefined value).

The EQW bits in the EQWR register retain their values in a reset.

For example, in the case of the NTSC specification, the low-level pulse width is approximately 2.4 µs. If the display operating clock frequency is 14.31818 MHz, a value of 2.4 µs × 14.31818 MHz = 35 should be set in this register.

5.5.9 Separation Width Register (SPWR)

Register Address: H'02A

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	SPW									
Initial value:	—	—	—	—	—	—	*	*	*	*	*	*	*	*	*	*
R/W:	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: * Value is retained.

The separation width register (SPWR) is a 16-bit readable/writable register that specifies the low-level pulse width of $\overline{\text{CSYNC}}$ signal separation pulses in dot-clock units. Separation pulses are generated at the start and in the middle of each raster. Set an SPW value of less than 1/2 the horizontal scan interval.

This register is valid when CYS1 is set to 1 in display mode register 2 (DSMR2).

Bits 15 to 10 of SPWR are reserved. Only 0 should be written to these bits (a read will return an undefined value).

The SPW bits in the SPWR register retain their values in a reset.

If HC is the horizontal scan interval, in the case of the NTSC specification, for example, the separation pulse low width is approximately HC/2 – 4.7 µs. If HC is 63.555 µs and the display operating clock frequency is 14.31818 MHz, a value of (63.555 µs/2 – 4.7) µs × 14.31818 MHz = 357 should be set in this register.

5.5.10 Video Display Position Registers (VPR)

Register Address: H'02C

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VPR (HVP)	—	—	—	—	—	—	HVP									
Initial value:	—	—	—	—	—	—	*	*	*	*	*	*	*	*	*	*
R/W:	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Register Address: H'02D

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VPR (VVP)	—	—	—	—	—	—	—	VVP								
Initial value:	—	—	—	—	—	—	—	*	*	*	*	*	*	*	*	*
R/W:	—	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: * Value is retained.

The video display position registers (VPR) are 16-bit readable/writable registers that specify the video horizontal and vertical output timing.

1. Video Horizontal Display Start Position (HVP Fields)
   This field sets the video horizontal start position in dot-clock units.
2. Video Vertical Display Start Position (VVP Fields)
   This field sets the video vertical start position in raster-line units.

When the SCM1 and SCM0 bits in the display mode register (DSMR) are set to 11 or 10 (interlace sync & video mode or interlace mode), bit 0 in VVP fields should be cleared to 0.

Set the start position so that the video display area does not extend beyond the frame buffer display screen. Unlike the HDS and VDS fields in the display window registers (DSWR), the screen coordinate upper-left reference values should be set in the HVP and VVP fields. In the horizontal direction the upper-left point is 0, and the right direction is positive, with changes made one by one in dot units. In the vertical direction the upper-left point is 0, and the downward direction is positive, with changes made one by one in line units.

Write 0 to bits that are not used for the HVP and VVP fields (a read will return an undefined value).

The HVP and VVP bits in the VPR (HVP/VVP) registers retain their values in a reset.

5.5.11 Video Area Start Address Registers 0 to 2 (VSAR0 to VSAR2)

Register Address: H'031 to H'032

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VSAR0	—	—	—	—	—	—	—	—	—	VSAH0						
Initial value:	—	—	—	—	—	—	—	—	—	*	*	*	*	*	*	*
R/W:	—	—	—	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VSAR0	VSAL0						—	—	—	—	—	—	—	—	—	—
Initial value:	*	*	*	*	*	*	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	—	—	—	—	—	—	—	—	—	—

Register Address: H'033 to H'034

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VSAR1	—	—	—	—	—	—	—	—	—	VSAH1						
Initial value:	—	—	—	—	—	—	—	—	—	*	*	*	*	*	*	*
R/W:	—	—	—	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VSAR1	VSAL1						—	—	—	—	—	—	—	—	—	—
Initial value:	*	*	*	*	*	*	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	—	—	—	—	—	—	—	—	—	—

Register Address: H'035 to H'036

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VSAR12	—	—	—	—	—	—	—	—	—	VSAH2						
Initial value:	—	—	—	—	—	—	—	—	—	*	*	*	*	*	*	*
R/W:	—	—	—	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VSAR2	VSAL2						—	—	—	—	—	—	—	—	—	—
Initial value:	*	*	*	*	*	*	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	—	—	—	—	—	—	—	—	—	—

Note: * Value is retained.

The video area start address registers 0 to 2 (VSAR0 to VSAR2) are 16-bit readable/writable registers that specify the memory areas used as UGM video areas. Only the upper 13 bits (A22 to A10) of the start physical addresses are specified by the video area start address fields (VSAH, VSAL).

Three video storage areas are used, of the size specified by VSIZEX and VSIZEY. Each area has a memory-unit address layout, and should be set as shown in figure 5.1.

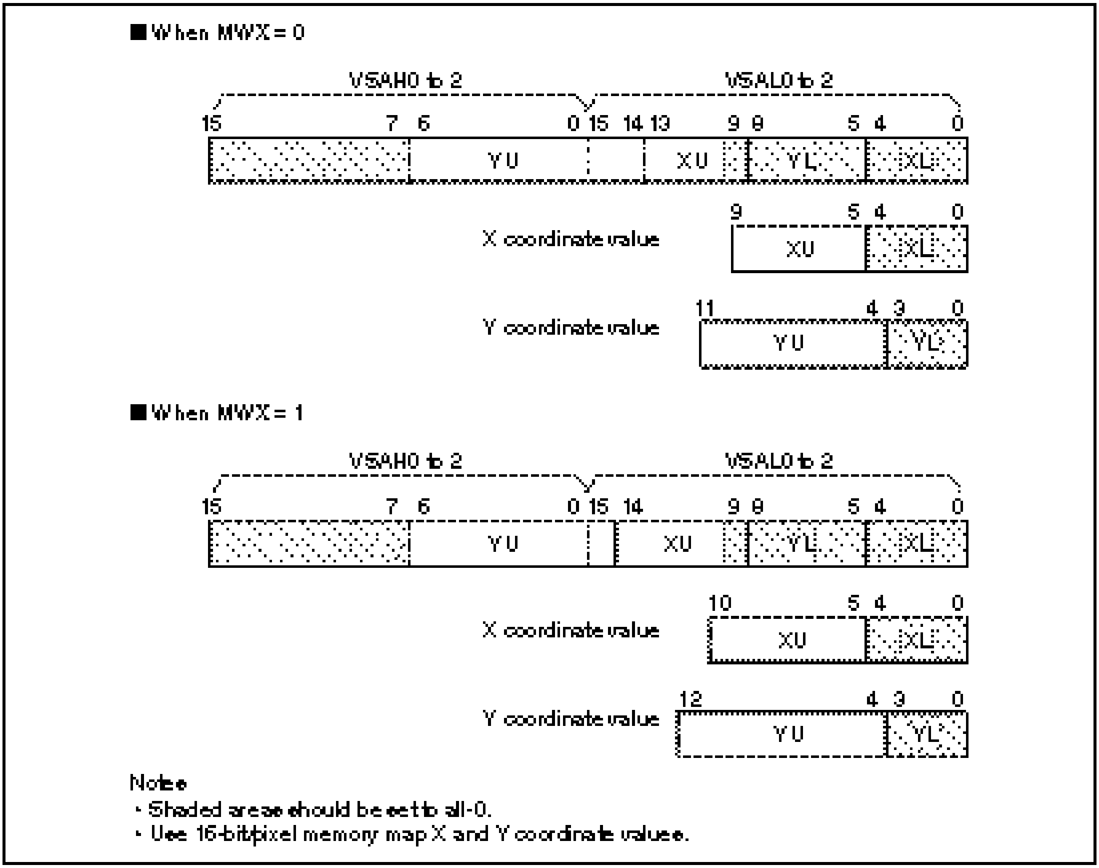


Figure 5.1 Video Storage Area Address Arrangement

When the VIE bit in the video incorporation mode register (VIMR) is 1, the area in which the most recent image incorporated by video incorporation was stored is automatically selected as the area used for display. When the VIE bit is 0, the video storage area holding the most recent image is displayed.

New values set when these registers are modified become effective when the display is updated internally in the case of display output, or when the next image is incorporated (at the rise of the $\overline{\text{VVS}}$ input) in the case of image incorporation.

Write 0 to bits that are not used for VSARH0 to VSARH2 and VSARL0 to VSARL2. (a read will return an undefined value).

The VSAR0 to VSAR2 retain their values in a reset.

5.5.12 Video Window Size Registers (VSIZER)

Register Address: H'037

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VSIZER	—	—	—	—	—	—	VSIZEX									—
Initial value:	—	—	—	—	—	—	*	*	*	*	*	*	*	*	*	—
R/W:	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	—

Register Address: H'038

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VSIZER	—	—	—	—	—	—	VSIZEY									—
Initial value:	—	—	—	—	—	—	*	*	*	*	*	*	*	*	*	—
R/W:	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	—

Note: * Value is retained.

The video window size registers (VSIZER) are two 16-bit readable/writable registers that specify the video window display size. Set the value obtained by multiplying the number of effective pixels input from off-chip by the reduction (thinning-out) ratio, VSIZ, at the time of incorporation. Set 0 for the least significant bits of X and Y as shown in the register diagram. This makes the set values of VSIZEX and VSIZEY even numbers.

Write 0 to bits that are not used for the VSIZEX and VSIZEY fields (a read will return an undefined value).

The VSIZER retain their values in a reset.

5.5.13 Video Incorporation Mode Register (VIMR)

Register Address: H'039

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VID1	VID0	—	—	—	—	VSIZ4	VSIZ3	VSIZ2	VSIZ1	VSIZ0	VINM	ODEN1	ODEN0	RGB	VIE
Initial value:	1	1	—	—	—	—	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The video incorporation mode register (VIMR) is a 16-bit readable/writable register that is used to make various video incorporation settings.

Bits 13 to 10 of the VIMR are reserved. Only 0 should be written to these bits (a read will return an undefined value).

In a reset, bits VID1 and VID0 are initialized to 1, and the other bits are initialized to 0.

Bits 15 and 14—Video Window Status (VID1, VID0): These bits are status flags that indicate the video area storing the most recent image incorporated from the video input. Note that these bits are different in nature from the other bits in this register. The value of these bits is significant only when the VIE bit is cleared to 0. Note that the meaning of these bits is not guaranteed if video incorporation proceeds while the VIE bit is set to 1.

Only 00 should be written to these bits (although the write value is ignored).

The meaning of the values read from these bits is shown below.

Bit 15: VID1	Bit 14: VID0	Description
0	0	Most recent image is in video area 0. When video window (VWE) is 1, video area 0 is displayed.
	1	Most recent image is in video area 1. When video window (VWE) is 1, video area 1 is displayed.
1	0	Most recent image is in video area 2. When video window (VWE) is 1, video area 2 is displayed.
	1	Indicates initial state after a reset. When video window (VWE) is 1, video area 0 is displayed. (Initial value)

To save or fetch an image as a still picture, video incorporation must be halted. The sequence of operations is: halt video incorporation, read the video window status, and fetch the still picture from the relevant area.

Bits 13 to 10—Reserved: Only 0 should be written to these bits (a read will return an undefined value).

Bits 9 to 5—Video Incorporation Reduction (Thinning-Out) Ratio (VSIZ4 to VSIZ0): These bits set the reduction ratio when performing video incorporation.

Bit 9: VSIZ4	Bit 8: VSIZ3	Bit 7: VSIZ2	Bit 6: VSIZ1	Vertical Reduction Ratio	Horizontal Reduction Ratio (VSIZ0 = 0)	Horizontal Reduction Ratio (VSIZ0 = 1)
0	0	0	0	1	1	1/2
			1	1	1/3	Setting prohibited
		1	0	1	Setting prohibited	Setting prohibited
			1	1	Setting prohibited	Setting prohibited
	1	0	0	1/2	Setting prohibited	1/2
			1	1/2	1/3	1/6
		1	0	1/2	1/4	Setting prohibited
			1	1/2	Setting prohibited	Setting prohibited
1	0	0	0	1/3	Setting prohibited	Setting prohibited
			1	1/3	1/3	1/6
		1	0	1/3	Setting prohibited	Setting prohibited
			1	1/3	Setting prohibited	Setting prohibited
	1	0	0	1/4	Setting prohibited	Setting prohibited
			1	1/4	Setting prohibited	1/6
		1	0	1/4	1/4	Setting prohibited
			1	1/4	Setting prohibited	Setting prohibited

Bit 4—Video Incorporation Mode (VINM): Specifies the field order in video incorporation.

Bit 4: VINM	Description
0	Field for which $\overline{\text{VODD}}$ input is low (lines 1, 3, 5, ...) is incorporated first, followed by field for which $\overline{\text{VODD}}$ input is high (lines 2, 4, 6, ...). (Initial value)
1	Field for which $\overline{\text{VODD}}$ input is high (lines 2, 4, 6, ...) is incorporated first, followed by field for which $\overline{\text{VODD}}$ input is low (lines 1, 3, 5, ...).

Bits 3 and 2—Incorporated Field Select (ODEN1, ODEN0): These bits select the field for which video input scanning method specification and incorporation are to be performed in video incorporation.

Bit 3: ODEN1	Bit 2: ODEN0	Description
0	0	Input video is non-interlace. Do not input interlace signal. (Initial value)
	1	Input video is interlace, and frame screens are incorporated with combination of even and odd fields. Supplementing is not performed for operation when fields are combined.
1	0	Input video is interlace, and only fields for which $\overline{\text{VODD}}$ signal is low (odd fields) are incorporated. Number of scanning lines of incorporated image is 1/2 number of frame screen scanning lines.
	1	Input video is interlace, and only fields for which $\overline{\text{VODD}}$ signal is high (even fields) are incorporated. Number of scanning lines of incorporated image is 1/2 number of frame screen scanning lines.

Bit 1—RGB Conversion Mode (RGB): Selects whether RGB conversion is to be performed in video incorporation.

Bit 1: RGB	Description
0	YUV4:2:2 data is stored directly in UGM, without conversion to RGB. This data cannot be used for any purpose except display in the video window. (Initial value)
1	Data undergoes RGB conversion and is stored in UGM as RGB data. This data can be used as multi-valued source data.

Bit 0—Video Incorporation Enable (VIE): Enables or disables video incorporation.

Bit 0: VIE	Description
0	Video incorporation is not performed. (Initial value)
1	Video incorporation is performed.

5.5.14 Cursor Registers (CSR)

Register Address: H'03A

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CSR (HCS1)	BLINKA						HCS1									
Initial value:	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Register Address: H'03B

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CSR (VCS1)	BLINKB						—	VCS1								
Initial value:	*	*	*	*	*	*	—	*	*	*	*	*	*	*	*	*
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Register Address: H'03C

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CSR (HCS2)	—	—	—	—	—	—	HCS2									
Initial value:	—	—	—	—	—	—	*	*	*	*	*	*	*	*	*	*
R/W:	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Register Address: H'03D

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CSR (VCS2)	—	—	—	—	—	—	—	VCS2								
Initial value:	—	—	—	—	—	—	—	*	*	*	*	*	*	*	*	*
R/W:	—	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: * Value is retained.

The cursor registers (CSR) are 16-bit readable/writable registers that specify the cursor 1 and 2 horizontal and vertical output timing and the length of the cursor blink shape A and B display intervals.

1. Cursor 1 Horizontal Display Start Position (HCS1)

   These bits set the cursor 1 horizontal display start position in dot-clock units.

2. Cursor 1 Vertical Display Start Position (VCS1)

   These bits set the cursor 1 vertical display start position in raster-line units.

3. Cursor 2 Horizontal Display Start Position (HCS2)

   These bits set the cursor 2 horizontal display start position in dot-clock units.

4. Cursor 2 Vertical Display Start Position (VCS2)

   These bits set the cursor 2 vertical display start position in raster-line units.

5. Cursor Blink Shape A Display Interval Length (BLNKA)

   These bits set, in field units, the length of the interval during which cursor shape A (stored in the cursor area) is displayed. These bits must not be cleared to 0. This field is used for both cursor 1 and cursor 2. Display shape switching is performed simultaneously for both cursors.

6. Cursor Blink Shape B Display Interval Length (BLNKB)

   These bits set, in field units, the length of the interval during which cursor shape B (stored in the cursor area) is displayed. These bits must not be cleared to 0. This field is used for both cursor 1 and cursor 2. Display shape switching is performed simultaneously for both cursors.

The cursor is 32 × 32 pixels in size, and is displayed in the color assigned in the color palette register. Set the start positions so that the upper-left coordinates of the cursor display area do not extend outside the frame buffer display screen. Also set the start positions so that cursors 1 and 2 do not overlap, as cursor 1 will have priority and cursor 2 will be lost in this case.

Unlike the HDS and VDS fields in the display window registers (DSWR), the screen coordinate upper-left reference values should be set in the HCS and VCS fields. In the horizontal direction the upper-left point is 0, and the right direction is positive, with changes made one by one in dot units. In the vertical direction the upper-left point is 0, and the downward direction is positive, with changes made one by one in line units.

In cursor blinking, in the cursor display A interval, the 1024 bytes of data from the address specified by the cursor area start address register are used for display. In the cursor display B interval, the 1024 bytes of data from the location obtained by adding 1024 bytes to the address specified by the cursor area start address register are used for display.

Write 0 to bits that are not used for the HCS1, VCS1, HCS2, VCS2, BLINKA, and BLINKB fields (a read will return an undefined value).

The HCS1, VCS1, HCS2, VCS2, BLINKA, and BLINKB bits in the CSR registers retain their values in a reset.

5.5.15 Cursor Area Start Address Registers 1 and 2 (CSAR1, CSAR2)

Register Address: H'03E

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CSAR1	CSAL1 (address A15–A11 setting)					—	—	—	—	CSAH1 (address A22–A16 setting)						
Initial value:	*	*	*	*	*	—	—	—	—	*	*	*	*	*	*	*
R/W:	R/W	R/W	R/W	R/W	R/W	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Register Address: H'03F

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CSAR2	CSAL2 (address A15–A11 setting)					—	—	—	—	CSAH2 (address A22–A16 setting)						
Initial value:	*	*	*	*	*	—	—	—	—	*	*	*	*	*	*	*
R/W:	R/W	R/W	R/W	R/W	R/W	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: * Value is retained.

The cursor area start address registers 1 and 2 (CSAR1, CSAR2) are 16-bit readable/writable registers that specify the memory areas used as cursor areas in the UGM. The upper bits (A22 to A16) of the start physical address of the cursor area are set in the cursor area start address high (CSAH) field, and the lower bits (A15 to A11) in the cursor area start address low (CSAL) field.

Set the cursor A shape in the 1024 bytes from the set address, and the cursor B shape in the next 1024 bytes.

The new values set when these registers are modified become effective when internal updating is performed.

Cursor display data should be set in linear address data format.

Bits 10 to 7 of CSAR1 and CSAR2 are reserved. Only 0 should be written to these bits (a read will return an undefined value).

The CSAL1, CSAL2, CSAH1, and CSAH2 fields in the CSAR1 and CSAR2 registers retain their values in a reset.

5.6 Rendering Control Registers

The rendering control registers comprise two command status registers, mapped onto addresses (A10–A1) H'01F to H'020.

5.6.1 Command Status Registers (CSTR)

Register Address: H'01F to H'020

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	CSTH (address A22–A16 setting)						
Initial value:	—	—	—	—	—	—	—	—	—	*	*	*	*	*	*	*
R/W:	—	—	—	—	—	—	—	—	—	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CSTL (address A15–A1 setting)															—
Initial value:	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	—

Note: * Value is retained.

The command status registers (CSTR) are 16-bit read-only registers that store the address of the command word (op code word) being executed when a frame change is performed.

The upper bits (A22 to A16) of the command word address are indicated by the CSTH field, and the lower bits (A15 to A1) by the CSTL field. The address indicated by the CSTH and CSTL fields is a word address.

Bits that are not used for the CSTH and CSTL fields are always read as 0.

The CSTH and CSTL fields in the CSTR registers retain their values in a reset.

5.7 Input Control Registers

The input control registers comprise five 16-bit registers related to the control of input data conversion, mapped onto addresses (A10–A1) H'021 to H'025. The settings in these registers are valid when the setting of bits YUV2, YUV1, and YUV0 in the input data conversion mode register (IEMR) is 001, 010, 011, or 111.

5.7.1 Image Data Transfer Start Address Registers (ISAR)

Register Address: H'021 to H'022

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	ISAH (address A22–A16 setting)						
Initial value:	—	—	—	—	—	—	—	—	—	0	0	0	0	0	0	0
R/W:	—	—	—	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ISAL (address A15–A1 setting)															—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	—

The image data transfer start address registers (ISAR) are 16-bit readable/writable registers that specify the image data transfer destination as a physical address when the setting of bits YUV2, YUV1, and YUV0 is 001, 010, 011, or 111. The upper bits (A22 to A16) of the start address are set in the ISAH field, and the lower bits (A15 to A1) in the ISAL field. The address indicated by the ISAH and ISAL fields is a word address.

If the value of these registers is modified during a series of data conversion operations from the time bits YUV2, YUV1, and YUV0 are set to 001, 010, 011, or 111 by the CPU until YUV mode is cleared automatically by the Q2SD, operation will be unstable.

Write 0 to bits that are not used for the ISAH and ISAL fields.

The values of the ISAH and ISAL fields in the ISAR registers are initialized to all-0 by a reset.

These registers are not incremented when image data is transferred.

5.7.2 Image Data Size Registers (IDSR)

Register Address: H'023

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	IDSX										
Initial value:	—	—	—	—	—	0	0	0	0	0	0	0	0	0	0	0
R/W:	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Register Address: H'024

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	IDSY									
Initial value:	—	—	—	—	—	—	0	0	0	0	0	0	0	0	0	0
R/W:	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: * Do not set 0 in bit 0 of IDSX.

The image data size registers (IDSR) are two 16-bit readable/writable registers that specify the image data X size and Y size when the setting of bits YUV2 to YUV0 is 001, 010, 011, or 111. For the image data X size, set the number of pixels when YUV2–YUV0 = 001, 010, or 011, and set 1/2 the number of pixels when YUV2–YUV0 = 111. An even number should be set for the X size (IDSX0 bit = 0).

If the value of these registers is modified during a series of data conversion operations from the time bits YUV2, YUV1, and YUV0 are set to 001, 010, 011, or 111 by the CPU until YUV mode is cleared automatically by the Q2SD, operation will be unstable.

Write 0 to bits that are not used for the IDSX and IDSY fields.

The values of the IDSX and IDSY bits in the IDSR registers are initialized to all-0 by a reset.

5.7.3 Image Data Entry Register (IDER)

Register Address: H'025

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IDE															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

The image data entry register (IDER) is a 16-bit write-only register that comprises the entry in which image data is input when the setting of bits YUV2, YUV1, and YUV0 is 001, 010, 011, or 111.

The IDER is initialized to H'0000 by a reset.

5.8 Memory Control Registers (2)

Memory control registers (2) comprise registers related to background screen control, mapped onto addresses (A10–A1) H'026 to H'027.

5.8.1 Background Start Coordinate Registers (BGSR)

Register Address: H'026

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	BGSX									
Initial value:	—	—	—	—	—	—	*	*	*	*	*	*	*	*	*	*
R/W:	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Register Address: H'027

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	BGSY													
Initial value:	—	—	*	*	*	*	*	*	*	*	*	*	*	*	*	*
R/W:	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: * Value is retained.

The background start coordinate registers (BGSR) are two 16-bit readable/writable registers that specify the background screen start coordinates. The settings should be made so that the background screen does not overlap the frame buffers. Write 0 to bits that are not used for the BGSX and BGSY fields (a read will return an undefined value).

The BGSX and BGSY bits in the BGSR registers retain their values in a reset.

5.9 Rendering Control Registers (2)

Rendering control registers (2), comprising registers that indicate the internal status when drawing is suspended, are mapped onto addresses (A10–A1) H'040 to H'04B.

When reading these registers, first set RBRK to 1 in the system control register (SYSR) and wait until BRK is set to 1. If these registers are read before BRK is set to 1, undefined values will be returned.

5.9.1 Current Pointer Registers (CURR)

Register Address: H'040

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	XC													
Initial value:	—	—	*	*	*	*	*	*	*	*	*	*	*	*	*	*
R/W:	—	—	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Register Address: H'041

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	YC													
Initial value:	—	—	*	*	*	*	*	*	*	*	*	*	*	*	*	*
R/W:	—	—	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Note: * Value is retained.

The current pointer registers (CURR) are two 16-bit read-only registers that indicate the current pointer coordinates.

When these registers are read, bits that are not used for the XC and YC fields are always read as 0.

The XC and YC bits in the CURR registers retain their values in a reset.

Bit 13 is the sign bit.

5.9.2 Local Offset Registers (LCOR)

Register Address: H'042

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	XO													
Initial value:	—	—	*	*	*	*	*	*	*	*	*	*	*	*	*	*
R/W:	—	—	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Register Address: H'043

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	YO													
Initial value:	—	—	*	*	*	*	*	*	*	*	*	*	*	*	*	*
R/W:	—	—	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Note: * Value is retained.

The local offset registers (LCOR) are two 16-bit read-only registers that indicate the offset coordinates.

When these registers are read, bits that are not used for the XO and YO fields are always read as 0.

The XO and YO bits in the LCOR registers retain their values in a reset.

Bit 13 is the sign bit.

5.9.3 User Clipping Area Registers (UCLR)

Register Address: H'044

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Upper-left X	—	—	UXMIN													
Initial value:	—	—	*	*	*	*	*	*	*	*	*	*	*	*	*	*
R/W:	—	—	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Register Address: H'045

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Upper-left Y	—	—	UYMIN													
Initial value:	—	—	*	*	*	*	*	*	*	*	*	*	*	*	*	*
R/W:	—	—	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Register Address: H'046

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Lower-right X	—	—	UXMAX													
Initial value:	—	—	*	*	*	*	*	*	*	*	*	*	*	*	*	*
R/W:	—	—	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Register Address: H'047

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Lower-right Y	—	—	UYMAX													
Initial value:	—	—	*	*	*	*	*	*	*	*	*	*	*	*	*	*
R/W:	—	—	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Note: * Value is retained.

The user clipping area registers (UCLR) are 16-bit read-only registers that indicate the user clipping area.

When these registers are read, bits that are not used for the UXMIN, UYMIN, UXMAX, and UYMAX fields are always read as 0.

The UXMIN, UYMIN, UXMAX, and UYMAX bits in the UCLR registers retain their values in a reset.

Bit 13 is the sign bit.

5.9.4 System Clipping Area Registers (SCLR)

Register Address: H'048

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Lower-right X	—	—	SXMAX													
Initial value:	—	—	*	*	*	*	*	*	*	*	*	*	*	*	*	*
R/W:	—	—	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Register Address: H'049

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Lower-right Y	—	—	SYMAX													
Initial value:	—	—	*	*	*	*	*	*	*	*	*	*	*	*	*	*
R/W:	—	—	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Note: * Value is retained.

The system clipping area registers (SCL) are two 16-bit read-only registers that indicate the system clipping area.

When these registers are read, bits that are not used for the SXMAX, and SYMAX fields are always read as 0.

The SXMAX and SYMAX bits in the SCLR registers retain their values in a reset.

Bit 13 is the sign bit.

5.9.5 Return Address Registers (RTNR)

Register Address: H'04A to H'04B

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	RTNH (address A22–A16 setting)						
Initial value:	—	—	—	—	—	—	—	—	—	*	*	*	*	*	*	*
R/W:	—	—	—	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RTNL (address A15–A1 setting)															—
Initial value:	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	—

Note: * Value is retained.

The return address registers (RTNR) are 16-bit readable/writable registers that specify the return address.

The upper bits (A22 to A16) of the start address are set in the RTNH field, and the lower bits (A15 to A1) in the RTNL field.

The address (bits A22 to A1) indicated by the RTNH and RTNL fields is a word address.

Write 0 to bits that are not used for the RTNH and RTNL fields (a read will return an undefined value).

The RTNH and RTNL fields in the RTNR registers retain their values in a reset.

5.9.6 Color Offset Register (COLOR)

Register Address: H'04A to H'04D

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Sign	COOFR				Sign	COOFG					Sign	COOFB			
Initial value:	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Positions	Name	Description
15 to 11	COOFR (Color offset R)	Color offset red component
10 to 5	COOFG (Color offset G)	Color offset green component
4 to 0	COOFB (Color offset B)	Color offset blue component

The offset components are treated as signed integers.

This register can be used by the POLYGON4A command. In 16-bit/pixel drawing, if the rendering attribute COOF bit is set to 1, the result of adding the value in the COLOR register to the value of the multi-valued source data is drawn. The operation is performed by saturation processing. In 8-bit/pixel drawing, the rendering attribute COOF bit must be cleared to 0.

5.10 Color Palette

The color palette is mapped onto addresses (A10–A1) H'100 to H'2FF. Settings can be made for 256 colors, with 6 bits each for R, G, and B. The color palette can only be used in 8-bit/pixel mode.

When the color palette is accessed by the CPU, bits GBM2 to GBM0 in the rendering mode register (REMR) should be set to 000, 010, 100, or 110.

In the Q2SD, the color palette set values are retained regardless of the GBM values.

5.10.1 Color Palette Registers H/L000 to H/L255 (CP000RH/L to CP255RH/L)

Register Address: H'100 to H'101

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CP000RH	—	—	—	—	—	—	—	—	R000 (Red: 6 bits)						—	—
Initial value:	—	—	—	—	—	—	—	—	*	*	*	*	*	*	—	—
R/W:	—	—	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	—	—

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CP000RL	G000 (Green: 6 bits)						—	—	B000 (Blue: 6 bits)						—	—
Initial value:	*	*	*	*	*	*	—	—	*	*	*	*	*	*	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	—	—	R/W	R/W	R/W	R/W	R/W	R/W	—	—

Register Address: H'102 to H'103

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CP001RH	—	—	—	—	—	—	—	—	R001 (Red: 6 bits)						—	—
Initial value:	—	—	—	—	—	—	—	—	*	*	*	*	*	*	—	—
R/W:	—	—	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	—	—

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CP001RL	G001 (Green: 6 bits)						—	—	B001 (Blue: 6 bits)						—	—
Initial value:	*	*	*	*	*	*	—	—	*	*	*	*	*	*	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	—	—	R/W	R/W	R/W	R/W	R/W	R/W	—	—

⋮

Register Address: H'2FE to H'2FF

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CP255RH	—	—	—	—	—	—	—	—	R255 (Red: 6 bits)						—	—
Initial value:	—	—	—	—	—	—	—	—	*	*	*	*	*	*	—	—
R/W:	—	—	—	—	—	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	—	—

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CP255RL	G255 (Green: 6 bits)						—	—	B255 (Blue: 6 bits)						—	—
Initial value:	*	*	*	*	*	*	—	—	*	*	*	*	*	*	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	—	—	R/W	R/W	R/W	R/W	R/W	R/W	—	—

Note: * Value is retained.

The color Palette Registers H/L000 to H/L255 (CP000RH/L to CP255RH/L) are 32-bit readable/writable registers. Their settings are valid in 8-bit/pixel mode.

The color palette is controlled in 2-word units comprising one pixel. The same units must therefore be used for accesses to the color palette registers.

When writing to color palette registers, first write to the R register, then to the G and B registers. The new R color palette set value becomes effective when the G and B registers are set.

When reading color palette registers, first read the R register, then the G and B registers.

When accessing color palette registers, it is not possible to access another Q2SD register between the R register and the G and B registers.

Longword (32-bit) access should therefore be used for color palette registers to enable both the R register and the G and B registers to be accessed at one time.

Section 6 Usage Notes

6.1 Power-On Sequence

The timing of the CLK0, CLK1, and RESET signals at power-on is shown in figure 6.1. Set 50 ms or less as the time from the rise of VCCn to the rise of CLK0/CLK1, and 100 ms or more as the time from the rise of VCCn to the rise of RESET. If CLK0 and CLK1 are halted for a long time (50 ms or more) after powering on, the device may be permanently damaged.

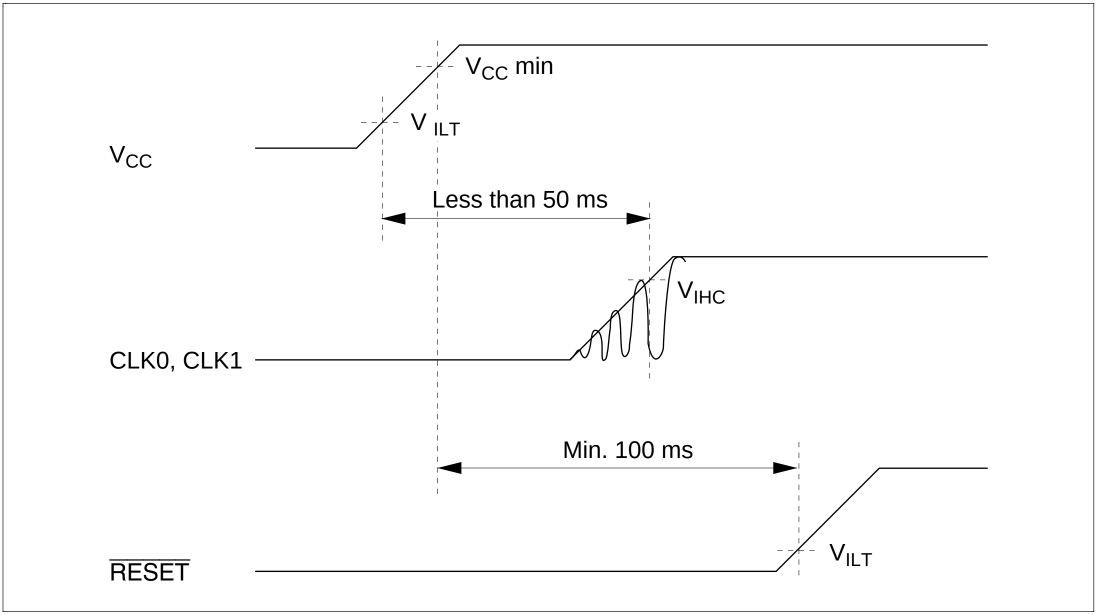


Figure 6.1 Power-On Sequence

6.2 Use of 64-Mbit SDRAM (×16 Type)

The Q2SD references the value of bits MES1 and MES0 in the memory mode register (MMR) following the elapse of 70 tcyc0 after a hardware reset, and makes the UDQM1 pin the MA13 signal output pin if MES1, MES0 = 1, 0, or the upper word upper byte input/output mask signal output pin if MES1, MES0 ≠ 1, 0. If the setting of MES1 and MES0 has not been carried out by this time, the clearance values MES1, MES0 = 0, 0 resulting from the hardware reset will be referenced.

Therefore, only when using the MES1, MES0 = 1, 0 mode (64-Mbit (×16) memory size, one memory used, 16-bit bus), the MES1, MES0 = 1, 0 setting must be made before the elapse of 70 tcyc0 after a hardware reset.

Section 7 Electrical Characteristics

7.1 Absolute Maximum Ratings

Table 7.1 Absolute Maximum Ratings

Item	Symbol	Value	Unit
Power supply voltage	V_{CC} *[1]	–0.3 to +4.6	V
Input voltage	V_{in} *[1]	–0.3 to V_{CC} +0.3	V
Permissible output low current	$\| I_{oL} \|$ *[2]	2	mA
Total permissible output low current	$\| \Sigma I_{oL} \|$ *[3]	172	mA
Permissible output high current	$\| -I_{oH} \|$ *[2]	2	mA
Total permissible output high current	$\| \Sigma(I_{oH}) \|$ *[3]	172	mA
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	–55 to +125	°C

Notes: 1. Value based on GND = 0 V. Includes DAV_{CC} and $PLLV_{CC}$.
2. The permissible output current is the maximum value of the current drawn in or flowing out from one output pin and one input/output pin.
3. The total permissible output current is the sum of currents drawn in or flowing out from output pins and input/output pins.

Caution: Permanent damage to the chip may result if absolute maximum ratings are exceeded. In normal operation, it is advisable to observe the recommended operating conditions. Exceeding these conditions may adversely affect the reliability of the chip.

7.2 Recommended Operating Conditions

7.2.1 Recommended Operating Conditions

Table 7.2 Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Power supply voltage	V_{CC}*	3.0	3.3	3.6	V
Input low voltage (except CLK0, CLK1)	V_{ILT}*	0	—	0.6	V
Input low voltage (CLK0, CLK1)	V_{ILC}*	0	—	0.6	V
Input high voltage (except CLK0, CLK1)	V_{IHT}*	2.2	—	V_{CC}	V
Input high voltage (CLK0, CLK1)	V_{IHC}*	$0.8V_{CC}$	—	V_{CC}	V
Operating temperature	T_{opr}	0	25	70	°C

Note: * Value based on GND = 0 V.

7.3 Electrical Characteristics Test Methods

7.3.1 Timing Testing

The output low voltage for timing testing is 1.5 V. The output high voltage for timing testing is 1.5 V.

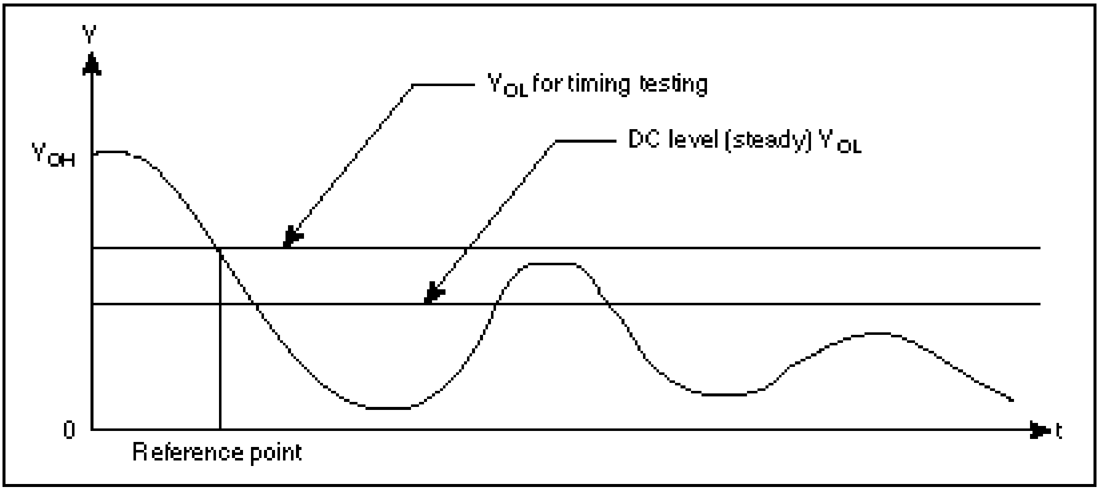


Figure 7.1 Basis of V_{OL} Timing Testing

7.3.2 Test Load Circuit (All Output and Input/Output Pins)

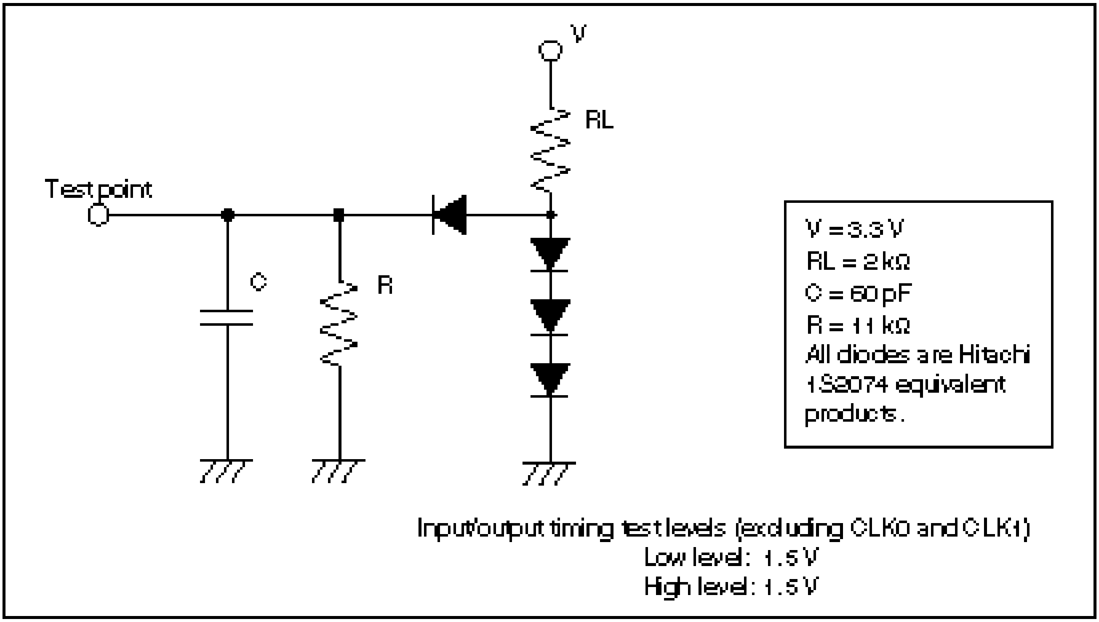


Figure 7.2 Test Load Circuit

7.4 Electrical Characteristics

7.4.1 DC Characteristics

Table 7.3 DC Characteristics

Unless otherwise indicated, V_{CC} = DACV$_{CC}$ = PLLV$_{CC}$ = 3.3 V ±0.3 V, GND = DACGND = PLLGND = 0 V, T_a = 0 to +70°C.

Item	Pin Names	Symbol	Min	Max	Unit	Test Conditions
Input high voltage (CMOS level)	I1	V_{IHC}	0.8 × V_{CC}	V_{CC} + 0.3	V	
Input low voltage (CMOS level)		V_{ILC}	–0.3	V_{CC} × 0.2		
Input high voltage (TTL level)	I2, IO	V_{IHT}	2.2	V_{CC} + 0.3	V	
Input low voltage (TTL level)		V_{ILT}	–0.3	V_{CC} × 0.2		
Input leakage current	I1, I2	I_{in}	—	1	µA	V_{in} = 0 – V_{CC}
Three-state leakage current (off state)	IO, O	I_{TSI}	—	1		V_{in} = 0.4 – V_{CC}
Output high voltage	IO, O	V_{OH}	2.2	—	V	I_{OH} = –200 µA
Output low voltage	IO, O	V_{OL}	—	0.6		I_{OL} = 1.6 mA
Input capacitance	IO	C_{in}	—	20	pF	Vin = 0 V
	I1, I2		—	20		T_a = 25°C f = 1.0 MHz
Current dissipation		I_{CC}	—	350	mA	Data bus operating/display operating/ command being executed

Note: The symbols used in table 7.3 are explained below.

Symbol	Input	Output	High-Z	Pull-up	Pin Names
I1	CMOS	—	—	—	CLK0, CLK1
I2	TTL	—	—	—	MOD2 to MOD0, RESET, A22 to A1, CS1, CS0, RD, WE1, WE0, DACK, VIN7 to VIN0, VHS, VVS, VODD, VQCLK
IO	TTL	CMOS	Yes	—	D15 to D0, HSYNC/EXHSYNC, VSYNC/EXVSYNC, ODDF, MD31 to MD0
O	—	CMOS	—	—	DREQ, WAIT, IRL, CSYNC, DISP, CDE, MA13 to MA0, MCS, MWE, MRAS, MCAS, LDQM1, LDQM0, UDQM1, UDQM0, MCLK

7.4.2 AC Characteristics

Unless otherwise indicated, V_{CC} = DACV_{CC} = PLLV_{CC} = 3.3 V ±0.3 V, GND = DACGND = PLLGND = 0 V, T_a = 0 to +70°C.

Clocks

Table 7.4 Input Clocks (Pins MODE2 to MODE0 = 000, 001, or 010: Multiplication On)

Item	Symbol	Min	Max	Unit	Test Conditions	Notes
CLK0 cycle time 1	t_{cyc}	15	25	ns	Figure 7.3	×1
CLK0 cycle time 2	t_{cyc}	30	50	ns		×2
CLK0 cycle time 3	t_{cyc}	60	100	ns		×4
CLK0 high pulse width	t_{CPWH}	5.5	—	ns		
CLK0 low pulse width	t_{CPWL}	5.5	—	ns		
MCLK cycle time	t_{cyc0}	15	25	ns		
MCLK high pulse width	t_{CMPWH}	5.0	—	ns		
MCLK low pulse width	t_{CMPWL}	5.0	—	ns		
CLK1 cycle time 1	t_{cyc1}	30	200	ns		
CLK1 high pulse width	t_{C1PWH}	10	—	ns		
CLK1 low pulse width	t_{C1PWL}	10	—	ns		
CLK1 duty	t_{C1DT}	$0.5t_{cyc1} - 0.07t_{cyc1}$	$0.5t_{cyc1} + 0.07t_{cyc1}$	ns		
CLK1 rise time	t_{cr}	—	5.0	ns		
CLK1 fall time	t_{cf}	—	5.0	ns		
MCLK rise time	t_{mcr}	—	4.5	ns		
MCLK fall time	t_{mcf}	—	4.5	ns		

Reset

Table 7.5 Reset

Item	Symbol	Min	Max	Unit	Test Conditions	Notes
$\overline{\text{RESET}}$ low pulse width	t_{RESW}	40	—	t_{cyc0}	Figure 7.4	

CPU Read Cycle

Table 7.6 CPU Read Cycle

Item	Symbol	Min	Max	Unit	Test Conditions	Notes
Address setup time	t_{ADS}	0	—	ns	Figure 7.5	
Address hold time	t_{ADH}	0	—	ns		1
$\overline{\text{CSn}}$ setup time	t_{CSS}	0	—	ns		2
$\overline{\text{CSn}}$ hold time	t_{CSH}	0	—	ns		3
$\overline{\text{WAIT}}$ cycle start time 1	t_{WAS1}	—	$3t_{cyc0}$ + 15	ns		
$\overline{\text{RD}}$ high width	t_{RDHW}	t_{cyc0}	—	ns		
Read data setup time with respect to $\overline{\text{WAIT}}$	t_{RDDWS}	0	—	ns		
$\overline{\text{WAIT}}$ drive time	t_{WAD}	t_{cyc0}	—	ns		
Read data turn-on time	t_{RDDON}	0	—	ns		
Read data hold time	t_{RDDH}	1.5	—	ns		
Read data turn-off time	t_{RDDOF}	1.5	—	ns		
$\overline{\text{WE}}$ high widt	t_{WEHW}	t_{cyc0}	—	ns		

Notes: 1. Address signals A22 to A1 must be held at least until the rise of $\overline{\text{WAIT}}$.

2. If the fall of $\overline{\text{CSn}}$ is later than the fall of $\overline{\text{RD}}$, the specifications for t_{ADS}, t_{WAS1}, t_{RDDON}, and t_{WEHW} are from the fall of $\overline{\text{CSn}}$. $\overline{\text{CSn}}$ = $\overline{\text{CS0}}$, $\overline{\text{CS1}}$.

3. If the rise of $\overline{\text{CSn}}$ is earlier than the rise of $\overline{\text{RD}}$, the specifications for t_{ADH}, t_{RDDH}, t_{RDDOF}, and t_{WEHW} are from the rise of $\overline{\text{CSn}}$. $\overline{\text{CSn}}$ = $\overline{\text{CS0}}$, $\overline{\text{CS1}}$.

CPU Write Cycle

Table 7.7 CPU Write Cycle

Item	Symbol	Min	Max	Unit	Test Conditions	Notes
Address setup time	t_{ADS}	0	—	ns	Figure 7.6	
Address hold time	t_{ADH}	2	—	ns		
$\overline{\text{CSn}}$ setup time	t_{CSS}	0	—	ns		1
$\overline{\text{CSn}}$ hold time	t_{CSH}	0	—	ns		2
$\overline{\text{RD}}$ high width	t_{RDHW}	t_{cyc0}	—	ns		
$\overline{\text{WAIT}}$ drive time	t_{WAD}	t_{cyc0}	—	ns		
$\overline{\text{WAIT}}$ cycle start time 2	t_{WAS2}	—	$3t_{cyc0} + 15$	ns		
$\overline{\text{WE}}$ high width	t_{WEHW}	t_{cyc0}	—	ns		3
Write data setup time with respect to $\overline{\text{WE}}$	t_{WRDES}	$2t_{cyc0}$	—	ns		3
Write data hold time	t_{WRDH}	2	—	ns		

Notes: 1. If the fall of $\overline{\text{CSn}}$ is later than the fall of $\overline{\text{WEn}}$, the specifications for t_{ADS}, t_{RDHW}, and t_{WAS2} are from the fall of $\overline{\text{CSn}}$. $\overline{\text{CSn}}$ = $\overline{\text{CS0}}$, $\overline{\text{CS1}}$; $\overline{\text{WEn}}$ = $\overline{\text{WE0}}$, $\overline{\text{WE1}}$.

2. If the rise of $\overline{\text{CSn}}$ is earlier than the rise of $\overline{\text{WEn}}$, the specifications for t_{ADH}, t_{RDHW}, t_{WRDES}, t_{WRDH}, and t_{WRDOF} are from the rise of $\overline{\text{CSn}}$. $\overline{\text{CSn}}$ = $\overline{\text{CS0}}$, $\overline{\text{CS1}}$; $\overline{\text{WEn}}$ = $\overline{\text{WE0}}$, $\overline{\text{WE1}}$.

3. $\overline{\text{WEn}}$ = $\overline{\text{WE0}}$, $\overline{\text{WE1}}$.

DMA Write Cycle

Table 7.8 DMA Write Cycle

Item	Symbol	Min	Max	Unit	Test Conditions	Notes
$\overline{RD}$ high width	t_{RDHW}	t_{cyc0}	—	ns	Figure 7.7 (1), (2), (3), (4)	
$\overline{RD}$ low width	t_{RDLW}	$3t_{cyc0}$	—	ns		
$\overline{WE}$ high width	t_{WEHW}	t_{cyc0}	—	ns		
Write data hold time	t_{WRDH}	2	—	ns		
Write data setup time with respect to $\overline{RD}$	t_{WRDRS}	$2t_{cyc0}$	—	ns		
$\overline{DREQ}$ negate time with respect to $\overline{RD}$	t_{DARN}	—	$3t_{cyc0}$ + 15	ns		
$\overline{DREQ}$ assert time with respect to $\overline{RD}$	t_{DARA}	$3t_{cyc0}$ + 15	—	ns		
$\overline{DACK}$ setup time with respect to $\overline{RD}$	t_{DARS}	0	—	ns		
$\overline{DACK}$ hold time with respect to $\overline{RD}$	t_{DARH}	0	—	ns		
$\overline{DACK}$ setup time with respect to $\overline{WE}$	t_{DAWS}	0	—	ns		
$\overline{DACK}$ hold time with respect to $\overline{WE}$	t_{DAWH}	0	—	ns		
$\overline{WE}$ low width	t_{WELW}	$3t_{cyc0}$	—	ns		
Write data setup time with respect to $\overline{WE}$	t_{WRDWS}	$2t_{cyc0}$	—	ns		
Write data hold time with respect to $\overline{WE}$	t_{WRDWH}	2	—	ns		
$\overline{DREQ}$ negate time with respect to $\overline{WE}$	t_{DAWN}	—	$3t_{cyc0}$ + 15	ns		
$\overline{DREQ}$ hold time with respect to $\overline{WE}$	t_{DAWA}	$3t_{cyc0}$ + 15	—	ns		

Notes: 1. If the fall of $\overline{DACK}$ is later than the fall of $\overline{RD}$, the specification for t_{RDLW} is from the fall of $\overline{DACK}$.

2. If the rise of $\overline{DACK}$ is earlier than the rise of $\overline{RD}$, the specifications for t_{RDLW}, t_{WRDH}, and t_{WRDRS} are from the rise of $\overline{DACK}$.

3. If the fall of $\overline{DACK}$ is later than the fall of $\overline{WEn}$, the specification for t_{WELW} is from the fall of $\overline{DACK}$. $\overline{WEn}$ = $\overline{WE0}$, $\overline{WE1}$.

4. If the rise of $\overline{DACK}$ is earlier than the rise of $\overline{WEn}$, the specifications for t_{WELW}, t_{WRDWS}, and t_{WRDWH} are from the rise of $\overline{DACK}$. $\overline{WEn}$ = $\overline{WE0}$, $\overline{WE1}$.

Interrupt Output

Table 7.9 Interrupt Output

Item	Symbol	Min	Max	Unit	Test Conditions	Notes
$\overline{\text{IRL}}$ delay time	t_{IRD}	—	15	ns	Figure 7.8	

UGM Read Cycle

Table 7.10 UGM Read Cycle

Item	Symbol	Min	Max	Unit	Test Conditions	Notes
MD input setup time	t_{MDIS}	6	—	ns	Figure 7.9	
MD input hold time	t_{MDIH}	3	—	ns		
MD input turn-on time	t_{MDIN}	0	—	ns		
MD input turn-off time	t_{MDIF}	—	9	ns		
MA delay time	t_{MAD}	—	12	ns		
MA hold time	t_{MAH}	1	—	ns		
MD output turn-off time	t_{MDOF}	—	12	ns		
MD output turn-on time	t_{MDON}	0	—	ns		
MCS delay time	t_{MCSD}	—	12	ns		
MCS hold time	t_{MCSH}	1	—	ns		

UGM Write Cycle

Table 7.11 UGM Write Cycle

Item	Symbol	Min	Max	Unit	Test Conditions	Notes
MD output delay time	t_{MDOD}	—	12	ns	Figure 7.10	
MD output hold time	t_{MODH}	1	—	ns		
MA delay time	t_{MAD}	—	12	ns		
MA hold time	t_{MAH}	1	—	ns		
MCS delay time	t_{MCSD}	—	12	ns		
MCS hold time	t_{MCSH}	1	—	ns		

UGM Refresh Cycle/Mode Register Setting Cycle

Table 7.12 UGM Refresh Cycle/Mode Register Setting Cycle

Item	Symbol	Min	Max	Unit	Test Conditions	Notes
MA delay time	t_{MAD}	—	12	ns	Figure 7.11 (1), (2)	
MA hold time	t_{MAH}	1	—	ns		
MCS delay time	t_{MCSD}	—	12	ns		
MCS hold time	t_{MCSH}	1	—	ns		

Master Display Mode

Table 7.13 Master Display Mode

Item	Symbol	Min	Max	Unit	Test Conditions	Notes
HSYNC delay time from CLK1	t_{HSDD}	—	15	ns	Figure 7.12	
VSYNC delay time from CLK1	t_{VSDD}	—	15	ns		
ODDF delay time from CLK1	t_{ODDD}	—	15	ns		
CSYNC delay time from CLK1	t_{SYDD}	—	15	ns		
DISP delay time from CLK1	t_{DIDD}	—	15	ns		
CDE delay time from CLK1	t_{CDEDD}	—	15	ns		

TV Sync Display Mode

Table 7.14 TV Sync Display Mode

Item	Symbol	Min	Max	Unit	Test Conditions	Notes
DISP delay time from CLK1	t_{DIDD}	—	15	ns	Figure 7.13 (1), (2)	
CDE delay time from CLK1	t_{CDEDD}	—	15	ns		
$\overline{EXHSYNC}$ low width	t_{EXLLW}	$4t_{cyc1}$	—	ns		
$\overline{EXHSYNC}$ high width	t_{EXHHW}	$4t_{cyc1}$	—	ns		
$\overline{EXHSYNC}$ reception undefined time 1	t_{EXH1}	5	—	ns		
$\overline{EXHSYNC}$ reception undefined time 2	t_{EXH2}	5	—	ns		
DISP start time with respect to $\overline{EXHSYNC}$	t_{DIEXH}	hds – 1	hds – 1	t_{cyc1}		*
$\overline{EXVSYNC}$ low width	t_{EXVLW}	3HC	—	t_{cyc1}		
$\overline{EXVSYNC}$ reception undefined time 1	t_{EXV1}	5	—	ns		
$\overline{EXVSYNC}$ reception undefined time 2	t_{EXV2}	5	—	ns		
$\overline{ODDF}$ reception undefined time 1	t_{OD1}	(ys + yw) × HC	—	t_{cyc1}		
$\overline{ODDF}$ reception undefined time 2	t_{OD2}	$1t_{cyc1}$	—	ns		

Note: * hds = hsw + xs

Video Interface

Table 7.15 Video Interface

Item	Symbol	Min	Max	Unit	Test Conditions	Notes
VQCKL high pulse width	t_{QHW}	15	—	ns	Figure 7.14 (1), (2)	
VQCKL low pulse width	t_{QLW}	15	—	ns		
VODD setup time	t_{VOS}	1		t_{cyc0}		
VIN setup time	t_{VNS}	5		ns		
VIN hold time	t_{VNH}	11.7		ns		
$\overline{VVS}$ low pulse width	t_{VVL}	2		Hline		*
$\overline{VHS}$ low pulse width	t_{VHL}	64		t_{cyc0}		
VQCLK rise—VQCLK rise interval	t_{QQP}	34.5		ns		$t_{QQP} > 2 \times t_{cyc0}$

Note: * Hline is the $\overline{VHS}$ cycle.

Video DAC

Table 7.16 Video DAC

Item	Symbol	Min	Max	Unit	Test Conditions	Notes
Resolution		8	8	Bit	DC test	
Differential linearity error		—	0.5	LSB	DC test	
Conversion speed		—	33	MHz	Data write test	
Maximum output current	I_{out}		3	mA		
Analog full-scale output		0.9	1.1	V	DC test	
Analog zero-scale output		–0.1	0.1	V	DC test	
Full-scale error		–10	10	%	DC test	

7.5 Timing Charts

7.5.1 Clocks

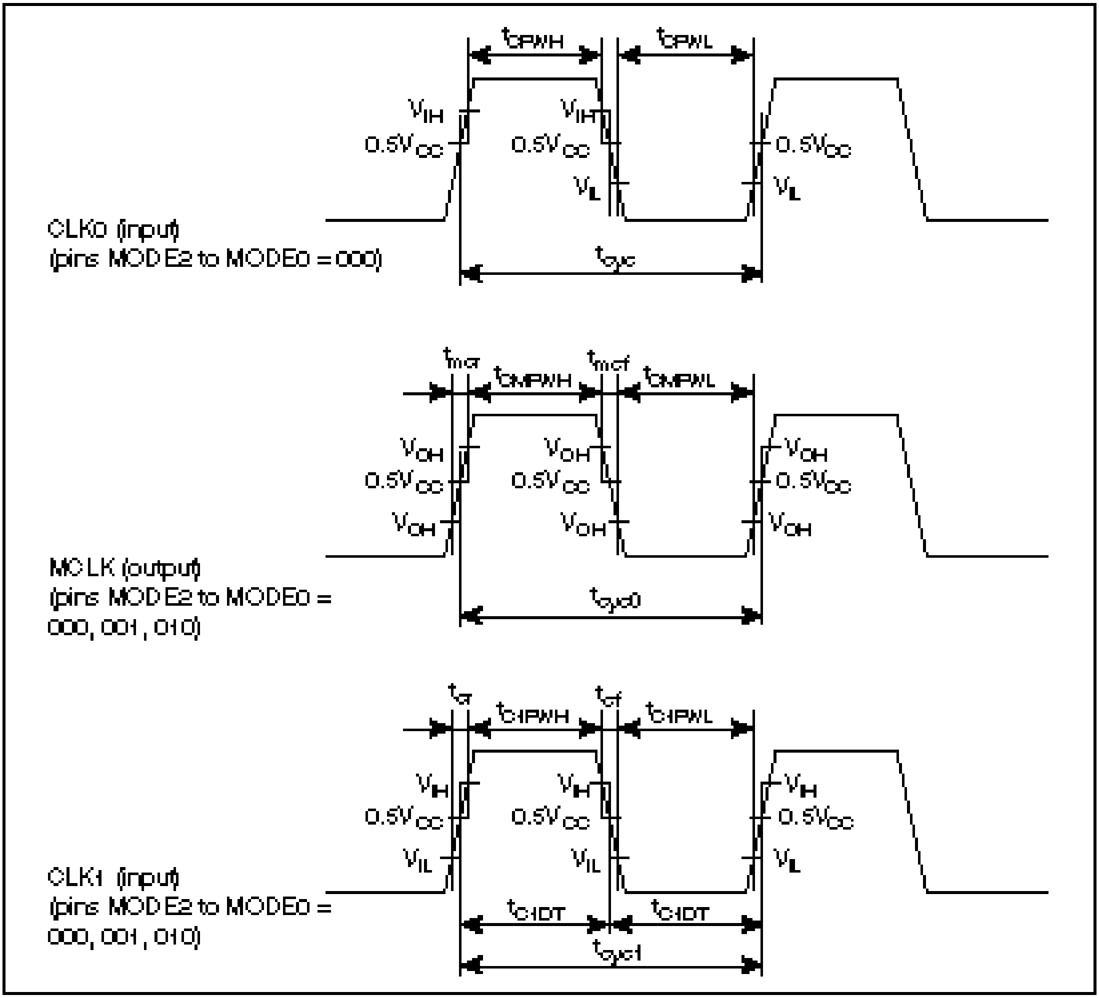


Figure 7.3 Input Clocks

7.5.2 Reset Timing

Figure 7.4 Reset Timing

7.5.3 CPU Read Cycle Timing

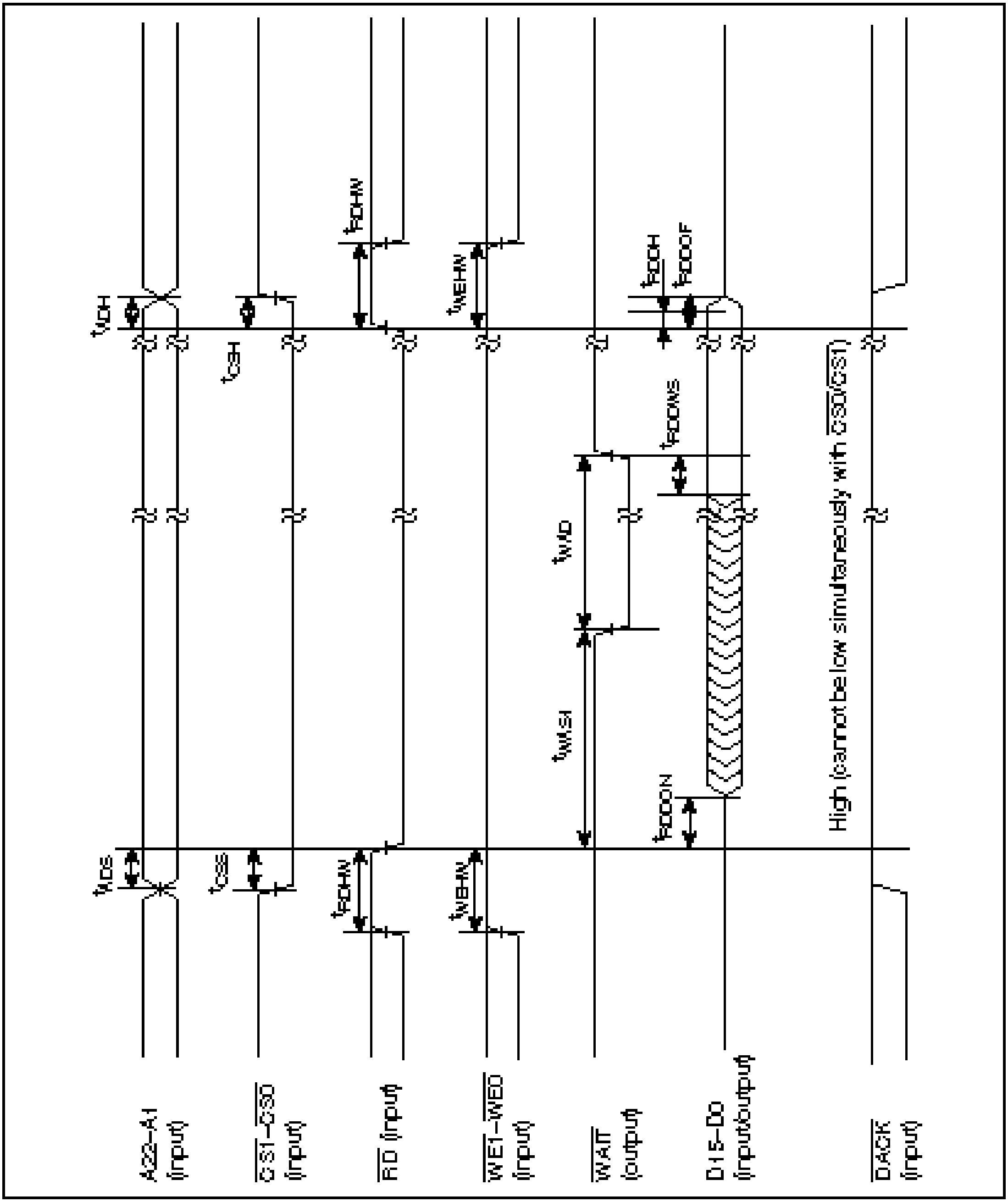


Figure 7.5 CPU Read Cycle Timing (CPU ← Q2SD) with Hardware Wait

7.5.4 CPU Write Cycle Timing

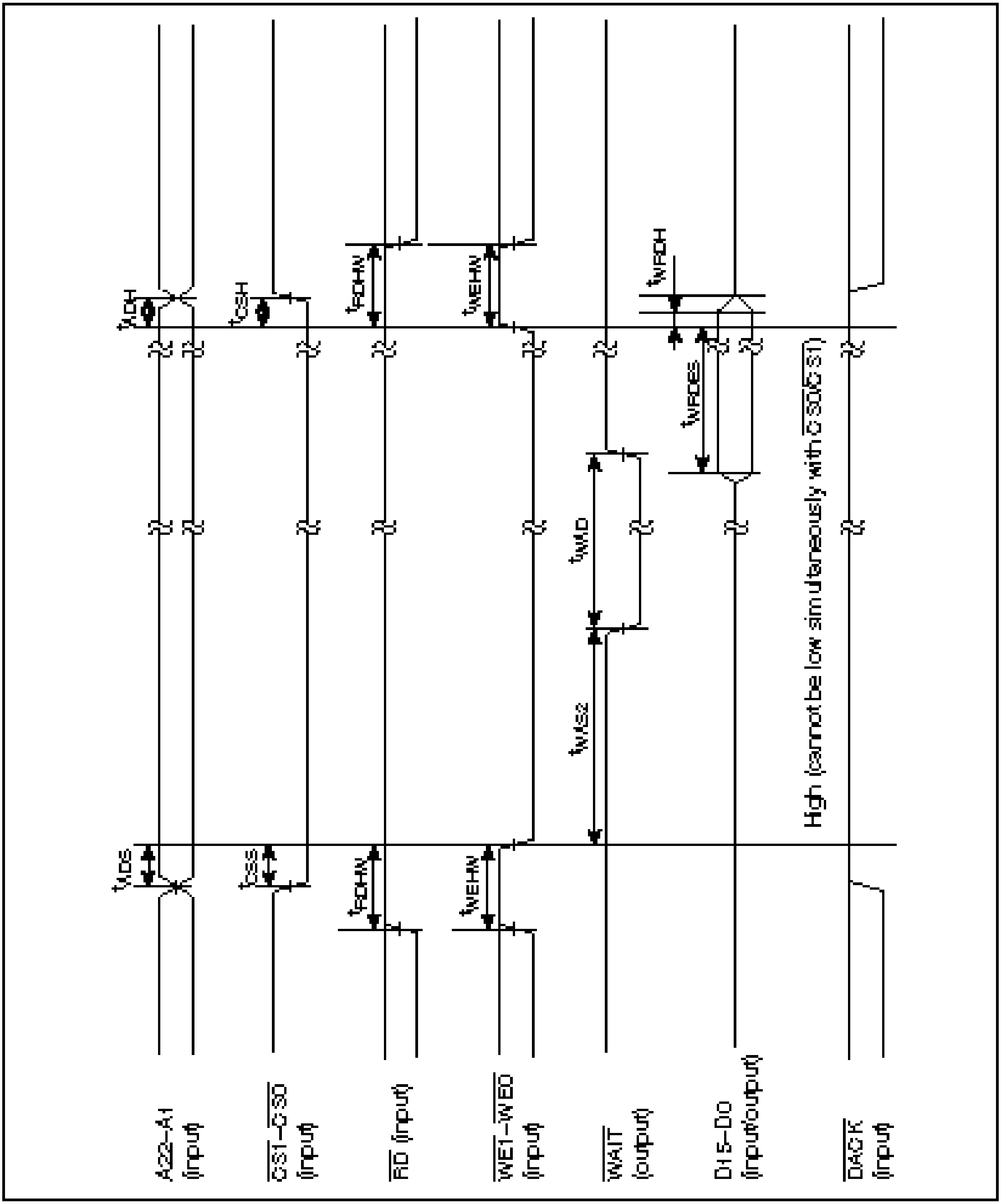


Figure 7.6 CPU Read Cycle Timing (CPU → Q2SD) with Hardware Wait

7.5.5 DMA Write Cycle Timing (DMAC → Q2SD)

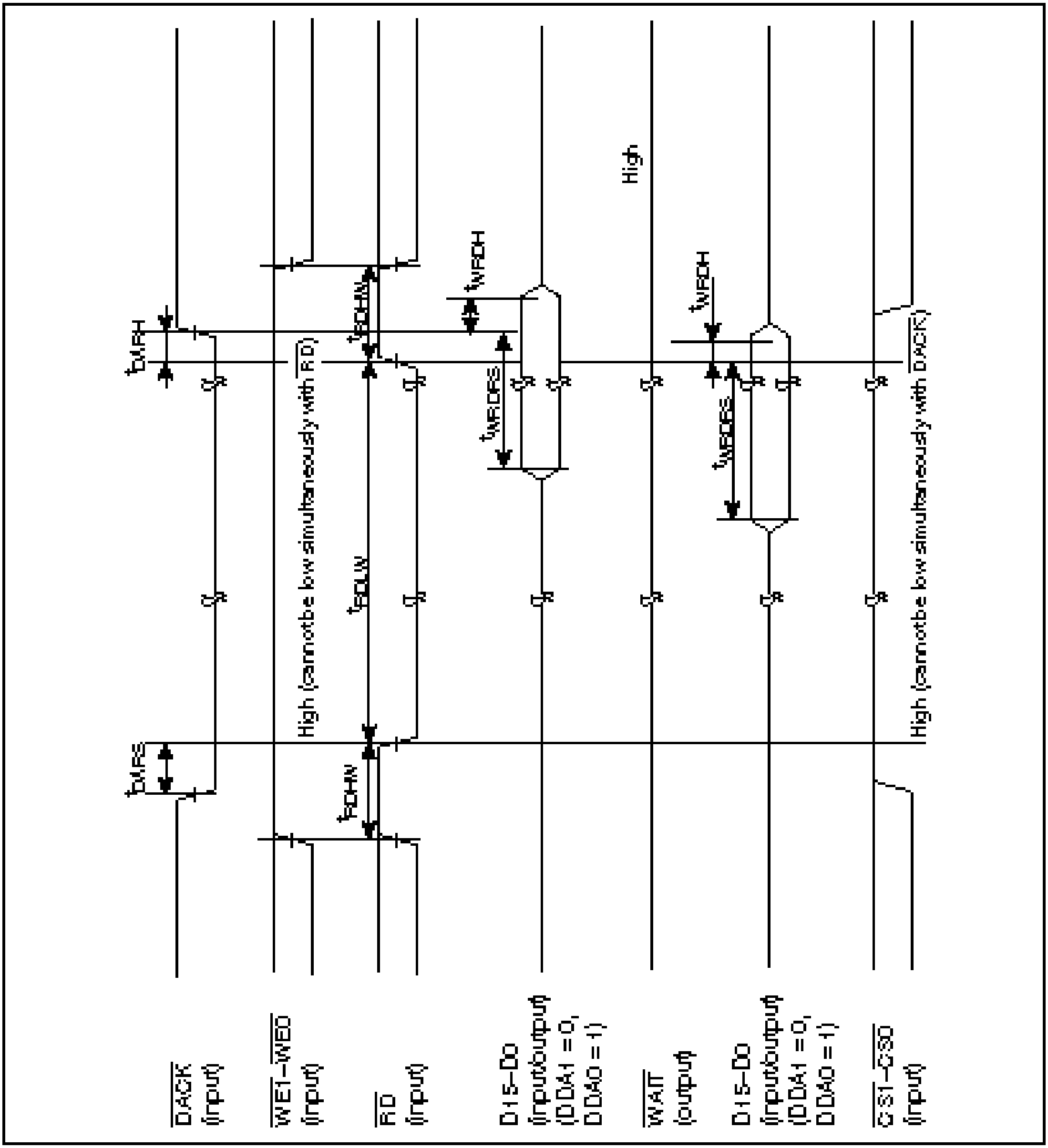


Figure 7.7 (1) DMA Write Cycle Timing (Single Address, DMAC → Q2SD)

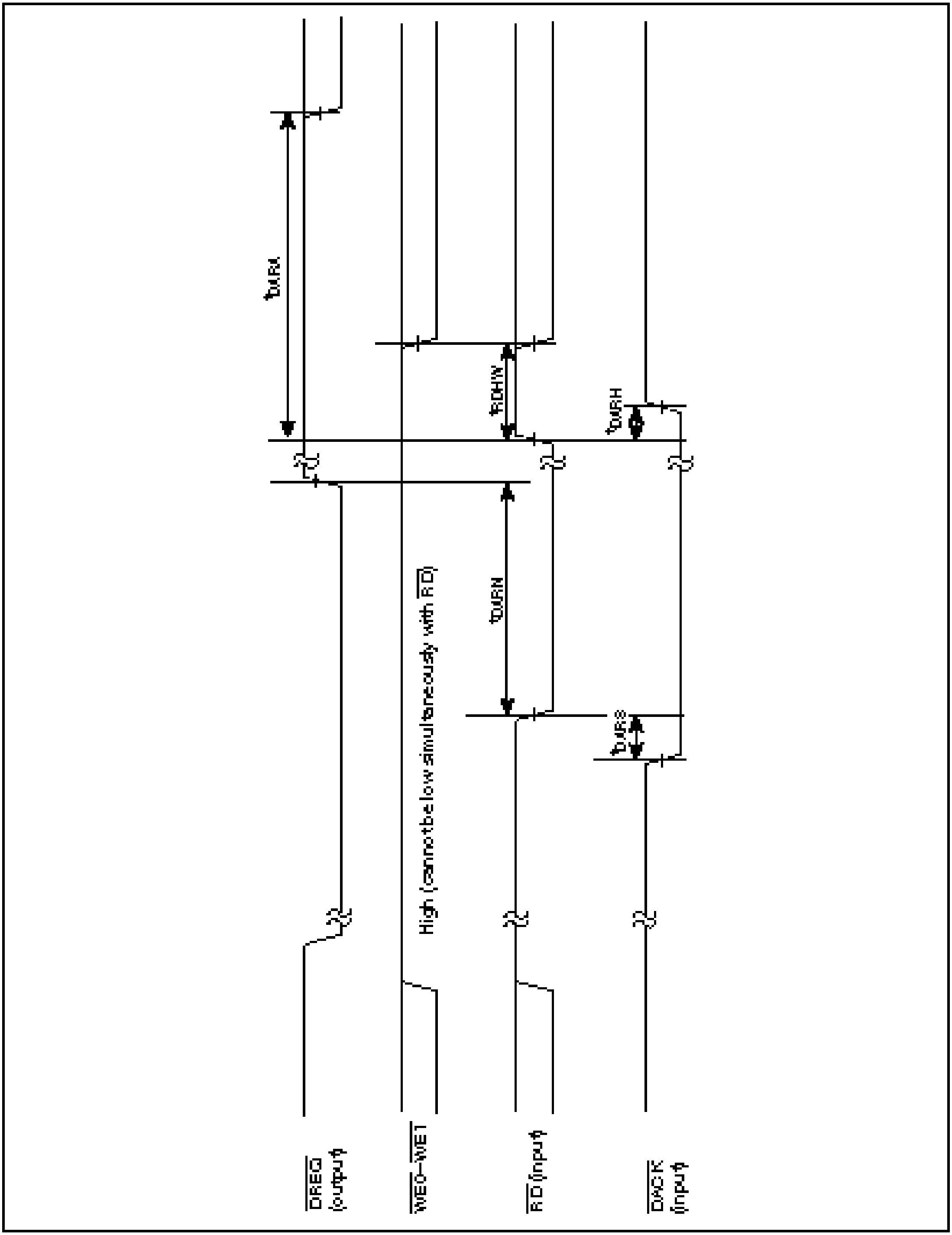


Figure 7.7 (2) DMA Write Cycle Timing (Single Address, DMAC → Q2SD)

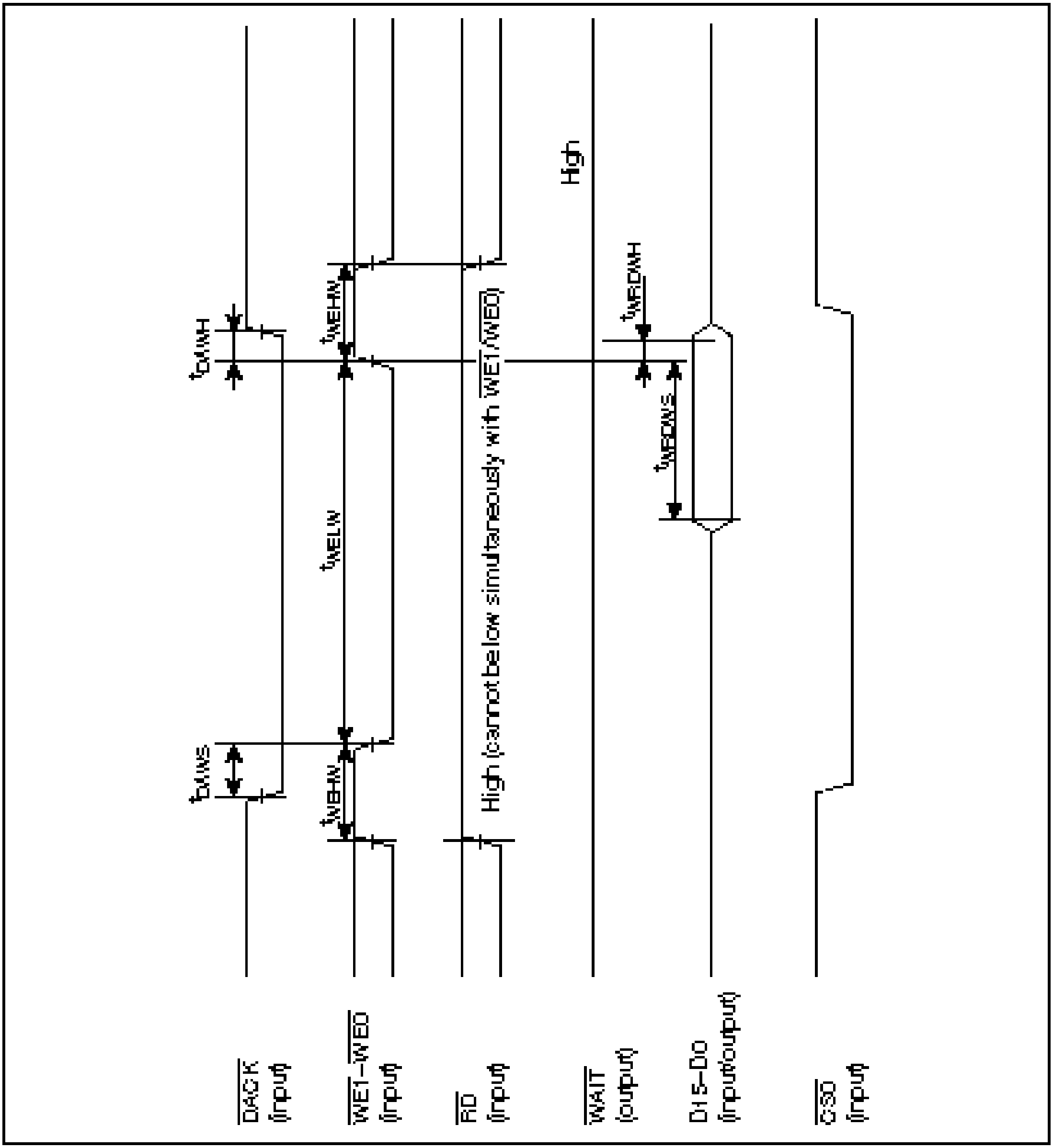


Figure 7.7 (3)   DMA Write Cycle Timing (Dual Address, DMAC → Q2SD)

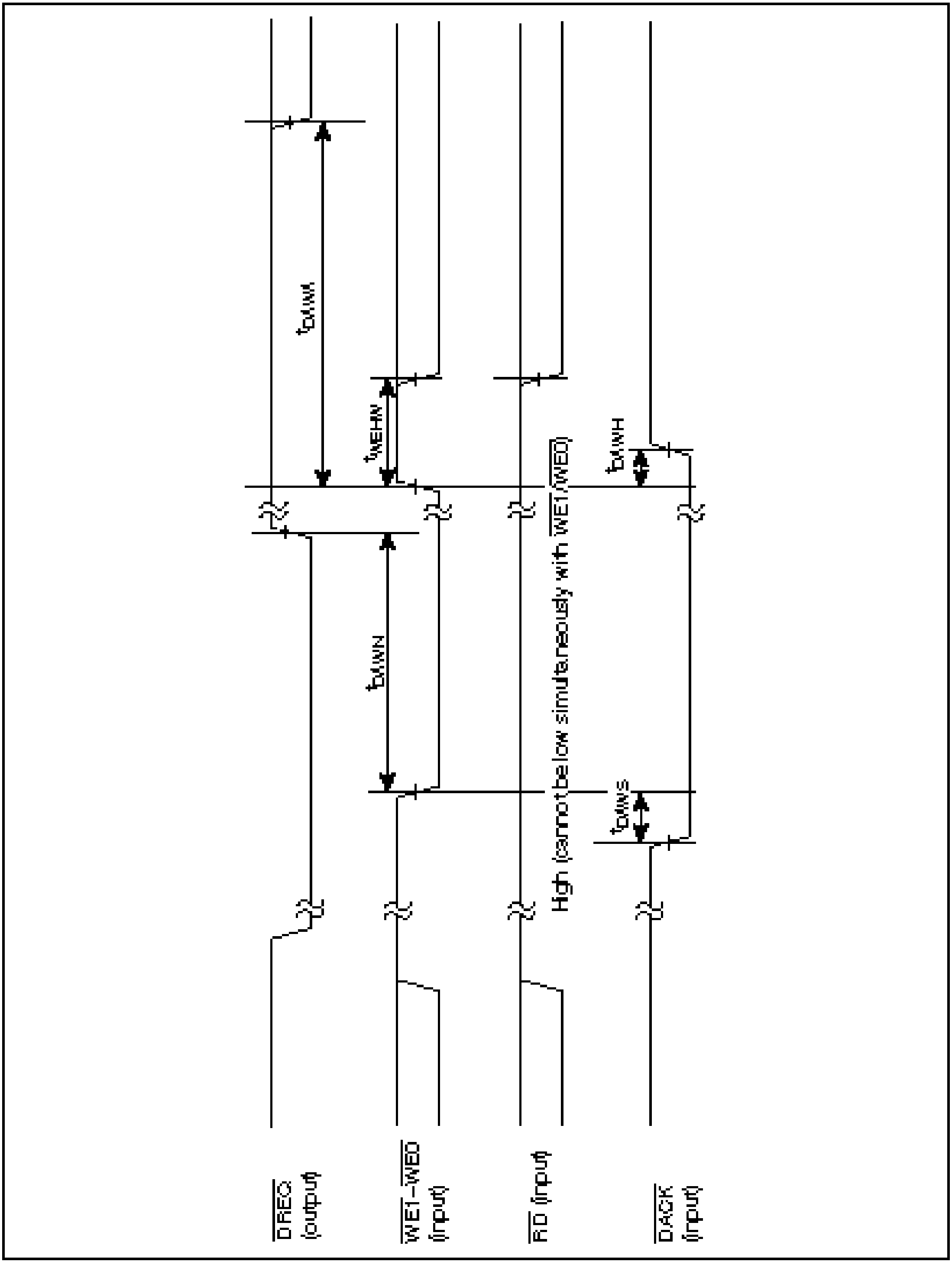


Figure 7.7 (4) DMA Write Cycle Timing (Dual Address, DMAC → Q2SD)

7.5.6 Interrupt Output Timing

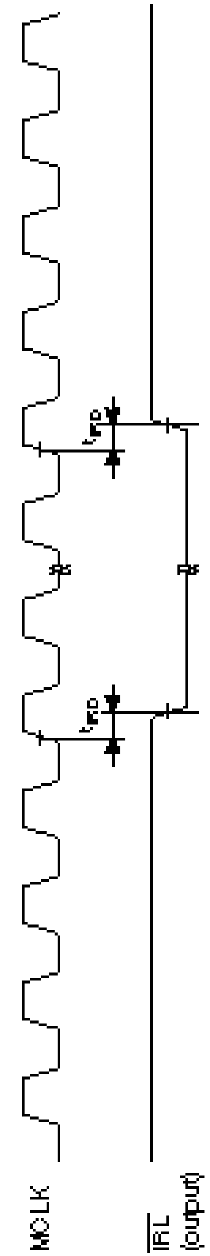


Figure 7.8 Interrupt Output Timing

7.5.7 UGM Read Cycle Timing

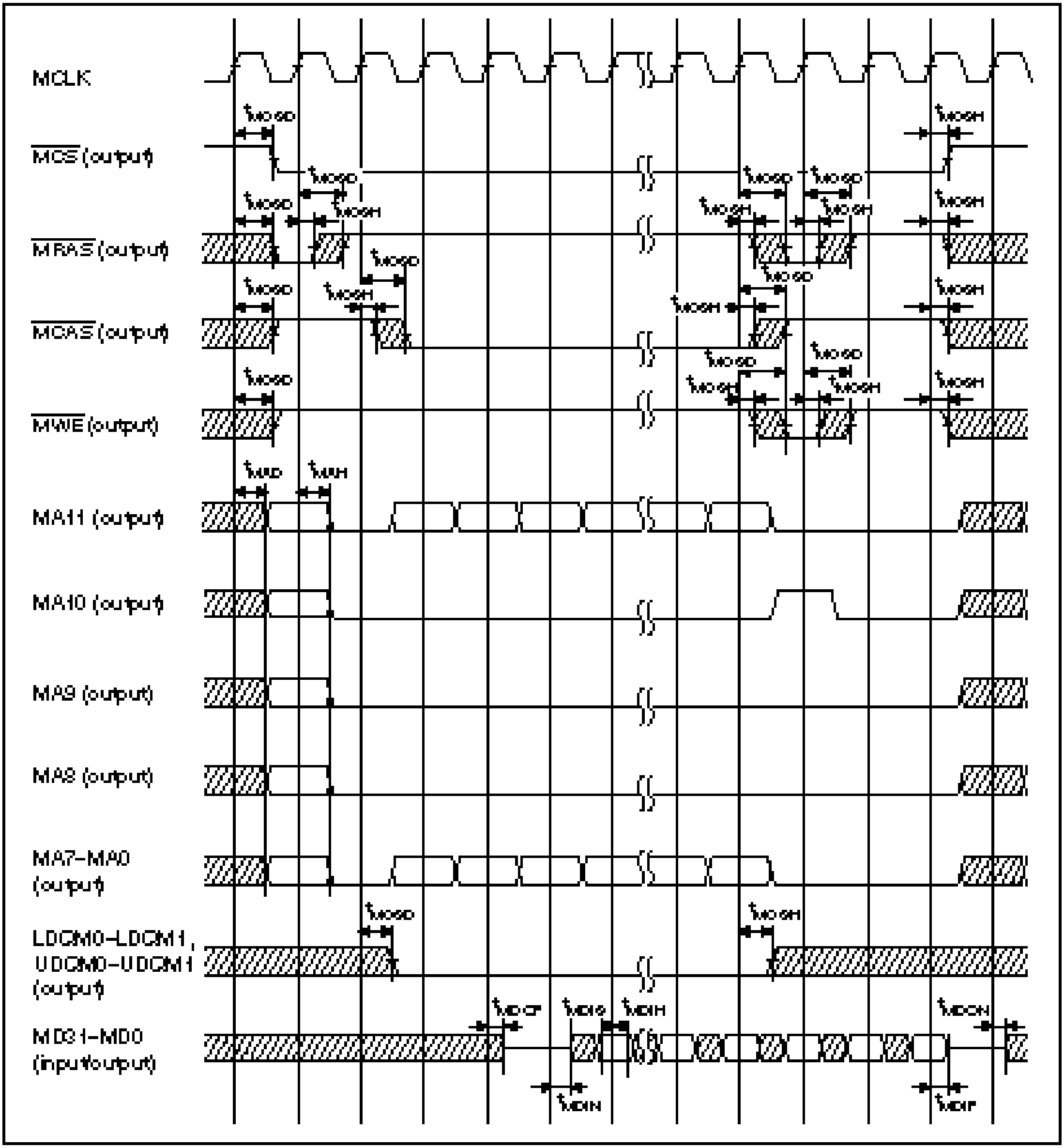


Figure 7.9 UGM Read Cycle Timing

7.5.8 UGM Write Cycle Timing

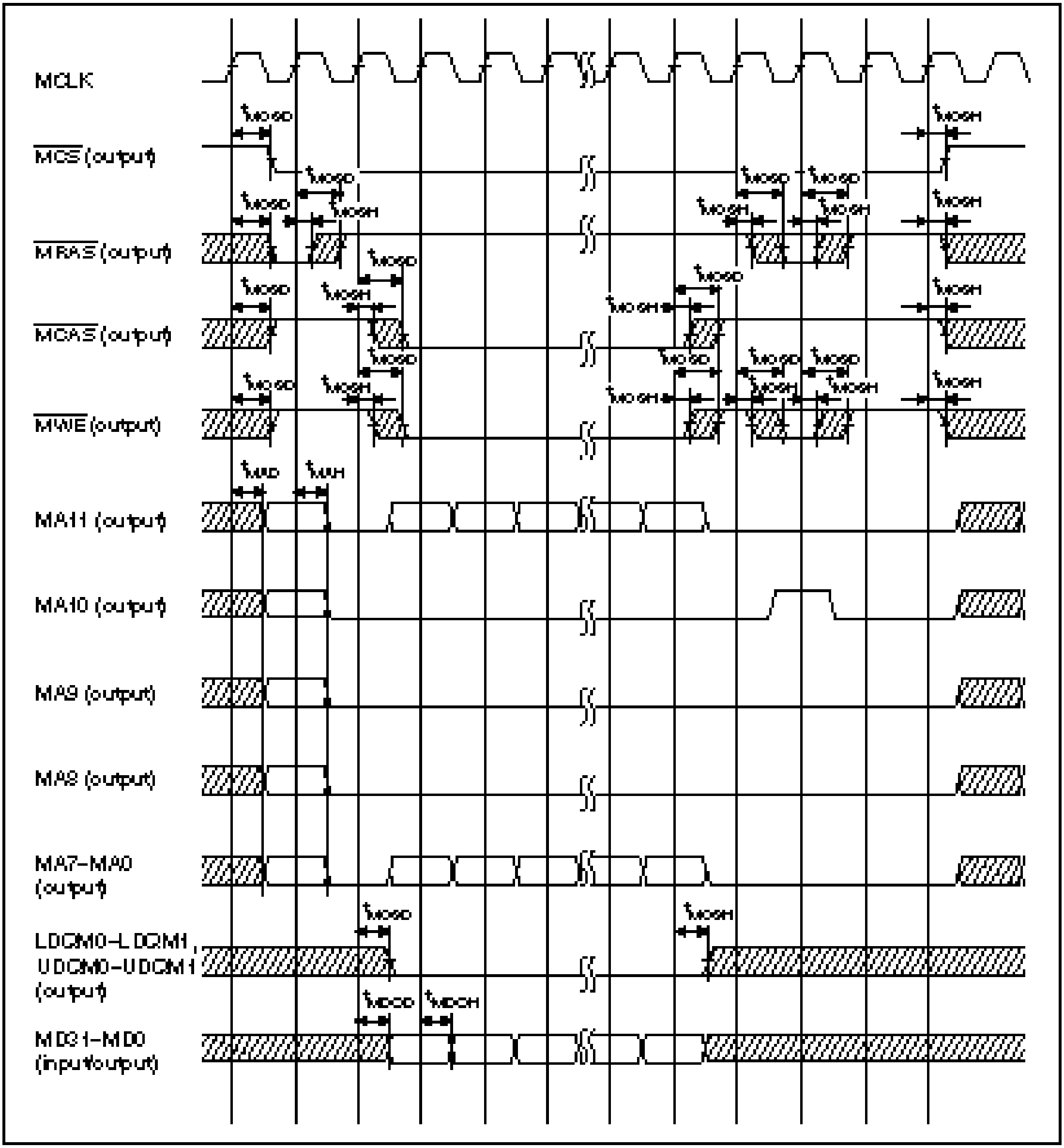


Figure 7.10 UGM Write Cycle Timing

7.5.9 UGM Refresh Cycle Timing and Mode Register Setting Timing

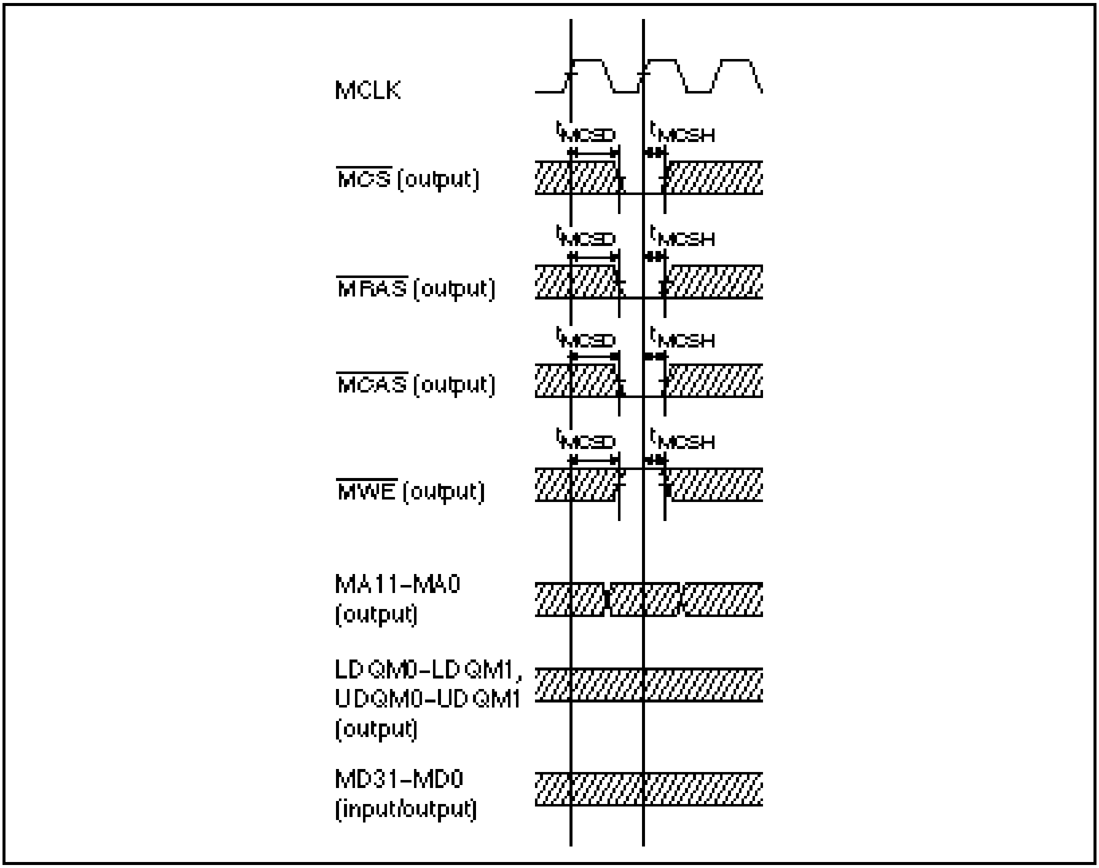


Figure 7.11 (1) UGM Refresh Cycle Timing

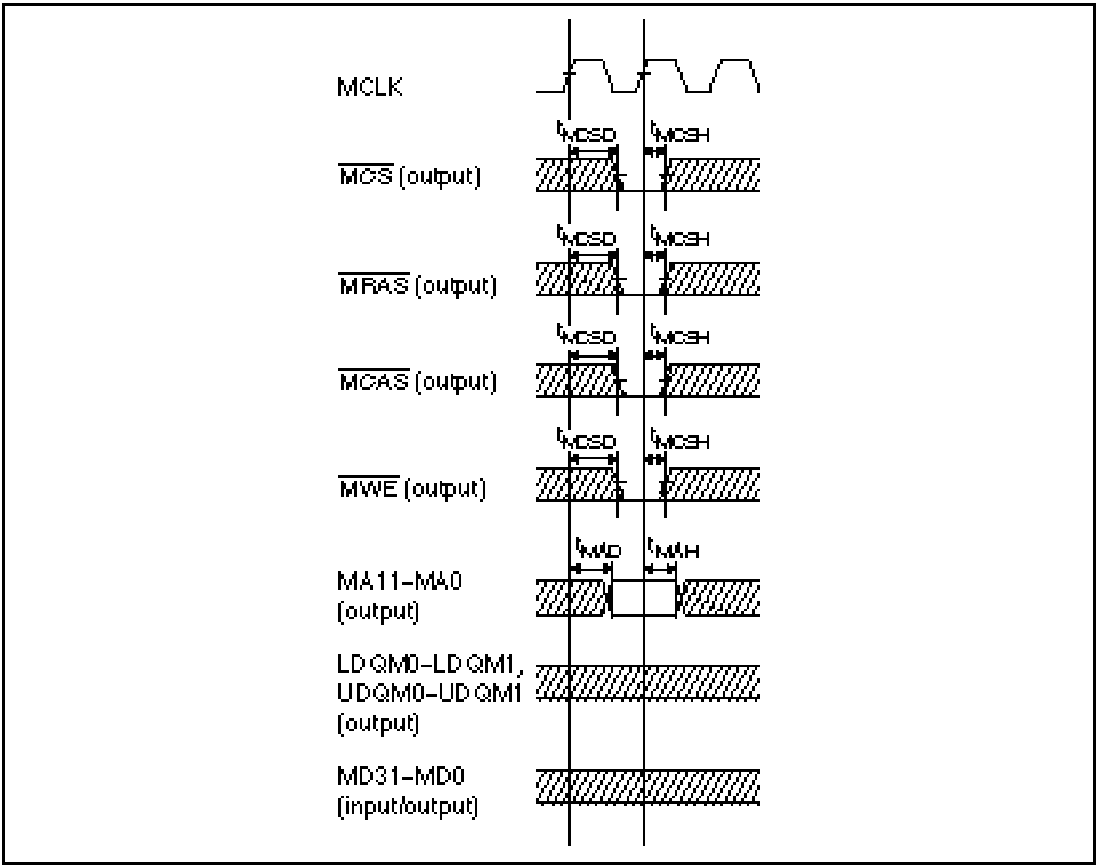


Figure 7.11 (2) UGM Mode Register Setting Cycle Timing

7.5.10 Master Mode Display Timing

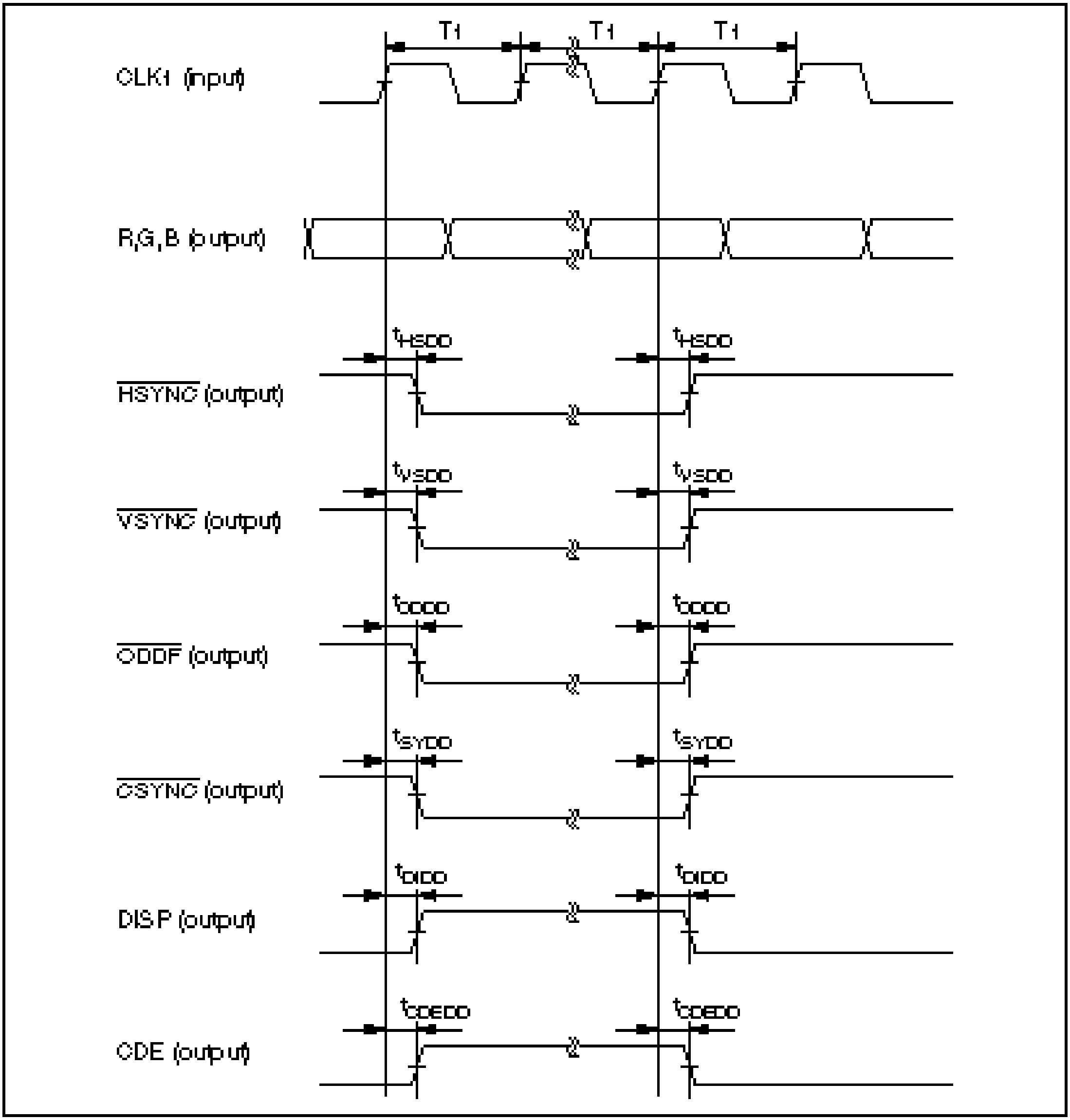


Figure 7.12 Master Mode Display Timing

7.5.11 TV Sync Mode Display Timing

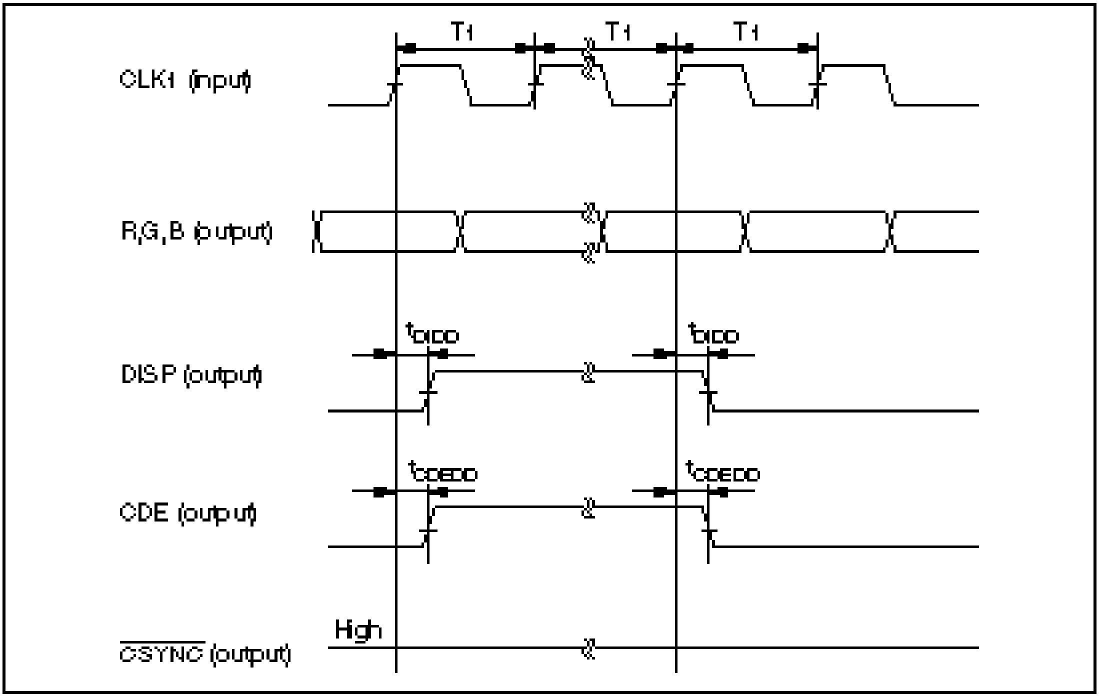


Figure 7.13 (1) TV Sync Mode Display Timing

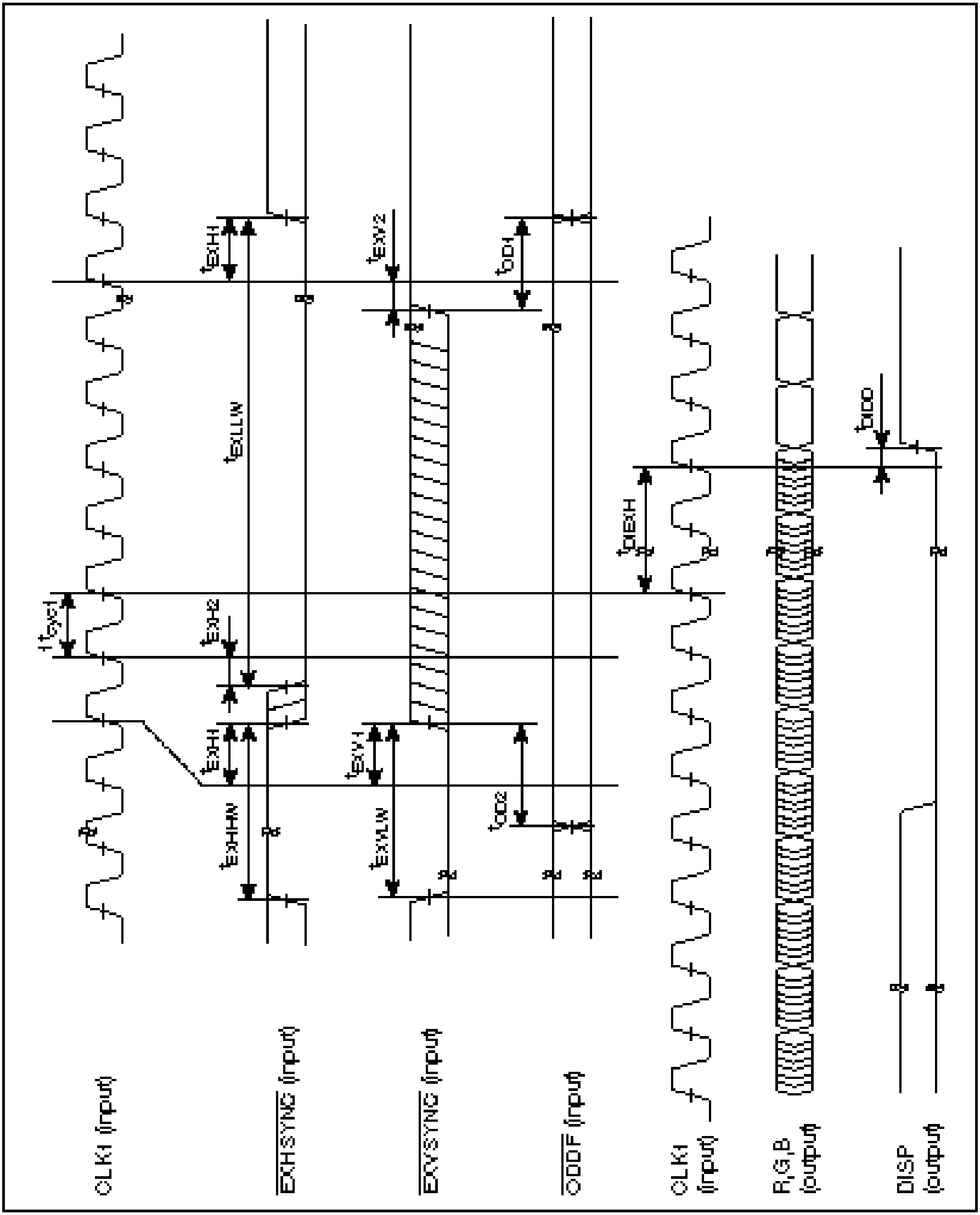


Figure 7.13 (2) TV Sync Mode Display Timing

7.5.12 Video Interface Timing

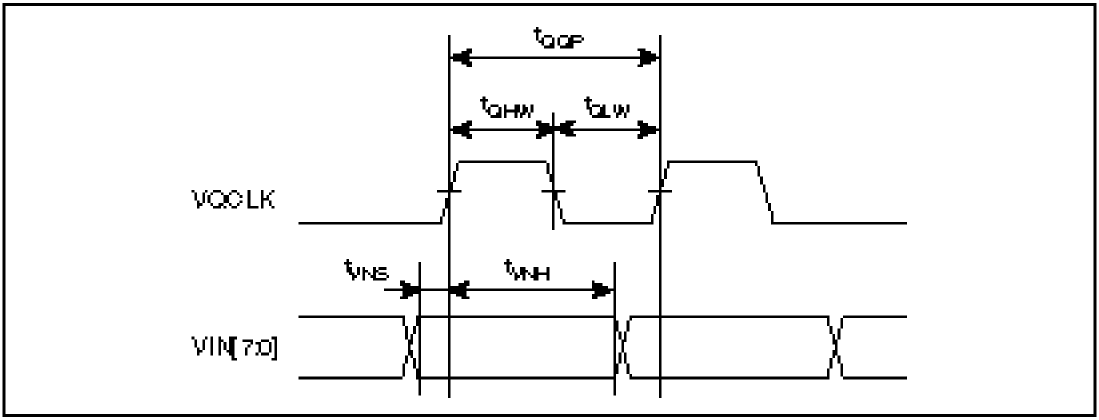


Figure 7.14 (1) Video Interface Timing

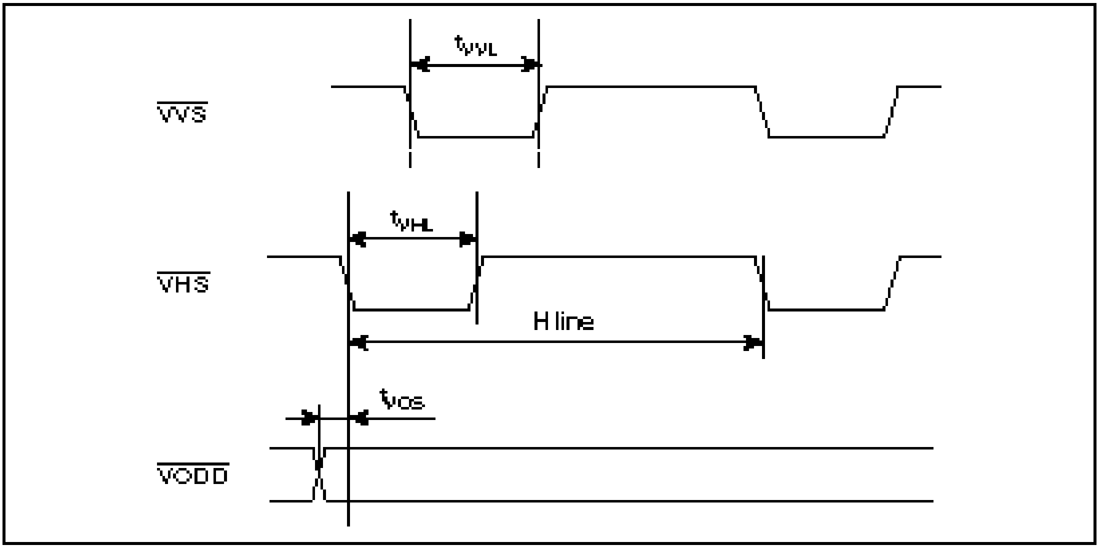


Figure 7.14 (2) Video Interface Timing

Appendix A Initial Register Values

Table A.1 Initial Register Values after Hardware Reset

Register Address CS1	Register Address A [10:1]	R/W	Register Name		Abbreviation	Data 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	—	—	—		—	—															
0	000	R/W	System control		SYSR	1	1	0			0	0	0	DEM		0	0	0	0		
	001	R	Status		SR	0	0	0	0	0	0	0	DEF	0	1			0	1	0	0
	002	W	Status register clear		SRCR	TVCL	FRCL	DMCL	CECL	VBCL	TRCL	CSCL		ERCL							
	003	R/W	Interrupt enable		IER	0	0	0	0	0	0	0		0							
	004	R/W	Memory mode		MEMR											0	0				0
	005	R/W	Display mode		DSMR	0				0	0			1	0	SGM		1	0	0	0
	006	R/W	Rendering mode		REMR	0									MWX				GEM		
	007	R/W	Input data conversion mode		IEMR												0	0	0	0	0
	010	R/W	DMA transfer start address	H	DMASR										0	0	0	0	0	0	0
	011	R/W		L		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	012	R/W	DMA transfer word count	L	DMAWR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	021	R/W	Image data transfer start address	H	ISAR										0	0	0	0	0	0	0
	022	R/W		L		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	023	R/W	Image data size	X	IDSR						0	0	0	0	0	0	0	0	0	0	0
	024	R/W		Y								0	0	0	0	0	0	0	0	0	0
	025	W	Image data entry		IDER	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	026	R/W	DMA transfer word count	H	DMAWR														0	0	0
	028	R/W	Display mode 2		DSMR2				0	0	0	0	0	GSV		0		0	0	0	0
	029	R/W	Video incorporation mode		VIMR	1	1					0	0	0	0	0	0	0	0	0	0

Only bits marked ☐ are affected by a reset. Registers other than those shown above are not affected by a reset.

Appendix B Drawing Commands and Parameters

B.1 Relationship Between Drawing Commands and Rendering Attributes

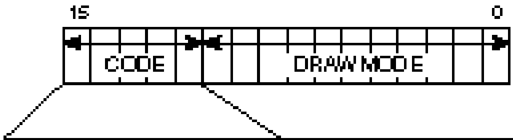
Table B.1 Relationship Between Drawing Commands and Rendering Attributes

Command	Reference Data				Drawing Destination		Rendering Attributes													
	Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work	TRNS	STYL	CLIP	NET	ECS	HALF	WORK	Bold Line Drawing	FST	LNi	EDG	REL	COOF	Line drawing edge
POLYGON4A	O		A		O		*1	*1	O	*1	*1		*1		O	*1		*2	O	
POLYGON4B		O	A		O		O	O	O	O	O	O	O					O		
POLYGON4C			A	O	O				O	*1	*1		*1		O					
LINE				O	O				O	O	O			O						
RLINE				O	O				O	O	O			O						
PLINE		O			O		O	O	O	O	O									O
RPLINE		O			O		O	O	O	O	O									O
FTRAP						O			O		B						O			
RFTRAP						O			O		B						O			
CLRW						O			O											
LINEW				V		O			O		O									
RLINEW				V		O			O		O									
MOVE																				
RMOVE																				
LCOFS																				
RLCOFS																				
CLIP																				
WPR																				
JUMP																		O		
GOSUB																		O		
RET																				
NOPs																				
VBKEM																				
TRAP																				

O: Can be used
V: Can be used (specified color is binary ECS bit value)
A: Referenced depending on mode (valid when WORK = 1)
B: Referenced depending on mode (valid when EDG = 1)
*1: Referenced depending on mode (clear to 0 when FST = 1)
*2: Referenced depending on mode (clear to 0 when LNi = 1)
Blank: Cannot be used (clear to 0)

B.2 Drawing Command Codes

Table B.2 Drawing Command Codes

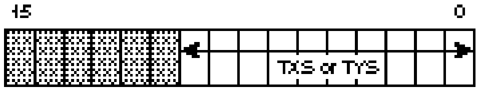


CODE					COMMAND
0	0	0	0	0	POLYGON4A
0	0	0	0	1	POLYGON4B
0	0	0	1	0	POLYGON4C
0	1	0	0	0	FTRAP
0	1	0	0	1	RFTRAP
0	1	0	1	0	LINEW
0	1	0	1	1	RLINEW
0	1	1	0	0	LINE
0	1	1	0	1	RLINE
0	1	1	1	0	PLINE
0	1	1	1	1	RPLINE
1	0	0	0	0	MOVE
1	0	0	0	1	RMOVE
1	0	0	1	0	LCOFS
1	0	0	1	1	RLCOFS
1	0	1	0	0	CLRW
1	0	1	0	1	UCLIP
1	0	1	1	0	WPR
1	0	1	1	1	SCLIP
1	1	0	0	0	JUMP
1	1	0	0	1	GOSUB
1	1	0	1	0	VBKEM
1	1	0	1	1	RET
1	1	1	1	1	TRAP
1	1	1	1	0	NOP3

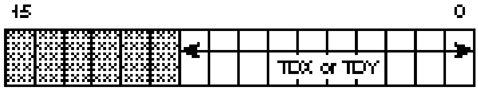
B.3 Drawing Command Parameter Specifications

POLYGON4 Commands

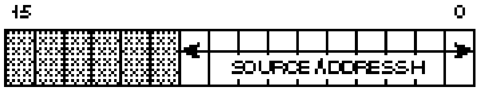
: Fixed at 0



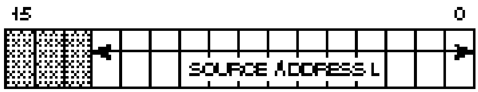
Source starting point TXS or TYS
Given as unsigned max. 10-bit data.
Specify correctly according to source area size.



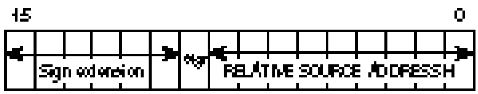
Source size TDX or TDY
Given as unsigned max. 10-bit data.
TDX can only be set in 8-pixel units.



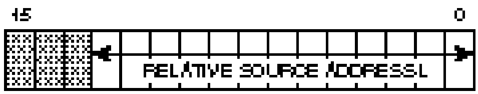
1-bit/pixel source start upper address
Given as upper 10 bits.



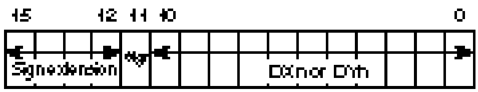
1-bit/pixel source start lower address
Given as lower 13 bits.
Source address is set as a byte address.



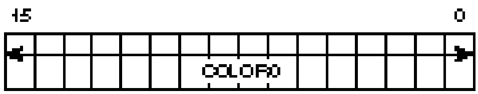
Source start relative upper address
Given as upper 10 bits.
Use sign extension in upper vacant bits.



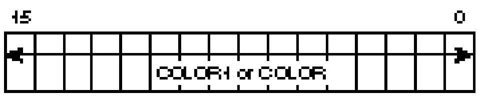
Source start relative lower address
Given as lower 13 bits.



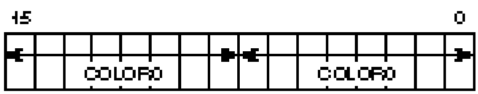
Rendering, work coordinate
Vertex coordinate DXn or DYn ($1 \leq n \leq 4$)
Given as signed 12-bit data.
Use sign extension in upper vacant bits.



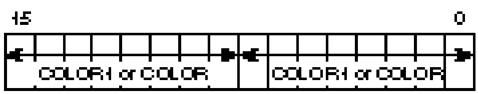
16-bit/pixel color specification
Color data 0 given as 16-bit data.



16-bit/pixel color specification
Color data 1 given as 16-bit data.

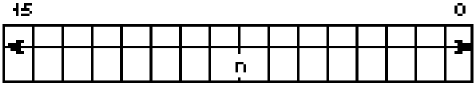


8-bit/pixel color specification
Color data 0 given as repeated 8-bit data.

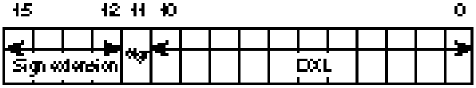


8-bit/pixel color specification
Color data 1 given as repeated 8-bit data.

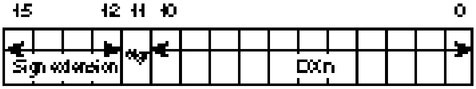
FTRAP, RFTRAP



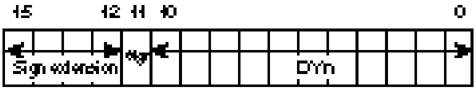
Number of vertices (2 ≤ n ≤ 65,535), absolute
(1 ≤ n ≤ 65,535), relative
Given as unsigned 16-bit data.



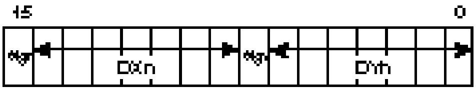
Lefthand side coordinate DXL
Given as signed 12-bit data.
Use sign extension in upper vacant bits.



Absolute coordinate
Vertex coordinate DXn (2 ≤ n ≤ 65,535)
Given as signed 12-bit data.
Use sign extension in upper vacant bits.

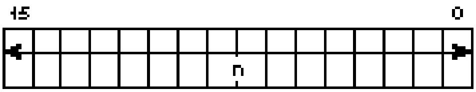


Absolute coordinate
Vertex coordinate DYn (2 ≤ n ≤ 65,535)
Given as signed 12-bit data.
Use sign extension in upper vacant bits.

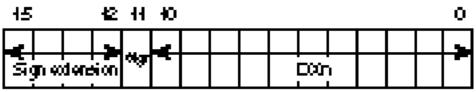


Relative coordinates
Vertex coordinates DXn, DYn (1 ≤ n ≤ 65,535)
Given as signed 8-bit data.

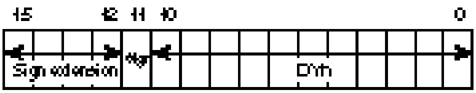
LINEW, RLINEW



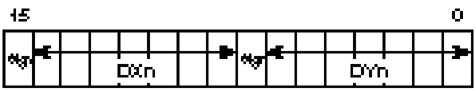
Number of vertices (2 ≤ n ≤ 65,535), absolute
(1 ≤ n ≤ 65,535), relative
Given as unsigned 16-bit data.



Absolute coordinate
Vertex coordinate DXn (2 ≤ n ≤ 65,535)
Given as signed 12-bit data.
Use sign extension in upper vacant bits.

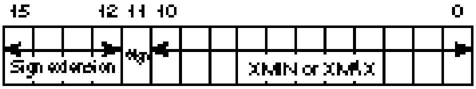


Absolute coordinate
Vertex coordinate DYn (2 ≤ n ≤ 65,535)
Given as signed 12-bit data.
Use sign extension in upper vacant bits.

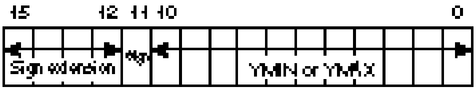


Relative coordinates
Vertex coordinates DXn, DYn (1 ≤ n ≤ 65,535)
Given as signed 8-bit data.

CLRW

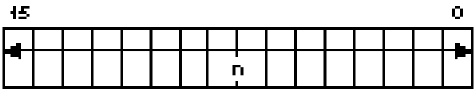


Left and right X coordinates XMIN, XMAX
Given as unsigned 12-bit data.

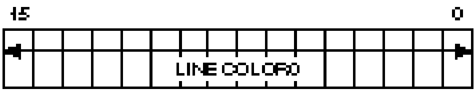


Upper and lower Y coordinates YMIN, YMAX
Given as signed 12-bit data.

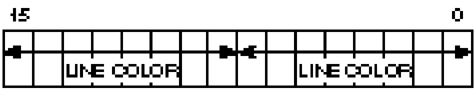
LINE, RLINE



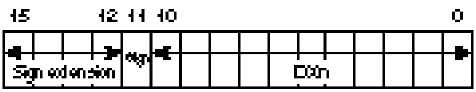
Number of vertices (2 ≤ n ≤ 65,535), absolute
(1 ≤ n ≤ 65,535), relative
Given as unsigned 16-bit data.



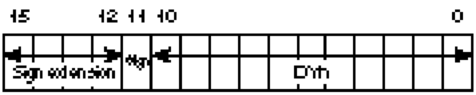
16-bit/pixel color specification
Color data given as 16-bit data.



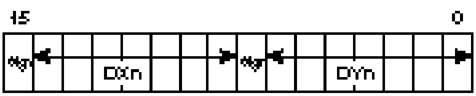
8-bit/pixel color specification
Color data given as repeated 8-bit data.



Absolute coordinate
Vertex coordinate DXn (2 ≤ n ≤ 65,535)
Given as signed 12-bit data.
Use sign extension in upper vacant bits.

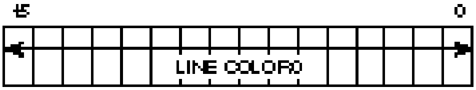


Absolute coordinate
Vertex coordinate DYn (2 ≤ n ≤ 65,535)
Given as signed 12-bit data.
Use sign extension in upper vacant bits.

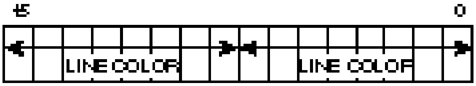


Relative coordinates
Vertex coordinates DXn, DYn (1 ≤ n ≤ 65,535)
Given as signed 8-bit data.

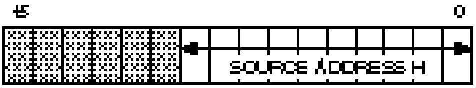
: Fixed at 0



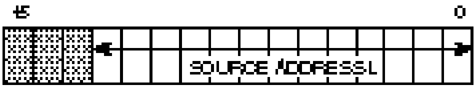
16-bit/pixel color specification
Color data given as 16-bit data.



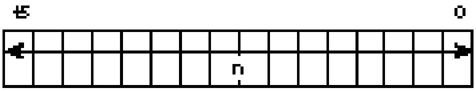
8-bit/pixel color specification
Color data given as repeated 8-bit data.



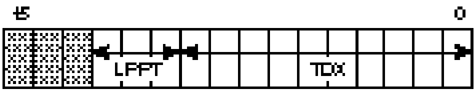
1-bit/pixel source start upper address
Given as upper 10 bits.



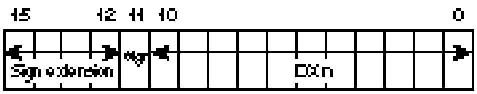
1-bit/pixel source start lower address
Given as lower 13 bits.
Source address is set as a byte address.



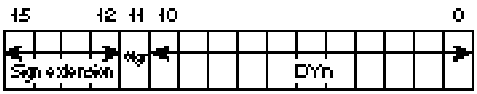
Number of vertices ($2 \leq n \leq 65,535$), absolute
($1 \leq n \leq 65,535$), relative
Given as unsigned 16-bit data.



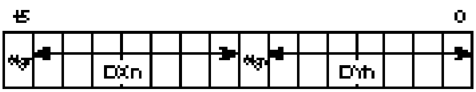
Source size TDX
Line pattern pointer LPPT
Given as unsigned max. 10-bit data.
TDX can only be set in 8-pixel units.



Absolute coordinate
Vertex coordinate DXn ($2 \leq n \leq 65,535$)
Given as signed 12-bit data.
Use sign extension in upper vacant bits.

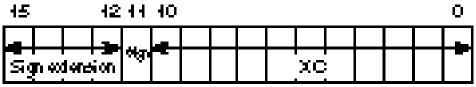


Absolute coordinate
Vertex coordinate DYn ($2 \leq n \leq 65,535$)
Given as signed 12-bit data.
Use sign extension in upper vacant bits.

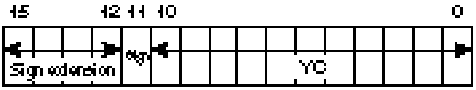


Relative coordinates
Vertex coordinates DXn, DYn ($1 \leq n \leq 65,535$)
Given as signed 8-bit data.

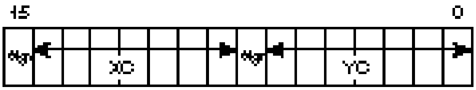
MOVE, RMOVE



Absolute coordinate
Vertex coordinate XC
Given as signed 12-bit data.
Use sign extension in upper vacant bits.

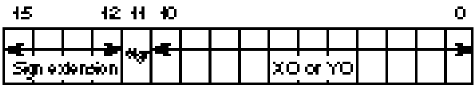


Absolute coordinate
Vertex coordinate YC
Given as signed 12-bit data.
Use sign extension in upper vacant bits.

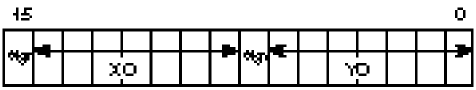


Relative coordinates
Vertex coordinates XC, YC
Given as signed 8-bit data.

LCOFS, RLCOFS



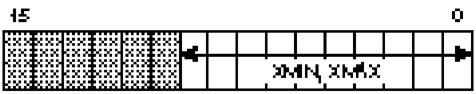
Relative specification
Local offset value XO or YO
Given as signed 12-bit data.
Use sign extension in upper vacant bits.



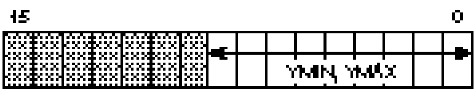
Relative specification
Local offset values XO, YO
Given as signed 8-bit data.

UCLIP, SCLIP

: Fixed at 0



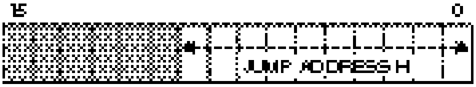
Left and right X coordinates XMIN, XMAX
Given as unsigned 10-bit data.



Upper and lower Y coordinates YMIN, YMAX
Given as unsigned 9-bit data.

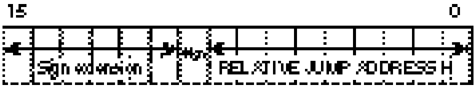
JUMP

: Fixed at 0

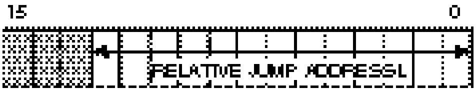


Jump destination upper address
Given as upper 10 bits.

Jump destination lower address
Given as lower 13 bits.
Jump destination address is set as an even byte address.



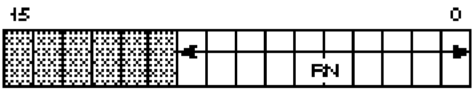
Relative jump destination upper address
Given as upper 10 bits.
Use sign extension in upper vacant bits.



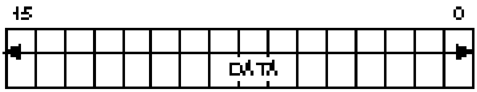
Relative jump destination lower address
Given as lower 13 bits.
Jump destination address is set as an even byte address.

WPR

: Fixed at 0

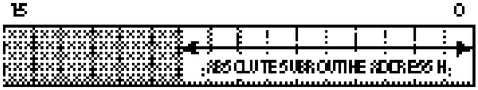


Register number RN
Given as 10-bit data.
Settable registers are limited.

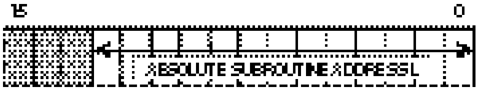


Data
Given as 16-bit data.

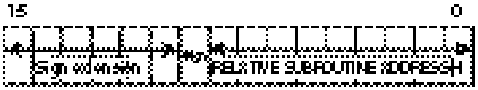
: Fixed at 0



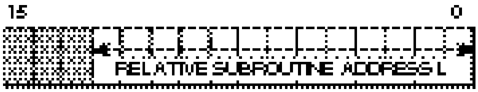
Subroutine upper address
Given as upper 10 bits.



Subroutine lower address
Given as lower 13 bits.
Subroutine destination address is set as an even byte address.



Relative subroutine destination upper address
Given as upper 10 bits.
Use sign extension in upper vacant bits.



Relative subroutine destination lower address
Given as lower 13 bits.
Subroutine destination address is set as an even byte address.

Appendix C Drawing Algorithms

Straight Line Drawing Algorithms: 8-Point Drawing and 4-Point Drawing

Figures C.1 (a) and (b) show examples of straight lines plotted on a bit-mapped display. Circles in the figures represent pixels. Due to the characteristics of a bit-mapped display, a straight line is drawn with the pixels arranged in a path differing slightly from an actual straight line. The same line is drawn in figures C.1 (a) and (b), but the algorithms are different, and so the pixel arrangements are also different. In both figures the line starts at the bottom left of the figure and is drawn dot by dot toward the top right corner. With the method shown in figure C.1 (a), the next dot drawn is to the right, or diagonally to the upper right, of the current dot. With the method shown in figure C.1 (b), on the other hand, the next dot drawn is to the right of, or directly above, the current dot.

For the sake of convenience, the method in figure C.1 (a) is here called 8-point drawing, and that in figure C.1 (b), 4-point drawing.

The difference between 8-point and 4-point drawing is illustrated in figure C.2. With 4-point drawing, the move to draw the next dot can be made in one of only four directions, up, down, left, or right (figure C.2 (b)). With 8-point drawing, moves can also be made in the four diagonal directions (figure C.2 (a)).

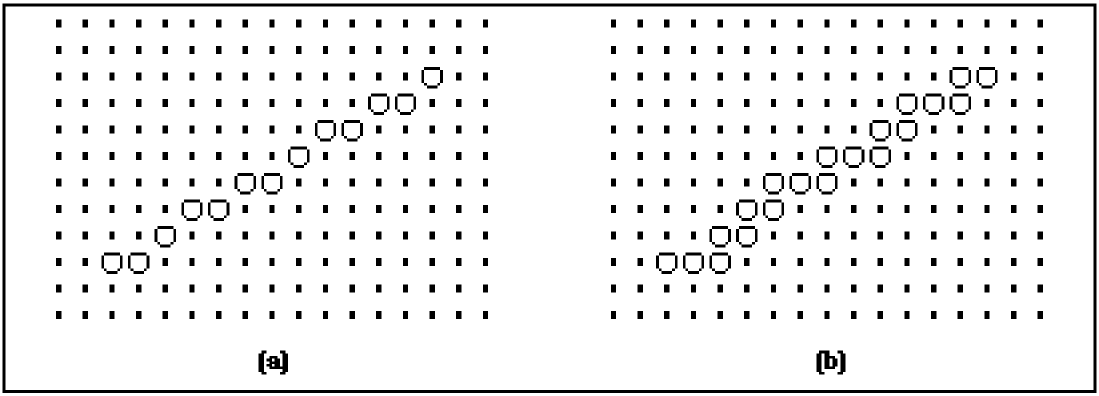


Figure C.1 Two Representations of a Straight Line on a Raster Display

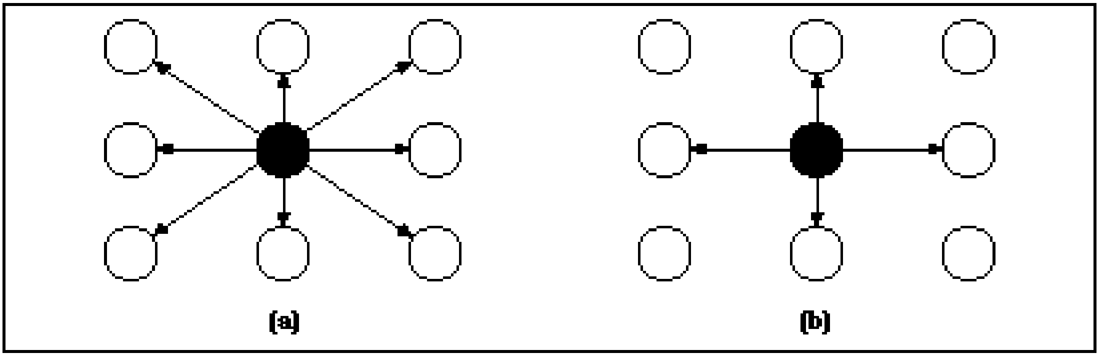


Figure C.2 Comparison of (a) 8-Point Drawing and (b) 4-Point Drawing

Next, 8-point drawing straight line approximation is described, using figure C.3 (a). After pixel A is drawn, either pixel B or pixel C is selected; the basis for selection is proximity to an actual straight line. The same approach is also used in 4-point drawing (figure C.3 (b)).

A comparison between 8-point drawing and 4-point drawing shows that closer approximation to a straight line can be achieved with 8-point drawing. However, the algorithm is correspondingly complex, requiring longer processing time.

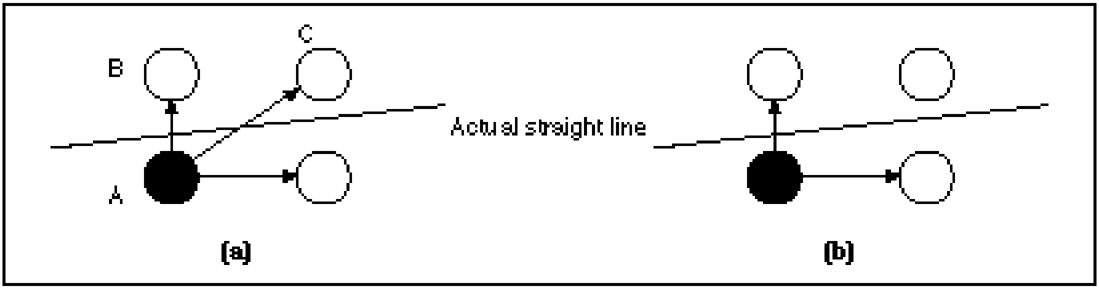
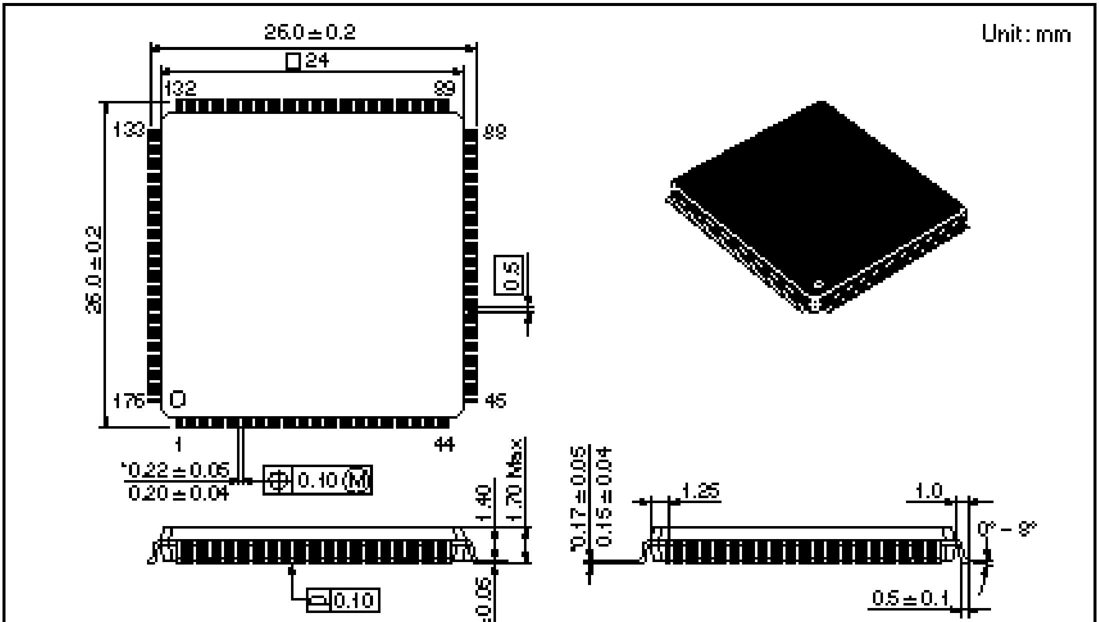


Figure C.3 Drawing Dot Determination Process in (a) 8-Point Drawing and (b) 4-Point Drawing

Readers interested in drawing algorithms can find further information in the sources listed below.

1. Jerry van Aken: “Curve-Drawing Algorithms for Raster Display,” ACM Trams. Graph. Vol. 4, No. 2—(April, 1985), 147–169.
2. J.E.Bresenham: “Algorithm for Computer Control of a Digital Plotter,” IBM Syst. J. Vol. 4, No. 1 (1965), 25–30
3. J.E.Bresenham: “A Liner Algorithm for Incremental Digital Display of Digital Arcs,” Commum. ACM. Vol. 20, No. 2 (February 1977), 100–106
4. P.E.Danielsson “Incremental Curve Generation,” IEEE Trans. Comput. Vol. C-19 (September 1970), 783-793
5. W.J.Jr.Bernard: “An Improved Algorithm for the Generation of Nonparametric Curves,” IEEE Trans. Comput. Vol. C-22, No. 12 (December 1973), 1052–1060
6. Jerry van Aken: “An Efficient Ellipse—Drawing Algorithm,” IEEE Comput. Graph & Appl. Vol. 4, No. 9 (September 1984), 24–35
7. Y.Suenaga: “A High-Speed Algorithm for the Generation of Straight Lines and Circular Arcs,” IEEE Trans. Comput. Vol. C-28, No. 10 (October 1979), 728–736



Hitachi Code	FP-176
JEDEC	—
EIAJ	Conforms
Weight (reference value)	1.9 g

Figure D.1 Package Dimensions (FP-176)

Appendix E Display Operating Clock and Screen Synthesis

The display operating clock (CLK1) and possible FG screen, BG screen, and video screen display synthesis ranges are shown in tables E.1 to E.8.

The following symbols are used in the tables:

O: Display synthesis possible

×: Display synthesis not possible

Table E.1 32-Bit UGM Bus Width, 66 MHz Q2SD Operating Frequency

Display Screen Configuration			Screen Synthesis Possibility			
FG Screen	**BG Screen**	**Video Screen**	**320 × 240 CLK1: 6.5 MHz**	**480 × 240 9.5 MHz**	**640 × 480 25 MHz**	**800 × 480 33 MHz**
8bpp *1	—	—	O	O	O	O
16bpp	—	—	O	O	O	O
8bpp	8bpp	—	O	O	O	O
8bpp	16bpp	—	O	O	× *2	×
16bpp	8bpp	—	O	O	× *2	×
16bpp	16bpp	—	O	O	×	×
8bpp	—	16bpp	O	O	×	×
16bpp	—	16bpp	O	O	×	×
8bpp	8bpp	16bpp	O	O	×	×
8bpp	16bpp	16bpp	O	O	×	×
16bpp	8bpp	16bpp	O	O	×	×
16bpp	16bpp	16bpp	O	O	×	×

Notes: 1. bpp: Bits per pixel
2. O if there is no video input

Table E.2 32-Bit UGM Bus Width, 60 MHz Q2SD Operating Frequency

Display Screen Configuration			Screen Synthesis Possibility			
FG Screen	**BG Screen**	**Video Screen**	**320 × 240 CLK1: 6.5 MHz**	**480 × 240 9.5 MHz**	**640 × 480 25 MHz**	**800 × 480 33 Mhz ***
8bpp	—	—	O	O	O	
16bpp	—	—	O	O	O	
8bpp	8bpp	—	O	O	O	
8bpp	16bpp	—	O	O	×	
16bpp	8bpp	—	O	O	×	
16bpp	16bpp	—	O	O	×	
8bpp	—	16bpp	O	O	×	
16bpp	—	16bpp	O	O	×	
8bpp	8bpp	16bpp	O	O	×	
8bpp	16bpp	16bpp	O	O	×	
16bpp	8bpp	16bpp	O	O	×	
16bpp	16bpp	16bpp	O	×	×	

Note: * Not possible since Q2SD operating frequency > twice dot clock.
However, video input is possible if the Q2SD operating frequency is 64 MHz or higher.

Table E.3 32-Bit UGM Bus Width, 50 MHz Q2SD Operating Frequency

Display Screen Configuration			Screen Synthesis Possibility			
FG Screen	**BG Screen**	**Video Screen**	**320 × 240 CLK1: 6.5 MHz**	**480 × 240 9.5 MHz**	**640 × 480 25 MHz**	**800 × 480 33 MHz ***
8bpp	—	—	O	O	O	
16bpp	—	—	O	O	O	
8bpp	8bpp	—	O	O	×	
8bpp	16bpp	—	O	O	×	
16bpp	8bpp	—	O	O	×	
16bpp	16bpp	—	O	O	×	
8bpp	—	16bpp	O	O	×	
16bpp	—	16bpp	O	O	×	
8bpp	8bpp	16bpp	O	O	×	
8bpp	16bpp	16bpp	O	×	×	
16bpp	8bpp	16bpp	O	×	×	
16bpp	16bpp	16bpp	O	×	×	

Note: * Not possible since Q2SD operating frequency > twice dot clock.
However, video input is possible if the Q2SD operating frequency is 64 MHz or higher.

Table E.4 32-Bit UGM Bus Width, 40 MHz Q2SD Operating Frequency

Display Screen Configuration			Screen Synthesis Possibility			
FG Screen	**BG Screen**	**Video Screen**	**320 × 240 CLK1: 6.5 MHz**	**480 × 240 9.5 MHz**	**640 × 480 25 MHz ***	**800 × 480 33 MHz ***
8bpp	—	—	O	O		
16bpp	—	—	O	O		
8bpp	8bpp	—	O	O		
8bpp	16bpp	—	O	O		
16bpp	8bpp	—	O	O		
16bpp	16bpp	—	O	O		
8bpp	—	16bpp	O	O		
16bpp	—	16bpp	O	O		
8bpp	8bpp	16bpp	O	×		
8bpp	16bpp	16bpp	O	×		
16bpp	8bpp	16bpp	O	×		
16bpp	16bpp	16bpp	×	×		

Note: * Not possible since Q2SD operating frequency > twice dot clock.
However, video input is possible if the Q2SD operating frequency is 64 MHz or higher.

Table E.5 16-Bit UGM Bus Width, 66 MHz Q2SD Operating Frequency

Display Screen Configuration			Screen Synthesis Possibility			
FG Screen	**BG Screen**	**Video Screen**	**320 × 240 CLK1: 6.5 MHz**	**480 × 240 9.5 MHz**	**640 × 480 25 MHz**	**800 × 480 33 MHz**
8bpp	—	—	O	O	O	O
16bpp	—	—	O	O	O	×
8bpp	8bpp	—	O	O	O	×
8bpp	16bpp	—	O	O	×	×
16bpp	8bpp	—	O	O	×	×
16bpp	16bpp	—	O	O	×	×

Table E.6 16-Bit UGM Bus Width, 60 MHz Q2SD Operating Frequency

Display Screen Configuration			Screen Synthesis Possibility			
FG Screen	BG Screen	Video Screen	320 × 240 CLK1: 6.5 MHz	480 × 240 9.5 MHz	640 × 480 25 MHz	800 × 480 33 MHz *
8bpp	—	—	O	O	O	
16bpp	—	—	O	O	×	
8bpp	8bpp	—	O	O	×	
8bpp	16bpp	—	O	O	×	
16bpp	8bpp	—	O	O	×	
16bpp	16bpp	—	O	O	×	

Note: * Not possible since Q2SD operating frequency > twice dot clock.

Table E.7 16-Bit UGM Bus Width, 50 MHz Q2SD Operating Frequency

Display Screen Configuration			Screen Synthesis Possibility			
FG Screen	BG Screen	Video Screen	320 × 240 CLK1: 6.5 MHz	480 × 240 9.5 MHz	640 × 480 25 MHz	800 × 480 33 MHz
8bpp	—	—	O	O	O	
16bpp	—	—	O	O	×	
8bpp	8bpp	—	O	O	×	
8bpp	16bpp	—	O	O	×	
16bpp	8bpp	—	O	O	×	
16bpp	16bpp	—	O	O	×	

Table E.8 16-Bit UGM Bus Width, 40 MHz Q2SD Operating Frequency

Display Screen Configuration			Screen Synthesis Possibility			
FG Screen	BG Screen	Video Screen	320 × 240 CLK1: 6.5 MHz	480 × 240 9.5 MHz	640 × 480 25 MHz *	800 × 480 33 MHz *
8bpp	—	—	O	O		
16bpp	—	—	O	O		
8bpp	8bpp	—	O	O		
8bpp	16bpp	—	O	O		
16bpp	8bpp	—	O	O		
16bpp	16bpp	—	O	×		

Note: * Not possible since Q2SD operating frequency > twice dot clock.

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