SINO WEALTH

SH7106R/07AR/07BR

3 1/2 Digit A/D Converter

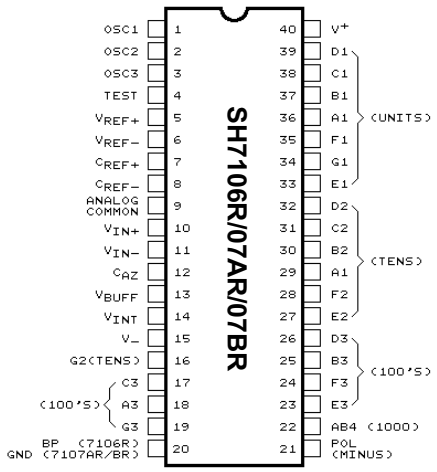
Features

- Guaranteed zero reading with zero input
- True polarity indication for precision null detection
- Low noise
- Convenient 9V battery operation
- Low power operation-10mW
- High Impedance CMOS differential inputs $10^{12}\Omega$
- True differential input and reference
- No additional active components required
- Direct display drive for SH7106R LCD,SH7107AR/BR LED
- Low linearity error: guaranteed less than 1 count
- Internal reference with low temperature drift
- Applications: digital panel meters, digital multimeters, thermometers, capacitance meters, pH meters, photometers, etc.
- 40-pin DIP package

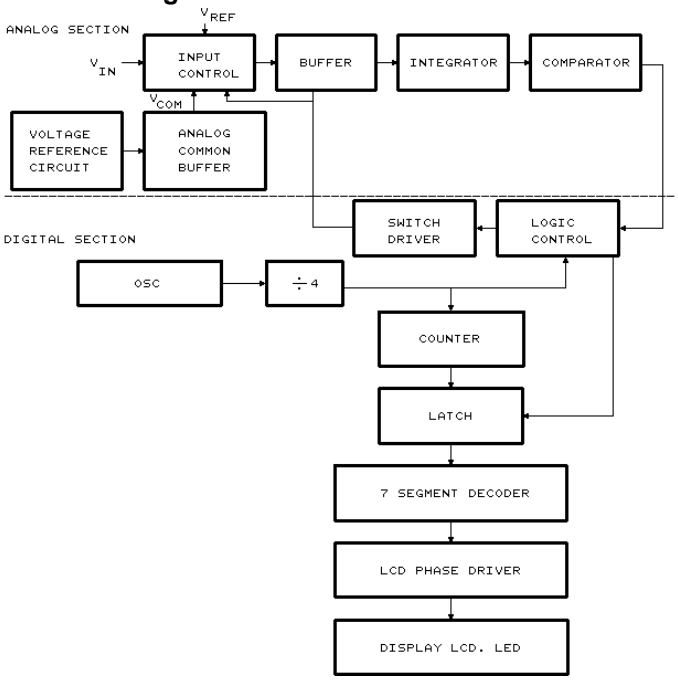
General Description

The SH7106R and SH7107AR/BR are high performance, low power 3 1/2 digit A/D converters. All the necessary active devices are contained in a single CMOS IC, including a seven-segment decoder, display driver, voltage reference, and clock. SH7106R is designed to interface with a liquid crystal display (LCD) and SH7107AR/BR will directly drive an instrument sized light emitting diode (LED) display. The SH7106R and SH7107AR/BR bring together a combination of high accuracy and versatility. High accuracy, like auto-zero to less than 100μV for 2.00V full-scale measurement, or 10μV for 200.0 mV full-scale measurement, input bias current of 10 pA max, and rollover of less than one count. The versatility of true differential input and voltage reference is useful in all systems, such as strain gauges or bridge-type tranducers.

Pin Configuration



Block Diagram



Pin Description

Pin No.	Designation	Description
1	OSC1	Pins 1, 2 & 3 make up the oscillator section. For a 48KHz clock (3 readings per second), connect pin 1 to the junction of a 100KΩ resistor and a 100 pF capacitor. The 100KΩ resistor is tied to pin 2 and the 100pF capacitor is tied to pin 3
2	OSC2	See pin 1
3	OSC3	See pin 1
4	TEST	Lamp test. When pulled high (to V_+), all segments will be turned on and the display should read "-1888". It may also be used as a negative supply for externally generated decimal points
5	V_{REF+}	This analog input is required to generate a full-scale output (1,999 counts). Place 100 mV between pins 5 and 6 for 200.0mV full-scale. Place 1.00 volt between pins 5 and 6 for 2.000 volt full-scale
6	V_{REF-}	See pin 5
7	C_{REF+}	A 0.1μF capacitor is used in most applications. If a large common-mode voltage exists (for example the V_{IN-} pin is not at analog common), and a 200 mV scale is used, a 1.0μF capacitor is recommended which will hold the rollover error to 0.5 count
8	C_{REF-}	See pin 7
9	Analog Common	This pin is primarily used to set the analog common-mode voltage for battery operation or in systems where the input signal is referenced to the power supply
10	V_{IN+}	The analog high input signal is connected to this pin
11	V_{IN-}	The analog low input is connected to this pin
12	C_{AZ}	The size of the auto-zero capacitor influences the system noise. Use a 0.47μF capacitor for 200mV full-scale, and a 0.047μF capacitor for 2.000 volt full-scale
13	V_{BUFF}	Integration resistor connection. Use 47KΩ for a 200mV full-scale range and 470KΩ for 2.000V full-scale range
14	V_{INT}	Integrator output. Connection point for integration capacitor
15	V_-	Negative power supply voltage
16	G2	Activates the G section of the tens display
17	C3	Activates the C section of the hundreds display
18	A3	Activates the A section of the hundreds display

Pin Description (continued)

Pin No.	Designation	Description
19	G3	Activates the G section of the hundreds display
20	BP GND	LCD Backplane drive output (SH7106) Digital Ground (SH7107AR), but keep floating for SH7107BR
21	POL	Activates the negative polarity display
22	AB4	Activates both halves of the 1 in the hundreds display
23	E3	Activates the E section of the hundreds display
24	F3	Activates the F section of the hundreds display
25	B3	Activates the B section of the hundreds display
26	D3	Activates the D section of the hundreds display
27	E2	Activates the E section of the tens display
28	F2	Activates the F section of the tens display
29	A2	Activates the A section of the tens display
30	B2	Activates the B section of the tens display
31	C2	Activates the C section of the tens display
32	D2	Activates the D section of the units display
33	E1	Activates the E section of the units display
34	G1	Activates the G section of the units display
35	F1	Activates the F section of the units display
36	A1	Activates the A section of the units display
37	B1	Activates the B section of the units display
38	C1	Activates the C section of the units display
39	D1	Activates the D section of the units display
40	V_+	Positive supply voltage

Functional Description

An input signal to be measured is applied to the integrating capacitance for a fixed time as determined by a clock counter. The accumulated charge will be proportional to the input signal, for a fixed clock rate and constant current. The resulting integral is returned to zero by integrating a reference signal of polarity opposite that of the input signal. The length of time required for the integrator to return to zero, as measured with the clock counter to display at output, is proportional to the average magnitude of the input signal over the integration period.

a. Analog Section

Figure 1 shows the block diagram of the Analog Section for SH7106R and SH7107AR/BR. Each measurement cycle is divided into three parts. They are: (1) Auto-zero [A-Z] (2) Signal integrated [INT] (3) Deintegrated [DE].

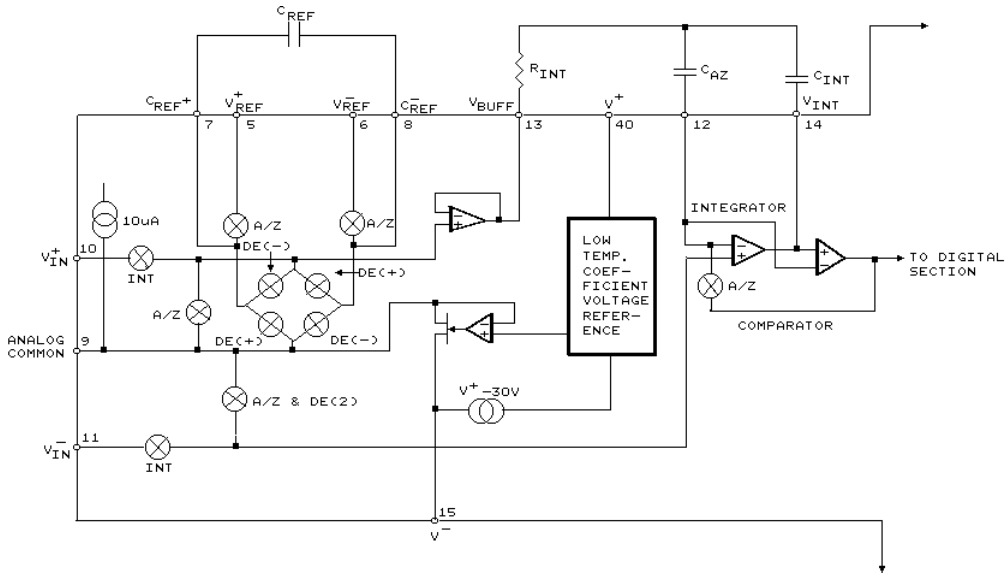


Figure 1. SH7106R/07AR/07BR Analog Section

1. Auto Zero Phase

During Auto-Zero, three steps occur:

(1) Input high and low are disconnected from the PIN and shorted to analog COMMON.
(2) The reference capacitor is charged to the reference voltage.
(3) A feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} which compensates for offset voltages in the buffer amplifier, integrator and comparator.

2. Signal Integrate Phase

During signal integrate, the auto zero loop is opened, the internal short is removed, and the internal inputs high and low are connected to the external pins. The converter then integrates the differential voltage between input high and input low for a fixed time (1000 counts). At the end of this phase, the polarity of the integrated signal is determined.

3. De-Integrate Phase

The final phase is de-integrate, or reference integrate. Input low is internally connected to Analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required to return to zero is proportional to the input signal. Specifically, the digital reading displayed is $1000 \left(\frac{Ain}{Vref} \right)$.

b. Digital Section

Figure 2, Figure 3 and Figure 4 show the digital section for the SH7106R and SH7107AR/BR, respectively. In the SH7106R, the internal digital ground is generated from a 6.2 volt Zener diode and a large p-channel follower. This supply is made stiff to absorb the relatively large capacitive current when the back plane (BP) is switched. The BP frequency is the clock frequency divided by 800. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases, negligible DC voltage exists across the segments.

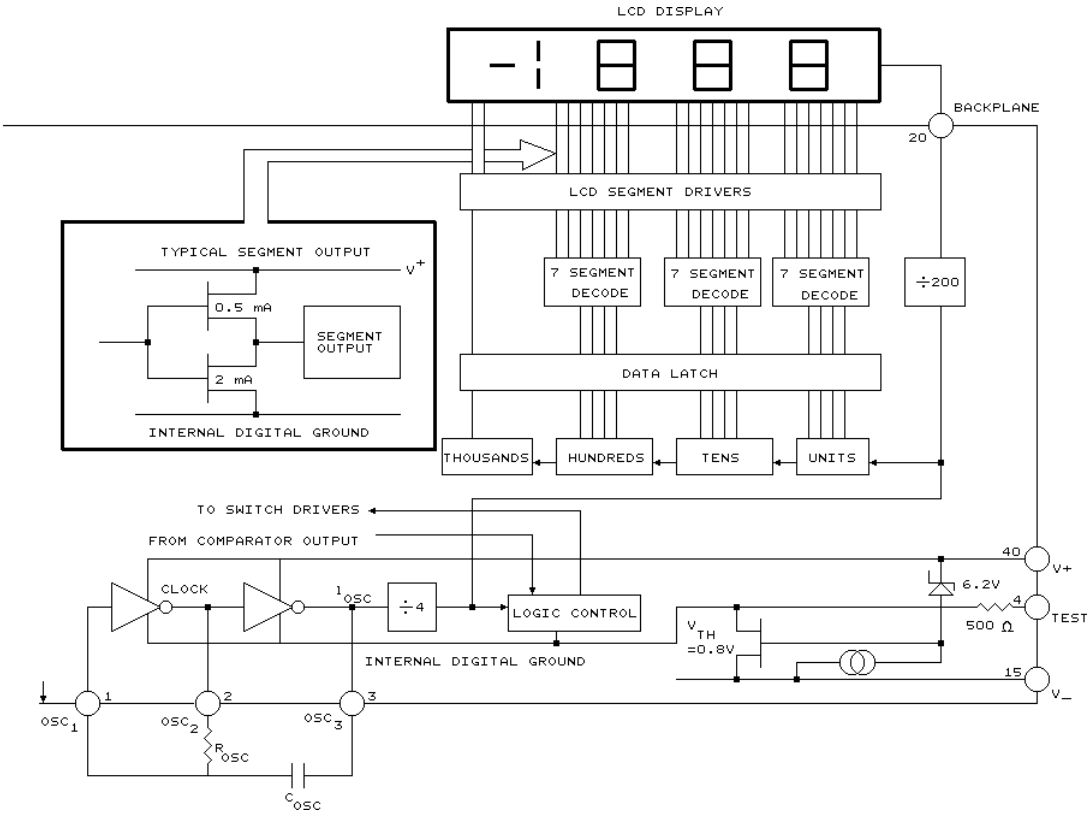


Figure 2. SH7106R Digital Section

Figure 3 is the Digital Section of the SH7107AR. It is identical to Figure 2 except the regulated supply and back plane drive have been eliminated and the segment drive has been increased from 2mA to 8mA. Pin 22 must sink current twice the drive capability.

Figure 4 is the Digital Section of the SH7107BR. It is similar to SH7107AR except SH7107BR provides an internal digital ground (same as SH7106R), hence the user does not need to provide an external digital ground for SH7107BR and keep pin 20 floating. It is suggested that user place a 120Ω resistor between V_+ and common anode LED to limit the current into SH7107BR, gaining better performance as well as saving energy.

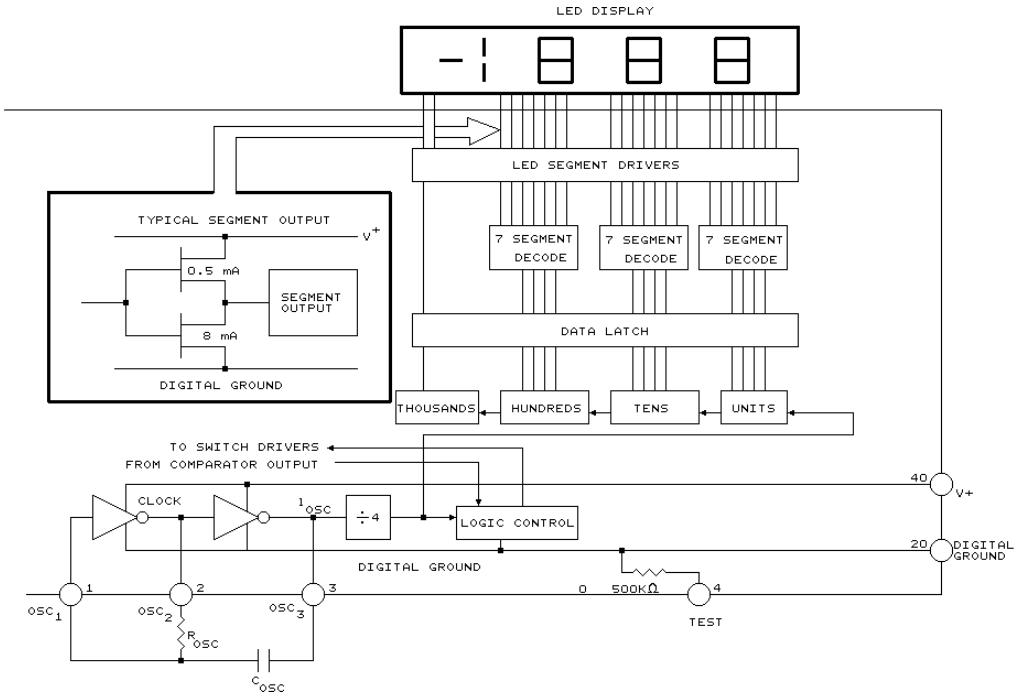


Figure 3. SH7107AR Digital Section

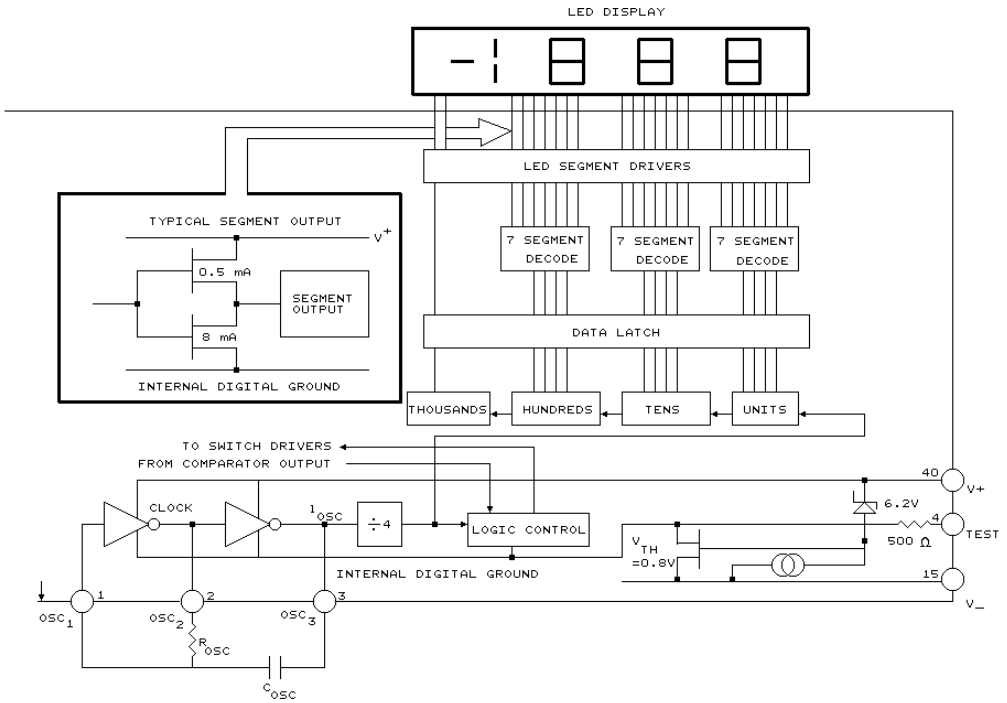
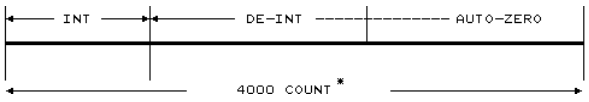


Figure 4. SH7107BR Digital Section

System Timing

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phase. These are: signal integrate (1000 counts), reference de-integrate (0 to 2000 counts) and auto-zero (1000 to 3000 counts). For signals less than full scale, auto-zero gets the unused portion of reference de-integrate. This makes complete measure cycles of 4000 (16000 clock pulses) independent of input voltage.



* Note: Actually, the total measurement cycle is 4001 counts for measured values less than 2000 counts. The measurement cycle becomes 4000 counts for overflow measurement.

Clock Circuit:

SH7106R/07AR/07BR may use the following three clocking methods:
1. An external oscillator connected to pin 1.
2. A crystal between pin 1 and pin 2.
3. An RC oscillator using all three pins (pin 1, 2 & 3).

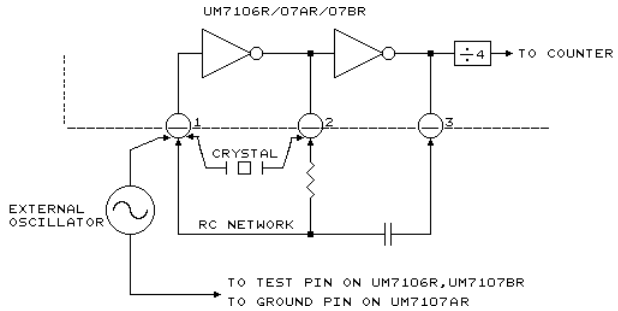


Figure 5. Clock Circuit

To achieve maximum rejection of 50/60Hz pick up, the signal integrate cycle should be a multiple of 50/60Hz. The following table describes the selection of oscillator frequencies for 50 or 60Hz respectively.

	Oscillator Frequencies
50Hz	..40KHz, 50KHz, 66 2/3KHz, 100KHz....
60Hz	..33 1/3KHz, 40KHz, 48KHz, 60KHz, 80KHz, 100KHz.....

Note that 40KHz (2.5 readings/second) will reject both 50 and 60Hz.

Component Value Selection

Integrating Resistor (R_{INT}):

The buffer amplifier and integrator are designed with class A output stages with 100μA of quiescent current each. They can supply 20μA drive current with negligible linearity errors. R_{INT} should be large enough to remain in linear region but small enough to reduce the leakage current on the PC board.
For 200mv full scale, R_{INT} is 47KΩ; 2.000 volt full scale needs a 470KΩ R_{INT}.

Integrating Capacitor (C_{INT}):

C_{INT} should be chosen to give the maximum voltage swing without causing the saturation of integrator output swing. According to the superior temperature coefficient — 20ppm/°C of analog common will be normally used as the differential voltage reference. It is fine for a nominal ±2.000V. full scale integrator output swing. For three readings/second (48KHz clock), a 0.22μF capacitor is suggested.
If a different oscillator frequency is used, C_{INT} must be changed in inverse proportion to maintain the nominal ±2.000V full scale integrator output swing. An additional requirement of C_{INT} is that C_{INT} must have low dielectric absorption to minimize rollover error. Polypropylene capacitors give undetectable errors table at reasonable cost.

Reference Voltage Capacitor (C_{REF}):

The reference voltage used to ramp the integrator output voltage back to zero during the reference integrate cycle is stored on C_{REF}. A 0.1µF capacitor gives good performance when V_{IN-} is tied to analog common. If a large analog common voltage exists (V_{REF-} unequal analog common) and a 200.0mV scale is used, a larger value is required to prevent rollover error. Generally 1.0µF will hold the rollover error to 0.5 count. In this case a mylar type dielectric capacitor is adequate.

Auto-Zero Capacitor (C_{AZ}):

The C_{AZ} value has some influence on system noise. The following combination is recommended:

Application	Adequate C_{AZ}
200.0mV Full Scale	0.47µF
2.000V Full Scale	0.047µF

It is better to use a mylar type capacitor to implement C_{AZ}.

Oscillator Components (R_{OSC}, C_{OSC}):

While using RC oscillator, the R_{OSC} (between pin 1 and pin 2) should be 100KΩ and C_{OSC} is selected from the following equation:

$$F_{OSC} = \frac{0.45}{R_{OSC}.C_{OSC}}$$ (R_{OSC} in MΩ, C_{OSC} in µF)

Reference Voltage Selection

The analog input required to generate full scale output (2000 counts) is $V_{IN} = 2\ V_{REF}$, thus:

Required Full Scale Voltage	V_{REF}
200.0mV	100.0mV
2.000V	1.000V

However, in many applications where an A/D converter is connected to a transducer, there may exist a nonunity scale factor between the input voltage and the digital reading. For instance, a pressure transducer output is 400mV for 2000 lb/in^2, rather than dividing the input voltage by two, the V_{REF} should be set to 200.0mV, then permit the transducer input to be used directly.

The differential voltage reference can also be used to read a digital zero when V_{IN} is not zero. This case is common in temperature measuring instrumentation. A compensating offset voltage can be applied between analog common and V_{IN-} and the transducer output is connected between V_{IN+} and analog common. The circuit is shown in Figure 6.

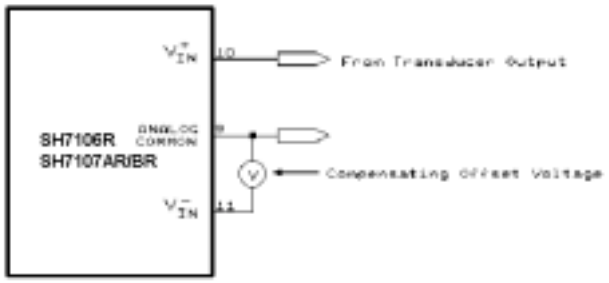


Figure 6. Circuit Used to Read a Digital Zero When V_{IN} is not Zero.

An external reference may be added to improve temperature stability; thus, the SH7106R/07AR/07BR devices with a lower analog common temperature drift may be used. The circuit is shown in Figure 7.

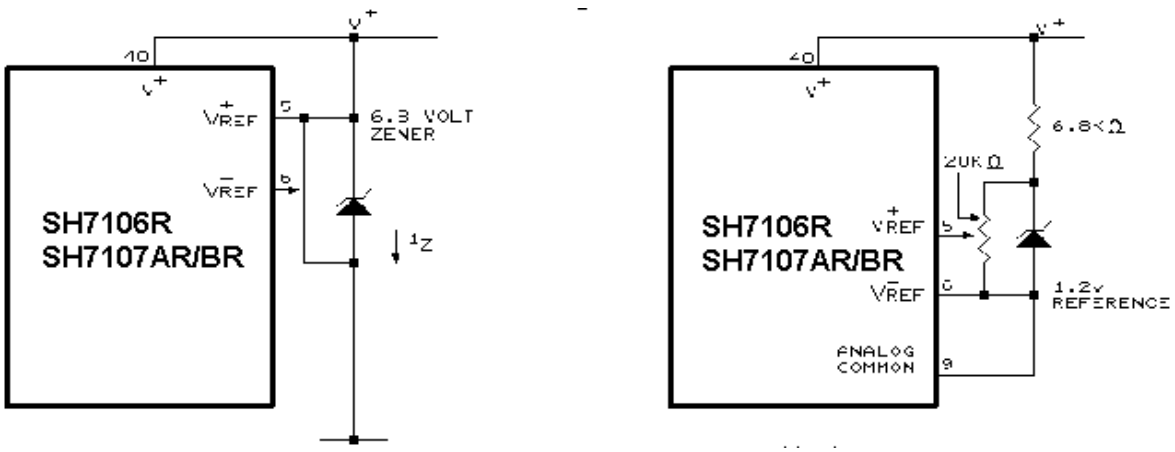


Figure 7. External Reference Voltage Circuits

Absolute Maximum Ratings*

Supply Voltage (V_+ to V_-) 15V
Analog Input Voltage (either input) . . . . . V_+ to V_-
Reference Input Voltage (either input) . . . . . V_+ to V_-
Clock Input . . . . . Test to V_+
Power Dissipation 800mW
Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . -55°C to +150°C
Lead Temperature (Soldering, 60 sec) . . . . . 300°C

***Comments**

Stresses above those shown under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

Unless otherwise noted, specifications apply to SH7106R at Vsupply (V_+ to V_-) = 9.0V, and SH7107AR/BR at Vsupply (V_+ to V_-) = 10.0V

T_A = 25°C, f clock = 48KHz, SH7106R is tested in the CKT of Figure 8, SH7107AR/BR is tested in the CKT of Figure 9.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
-	Zero input Reading	-000.0	±000.0	+000.0	Digital Reading	Vin = 0.0V Full Scale = 200.0mV
-	Ratiometric Reading	999	999/1000	1000	Digital Reading	Vin = Vref Vref = 100.0mV
-	Linearity (Max. Deviation From Best Straight Line Fit)	-1	±0.2	+1	Counts	Full Scale 200.0 mV or 2.000V
V_N	Noise	-	15	-	µV	Vin = 0V Full Scale 200.0mV
I_{LEAK}	Leakage Current Input	-	1	10	pA	Vin = 0V
-	Zero Reading Drift	-	0.2	1	µV/°C	Vin = 0V 0° < T_A < 70°C
-	Scale Factor Temp Coeff	-	1	5	ppm/°C	Vin = 199.0mV 0° < T_A < 70°C

DC Electrical Characteristics (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
$V_{ANA-COM}$	Analog Common Voltage (With respect to Positive Supply)	2.7	3.0	3.3	V	25KΩ Between common and positive supply
-	Temp Coeff of Analog Common	-	20	50	ppm/°C	25KΩ Between vommon and positive supply
I_{DD}	Supply Current (Doesn't include LED and Com. Current)	-	0.8	1.8	mA	Vin = 0
V_{LCDS}	SH7106R Only, Pk-Pk Segment Drive Voltage	4	5	6	V	
V_{LCDS}	SH7106R Only, Pk-Pk Back Plane Drive Voltage	4	5	6	V	
I_{LED}	SH7107AR/BR Only, Segment Sinking Current (Except pin 22)	5	8.0	-	mA	Vsupply = 5.0V Segment Voltage = 3V
I_{LED}	SH7107AR/BR Only, Segment Sinking Current (Pin 22 only)	10	16	-	mA	Vsupply = 5.0V Segment Voltage = 3V
-	Rollover Error	-1	±0.2	+1	Counts	$V_{IN-} = V_{IN+}$ = 200.0mV
-	Common-mode Rejection Ratio	-	50	200	µV/V	Vcm = ±1Vin, Vin = 0V Full-scale = 200.0mV

Application Circuits (for reference only)

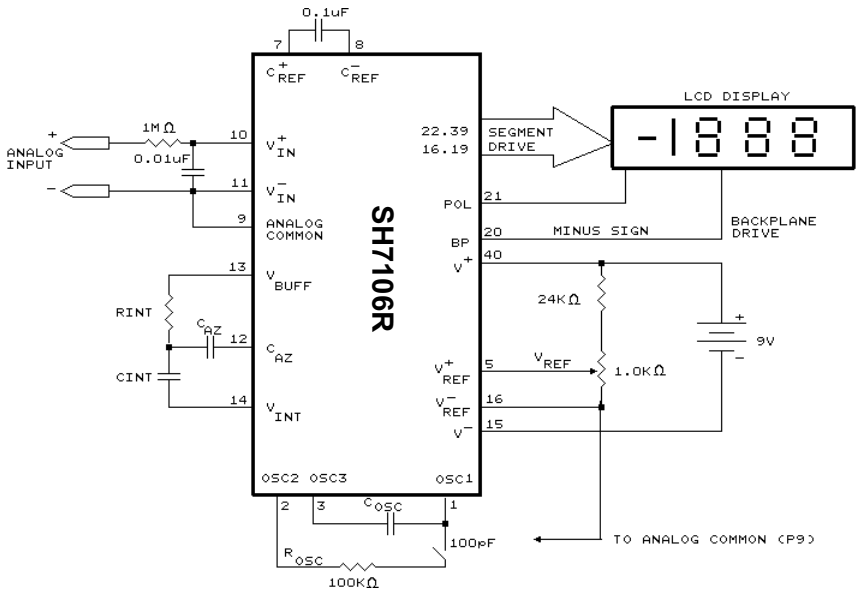


Figure 8

Component Value	Nominal Full-Scale Voltage	
	2.000V	**200.0mV**
C_{AZ}	0.047µF	0.47µF
R_{INT}	470KΩ	47KΩ
C_{INT}	0.22µF	0.22µF
V_{REF}	1.000V	100.0mV

Application Circuits (continued)

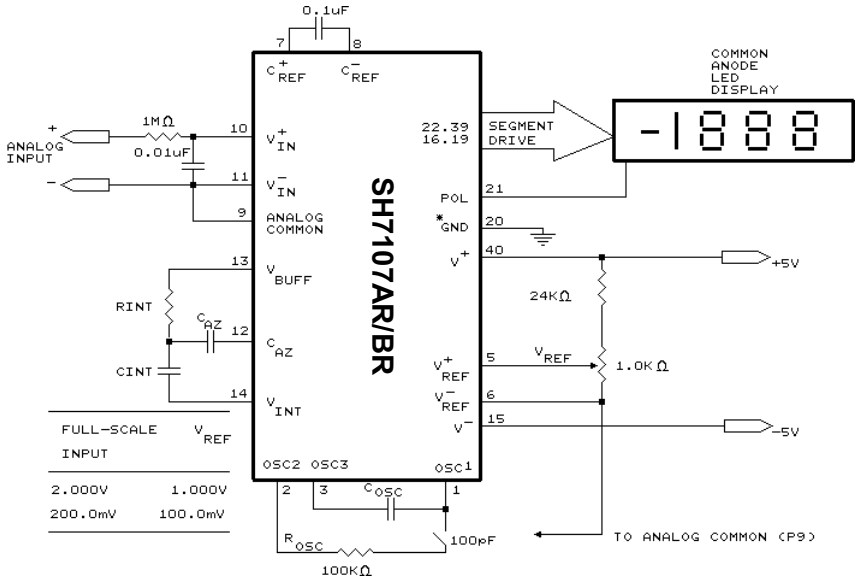


Figure 9

Component Value	Nominal Full-Scale Voltage	
	2.000V	**200.0mV**
C_{AZ}	0.047μF	0.47μF
R_{INT}	470KΩ	47KΩ
C_{INT}	0.22μF	0.22μF
V_{REF}	1.000V	100.0mV

* Note: For SH7107BR, pin 20 must be kept floating. Place a 120Ω resistor between V_+ and common anode LED. The digital ground of SH7107BR is internally generated in order to improve PCB layout.

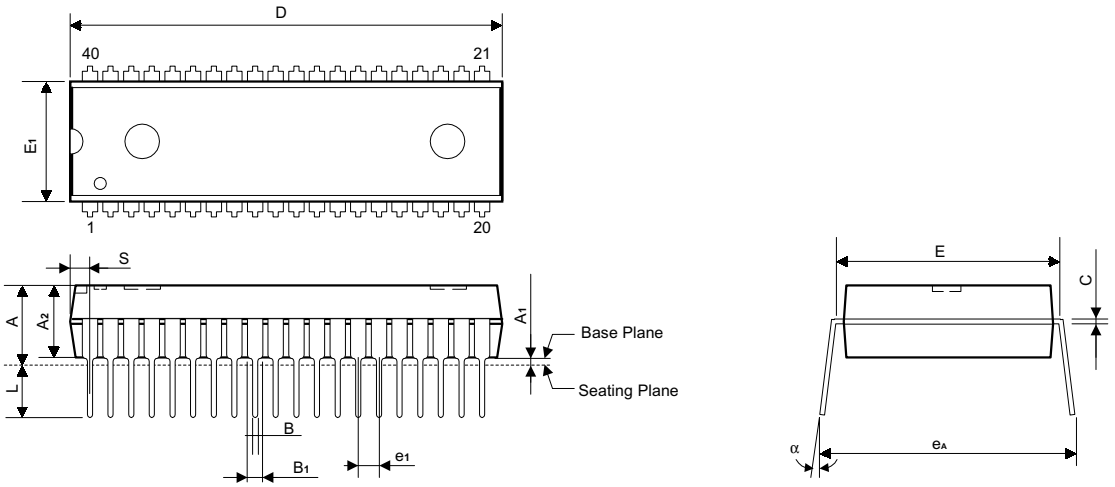
Ordering Information

Part No.	Function	Package
SH7106R	LCD display	40L DIP
SH7107AR/BR	LED display	40L DIP

Package Information

DIP 40L Outline Dimensions

unit: inches/mm



Symbol	Dimensions in inches	Dimensions in mm
A	0.210 Max.	5.33 Max.
A_1	0.010 Min.	0.25 Min.
A_2	0.155±0.010	3.94±0.25
B	0.018 +0.004 -0.002	0.46 +0.10 -0.05
B_1	0.050 +0.004 -0.002	1.27 +0.10 -0.05
C	0.010 +0.004 -0.002	0.25 +0.10 -0.05
D	2.055 Typ. (2.075 Max.)	52.20 Typ. (52.71 Max.)
E	0.600±0.010	15.24±0.25
E_1	0.550 Typ. (0.562 Max.)	13.97 Typ. (14.27 Max.)
e_1	0.100±0.010	2.54±0.25
L	0.130±0.010	3.30±0.25
α	0° ~ 15°	0° ~ 15°
e_A	0.655±0.035	16.64±0.89
S	0.093 Max.	2.36 Max.

Notes:
1. The maximum value of dimension D includes end flash.
2. Dimension E_1 does not include resin fins.
3. Dimension S includes end flash.