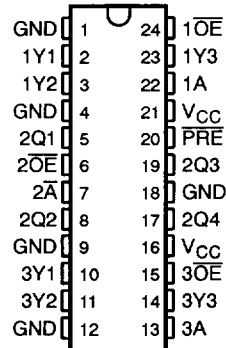


CDC330 CLOCK DRIVER WITH 3-STATE OUTPUTS

SCAS329A – OCTOBER 1993 – REVISED MARCH 1994

- Low Output Skew, Low Pulse Skew for Clock-Distribution and Clock-Generation Applications
- TTL-Compatible Inputs and Outputs
- Two Banks Distribute One Clock Input to Three Same-Frequency Clock Outputs
- One Bank Distributes One Clock Input to Four Half-Frequency Clock Outputs
- Internal Power-Up Circuit
- Distributed V_{CC} and Ground Pins Reduce Switching Noise
- Symmetrical Output Drive ($-32\text{-mA } I_{OH}$, $32\text{-mA } I_{OL}$)
- State-of-the-Art EPIC-IIB™ BICMOS Design Significantly Reduces Power Dissipation
- Packaged in Plastic Small-Outline Package

DW PACKAGE
(TOP VIEW)



description

The CDC330 is a high-performance, low-skew clock driver. It is specifically designed for applications requiring output signals at both the primary clock frequency and one-half the primary clock frequency.

This device contains two banks that fan out one input to three same-frequency outputs and one bank that fans out one input to four half-frequency outputs with minimum skew for clock distribution. Each bank of Y outputs switch in phase and at the same frequency as its clock (A) input. The four Q outputs switch at one-half the frequency of their clock ($2\bar{A}$) input.

When the output-enable ($2\bar{OE}$) input is low and the preset (\bar{PRE}) input is high, the Q outputs toggle on high-to-low transitions of $2\bar{A}$. Taking \bar{PRE} low asynchronously presets the Q outputs to the high level. When a bank's \bar{OE} input is high, the outputs are in the high-impedance state.

The CDC330 is characterized for operation from 0°C to 70°C.

FUNCTION TABLES

INPUTS		OUTPUTS
$n\bar{OE}$	nA	$nY1-nY3$
H	X	Z
L	L	L
L	H	H

$n = 1, 3$

INPUTS			OUTPUTS
$2\bar{OE}$	\bar{PRE}	$2\bar{A}$	$2Q1-2Q3$
H	X	X	Z
L	L	L	H
L	H	↓	Toggle

EPIC-IIB is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



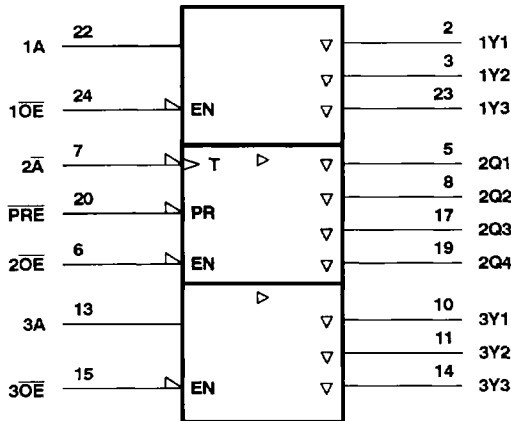
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1994, Texas Instruments Incorporated

CDC330 CLOCK DRIVER WITH 3-STATE OUTPUTS

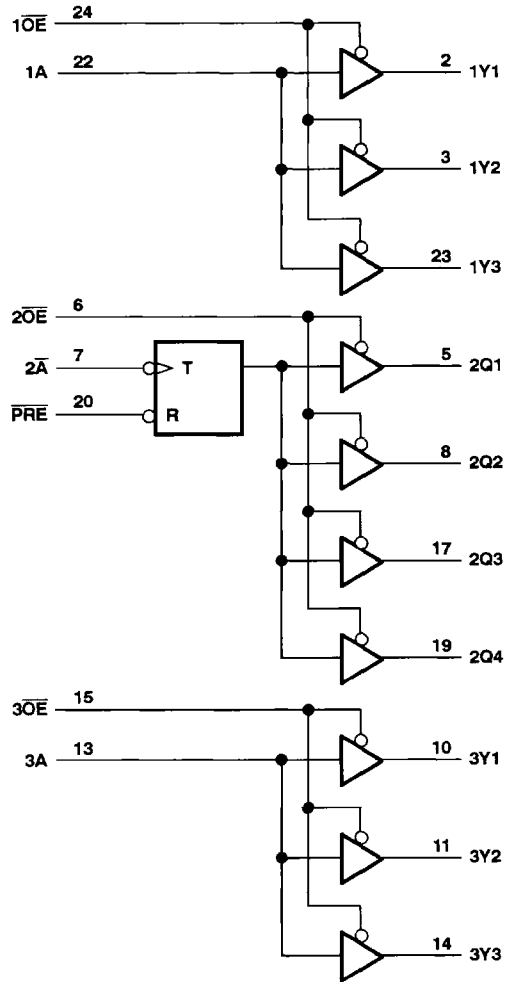
SCAS329A – OCTOBER 1993 – REVISED MARCH 1994

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, V_O	-0.5 V to 5.5 V
Current into any output in the low state, I_O	96 mA
Input clamp current, I_{IK} ($V_I < 0$)	-18 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.



CDC330
CLOCK DRIVER
WITH 3-STATE OUTPUTS

SCAS329A – OCTOBER 1993 – REVISED MARCH 1994

recommended operating conditions (see Note 2)

		MIN	MAX	UNIT
V _{CC}	Supply voltage	4.75	5.25	V
V _{IH}	High-level input voltage	2		V
V _{IL}	Low-level input voltage		0.8	V
V _I	Input voltage	0	V _{CC}	V
I _{OH}	High-level output current		-32	mA
I _{OL}	Low-level output current		32	mA
T _A	Operating free-air temperature	0	70	°C

NOTE 2: Unused pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT	
V _{IK}	V _{CC} = 4.75 V,	I _I = -18 mA			-1.2	V	
V _{OH}	V _{CC} = 4.75 V,	I _{OH} = -32 mA	2			V	
V _{OL}	V _{CC} = 4.75 V,	I _{OL} = 32 mA			0.5	V	
I _{IH}	V _{CC} = 5.25 V,	V _I = 2.7 V			50	μA	
I _{IL}	V _{CC} = 5.25 V,	V _I = 0.5 V			-50	μA	
I _{OZ}	V _{CC} = 5.25 V,	V _O = V _{CC} or GND			±50	μA	
I _O ‡	V _{CC} = 5.25 V,	V _O = 2.5 V	-30		-180	mA	
I _{CC}	V _{CC} = 5.25 V, V _I = V _{CC} or GND	I _O = 0,	Outputs high		11	40	mA
			Outputs low		15	30	
			Outputs disabled		10	30	
C _I	V _I = 2.5 V or 0.5 V				3	pF	
C _O	V _O = 2.5 V or 0.5 V				9	pF	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		MIN	MAX	UNIT
f _{clock}	Clock frequency	1A/3A (duty cycle 40 – 60%)	67	MHz
		2A (duty cycle 40 – 60%)	100	MHz
t _w	Pulse duration	1A/3A low	5.9	ns
		1A/3A high	5.9	
		2A low	2.8	
		2A high	4.5	
		PRE low	3	
t _{su}	Setup time	PRE inactive before 2A↓	2	ns



**CDC330
CLOCK DRIVER
WITH 3-STATE OUTPUTS**

SCAS329A – OCTOBER 1993 – REVISED MARCH 1994

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 3 and Figures 1 and 2)

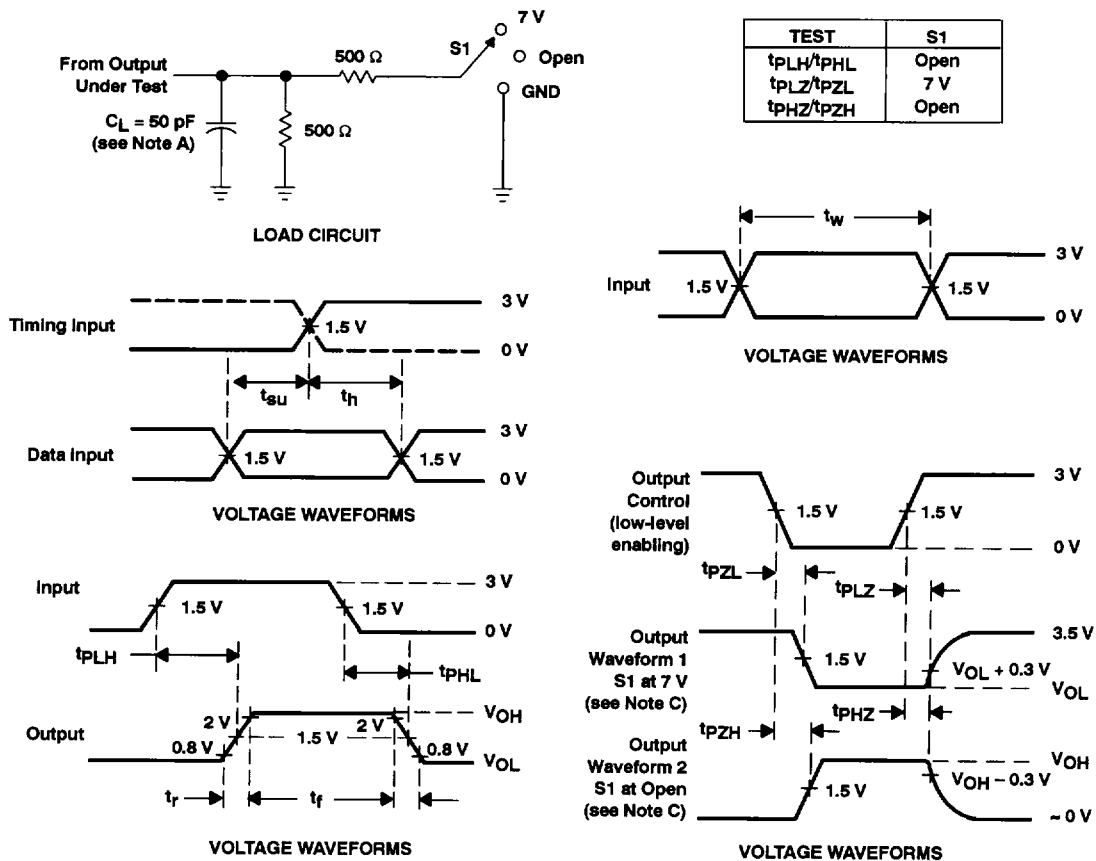
PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f_{max}^{\dagger}	1A or 3A	Any 1Y or 3Y	67		MHz
	$2\bar{A}$	Any Q	100		
t_{PLH}	Any A or \bar{A}	Any Y or Q		11	ns
t_{PHL}			10.5		
t_{PHL}	\overline{PRE}	Any Q		12.5	ns
t_{PZH}	Any \overline{OE}	Any Y or Q		9	ns
t_{PZL}			8.5		
t_{PHZ}	Any \overline{OE}	Any Y or Q		8.5	ns
t_{PLZ}			9		
$t_{sk(o)}$	1A	Any 1Y		0.4	ns
	3A	Any 3Y		0.4	
	1A or 3A	Any 1Y or 3Y		0.5	
	$2\bar{A}$	Any Q		0.4	
$t_{sk(pr)}$	Any A or \bar{A}	Any Y or Q		1	ns

\dagger Duty cycle 40 ~ 60%

NOTE 3: All specifications are valid only for all outputs switching.



PARAMETER MEASUREMENT INFORMATION



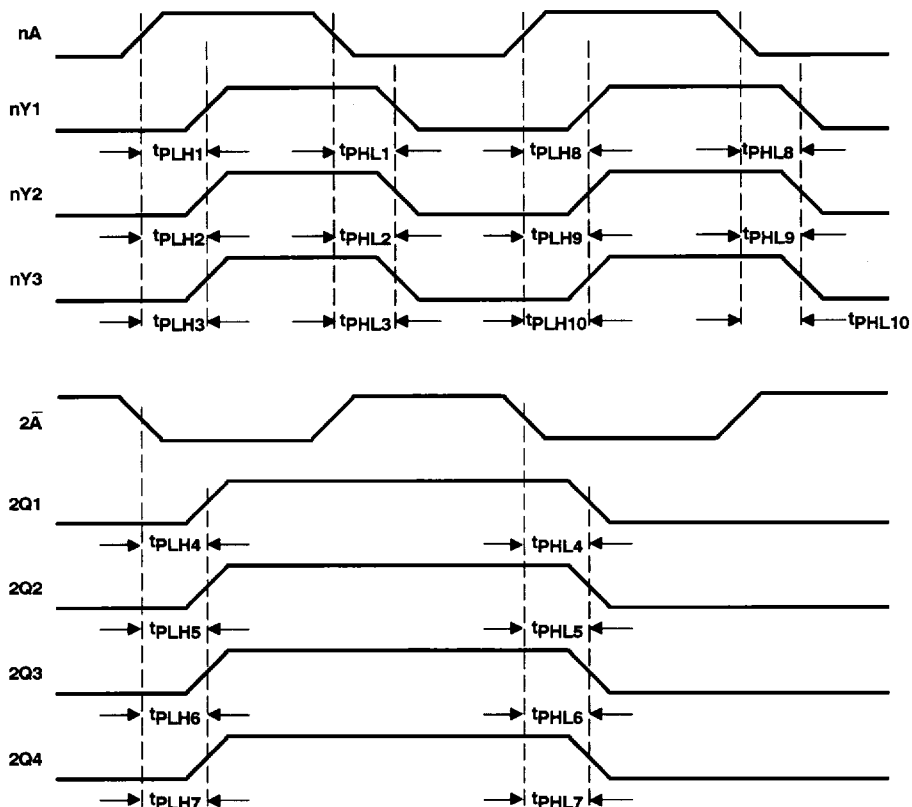
- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

**CDC330
CLOCK DRIVER
WITH 3-STATE OUTPUTS**

SCAS329A – OCTOBER 1993 – REVISED MARCH 1994

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. Output skew, $t_{sk(o)}$, is calculated as the greater of:
- The difference between the fastest and slowest of t_{PLHn} ($n = 1, 2, 3$)
 - The difference between the fastest and slowest of t_{PLHn} ($n = 4, 5, 6, 7$)
 - The difference between the fastest and slowest of t_{PLHn} ($n = 8, 9, 10$)
 - The difference between the fastest and slowest of t_{PHLn} ($n = 1, 2, 3$)
 - The difference between the fastest and slowest of t_{PHLn} ($n = 4, 5, 6, 7$)
 - The difference between the fastest and slowest of t_{PHLn} ($n = 8, 9, 10$)
- B. Process skew, $t_{sk(pr)}$, is calculated the same as output skew, $t_{sk(o)}$, across multiple CDC330 devices under identical operating conditions.

Figure 2. Waveforms for Calculation of $t_{sk(o)}$, $t_{sk(pr)}$



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265