FEATURES

- Low Cost
- Supports Full PCI Bus Bandwidth
- Single-chip PCI bus master/slave interface for add-on products
- Two 32-byte FIFOs (one for each data direction)
- 32-bit (S5932, S5933), 8- or 16-bit (S5930, S5931) add-on data bus width
- Four configurable base address regions (memory space or I/O)
- Data bus size matching and lane steering for 8 and 16-bit add-on data buses (master and slave)
- Supports PCI Burst transfers
- Dual address counters (one for writes, one for reads) for PCI port
- Throttle control on PCI port
- Two sets of mailbox registers with empty/full status and interrupts (16 bytes/set)
- Interrupt on PCI transfer complete and/or mailbox status
- Synchronous or asynchronous add-on interface
- Supports external byte-wide nvRAM (S5931, S5933) or serial nvRAM (S5930, S5931, S5932, S5933)
- Allows expansion BIOS ROM implementation within nvRAM
- Pass-thru interface permits PCI Bus access to add-on resources
- FIFO interface allows PCI bus mastering
- 120, 144 and 160 PQFP package

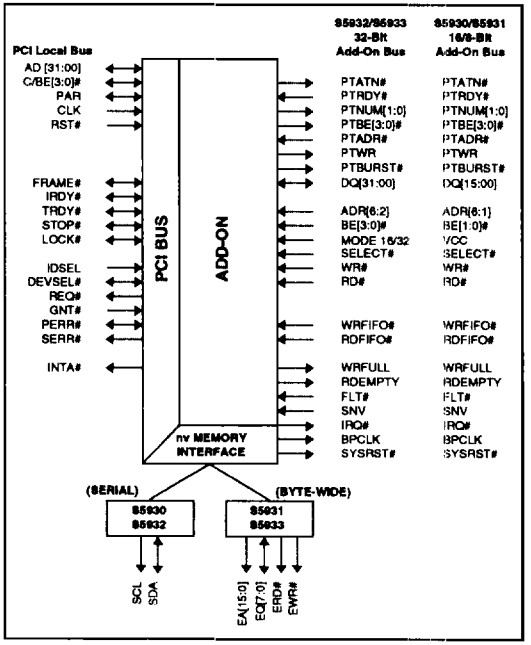
APPLICATIONS

- RAID Systems—File Servers/Work Stations
- Communication Boards—File Servers/Work Stations
- Image Processing—Video Conferencing, Editing, Multimedia, Games, Image Recognition
- Instrumentation, Custom Applications
- Data Acquisition Systems

GENERAL DESCRIPTION

AMCC's PCI Local Bus Master/Slave Controller provides a high performance single-chip interface between the PCI bus and custom add-on boards. Address decoding, bus mastering, burst transfer support, and all elements necessary to perform efficient and timely data transfers are provided within the device. A bidirectional, 32-bit wide FIFO is integrated which facilitates the system-to-system synchronization and data transfers between the local bus and the add-on application. A custom expansion BIOS can be implemented to perform any pre-boot initialization required for the add-on application. The external ROM/EPROM/nvRAM can be either in x8 or serial form and provides a convenient method to configure the S593X for a specific add-on application.

Figure 1. PCI Interface Controller Signal Groups



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The S593X is designed to permit direct connection between the PCI local bus and a variety of general purpose microprocessor-style buses. Bus master transfers can be performed on the PCI bus while device accesses occur on the add-on interface. PCI transfer addresses, transfer counts, mailbox registers, and control/status information are provided on the PCI interface as I/O or memory mapped locations on the PCI bus.

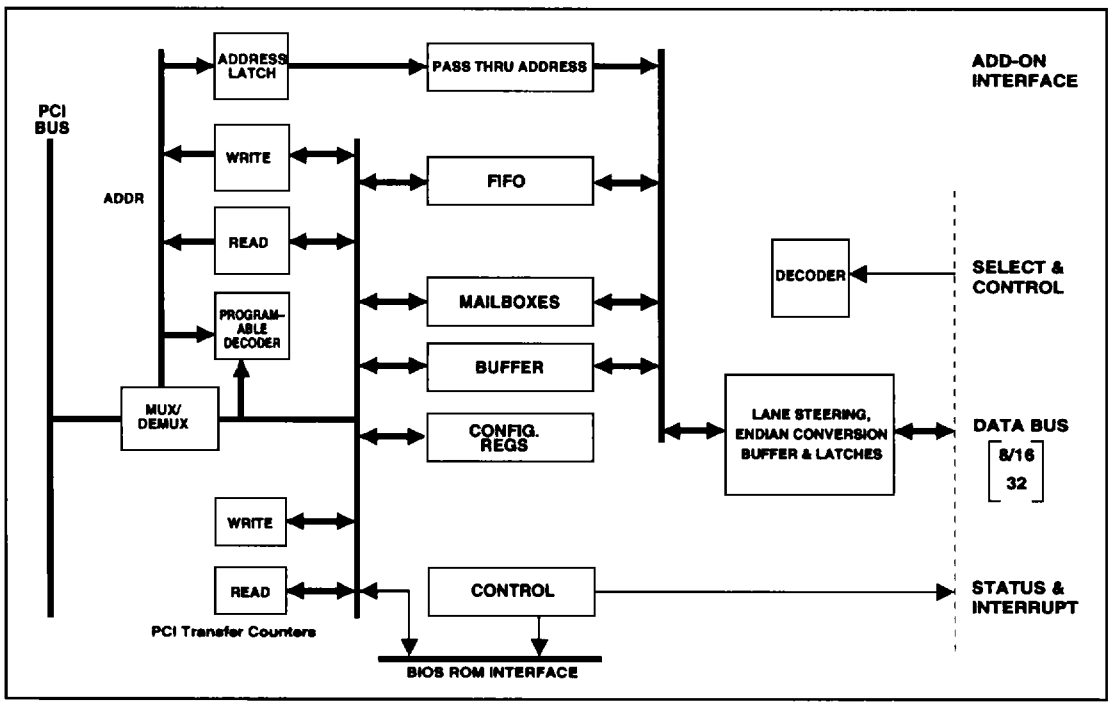
The S593X contains three signal groupings: the PCI bus interface, the EPROM interface, and the add-on general purpose bus interface signals.

APPLICATIONS

Many of the high-performance, complex peripheral functions in today's PCs require a dedicated, embedded microprocessor. Often, the functions desired and the local memory requirements necessary for these add-on products prohibit integration into a single device. The benefits from the embedded microprocessor approach come from the flexibility, time to market, and function complexity which only software techniques can achieve.

AMCC's PCI controllers provide a high performance, highly integrated, easy-to-use method to interface an embedded microprocessor subsystem to the PCI bus.

Figure 2. S5930–S5933 Block Diagram



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