

SN65512B, SN75512B VACUUM FLUORESCENT DISPLAY DRIVERS

SLDS016A – DECEMBER 1985 – REVISED OCTOBER 1989

- Each Device Drives 12 Lines
- 60-V Output Voltage Swing Capability
- 25-mA Output Source Current Capability
- High-Speed Serially-Shifted Data Input
- TTL-Compatible Inputs
- Latches on All Driver Outputs

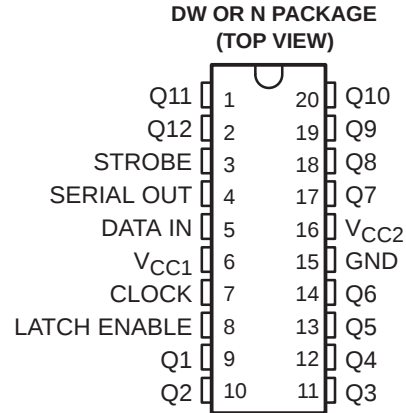
description

The SN65512B and SN75512B are monolithic BIDFET[†] integrated circuits designed to drive a dot matrix or segmented vacuum fluorescent display.

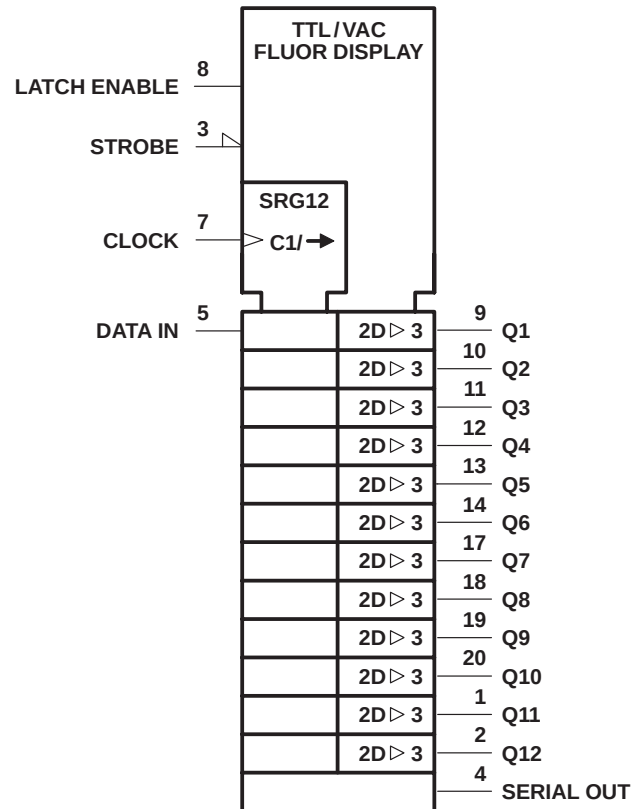
All device inputs are diode-clamped pnp inputs and assume a high logic level when open circuited. The nominal input threshold voltage is 1.5 V. Outputs are totem-pole structures formed by an npn emitter-follower and double-diffused MOS (DMOS) transistors.

The device consists of a 12-bit shift register, 12 latches, and 12 output AND gates. Serial data is entered into the shift register on the low-to-high transition of CLOCK. When high, LATCH ENABLE transfers the shift register contents to the outputs of the 12 latches. The active-low STROBE input enables all Q outputs. Serial data output from the shift register can be used to cascade shift registers. This output is not affected by LATCH ENABLE or STROBE.

The SN65512B is characterized for operation from -40°C to 85°C. The SN75512B is characterized for operation from 0°C to 70°C.



logic symbol[‡]



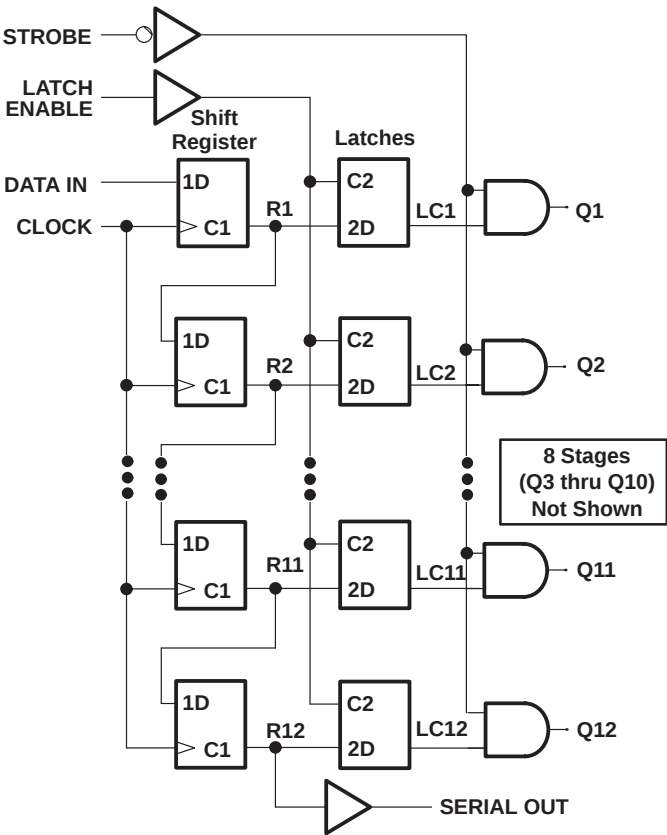
[‡] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

[†] BIDFET – Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip. This is a patented process.

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logic diagram (positive logic)



FUNCTION TABLE

FUNCTION	CONTROL INPUTS			SHIFT REGISTER R1 THRU R12	LATCHES LC1 THRU LC12	OUTPUTS	
	CLOCK	LATCH ENABLE	STROBE			SERIAL	Q1 THRU Q12
Load	↑ No ↑	X	X	Load and shift† No change	Determined by LATCH ENABLE‡	R12	Determined by STROBE
Latch	X	L H	X	As determined above	Stored data New data	R12	Determined by STROBE
Strobe	X	X	H L	As determined above	Determined by LATCH ENABLE‡	R12	All LC LC1 thru LC12, respectively

H = high level, L = low level, X = irrelevant, ↑ = low-to-high-level transition
† R12 takes on the state of R11, R11 takes on the state of R10, . . . R2 takes on the state of R1, and R1 takes on the state of the data input.
‡ New data enter the latches while LATCH ENABLE is high. These data are stored while LATCH ENABLE is low.

CLOCK

DATA IN

SR Contents

LATCH ENABLE

Latch Contents

STROBE

Q Outputs

Valid

Invalid

Valid

Previously Stored Data

New Data

Valid

The diagram is divided into two sections by a vertical line.

Left Section: EQUIVALENT OF EACH INPUT

This section shows the internal circuit of an input. It features a PNP transistor with its emitter connected to V_{CC1} and its base connected to the "Input" terminal. The base is also connected to a diode that points towards the input. The collector of the transistor is connected to a series of other transistors, which are represented by dashed lines, indicating a multi-stage internal structure.

Right Section: TYPICAL OF ALL OUTPUTS

This section shows the internal circuit of an output. It features an NPN transistor with its emitter connected to "GND". The collector is connected to the "Output" terminal. The base of the transistor is connected to a series of other transistors, which are represented by dashed lines, indicating a multi-stage internal structure. The output is also connected to V_{CC2} for Q Outputs and V_{CC1} for SERIAL OUT.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC1} (see Note 1)	15 V
Supply voltage, V_{CC2}	70 V
Input voltage, V_I	V_{CC1}
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A : SN65512B	–40°C to 85°C
SN75512B	0°C to 70°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTES: 1. Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW	585 mW
N	1150 mW	9.2 mW/°C	736 mW	589 mW

recommended operating conditions

		SN65512B		SN75512B		UNIT
		MIN	MAX	MIN	MAX	
Supply voltage, V_{CC1}		5	15	5	15	V
Supply voltage, V_{CC2}		0	60	0	60	V
High-level input voltage, V_{IH}		2		2		V
Low-level input voltage, V_{IL}			0.8		0.8	V
High-level output current, I_{OH}			–25		–25	mA
Low-level output current, I_{OL}	$V_{CC1} = 10\text{ V}$		5		5	mA
Clock frequency, f_{clock}	$V_{CC1} = 15\text{ V}, T_A = 25^\circ\text{C}$	0	4	0	4	MHz
	$V_{CC1} = 5\text{ V}, T_A = 25^\circ\text{C}$	0	1	0	1	
Pulse duration, CLOCK high or low, t_w	$V_{CC1} = 15\text{ V}, T_A = 25^\circ\text{C}$	100		100		ns
	$V_{CC1} = 5\text{ V}, T_A = 25^\circ\text{C}$	500		500		
Setup time, DATA IN valid before CLOCK $\uparrow$, t_{su} (see Figure 1)	$V_{CC1} = 15\text{ V}, T_A = 25^\circ\text{C}$	100		100		ns
	$V_{CC1} = 5\text{ V}, T_A = 25^\circ\text{C}$	250		250		
Hold time, DATA IN valid after CLOCK $\uparrow$, t_h (see Figure 1)	$V_{CC1} = 15\text{ V}, T_A = 25^\circ\text{C}$	50		50		ns
	$V_{CC1} = 5\text{ V}, T_A = 25^\circ\text{C}$	250		250		
Operating free-air temperature, T_A		–40	85	0	70	°C



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electrical characteristics over recommended operating free-air temperature range, $V_{CC2} = 60\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -12\text{ mA}$			-1.5	V
V_{OH}	High-level output voltage	Q outputs $I_{OH} = -25\text{ mA}$, $V_{CC1} = 10\text{ V}$	57.5	58		V
		SERIAL OUT $I_{OH} = -200\text{ }\mu\text{A}$, $V_{CC1} = 10\text{ V}$	9	9.5		
V_{OL}	Low-level output voltage	Q outputs $I_{OL} = 5\text{ mA}$, $V_{CC1} = 10\text{ V}$		2.6	5	V
		SERIAL OUT $I_{OL} = 200\text{ }\mu\text{A}$, $V_{CC1} = 10\text{ V}$		0.05	0.2	
I_{IH}	High-level input current	$V_{CC1} = 15\text{ V}$, $V_I = 5\text{ V}$		0.01	1	μA
I_{IL}	Low-level input current	$V_{CC1} = 15\text{ V}$, $V_I = 0.8\text{ V}$	-25	-150		μA
I_{CC1}	Supply current from V_{CC1}	$V_{CC1} = 15\text{ V}$ $V_I = 5\text{ V}$		80	500	μA
				2	6	mA
I_{CC2}	Supply current from V_{CC2}	$V_{CC1} = 15\text{ V}$ All outputs high		10	100	μA
				0.8	3	mA

[†] All typical values are at $V_{CC1} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

switching characteristics, $V_{CC1} = 10\text{ V}$, $V_{CC2} = 60\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low level output	$C_L = 30\text{ pF}$, See Figure 2		300	ns
t_{PLH}	Propagation delay time, low-to-high level output			300	ns
t_{THL}	Transition time, high-to-low level output			500	ns
t_{TLH}	Transition time, low-to-high level output			500	ns

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PARAMETER MEASUREMENT INFORMATION

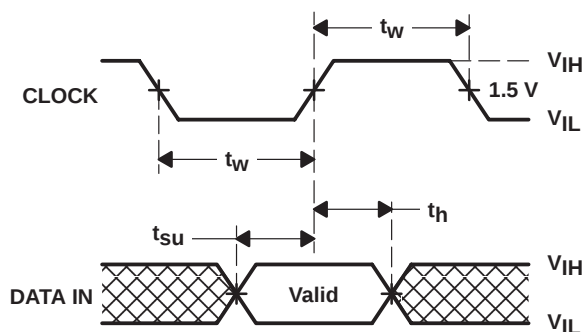


Figure 1. Input Timing Voltage Waveforms

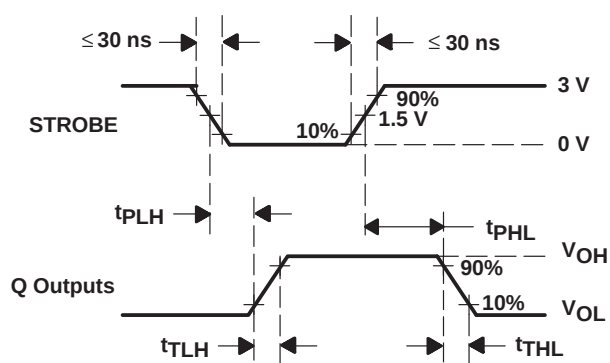


Figure 2. Switching Time Voltage Waveforms

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