ISL70444SEH, ISL73444SEH

19MHz Radiation Hardened 40V Quad Rail-to-Rail Input - Output, Low-Power Operational Amplifiers

FN8411
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The ISL70444SEH and ISL73444SEH (ISL7x444SEH) feature four low-power amplifiers optimized to provide maximum dynamic range. These operational amplifiers (op amps) feature a unique combination of rail-to-rail operation on the input and output as well as a slew enhanced front-end that provides ultra fast slew rates positively proportional to a given step size, thereby increasing accuracy under transient conditions, whether it's periodic or momentary. The ISL7x444SEH also offer low power, low offset voltage, and low temperature drift, making them ideal for applications requiring both high DC accuracy and AC performance. With <5µs recovery for Single Event Transients (SET) (LET_{TH} = 86.4MeV•cm^2/mg), the number of filtering components needed is drastically reduced. The ISL7x444SEH are also immune to single event latch-up because they are fabricated using the Renesas proprietary PR40 Silicon On Insulator (SOI) process.

The amplifiers are designed to operate over a single supply range of 2.7V to 40V or a split supply voltage range of ±1.35V to ±20V. Applications for these amplifiers include precision instrumentation, data acquisition, precision power supply controls, and process controls.

The ISL7x444SEH are available in a 14 Ld hermetic ceramic flatpack and die forms that operate across the temperature range of -55°C to +125°C.

Applications

- Precision instruments
- Active filter blocks
- Data acquisition
- Power supply control
- Process control

Features

- **Electrically screened to DLA SMD# 5962-13214**
- **Acceptance tested to 50krad(Si) (LDR) wafer-by-wafer**
- **<5µs recovery from SEE (LET_{TH} = 86.4MeV•cm^2/mg)**
- **Unity gain stable**
- **Rail-to-rail input and output**
- **Wide gain-bandwidth product 19MHz**
- **Wide single and dual supply range. . . . . 2.7V to 40V max**
- Low input offset voltage 400µV
- Low current consumption (per amplifier) . . . . . 1.1mA, typ
- No phase reversal with input overdrive
- Slew rate
  - Large signal 60V/µs
- Operating temperature range. . . . . -55°C to +125°C
- ISL70444SEH radiation acceptance (see TID report)
  - High dose rate (50-300rad(Si)/s). . . . . 300krad(Si) (ISL70444SEH only)
  - Low dose rate (0.01rad(Si)/s) . . . . . .50krad(Si)
- ISL73444SEH radiation acceptance (see TID report)
  - Low dose rate (0.01rad(Si)/s) . . . . . .50krad(Si)
- SEE hardness (see SEE report for details)
  - SEB LET_{TH} (V_S = ±21V). . . . . 86.4MeV•cm^2/mg
  - SEL immune (SOI Process)

Related Literature

- For a full list of related documents, visit our website:
  - ISL70444SEH, ISL73444SEH device pages

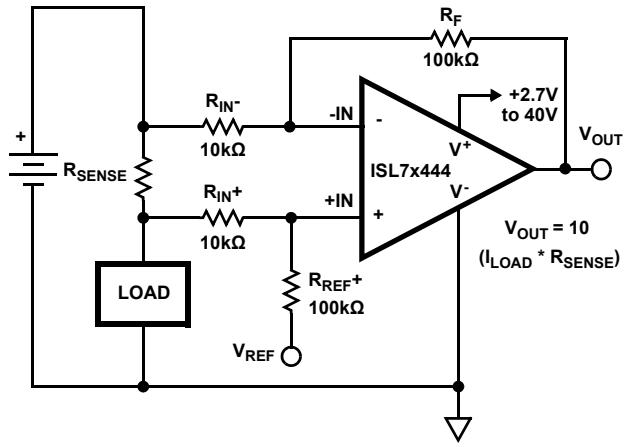

FIGURE 1. TYPICAL APPLICATION: SINGLE-SUPPLY, HIGH-SIDE CURRENT SENSE AMPLIFIER

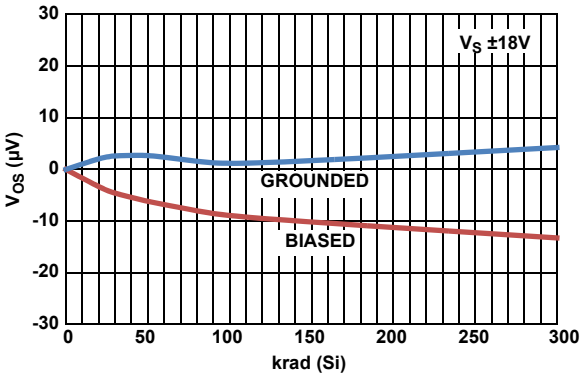

FIGURE 2. V_{OS} SHIFT vs HIGH DOSE RATE RADIATION

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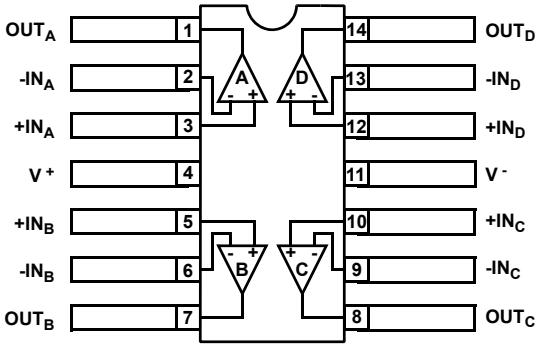
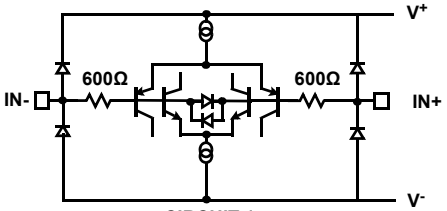
Pin Configuration

14 LD FLATPACK
TOP VIEW

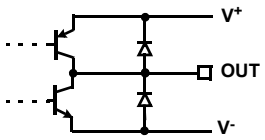


Pin Descriptions

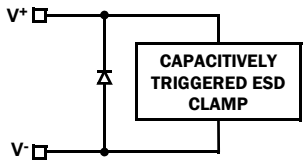
PIN NUMBER	PIN NAME	EQUIVALENT ESD CIRCUIT	DESCRIPTION
1	OUT_A	Circuit 2	Amplifier A output
2	$-IN_A$	Circuit 1	Amplifier A inverting input
3	$+IN_A$	Circuit 1	Amplifier A non-inverting input
4	V^+	Circuit 3	Positive power supply
5	$+IN_B$	Circuit 1	Amplifier B non-inverting input
6	$-IN_B$	Circuit 1	Amplifier B inverting input
7	OUT_B	Circuit 2	Amplifier B output
8	OUT_C	Circuit 2	Amplifier C output
9	$-IN_C$	Circuit 1	Amplifier C inverting input
10	$+IN_C$	Circuit 1	Amplifier C non-inverting input
11	V^-	Circuit 3	Negative power supply
12	$+IN_D$	Circuit 1	Amplifier D non-inverting input
13	$-IN_D$	Circuit 1	Amplifier D inverting input
14	OUT_D	Circuit 2	Amplifier D output
-	E-Pad	None	E-Pad under package (Unbiased, tied to package lid)



CIRCUIT 1



CIRCUIT 2



CIRCUIT 3

Ordering Information

ORDERING/SMD NUMBER (Note 2)	PART NUMBER (Note 1)	RADIATION HARDNESS (Total Ionizing Dose)	TEMP RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
5962F1321401VXC	ISL70444SEHVF	HDR to 300krad(Si), LDR to 50krad(Si)	-55 to +125	14 Ld Flatpack	K14.C
N/A	ISL70444SEHF/PROTO (Note 3)	N/A	-55 to +125	14 Ld Flatpack	K14.C
5962F1321401V9A	ISL70444SEHVX (Note 4)	HDR to 300krad(Si), LDR to 50krad(Si)	-55 to +125	Die	
N/A	ISL70444SEHX/SAMPLE (Notes 3, 4)	N/A	-55 to +125	Die	
N/A	ISL73444SEHF/PROTO (Note 3)	N/A	-55 to +125	14 Ld Flatpack	K14.C
5962L1321403VXC	ISL73444SEHVF	LDR to 50krad(Si)	-55 to +125	14 Ld Flatpack	K14.C
5962F1321403V9A	ISL73444SEHVX (Note 4)	LDR to 50krad(Si)	-55 to +125	Die	
N/A	ISL73444SEHX/SAMPLE (Notes 3, 4)	N/A	-55 to +125	Die	
N/A	ISL70444SEHEVAL1Z (Note 5)	N/A	Evaluation Board		

NOTES:

1. These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed must be used when ordering.
3. The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across temperature specified in the DLA SMD and are in the same form and fit as the qualified device. The /SAMPLE parts are capable of meeting the electrical limits and conditions specified in the DLA SMD. The /SAMPLE parts do not receive 100% screening across temperature to the DLA SMD electrical limits. These part types do not come with a Certificate of Conformance because they are not DLA qualified devices.
4. Die product tested at T_A = + 25°C. The wafer probe test includes functional and parametric testing sufficient to make the die capable of meeting the electrical performance outlined in the Electrical Specification tables starting on page 5.
5. The evaluation board uses /PROTO parts. The /PROTO parts are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity.

Absolute Maximum Ratings

Maximum Supply Voltage 42V
Maximum Supply Voltage (Note 8). 42V
Maximum Differential Input Current 20mA
Maximum Differential Input Voltage . . . . . 42V or V^- - 0.5V to V^+ + 0.5V
Min/Max Input Voltage . . . . . 42V or V^- - 0.5V to V^+ + 0.5V
Max/Min Input Current for Input Voltage >V^+ or <V^- . . . . . ±20mA
ESD Tolerance
Human Body Model (Tested per MIL-PRF-883 3015.7). 2kV
Machine Model (Tested per JESD22-A115-A). 200V
Charged Device Model (Tested per CDM-22CIOID). 750V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
14 Ld Flatpack Package (Notes 6, 7)	35	9

Storage Temperature Range. . . . . -65°C to +150°C

Recommended Operating Conditions

Ambient Operating Temperature Range . . . . . -55°C to +125°C
Maximum Operating Junction Temperature . . . . . +150°C
Single Supply Voltage . . . . . 3V ±10% to 36V ±10%
Split Rail Supply Voltage . . . . . ±1.5V ±10% to ±18V ±10%

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

NOTES:

6. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
7. For θ_{JC}, the case temperature location is the center of the package underside.
8. Tested in a heavy ion environment at LET = 86.4MeV • cm^2/mg at +125°C (T_C) for SEB. See Single Event Effects Test Report for more information.

Electrical Specifications V_S = ±18V

V_{CM} = V_O = 0V, R_L = Open, T_A = +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
Offset Voltage	V_{OS}	V_{CM} = 0V		20	400	µV
		V_{CM} = V^+ to V^-		80	**500**	µV
Offset Voltage Temperature Coefficient	TCV_{OS}	V_{CM} = V^+ - 2V to V^- + 2V		0.5		µV/°C
Input Offset Channel-to-Channel Match	ΔV_{OS}	V_{CM} = V^+		77	**800**	µV
		V_{CM} = V^-		117	**800**	µV
Input Bias Current	I_B	V_{CM} = 0V		189	**370**	nA
		V_{CM} = V^+		200	**370**	nA
		V_{CM} = V^-		262	**650**	nA
		V_{CM} = V^+ - 0.5V		200	**370**	nA
		V_{CM} = V^- + 0.5V		257	**650**	nA
Input Offset Current	I_{OS}	V_{CM} = V^+ to V^-	-30	0	30	nA
			-50	0	**50**	nA
Common-Mode Input Voltage Range	V_{CMIR}		**V^-**		**V^+**	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = V^- to V^+		112		dB
		V_{CM} = V^- to V^+	**70**			dB
		V_{CM} = V^+ - 0.5V to V^- + 0.5V		111		dB
		V_{CM} = V^+ - 0.5V to V^- + 0.5V	**80**			dB
Power Supply Rejection Ratio	PSRR	V^- = -18V; V^+ = 0.5V to 18V V^+ = 18V; V^- = -0.5V to -18V		143		dB
			83			dB
Open-Loop Gain	A_{VOL}	R_L = 10kΩ to ground		125		dB
			96			dB
Output Voltage High (V_{OUT} to V^+)	V_{OH}	R_L = No load		78	**160**	mV
		R_L = 10kΩ		118	**175**	mV
Output Voltage Low (V_{OUT} to V^-)	V_{OL}	R_L = No load		73	**160**	mV
		R_L = 10kΩ		110	**175**	mV
Output Short-Circuit Current	I_{SRC}	Sourcing; V_{IN} = 0V, V_{OUT} = -18V	**10**			mA

Electrical Specifications V_S = ±18V

V_{CM} = V_O = 0V, R_L = Open, T_A = +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
Output Short-Circuit Current	I_{SNK}	Sinking; V_{IN} = 0V, V_{OUT} = +18V	**10**			mA
Supply Current/Amplifier	I_S	Unity gain		1.5	1.75	mA
				1.95	**2.4**	mA
AC SPECIFICATIONS						
Gain Bandwidth Product	GBW	A_{CL} = 101, R_L = 10k		19		MHz
Voltage Noise Density	e_n	f = 10kHz		11.3		nV/√Hz
Current Noise Density	i_n	f = 10kHz		0.312		pA/√Hz
Large Signal Slew Rate	SR	A_V = 1, R_L = 10kΩ, V_O = $10V_{P-P}$	**60**			V/µs

Electrical Specifications V_S = ±2.5V

V_{CM} = V_O = 0V, R_L = Open, T_A = +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
Offset Voltage	V_{OS}	V_{CM} = 0V		20	400	µV
		V_{CM} = V^+ to V^-		80	**500**	µV
Offset Voltage Temperature Coefficient	TCV_{OS}	V_{CM} = V^+ - 2V to V^- + 2V		0.5		µV/°C
Input Offset Channel-to-Channel Match	ΔV_{OS}	V_{CM} = V^+		79	**800**	µV
		V_{CM} = V^-		119	**800**	µV
Input Bias Current	I_B	V_{CM} = 0V		202	**340**	nA
		V_{CM} = V^+		182	**340**	nA
		V_{CM} = V^-		229	**580**	nA
		V_{CM} = V^+ - 0.5V		181	**340**	nA
		V_{CM} = V^- + 0.5V		224	**580**	nA
Input Offset Current	I_{OS}	V_{CM} = V^+ to V^-	-30	0	30	nA
			-50	0	**50**	nA
Common-Mode Input Voltage Range	V_{CMIR}		**V^-**		**V^+**	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = V^- to V^+		92		dB
		V_{CM} = V^- to V^+	**70**			dB
		V_{CM} = V^+ - 0.5V to V^- + 0.5V		91		dB
		V_{CM} = V^+ - 0.5V to V^- + 0.5V	**74**			dB
Power Supply Rejection Ratio	PSRR	V^- = -2.5V; V^+ = 0.5V to 2.5V V^+ = 2.5V; V^- = -0.5V to -2.5V T_A = +25°C, +125°C		135		dB
			80			dB
		V^- = -2.5V; V^+ = 0.5V to 2.5V V^+ = 2.5V; V^- = -0.5V to -2.5V T_A = -55°CC	**70**			dB
Open-Loop Gain	A_{VOL}	R_L = 10kΩ to ground		118		dB
			90			dB
Output Voltage High (V_{OUT} to V^+)	V_{OH}	R_L = No load		53	**85**	mV
		R_L = 10kΩ		53	**105**	mV
		R_L = 600Ω			**400**	mV

Electrical Specifications V_S = ±2.5V

V_{CM} = V_O = 0V, R_L = Open, T_A = +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
Output Voltage Low (V_{OUT} to V^-)	V_{OL}	R_L = No load		53	**85**	mV
		R_L = 10kΩ		53	**105**	mV
		R_L = 600Ω			**400**	mV
Supply Current/Amplifier	I_S	Unity gain		1.1	1.25	mA
				1.6	**1.8**	mA
AC SPECIFICATIONS						
Gain Bandwidth Product	GBW	A_{CL} = 101, R_L = 10k		17		MHz
Voltage Noise Density	e_n	f = 10kHz		12.3		nV/√Hz
Current Noise Density	i_n	f = 10kHz		0.313		pA/√Hz
Large Signal Slew Rate	SR	A_V = 1, R_L = 10kΩ, V_O = $3V_{P-P}$		35		V/µs

Electrical Specifications V_S = ±1.5V

V_{CM} = V_O = 0V, R_L = Open, T_A = +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
Offset Voltage	V_{OS}	V_{CM} = 0V		51	400	µV
		V_{CM} = V_+ to V^-		80	**500**	µV
Input Offset Channel-to-Channel Match	ΔV_{OS}	V_{CM} = V^+		79	**800**	µV
		V_{CM} = V^-		119	**800**	µV
Input Bias Current	I_B	V_{CM} = 0V		220	**330**	nA
		V_{CM} = V^+		180	**330**	nA
		V_{CM} = V^-		225	**565**	nA
		V_{CM} = V^+ - 0.5V		180	**330**	nA
		V_{CM} = V^- + 0.5V		223	**565**	nA
Input Offset Current	I_{OS}	V_{CM} = V^+ to V^-	-30	0	30	nA
		V_{CM} = V^+ to V^-	**-50**	0	**50**	nA
Common-Mode Input Voltage Range	V_{CMIR}		**V^-**		**V^+**	V
Output Voltage High (V_{OUT} to V^+)	V_{OH}	R_L = No load		26	**39**	mV
		R_L = 10kΩ		30	**60**	mV
Output Voltage Low (V_{OUT} to V^-)	V_{OL}	R_L = No load		26	**39**	mV
		R_L = 10kΩ		42	**60**	mV
Supply Current/Amplifier	I_S	Unity Gain		1.1	1.24	mA
				1.57	**1.8**	mA
AC SPECIFICATIONS						
Gain Bandwidth Product	GBW	A_{CL} = 101, R_L = 10k		16		MHz
Voltage Noise Density	e_n	f = 10kHz		12		nV/√Hz
Current Noise Density	i_n	f = 10kHz		0.312		pA/√Hz

Electrical Specifications V_S = ±18V - Post Radiation

V_{CM} = V_O = 0V, R_L = Open, T_A = +25°C, unless otherwise noted. **Boldface limits apply across a total ionizing dose of 300krad(Si) with exposure of a high dose rate of 50 to 300rad(Si)/s (ISL70444SEH only) and across a total ionizing dose of 50krad(Si) with exposure at a low dose rate of <10mrad(Si)/s.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
Offset Voltage	V_{OS}	V_{CM} = V^+ to V^-			**500**	µV
Input Offset Channel-to-Channel Match	ΔV_{OS}	V_{CM} = V^+			**800**	µV
		V_{CM} = V^-			**800**	µV
Input Bias Current	I_B	V_{CM} = V^+			**650**	nA
		V_{CM} = V^-	**-650**			nA
Input Offset Current	I_{OS}	V_{CM} = V^+ to V^-	**-50**		**50**	nA
Common-Mode Input Voltage Range	V_{CMIR}		**V^-**		**V^+**	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = V^- to V^+	**70**			dB
		V_{CM} = V^- to V^+				
		V_{CM}= V^+ - 0.5V to V^- + 0.5V				dB
		V_{CM}= V^+ - 0.5V to V^- + 0.5V	**80**			dB
Power Supply Rejection Ratio	PSRR	V^- = -18V; V^+ = 0.5V to 18V V^+ = 18V; V^- = -0.5V to -18V				dB
			83			dB
Open-Loop Gain	A_{VOL}	R_L = 10kΩ to ground	96			dB
Output Voltage High (V_{OUT} to V^+)	V_{OH}	R_L = No load			**160**	mV
		R_L = 10kΩ			**175**	mV
Output Voltage Low (V_{OUT} to V^-)	V_{OL}	R_L = No load			**150**	mV
		R_L = 10kΩ			**165**	mV
Output Short-Circuit Current	I_{SRC}	Sourcing; V_{IN} = 0V, V_{OUT} = -18V	**10**			mA
Output Short-Circuit Current	I_{SNK}	Sinking; V_{IN} = 0V, V_{OUT} = +18V	**10**			mA
Supply Current/Amplifier	I_S	Unity gain			**2.4**	mA
Large Signal Slew Rate	SR	AV = 1, RL = 10kΩ, V_O = $10V_{P-P}$	**60**			V/µs

Electrical Specifications V_S = ±2.5V - Post Radiation

$V_{CM} = V_O = 0V$, R_L = Open, $T_A = +25°C$, unless otherwise noted. **Boldface limits apply a total ionizing dose of 300krad(Si) with exposure of a high dose rate of 50 to 300rad(Si)/s (ISL70444SEH only) and across a total ionizing dose of 50krad(Si) with exposure at a low dose rate of <10mrad(Si)/s.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
Offset Voltage	V_{OS}	$V_{CM} = V^+$ to V^-			**500**	µV
Input Offset Channel-to-Channel Match	ΔV_{OS}	$V_{CM} = V^+$			**800**	µV
		$V_{CM} = V^-$			**800**	µV
Input Bias Current	I_B	$V_{CM} = V^+$			**650**	nA
		$V_{CM} = V^-$	**-650**			nA
Input Offset Current	I_{OS}	$V_{CM} = V^+$ to V^-	**-50**		**50**	nA
Common-Mode Input Voltage Range	V_{CMIR}		**V^-**		**V^+**	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = V^-$ to V^+				dB
		$V_{CM} = V^-$ to V^+	**70**			dB
		$V_{CM} = V^+ - 0.5V$ to $V^- + 0.5V$				dB
		$V_{CM} = V^+ - 0.5V$ to $V^- + 0.5V$	**74**			dB
Power Supply Rejection Ratio	PSRR	$V^- = -2.5V$; $V^+ = 0.5V$ to $2.5V$ $V^+ = 2.5V$; $V^- = -0.5V$ to $-2.5V$				dB
			80			dB
Open-loop Gain	A_{VOL}	R_L = 10kΩ to ground	90			dB
Output Voltage High (V_{OUT} to V^+)	V_{OH}	R_L = No load			**85**	mV
		R_L = 10kΩ			**105**	mV
		R_L = 600Ω			**400**	mV
Output Voltage Low (V_{OUT} to V^-)	V_{OL}	R_L = No load			**85**	mV
		R_L = 10kΩ			**105**	mV
		R_L = 600Ω			**400**	mV
Supply Current/Amplifier	I_S	Unity gain			**1.8**	mA

Electrical Specifications V_S = ±1.5V - Post Radiation

$V_{CM} = V_O = 0V$, R_L = Open, $T_A = +25°C$, unless otherwise noted. **Boldface limits apply a total ionizing dose of 300krad(Si) with exposure of a high dose rate of 50 to 300rad(Si)/s (ISL70444SEH only) and across a total ionizing dose of 50krad(Si) with exposure at a low dose rate of <10mrad(Si)/s.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
Offset Voltage	V_{OS}	$V_{CM} = V^+$ to V^-			**500**	µV
Input Offset Channel-to-Channel Match	ΔV_{OS}	$V_{CM} = V^+$			**800**	µV
		$V_{CM} = V^-$			**800**	µV
Input Bias Current	I_B	$V_{CM} = V^+$			**650**	nA
		$V_{CM} = V^-$	**-650**			nA
Input Offset Current	I_{OS}	$V_{CM} = V^+$ to V^-	**-50**		**50**	nA
Common-Mode Input Voltage Range	V_{CMIR}		**V^-**		**V^+**	V
Output Voltage High (V_{OUT} to V^+)	V_{OH}	R_L = No load			**160**	mV
		R_L = 10kΩ			**175**	mV
Output Voltage Low (V_{OUT} to V^-)	V_{OL}	R_L = No load			**150**	mV
		R_L = 10kΩ			**165**	mV
Supply Current/Amplifier	I_S	Unity gain			**1.8**	mA

NOTE:

9. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

Typical Performance Curves

Unless otherwise specified, V_S ±18V, V_{CM} = 0, V_O = 0V, T_A = +25°C.

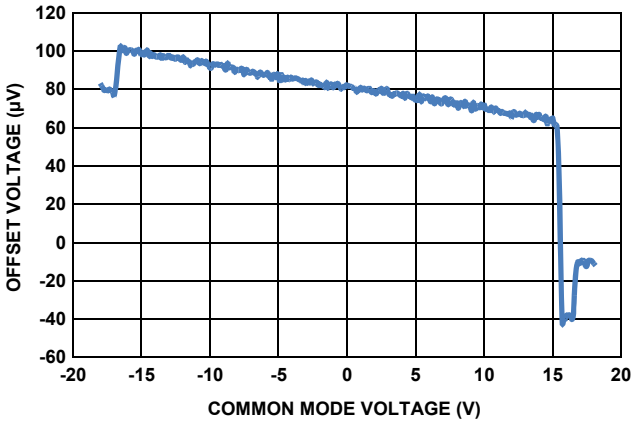


FIGURE 3. OFFSET VOLTAGE vs COMMON-MODE VOLTAGE

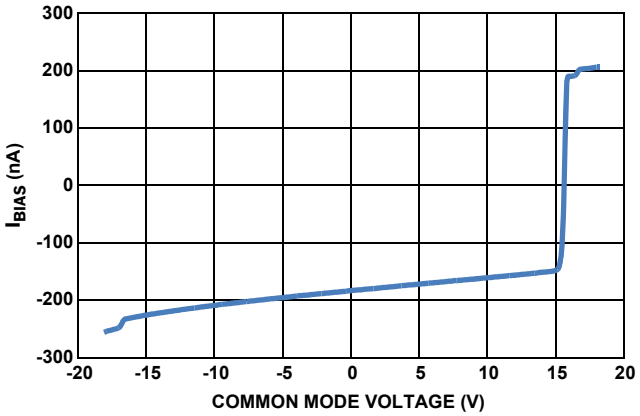


FIGURE 4. I_{BIAS} vs COMMON-MODE VOLTAGE

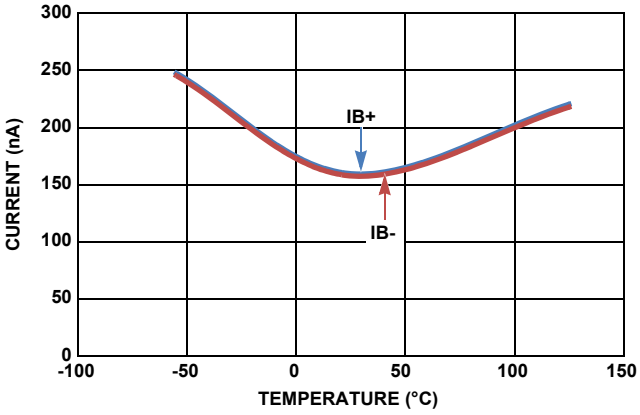


FIGURE 5. I_{BIAS} vs TEMPERATURE (V_S = ±18V)

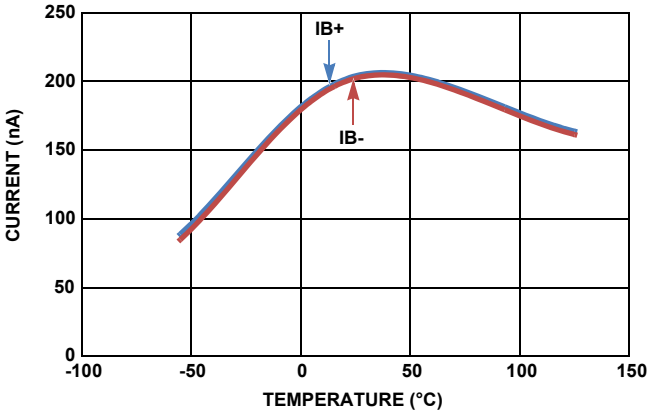


FIGURE 6. I_{BIAS} vs TEMPERATURE (V_S = ±2.5V)

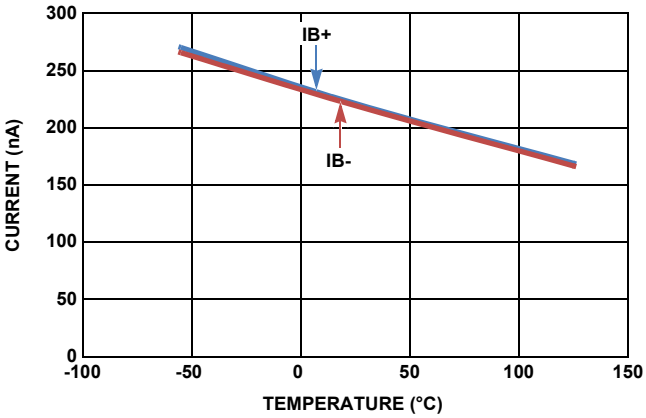


FIGURE 7. I_{BIAS} vs TEMPERATURE, (V_S = ±1.5V)

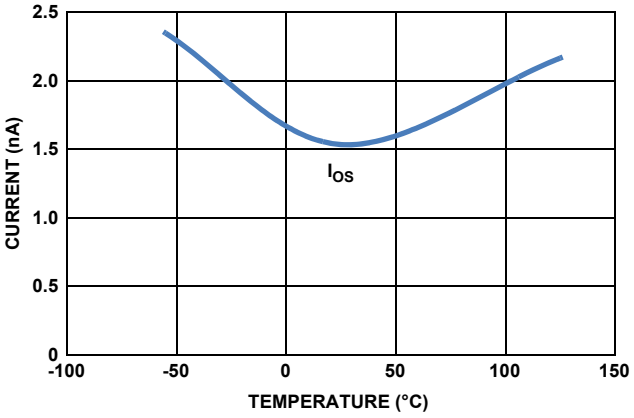


FIGURE 8. I_{OS} vs TEMPERATURE (V_S = ±18V)

Typical Performance Curves

Unless otherwise specified, V_S ±18V, V_{CM} = 0, V_O = 0V, T_A = +25°C. **(Continued)**

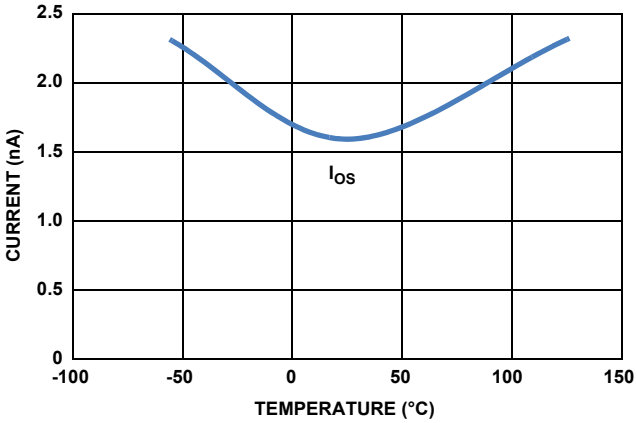


FIGURE 9. I_{OS} vs TEMPERATURE (V_S = ±2.5V)

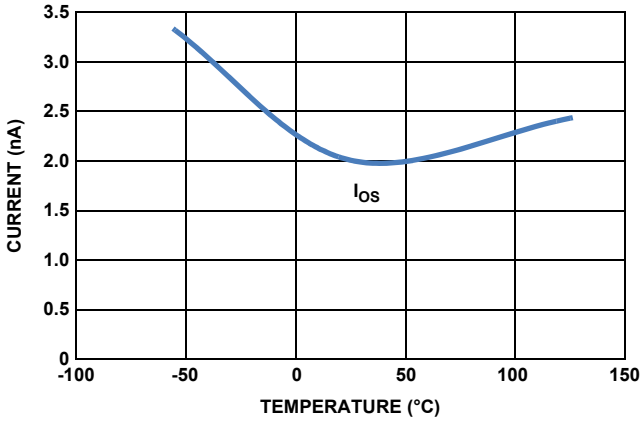


FIGURE 10. I_{OS} vs TEMPERATURE (V_S = ±1.5V)

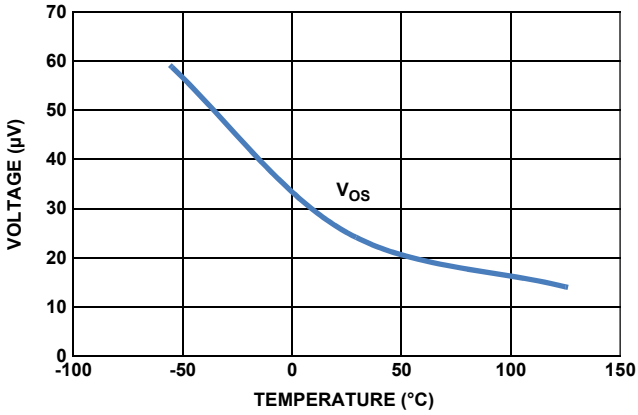


FIGURE 11. V_{OS} vs TEMPERATURE (V_S = ±18V)

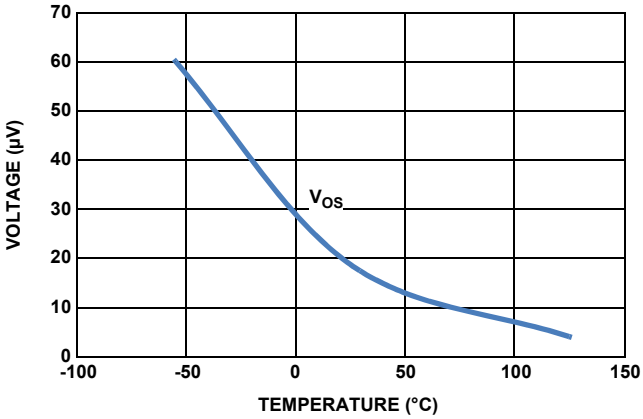


FIGURE 12. V_{OS} vs TEMPERATURE (V_S = ±2.5V)

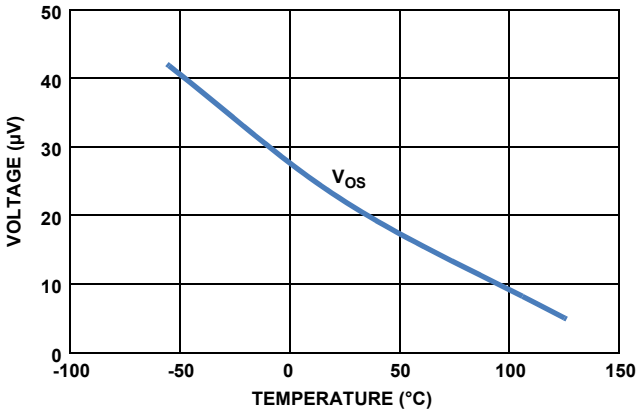


FIGURE 13. V_{OS} vs TEMPERATURE (V_S = ±1.5V)

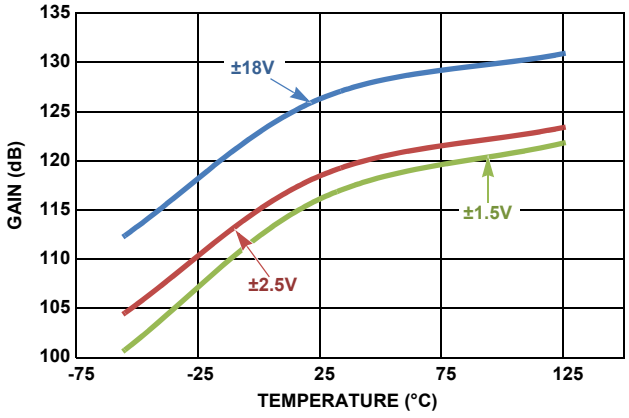


FIGURE 14. A_{VOL} vs TEMPERATURE vs SUPPLY VOLTAGE

Typical Performance Curves

Unless otherwise specified, V_S ±18V, V_{CM} = 0, V_O = 0V, T_A = +25°C. **(Continued)**

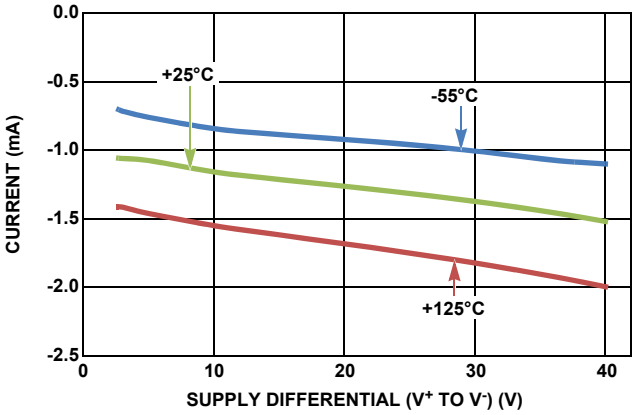


FIGURE 15. NEGATIVE SUPPLY CURRENT vs SUPPLY VOLTAGE

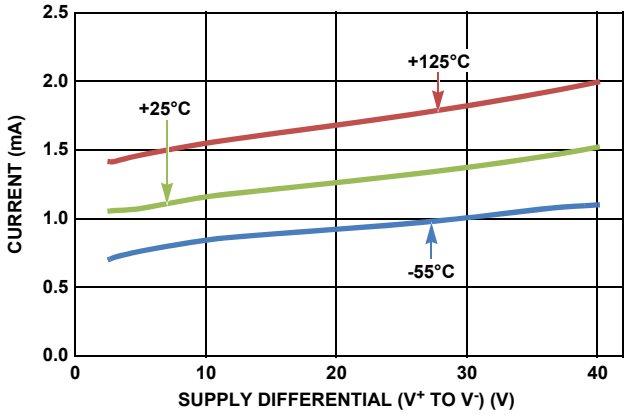


FIGURE 16. POSITIVE SUPPLY CURRENT vs SUPPLY VOLTAGE

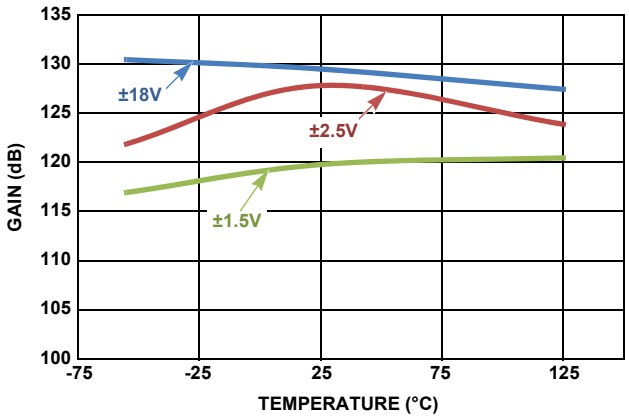


FIGURE 17. PSRR+ vs TEMPERATURE vs SUPPLY VOLTAGE

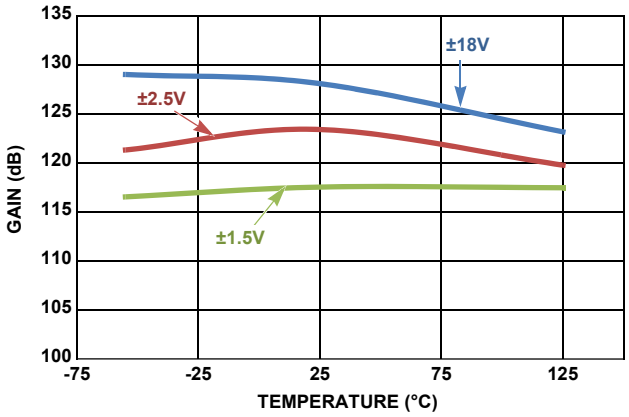


FIGURE 18. PSRR- vs TEMPERATURE vs SUPPLY VOLTAGE

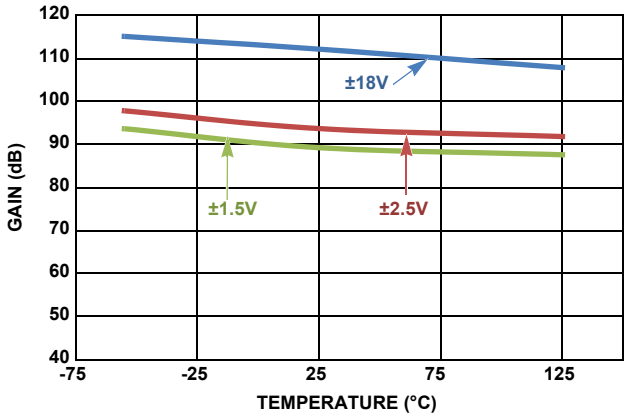


FIGURE 19. CMRR vs TEMPERATURE vs SUPPLY VOLTAGE

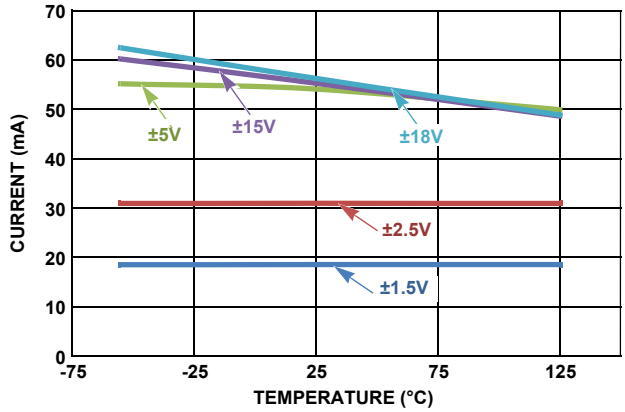


FIGURE 20. SHORT-CIRCUIT CURRENT vs TEMPERATURE

Typical Performance Curves

Unless otherwise specified, V_S ±18V, V_{CM} = 0, V_O = 0V, T_A = +25°C. **(Continued)**

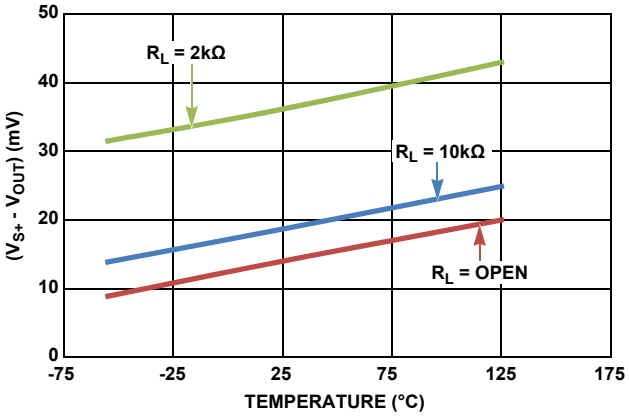


FIGURE 21. (V_S = ±1.5V) V_{OH} vs TEMPERATURE

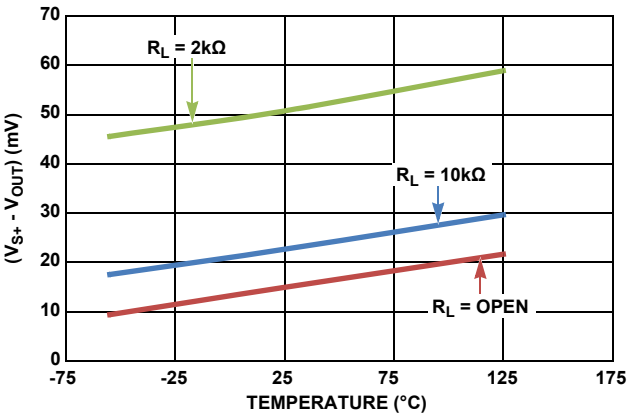


FIGURE 22. (V_S = ±2.5V) V_{OH} vs TEMPERATURE

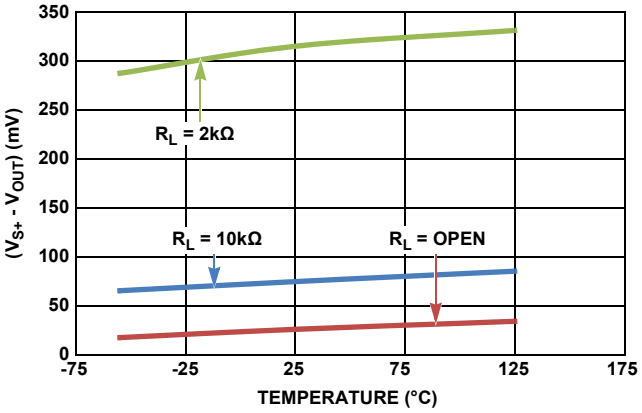


FIGURE 23. (V_S = ±18V) V_{OH} vs TEMPERATURE

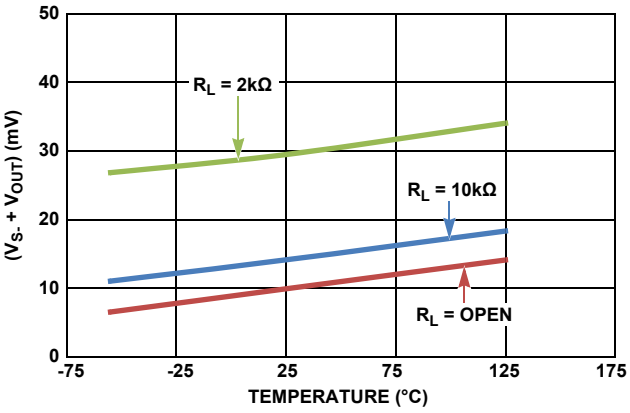


FIGURE 24. (V_S = ±1.5V) V_{OL} vs TEMPERATURE

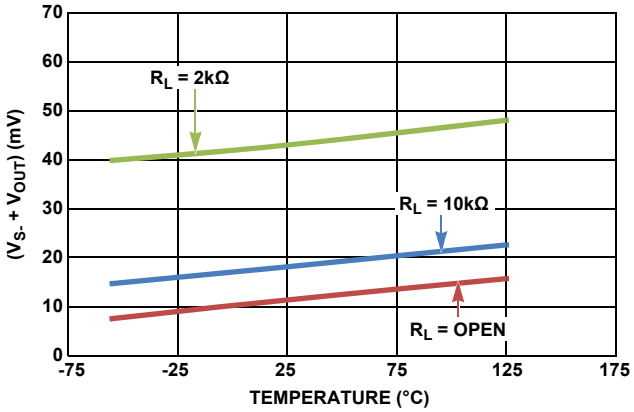


FIGURE 25. (V_S = ±2.5V) V_{OL} vs TEMPERATURE

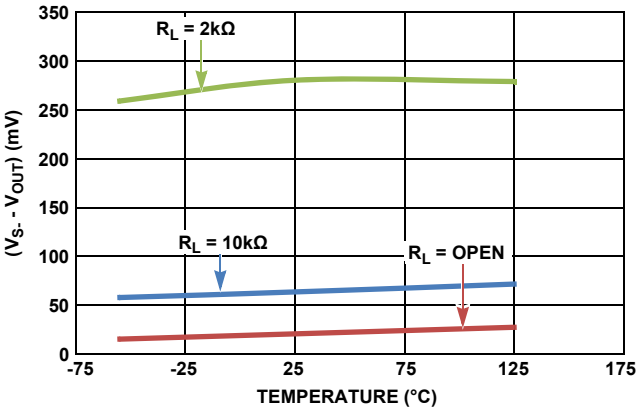


FIGURE 26. (V_S = ±18V) V_{OL} vs TEMPERATURE

Typical Performance Curves

Unless otherwise specified, V_S ±18V, V_{CM} = 0, V_O = 0V, T_A = +25°C. **(Continued)**

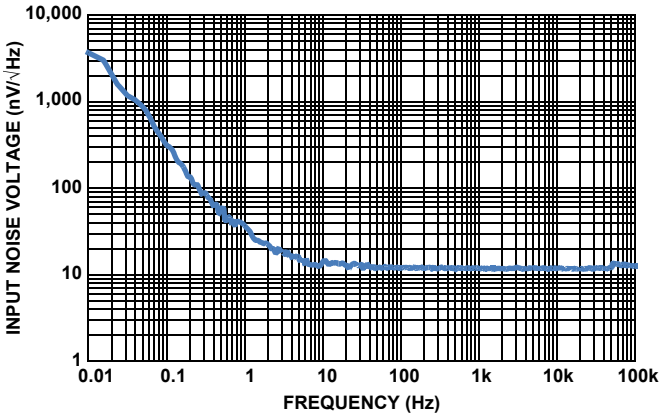


FIGURE 27. INPUT NOISE VOLTAGE SPECTRAL DENSITY (V_S = ±18V)

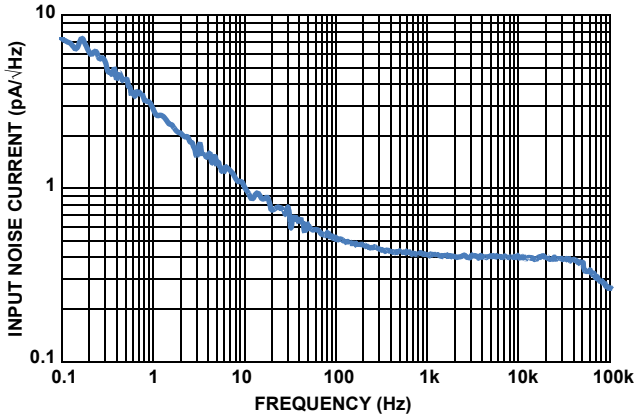


FIGURE 28. INPUT NOISE CURRENT SPECTRAL DENSITY (V_S = ±18V)

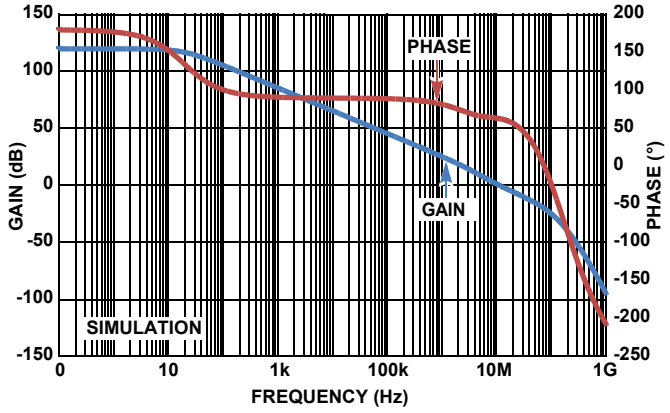


FIGURE 29. OPEN LOOP FREQUENCY RESPONSE (C_L = 0.01pF)

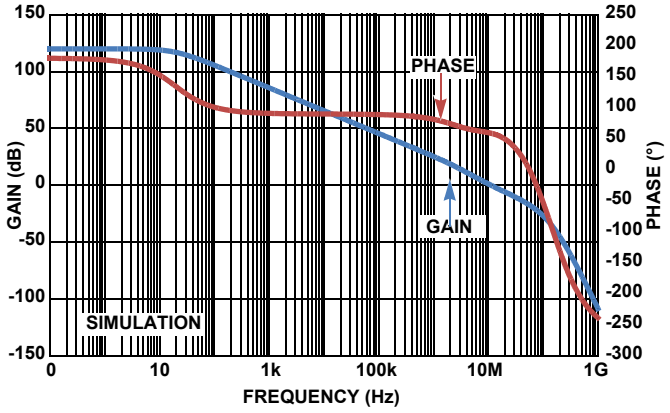


FIGURE 30. OPEN LOOP FREQUENCY RESPONSE (C_L = 10pF)

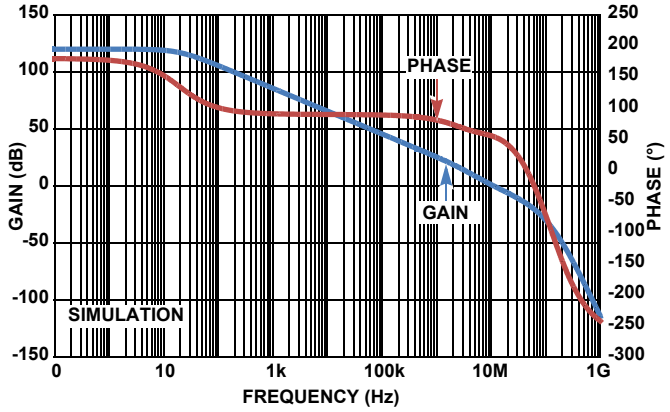


FIGURE 31. OPEN LOOP FREQUENCY RESPONSE (C_L = 22pF)

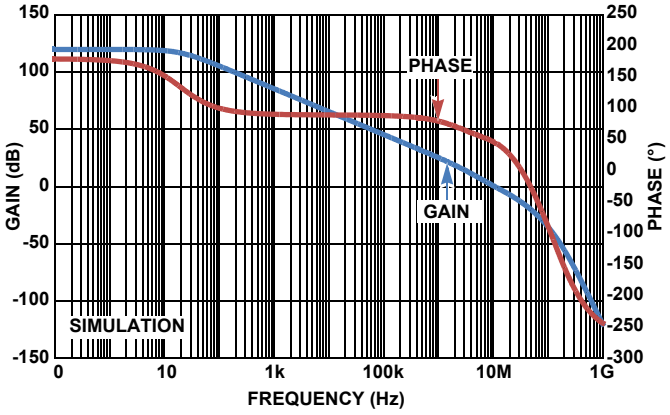


FIGURE 32. OPEN LOOP FREQUENCY RESPONSE (C_L = 47pF)

Typical Performance Curves

Unless otherwise specified, V_S ±18V, V_{CM} = 0, V_O = 0V, T_A = +25°C. **(Continued)**

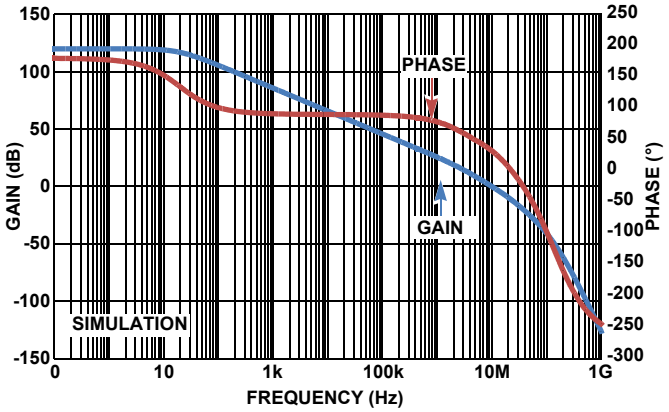


FIGURE 33. OPEN LOOP FREQUENCY RESPONSE (C_L = 100pF)

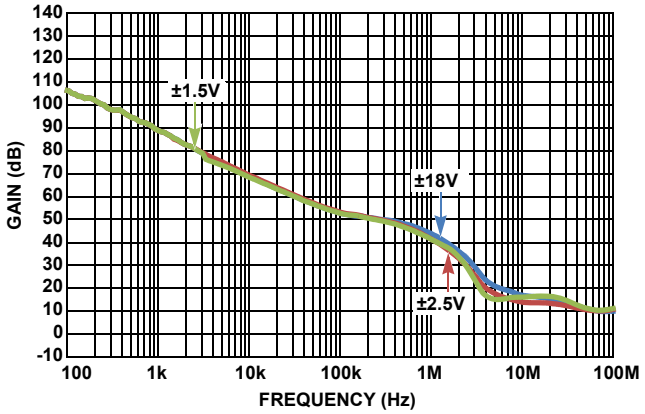


FIGURE 34. CMRR vs FREQUENCY

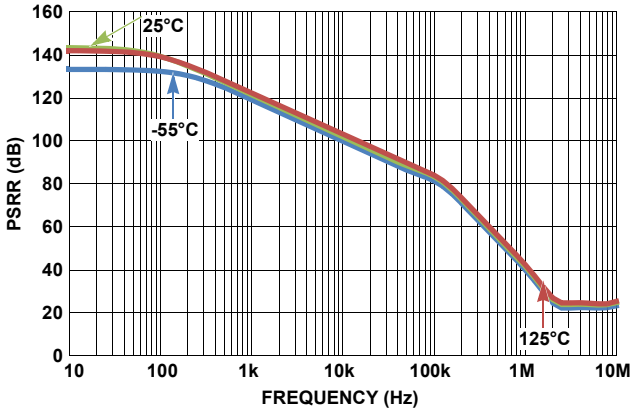


FIGURE 35. PSRR vs FREQUENCY, ±18V

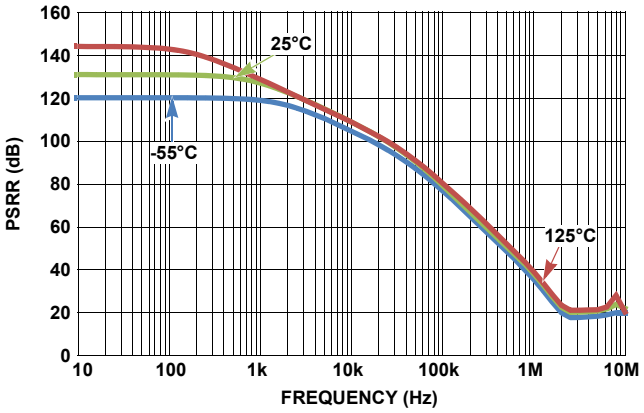


FIGURE 36. PSRR vs FREQUENCY, ±2.5V

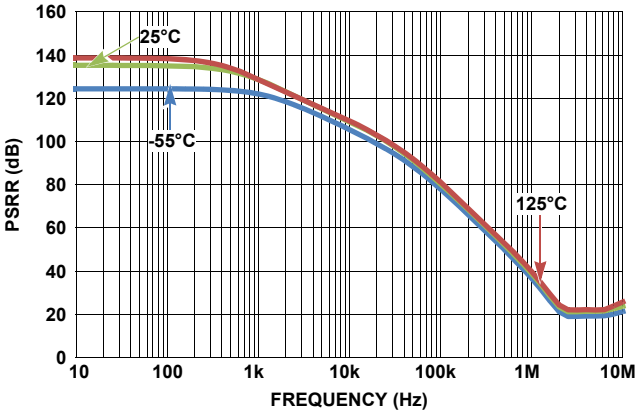


FIGURE 37. PSRR vs FREQUENCY, ±1.5V

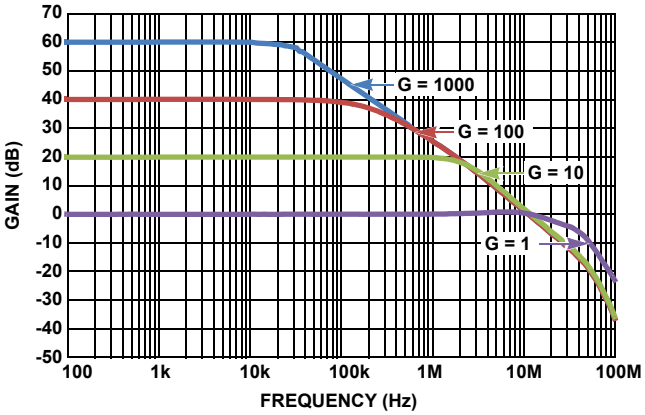


FIGURE 38. FREQUENCY RESPONSE vs CLOSED LOOP GAIN

Typical Performance Curves

Unless otherwise specified, V_S ±18V, V_{CM} = 0, V_O = 0V, T_A = +25°C. **(Continued)**

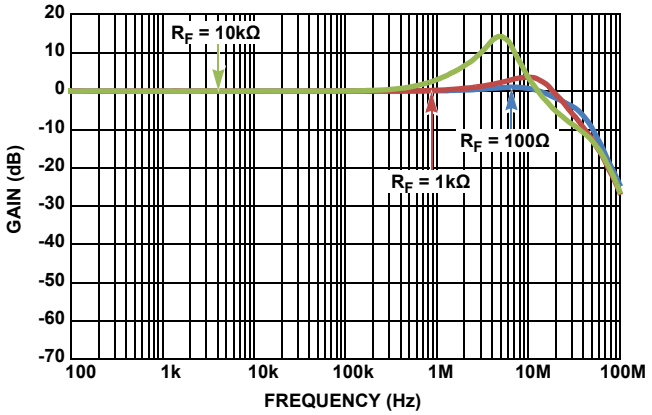


FIGURE 39. FREQUENCY RESPONSE vs FEEDBACK RESISTANCE (R_F)

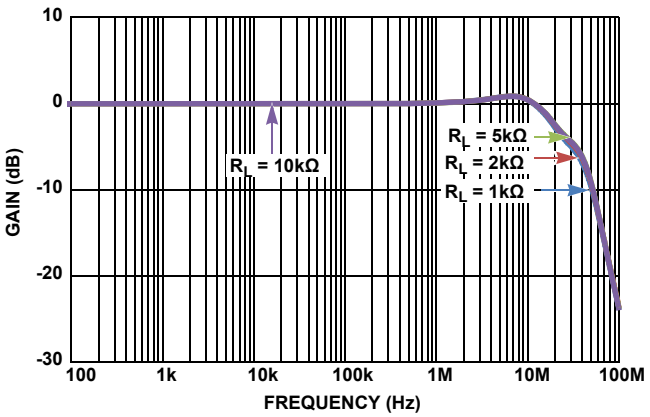


FIGURE 40. FREQUENCY RESPONSE vs LOAD RESISTANCE

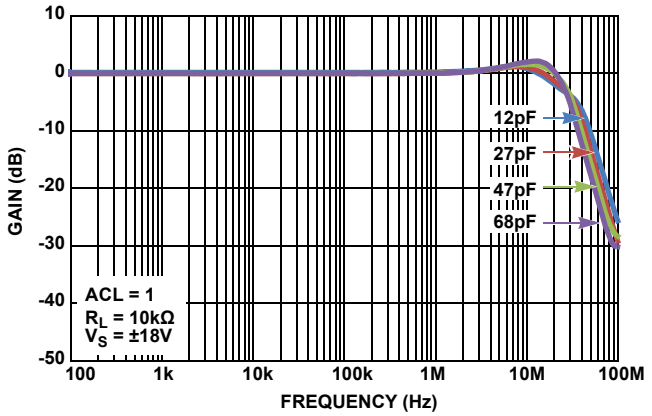


FIGURE 41. UNITY GAIN RESPONSE vs LOAD CAPACITANCE

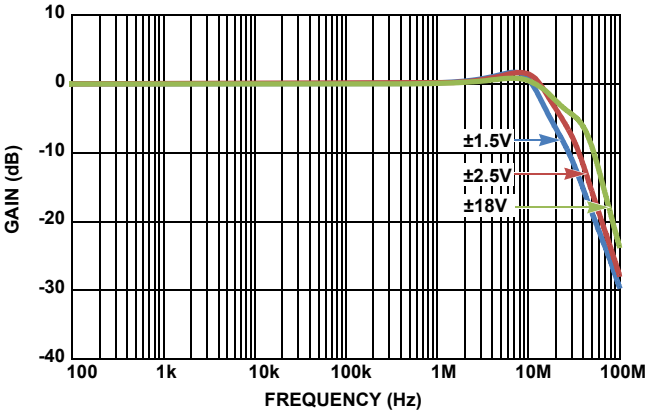


FIGURE 42. FREQUENCY RESPONSE vs SUPPLY VOLTAGE

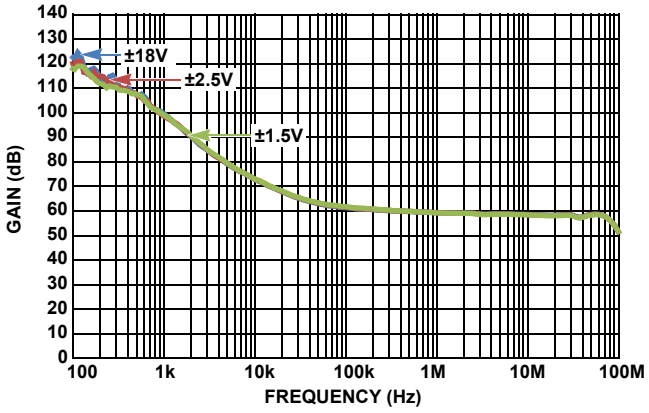


FIGURE 43. CROSSTALK REJECTION

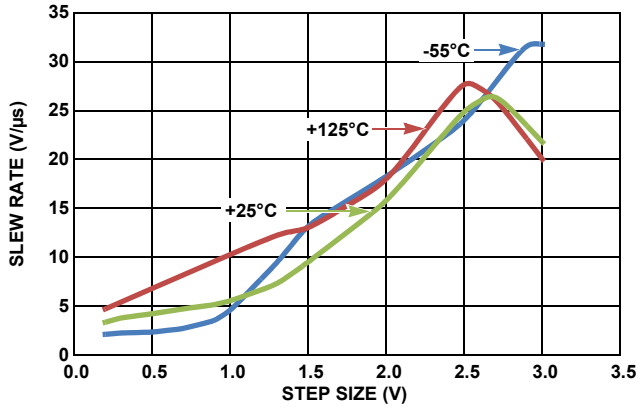


FIGURE 44. SLEW RATE vs STEP SIZE vs TEMPERATURE (V_S = ±1.5V)

Typical Performance Curves

Unless otherwise specified, V_S ±18V, V_{CM} = 0, V_O = 0V, T_A = +25°C. **(Continued)**

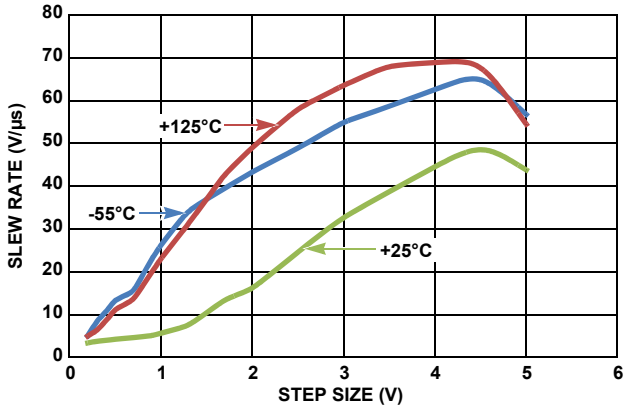


FIGURE 45. SLEW RATE vs STEP SIZE vs TEMPERATURE (V_S = ±2.5V)

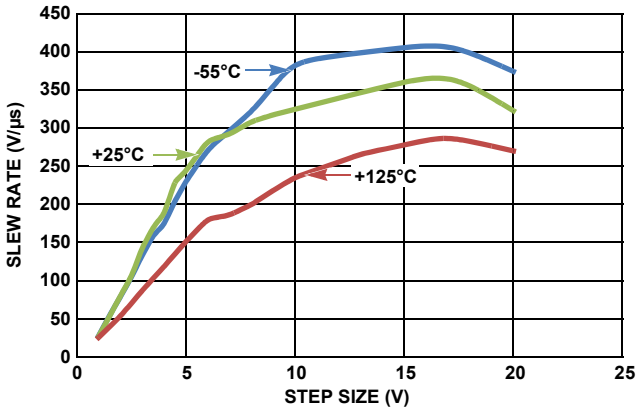


FIGURE 46. SLEW RATE vs STEP SIZE vs TEMPERATURE (V_S = ±18V)

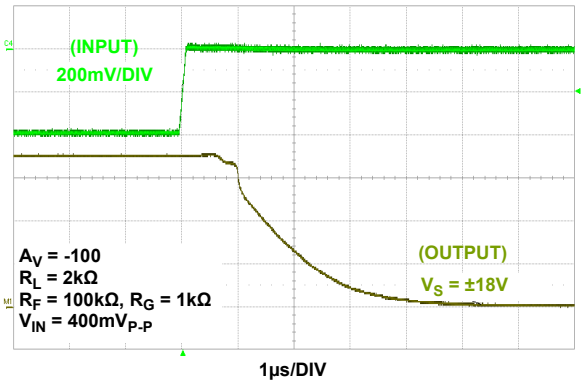


FIGURE 47. SATURATION RECOVERY (V_S = ±18V)

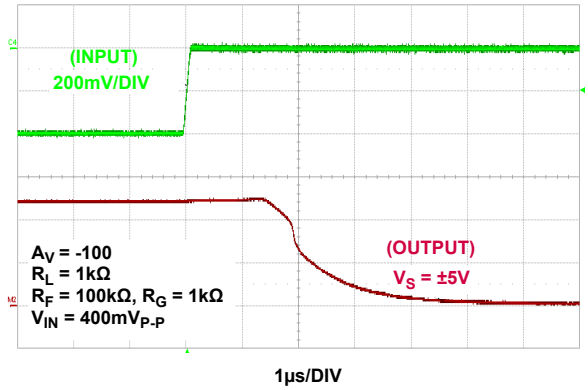


FIGURE 48. SATURATION RECOVERY (V_S = ±5V)

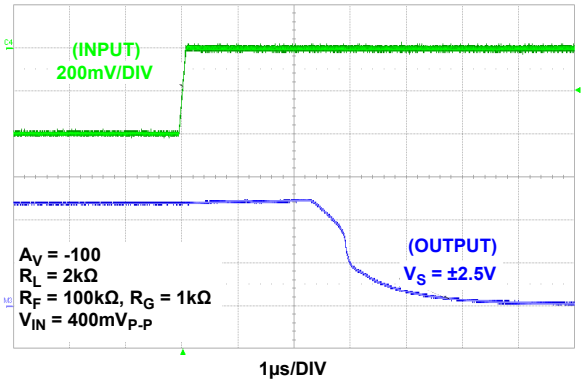


FIGURE 49. SATURATION RECOVERY (V_S = ±2.5V)

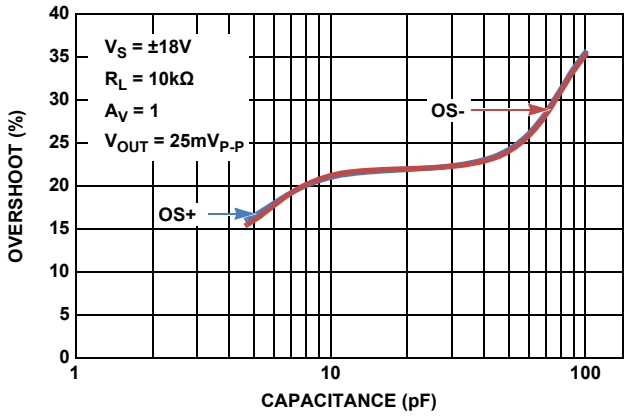


FIGURE 50. OVERSHOOT (%) vs LOAD CAPACITANCE

Typical Performance Curves

Unless otherwise specified, V_S ±18V, V_{CM} = 0, V_O = 0V, T_A = +25°C. **(Continued)**

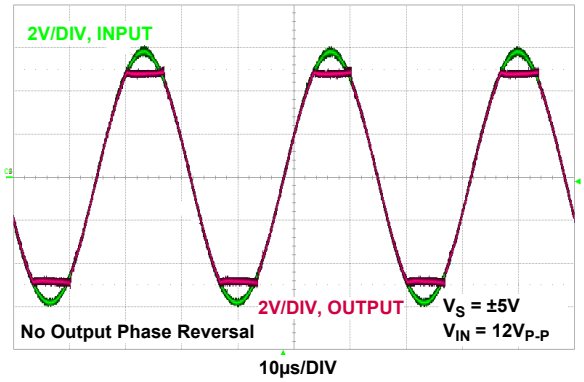


FIGURE 51. INPUT OVERDRIVE RESPONSE

Post High Dose Rate Radiation Characteristics

Unless otherwise specified, V_S ±18V, V_{CM} = 0, V_O = 0V, T_A = +25°C. This data is typical mean test data post radiation exposure at a high dose rate of 50 to 300rad(Si)/s (ISL70444SEH only). This data is intended to show typical parameter shifts due to high dose rate radiation. These are not limits nor are they guaranteed.

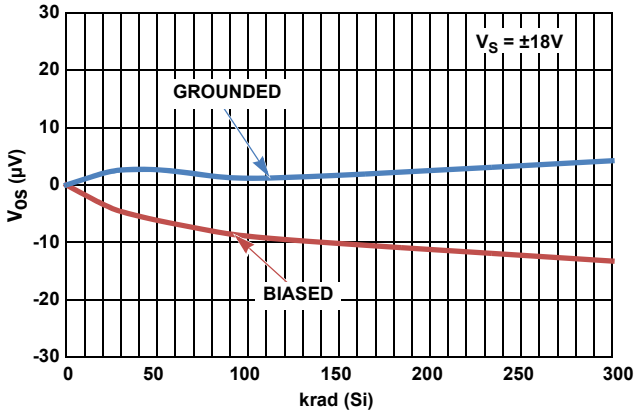


FIGURE 52. V_{OS} SHIFT vs HIGH DOSE RATE RADIATION

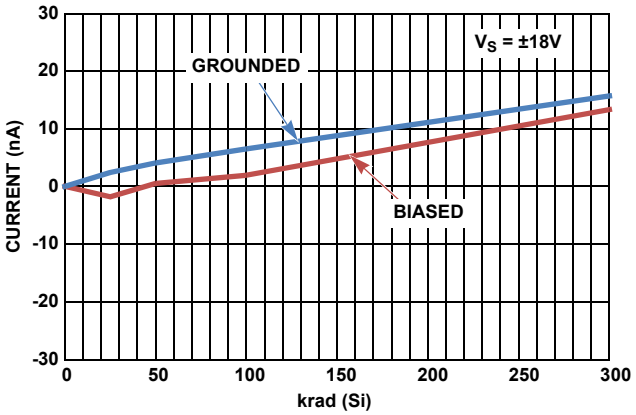


FIGURE 53. I_{BIAS} SHIFT vs HIGH DOSE RATE RADIATION

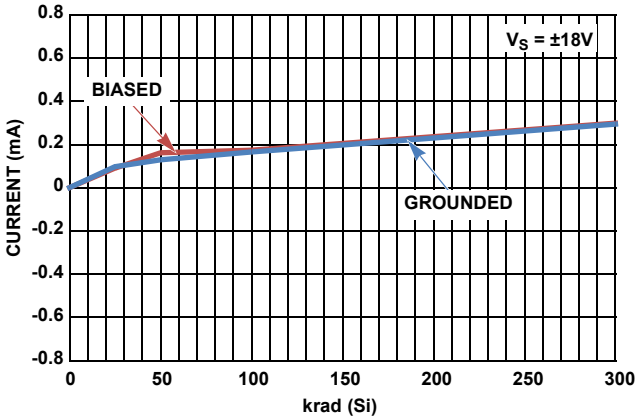


FIGURE 54. I^- SHIFT vs HIGH DOSE RATE RADIATION

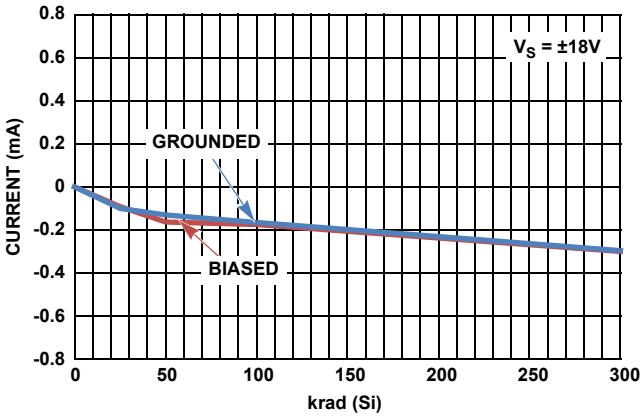


FIGURE 55. I^+ SHIFT vs HIGH DOSE RATE RADIATION

Post High Dose Rate Radiation Characteristics

Unless otherwise specified, V_S ±18V, V_{CM} = 0, V_O = 0V, T_A = +25°C. This data is typical mean test data post radiation exposure at a high dose rate of 50 to 300rad(Si)/s (ISL70444SEH only). This data is intended to show typical parameter shifts due to high dose rate radiation. These are not limits nor are they guaranteed.

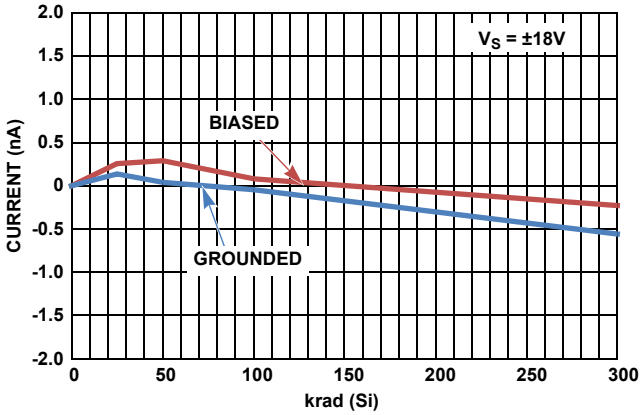


FIGURE 56. I_{OS} SHIFT vs HIGH DOSE RATE RADIATION

Post Low Dose Rate Radiation Characteristics

Unless otherwise specified, V_S ±18V, V_{CM} = 0, V_O = 0V, T_A = +25°C. This data is typical mean test data post radiation exposure at a low dose rate of <10mrad(Si)/s. This data is intended to show typical parameter shifts due to high dose rate radiation. These are not limits nor are they guaranteed.

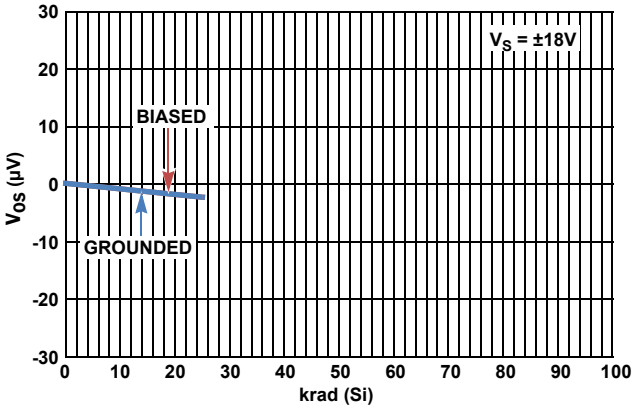


FIGURE 57. V_{OS} SHIFT vs LOW DOSE RATE RADIATION

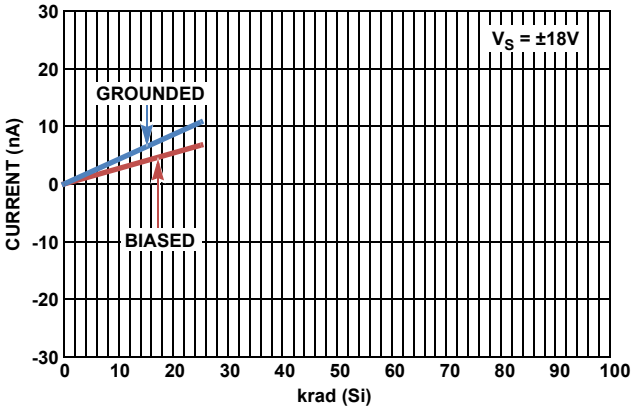


FIGURE 58. I_{BIAS} SHIFT vs LOW DOSE RATE RADIATION

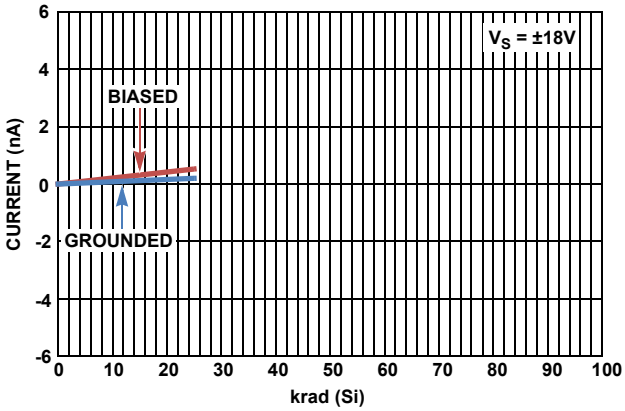


FIGURE 59. I_{OS} SHIFT vs LOW DOSE RATE RADIATION

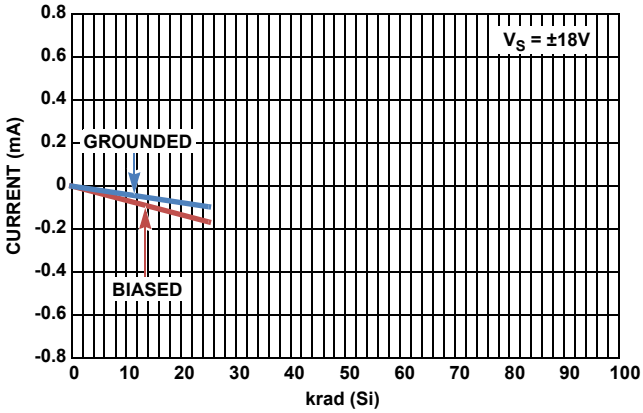


FIGURE 60. I^+ SHIFT vs LOW DOSE RATE RADIATION

Post Low Dose Rate Radiation Characteristics

Unless otherwise specified, V_S ±18V, V_{CM} = 0, V_O = 0V, T_A = +25°C. This data is typical mean test data post radiation exposure at a low dose rate of <10mrad(Si)/s. This data is intended to show typical parameter shifts due to high dose rate radiation. These are not limits nor are they guaranteed.

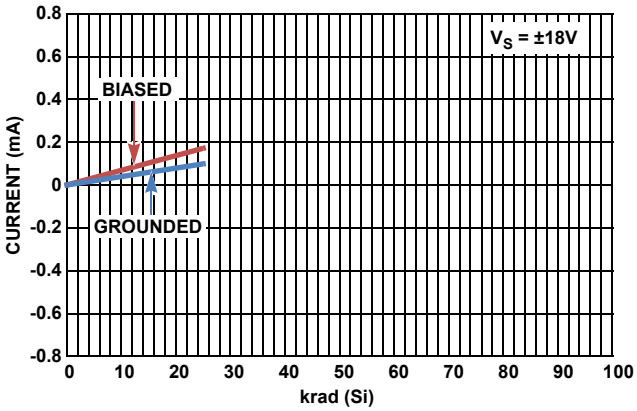


FIGURE 61. I^- SHIFT vs LOW DOSE RATE RADIATION

Applications Information

Functional Description

The ISL7x444SEH contain four high-speed and low-power op amps designed to take advantage of their full dynamic input and output voltage range with rail-to-rail operation. By offering low power, low offset voltage and low temperature drift coupled with its high bandwidth and enhanced slew rates upwards of 50V/µs, these op amps are ideal for applications requiring both high DC accuracy and AC performance. The ISL7x444SEH are manufactured using the Renesas PR40 silicon-on-insulator process, which makes these devices immune to single event latch-up and provides excellent radiation tolerance. These features make the devices an ideal choice for high reliability applications in harsh radiation-prone environments.

Operating Voltage Range

The ISL7x444SEH are designed to operate with a split supply rail from ±1.35V to ±20V or a single supply rail from 2.7V to 40V. The ISL7x444SEH are fully characterized in production for supply rails of 5V (±2.5V) and 36V (±18V). The power supply rejection ratio is typically 120dB over the full operating voltage range. The worst case Common-Mode Rejection Ratio (CMRR) across temperature is within 1.5V to 2V of each rail. When V_{CM} is inside that range, the CMRR performance is typically >110dB with a ±18V supply. The minimum CMRR performance across the -55°C to +125°C temperature range and radiation is >70dB over the full common-mode input range for power supply voltages from ±2.5V (5V) to ±18V (36V).

Input Performance

The slew enhanced front-end is a block that is placed in parallel with the main input stage and functions based on the input differential.

Input ESD Diode Protection

The input terminals (IN+ and IN-) have internal ESD protection diodes to the positive and negative supply rails, series connected 600Ω current limiting resistors and an anti-parallel diode pair across the inputs.

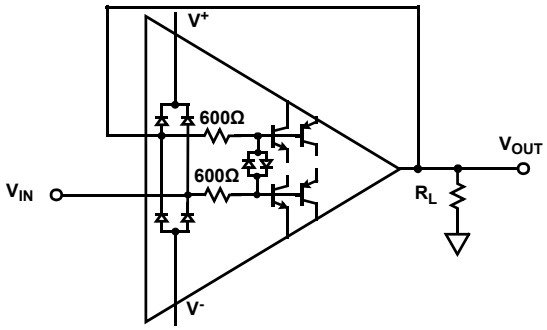


FIGURE 62. INPUT ESD DIODE CURRENT LIMITING, UNITY GAIN

Output Short-Circuit Current Limiting

The output current limit has a worst case minimum limit of ±8mA but may reach as high as ±100mA. The op amp can withstand a short-circuit to either rail for a short duration (<1s) as long as the maximum operating junction temperature is not violated. This applies to only one amplifier at a given time. Continued use of the device in these conditions may degrade the long term reliability of the part and is not recommended. Figure 20 shows the typical short-circuit currents that can be expected. The ISL7x444SEH's current limiting circuitry automatically lowers the current limit of the device if short-circuit conditions carry on for extended periods of time. This protects the device from malfunction; however, extended operation in this mode degrades the output rail-to-rail performance by increasing the V_{OH}/V_{OL} levels.

Output Phase Reversal

Output phase reversal is a change of polarity in the amplifier transfer function when the input voltage exceeds the supply voltage. The ISL7x444SEH are immune to output phase reversal, even when the input voltage is 1V beyond the supplies. This is illustrated in Figure 51 on page 18.

Power Dissipation

It is possible to exceed the +150°C maximum junction temperature under certain load and power supply conditions. It is therefore important to calculate the maximum junction temperature (T_{JMAX}) for all applications to determine if power supply voltages, load conditions, or package type need to be modified to remain in the safe operating range. These parameters are related using Equation 1:

$$T_{JMAX} = T_{MAX} + \theta_{JA} \times PD_{MAXTOTAL} \quad \text{(EQ. 1)}$$

where:

- $P_{DMAXTOTAL}$ is the sum of the maximum power dissipation of each amplifier in the package (PD_{MAX})
- Calculate PD_{MAX} for each amplifier using Equation 2:

$$PD_{MAX} = V_S \times I_{qMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L} \quad \text{(EQ. 2)}$$

where:

- T_{MAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- PD_{MAX} = Maximum power dissipation of one amplifier
- V_S = Total supply voltage
- I_{qMAX} = Maximum quiescent supply current of one amplifier
- V_{OUTMAX} = Maximum output voltage swing of the application

Slew Rate Enhancement

The ISL7x444SEH have slew enhanced front-end that increases the drive on the output transistors proportional to the differential voltage across the inputs. This increase in output drive shows up as increased transient current on top of the op amp's steady state supply current. If the voltage differential between the inputs remains constant, as in comparator applications, the added drive current to the output transistors becomes steady state and increases the DC power supply current of the IC. For this reason, we do not recommended using the ISL7x444SEH in a comparator configuration.

Unused Channel Configuration

If the application does not require the use of all four op amps, you must configure the unused channels to prevent it from oscillating. Any unused channels oscillate if the input and output pins are floating. The oscillationresults in higher than expected supply currents and possible noise injection into any of the active channels in use. The proper way to prevent oscillation is to short the output to the inverting input and tie the positive input to a known voltage, such as mid-supply.

When the V^- supply is less than or equal to -1.0V, configure your op amp as in Figure 63, or follow the configuration shown in Figure 64. The resistors in Figure 64 are of equal value and high resistance (≥10kΩ) to minimize current draw, while keeping the positive input at mid-supply. All unused op amps can have their inputs tied to the same resistor divider to minimize the number of components.

Tying the positive input to ground in Figure 64 (where V^- = GND) would produce a voltage differential across the inputs, as the inverting input would be at the op amp's V_{OL} and the positive input would be at GND, causing an increase in the steady state supply current. While this does not damage the op amp, the increased supply current would result in additional unnecessary power dissipation.

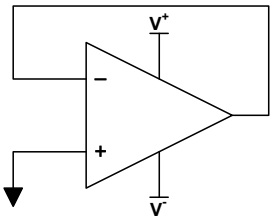


FIGURE 63. PREVENTING OSCILLATIONS IN UNUSED CHANNELS, SPLIT SUPPLY

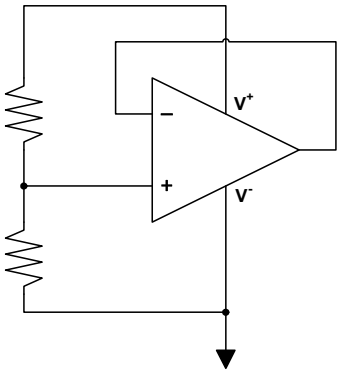


FIGURE 64. PREVENTING OSCILLATIONS IN UNUSED CHANNELS, SINGLE SUPPLY

Die Characteristics

Die Dimensions

2410µm x 3175µm (95 mils x 125 mils)
Thickness: 483µm ±25µm (19 mils ±1 mil)

Interface Materials

GLASSIVATION

Type: Nitrox
Thickness: 15kÅ

TOP METALLIZATION

Type: AlCu (99.5%/0.5%)
Thickness: 30kÅ

BACKSIDE FINISH

Silicon

PROCESS

PR40

Assembly Related Information

SUBSTRATE POTENTIAL

Floating

Additional Information

WORST CASE CURRENT DENSITY

$< 2 \times 10^5$ A/cm^2

TRANSISTOR COUNT

730

Weight of Packaged Device

0. 5952 grams (Typical)

Lid Characteristics

Finish: Gold
Potential: Unbiased, tied to E-pad under package
Case Isolation to Any Lead: 20×10^9 Ω (min)

Metallization Mask Layout

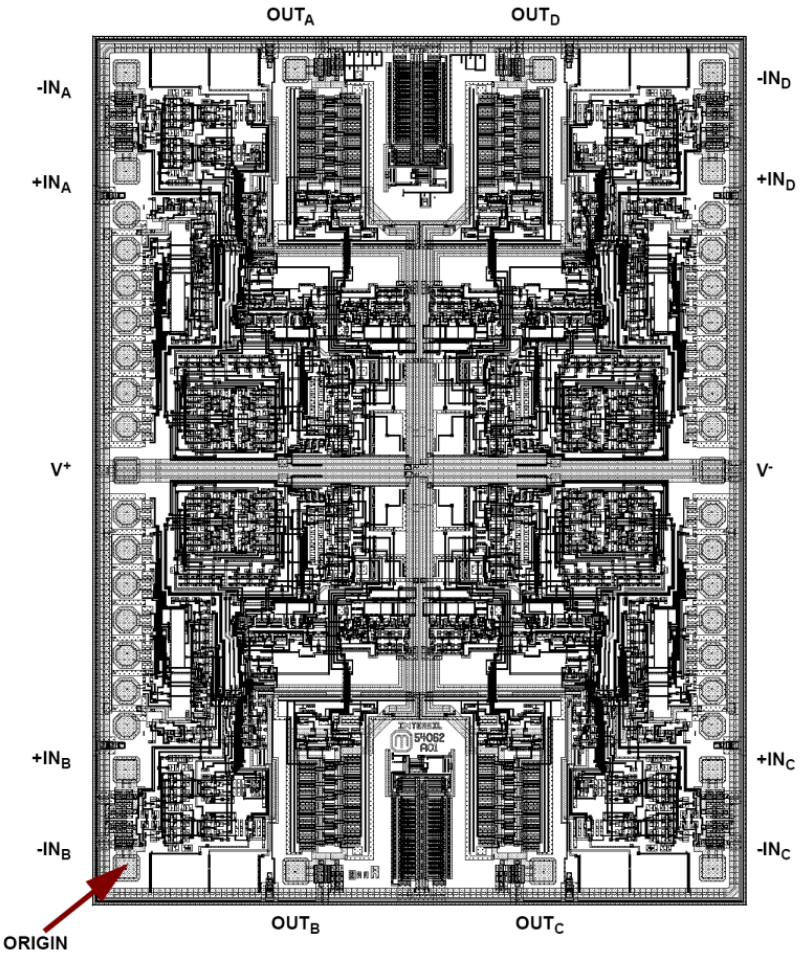


TABLE 1. DIE LAYOUT X-Y COORDINATES

PAD NAME	PAD NUMBER	X (µm)	Y (µm)	dX (µm)	dY (µm)	BOND WIRES PER PAD
OUT_B	2	599.0	-11.5	70	70	1
OUT_C	3	1472.0	-11.5	70	70	1
$-IN_C$	4	2071.0	0.0	70	70	1
$+IN_C$	12	2071.0	347.5	70	70	1
V^-	20	2071.0	1406.5	70	70	1
$+IN_D$	21	2071.0	2465.5	70	70	1
$-IN_D$	22	2071.0	2813.0	70	70	1
OUT_D	23	1472.0	2824.5	70	70	1
OUT_A	24	599.0	2824.5	70	70	1
$-IN_A$	25	0.0	2813.0	70	70	1
$+IN_A$	33	0.0	2465.5	70	70	1
V^+	41	0.0	1406.5	70	70	1
$+IN_B$	42	0.0	347.5	70	70	1
$-IN_B$	1	0.0	0.0	70	70	1

NOTE:

10. Origin of coordinates is the centroid of pad 42, “IN-B”.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure that you have the latest revision.

DATE	REVISION	CHANGE
Nov 16, 2020	8.00	Updated Note 3 and added Note 4. Updated Power Supply Rejection Ratio typical from 128 to 143 in the ±18V EC specification table. Updated Power Supply Rejection Ratio typical from 123 to 135 in the ±2.5V EC specification table. Updated Figure 35 and added Figures 36 and 37.
Aug 16, 2019	7.00	Updated SEE and TID ratings in Features section. Added radiation levels to ordering information table. Removed Table 1.
Mar 28, 2019	6.00	Updated links throughout document. Added ISL73444SEH information throughout document. Added Table 1. Updated Disclaimer.
Jan 19, 2018	5.00	Added “Slew Rate Enhancement” section on page 20. On page 21 - Updated “Unused Channel Configuration” section, updated Figure 61 and added Figure 62. Removed “About Intersil” section. Added new disclaimer.

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure that you have the latest revision. **(Continued)**

DATE	REVISION	CHANGE
Jul 6, 2017	4.00	Updated Related Literature section. Changed low input voltage from 300µV to 400µV in features list. Added Notes 3 and 4. Electrical Specification updates: **VS = ±18V table:** Updated Offset Voltage from “300” to “400” and “400” to “500”. Updated Input Offset Current from “-17” to “-30” (min) and “17” to “30” (max) unbolded values. Added another Input Offset Current line and bolded. Updated PSRR min from “88” to “83” **VS = ±2.5V table:** Updated Offset Voltage from “300” to “400” and “400” to “500”. Updated Input Offset Current from “-17” to “-30” (min) and “17” to “30” (max) unbolded values. Added another Input Offset Current line and bolded. Unbolded PSRR min value and added a new line with 70 min bolded. **VS = ±1.5V table:** Updated Offset Voltage from “300” to “400” and “400” to “500”. Updated Input Offset Current from “-17” to “-30” (min) and “17” to “30” (max) unbolded values. Added another Input Offset Current line and bolded. **VS = ±18V table (RAD):** Updated Offset Voltage from “400” to “500”. Updated Input Offset Current from “-17” to “-50” (min) and “17” to “50” (max). Updated PSRR min from “88” to “83” **VS = ±2.5V table (RAD):** Updated Offset Voltage from “400” to “500”. Updated Input Offset Current from “-17” to “-50” (min) and “17” to “50” (max). **VS = ±1.5V table (RAD):** Updated Offset Voltage from “400” to “500”. Updated Input Offset Current from “-17” to “-50” (min) and “17” to “50” (max).
Jun 5, 2015	3.00	Changed Die Dimensions on page 22: From 2410µm x 3175µm (80mils x 101mils) Thickness: 483µm ± 25µm (19mils ± 1 mil) To: Die Dimensions 2410µm x 3175µm (95mils x 125mils) Thickness: 483µm ± 25µm (19mils ± 1 mil)
Jul 31, 2014	2.00	On page 1: Updated Features bullet from: - SEL/SEB LETTH. . . . . 86.4MeVocm2/mg To: - SEB LET_{TH} (V_S = ±21V). . . . . 86.4 MeV/mg/cm2 - SEL Immune (SOI Process) Ordering Information table on page 4: Removed MSL note. Updated About Intersil verbiage.
Jun 14, 2013	1.00	Changed Radiation tolerance High dose rate from 100krad(Si) to 300krad(Si) on page 1 features and in Electrical Spec Table conditions on pages 7 and 8. Added SR spec for V_S = ±18V to Electrical Spec Table on page 8. Removed Max limit of 300 for V_{OS} Offset Voltage in V_S = ±18V, V_S = ±2.5V and V_S = ±1.5V Spec tables.
May 23, 2013	0.00	Initial Release.

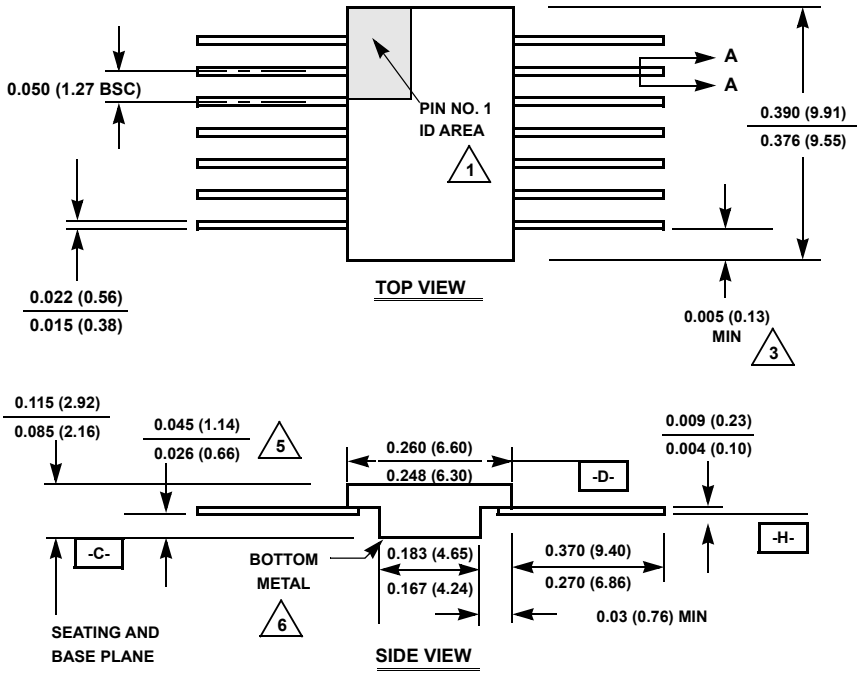
Package Outline Drawing

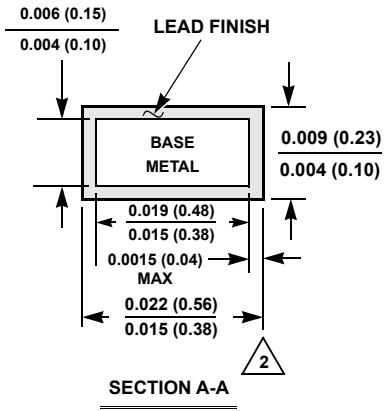
For the most recent package outline drawing, see K14.C.

K14.C

14 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

Rev 0, 9/12





NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions (section A-A) shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Measure dimension at all four corners.
4. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
5. Dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
6. The bottom of the package is a solderable metal surface.
7. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
8. Dimensions: INCH (mm). Controlling dimension: INCH.

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(Rev.1.0 Mar 2020)

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