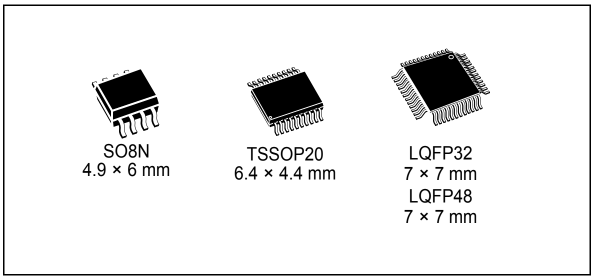
STM32G030x6/x8

Arm® Cortex®-M0+ 32-bit MCU, up to 64 KB Flash, 8 KB RAM, 2x USART, timers, ADC, comm. I/Fs, 2.0-3.6V

Datasheet - production data

Features

- Core: Arm® 32-bit Cortex®-M0+ CPU, frequency up to 64 MHz
- -40°C to 85°C operating temperature
- Memories
  - Up to 64 Kbytes of Flash memory with protection
  - 8 Kbytes of SRAM with HW parity check
- CRC calculation unit
- Reset and power management
  - Voltage range: 2.0 V to 3.6 V
  - Power-on/Power-down reset (POR/PDR)
  - Low-power modes: Sleep, Stop, Standby
  - V_{BAT} supply for RTC and backup registers
- Clock management
  - 4 to 48 MHz crystal oscillator
  - 32 kHz crystal oscillator with calibration
  - Internal 16 MHz RC with PLL option
  - Internal 32 kHz RC oscillator (±5 %)
- Up to 44 fast I/Os
  - All mappable on external interrupt vectors
  - Multiple 5 V-tolerant I/Os
- 5-channel DMA controller with flexible mapping
- 12-bit, 0.4 µs ADC (up to 16 ext. channels)
  - Up to 16-bit with hardware oversampling
  - Conversion range: 0 to 3.6V
- 8 timers: 16-bit for advanced motor control, four 16-bit general-purpose, two watchdogs, SysTick timer
- Calendar RTC with alarm and periodic wakeup from Stop/Standby



- Communication interfaces
  - Two I^2C-bus interfaces supporting Fast-mode Plus (1 Mbit/s) with extra current sink, one supporting SMBus/PMBus and wakeup from Stop mode
  - Two USARTs with master/slave synchronous SPI; one supporting ISO7816 interface, LIN, IrDA capability, auto baud rate detection and wakeup feature
  - Two SPIs (32 Mbit/s) with 4- to 16-bit programmable bitframe, one multiplexed with I^2S interface
- Development support: serial wire debug (SWD)
- All packages ECOPACK 2 compliant

Table 1. Device summary

Reference	Part number
STM32G030x6	STM32G030C6, STM32G030F6, STM32G030J6, STM32G030K6
STM32G030x8	STM32G030C8, STM32G030K8

This is information on a product in full production.

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1 Introduction

This document provides information on STM32G030x6/x8 microcontrollers, such as description, functional overview, pin assignment and definition, electrical characteristics, packaging, and ordering codes.

Information on memory mapping and control registers is object of reference manual.

Information on Arm®[a] Cortex®-M0+ core is available from the www.arm.com website.

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[a] Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

2 Description

The STM32G030x6/x8 mainstream microcontrollers are based on high-performance Arm® Cortex®-M0+ 32-bit RISC core operating at up to 64 MHz frequency. Offering a high level of integration, they are suitable for a wide range of applications in consumer, industrial and appliance domains and ready for the Internet of Things (IoT) solutions.

The devices incorporate a memory protection unit (MPU), high-speed embedded memories (8 Kbytes of SRAM and up to 64 Kbytes of Flash program memory with read protection, write protection), DMA, an extensive range of system functions, enhanced I/Os, and peripherals. The devices offer standard communication interfaces (two I^2Cs, two SPIs / one I^2S, and two USARTs), one 12-bit ADC (2.5 MSps) with up to 19 channels, a low-power RTC, an advanced control PWM timer, four general-purpose 16-bit timers, two watchdog timers, and a SysTick timer.

The devices operate within ambient temperatures from -40 to 85°C and with supply voltages from 2.0 V to 3.6 V. Optimized dynamic consumption combined with a comprehensive set of power-saving modes allows the design of low-power applications.

VBAT direct battery input allows keeping RTC and backup registers powered.

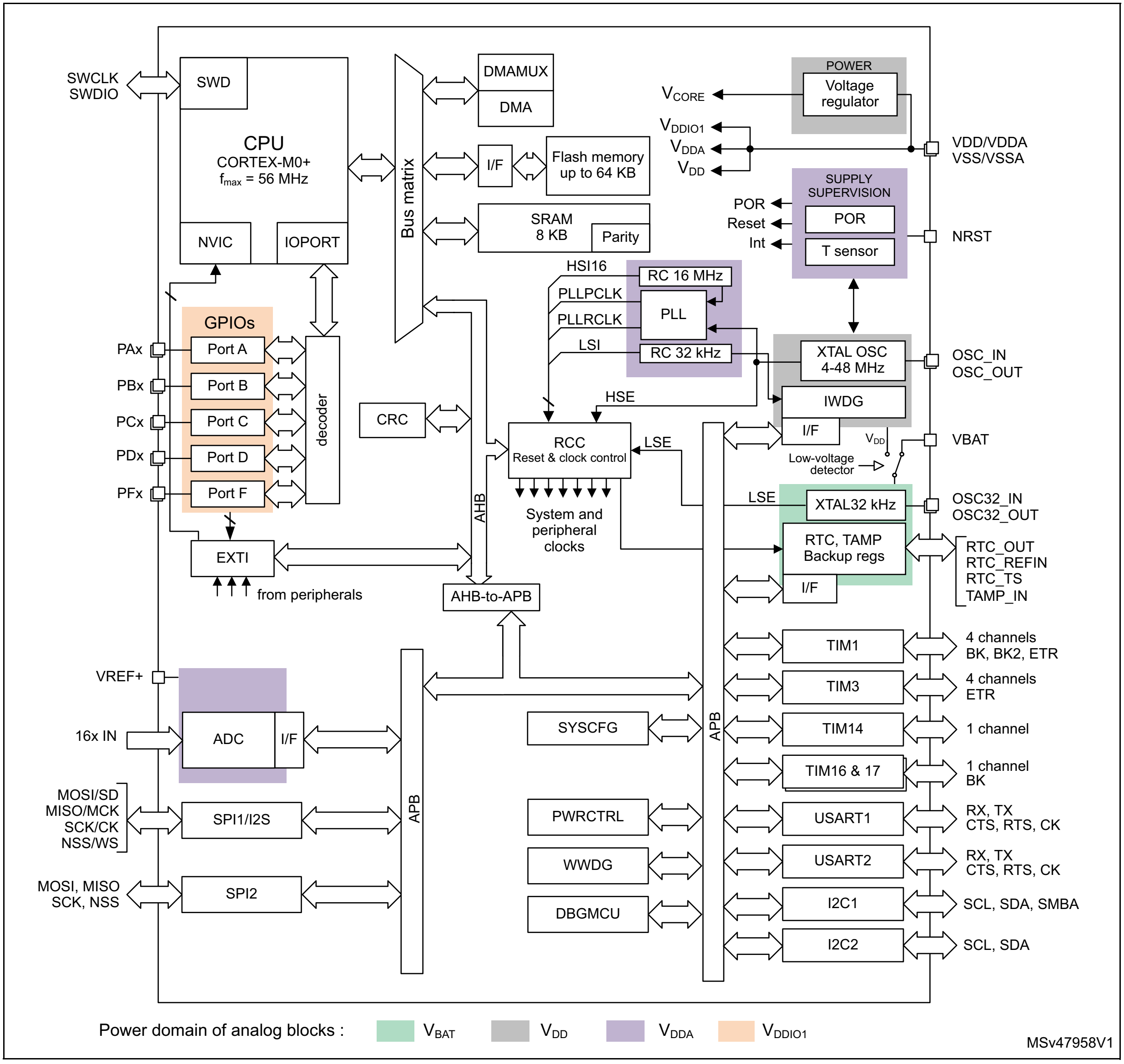
The devices come in packages with 8 to 48 pins.

Table 2. STM32G030x6/x8 family device features and peripheral counts

Peripheral		STM32G030_					
		_J6	_F6	_K6	_K8	_C6	_C8
Flash memory (Kbyte)		32	32	32	64	32	64
SRAM (Kbyte)		8 with parity					
Timers	Advanced control	1 (16-bit)					
	General-purpose	4 (16-bit)					
	SysTick	1					
	Watchdog	2					
Comm. interfaces	SPI [I2S](1)	2 [1]					
	I2C	2					
	USART	2					
RTC		Yes					
Tamper pins		2					
Random number generator		No					
AES		No					
GPIOs		5	17	29		43	
Wakeup pins		3	4				
12-bit ADC channels (external + internal)		5 + 2	14 + 2	16 + 2		16 + 3	
Internal voltage reference buffer		No					
Max. CPU frequency		64 MHz					
Operating voltage		2.0 to 3.6 V					
Operating temperature(2)		Ambient: -40 to 85 °C Junction: -40 to 105 °C					
Number of pins		8	20	32		48	

1. The numbers in brackets denote the count of SPI interfaces configurable as I^2S interface.
2. Depends on order code. Refer to *Section 7: Ordering information* for details.

Figure 1. Block diagram



3 Functional overview

3.1 Arm® Cortex®-M0+ core with MPU

The Cortex-M0+ is an entry-level 32-bit Arm Cortex processor designed for a broad range of embedded applications. It offers significant benefits to developers, including:

- a simple architecture, easy to learn and program
- ultra-low power, energy-efficient operation
- excellent code density
- deterministic, high-performance interrupt handling
- upward compatibility with Cortex-M processor family
- platform security robustness, with integrated Memory Protection Unit (MPU).

The Cortex-M0+ processor is built on a highly area- and power-optimized 32-bit core, with a 2-stage pipeline Von Neumann architecture. The processor delivers exceptional energy efficiency through a small but powerful instruction set and extensively optimized design, providing high-end processing hardware including a single-cycle multiplier.

The Cortex-M0+ processor provides the exceptional performance expected of a modern 32-bit architecture, with a higher code density than other 8-bit and 16-bit microcontrollers.

Owing to embedded Arm core, the STM32G030x6/x8 devices are compatible with Arm tools and software.

The Cortex-M0+ is tightly coupled with a nested vectored interrupt controller (NVIC) described in *Section 3.13.1*.

3.2 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

3.3 Embedded Flash memory

STM32G030x6/x8 devices feature up to 64 Kbytes of embedded Flash memory available for storing code and data.

Flexible protections can be configured thanks to option bytes:

- Readout protection (RDP) to protect the whole memory. Three levels are available:
  - Level 0: no readout protection
  - Level 1: memory readout protection: the Flash memory cannot be read from or written to if either debug features are connected, boot in RAM or bootloader is selected
  - Level 2: chip readout protection: debug features (Cortex-M0+ serial wire), boot in RAM and bootloader selection are disabled. This selection is irreversible.

Table 3. Access status versus readout protection level and execution modes

Area	Protection level	User execution			Debug, boot from RAM or boot from system memory (loader)		
		Read	Write	Erase	Read	Write	Erase
User memory	1	Yes	Yes	Yes	No	No	No
	2	Yes	Yes	Yes	N/A	N/A	N/A
System memory	1	Yes	No	No	Yes	No	No
	2	Yes	No	No	N/A	N/A	N/A
Option bytes	1	Yes	Yes	Yes	Yes	Yes	Yes
	2	Yes	No	No	N/A	N/A	N/A
Backup registers	1	Yes	Yes	N/A(1)	No	No	N/A(1)
	2	Yes	Yes	N/A	N/A	N/A	N/A

1. Erased upon RDP change from Level 1 to Level 0.

- Write protection (WRP): the protected area is protected against erasing and programming. Two areas per bank can be selected, with 2-Kbyte granularity.

The whole non-volatile memory embeds the error correction code (ECC) feature supporting:

- single error detection and correction
- double error detection
- readout of the ECC fail address from the ECC register

3.4 Embedded SRAM

STM32G030x6/x8 devices have 8 Kbytes of embedded SRAM with parity. Hardware parity check allows memory data errors to be detected, which contributes to increasing functional safety of applications.

The memory can be read/write-accessed at CPU clock speed, with 0 wait states.

3.5 Boot modes

At startup, the boot pin and boot selector option bit are used to select one of the three boot options:

- boot from User Flash memory
- boot from System memory
- boot from embedded SRAM

The boot pin is shared with a standard GPIO and can be enabled through the boot selector option bit. The boot loader is located in System memory. It manages the Flash memory reprogramming through one of the following interfaces:

- USART on pins PA9/PA10 or PA2/PA3
- I^2C-bus on pins PB6/PB7 or PB10/PB11

3.6 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link time and stored at a given memory location.

3.7 Power supply management

3.7.1 Power supply schemes

The STM32G030x6/x8 devices require a 2.0 V to 3.6 V operating supply voltage (V_{DD}). Several different power supplies are provided to specific peripherals:

- V_{DD} = 2.0 to 3.6 V

  V_{DD} is the external power supply for the internal regulator and the system analog such as reset, power management and internal clocks. It is provided externally through VDD/VDDA pin.
- V_{DDA} = 2.0 V to 3.6 V

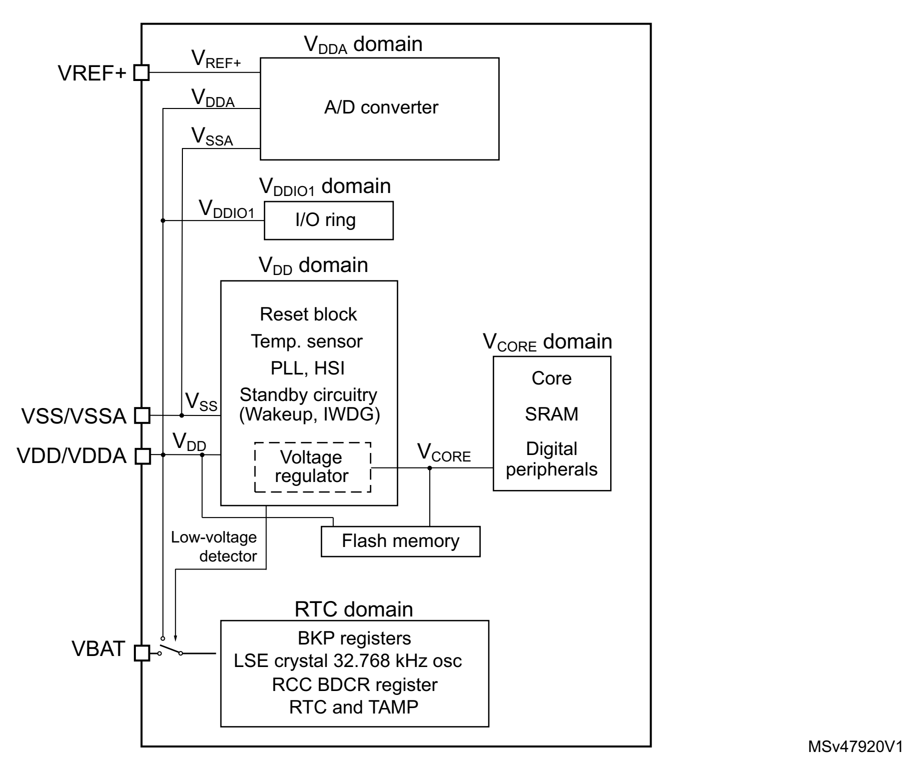
  V_{DDA} is the analog power supply for the A/D converter. V_{DDA} voltage level is identical to V_{DD} voltage as it is provided externally through VDD/VDDA pin.
- $V_{DDIO1} = V_{DD}$

  V_{DDIO1} is the power supply for the I/Os. V_{DDIO1} voltage level is identical to V_{DD} voltage as it is provided externally through VDD/VDDA pin.
- V_{BAT} = 1.55 V to 3.6 V. V_{BAT} is the power supply (through a power switch) for RTC, TAMP, low-speed external 32.768 kHz oscillator and backup registers when V_{DD} is not present. V_{BAT} is provided externally through VBAT pin. When this pin is not available on the package, VBAT bonding pad is internally bonded to the VDD/VDDA pin.
- V_{REF+} is the analog peripheral input reference voltage. When $V_{DDA} < 2$ V, V_{REF+} must be equal to V_{DDA}. When $V_{DDA} \geq 2$ V, V_{REF+} must be between 2 V and V_{DDA}. It can be grounded when the analog peripherals using V_{REF+} are not active.

V_{REF+} is delivered through VREF+ pin. On packages without VREF+ pin, V_{REF+} is internally connected with V_{DD}.

- V_{CORE}
  An embedded linear voltage regulator is used to supply the V_{CORE} internal digital power. V_{CORE} is the power supply for digital peripherals, SRAM and Flash memory. The Flash memory is also supplied with V_{DD}.

Figure 2. Power supply overview



3.7.2 Power supply supervisor

The device has an integrated power-on/power-down (POR/PDR) reset active in all power modes and ensuring proper operation upon power-on and power-down. It maintains the device in reset when the supply voltage is below $V_{POR/PDR}$ threshold, without the need for an external reset circuit.

3.7.3 Voltage regulator

Two embedded linear voltage regulators, main regulator (MR) and low-power regulator (LPR), supply most of digital circuitry in the device.

The MR is used in Run and Sleep modes. The LPR is used in Low-power run, Low-power sleep and Stop modes.

In Standby mode, both regulators are powered down and their outputs set in high-impedance state, such as to bring their current consumption close to zero.

3.7.4 Low-power modes

By default, the microcontroller is in Run mode after system or power reset. It is up to the user to select one of the low-power modes described below:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.
- **Low-power run** mode

  This mode is achieved with V_{CORE} supplied by the low-power regulator to minimize the regulator's operating current. The code can be executed from SRAM or from Flash, and the CPU frequency is limited to 2 MHz. The peripherals with independent clock can be clocked by HSI16.
- **Low-power sleep** mode

  This mode is entered from the low-power run mode. Only the CPU clock is stopped. When wakeup is triggered by an event or an interrupt, the system reverts to the Low-power run mode.
- **Stop 0 and Stop 1** modes

  In Stop 0 and Stop 1 modes, the device achieves the lowest power consumption while retaining the SRAM and register contents. All clocks in the V_{CORE} domain are stopped. The PLL, as well as the HSI16 RC oscillator and the HSE crystal oscillator are disabled. The LSE or LSI keep running. The RTC can remain active (Stop mode with RTC, Stop mode without RTC).

  Some peripherals with wakeup capability can enable the HSI16 RC during Stop mode, so as to get clock for processing the wakeup event. The main regulator remains active in Stop 0 mode while it is turned off in Stop 1 mode.
- **Standby** mode

  The Standby mode is used to achieve the lowest power consumption, with POR/PDR always active in this mode. The main regulator is switched off to power down V_{CORE} domain. The low-power regulator is switched off. The PLL, as well as the HSI16 RC oscillator and the HSE crystal oscillator are also powered down. The RTC can remain active (Standby mode with RTC, Standby mode without RTC).

  For each I/O, the software can determine whether a pull-up, a pull-down or no resistor shall be applied to that I/O during Standby mode.

  Upon entering Standby mode, register contents are lost except for registers in the RTC domain and standby circuitry.

  The device exits Standby mode upon external reset event (NRST pin), IWDG reset event, wakeup event (WKUP pin, configurable rising or falling edge) or RTC event (alarm, periodic wakeup, timestamp, tamper), or when a failure is detected on LSE (CSS on LSE).

3.7.5 Reset mode

During and upon exiting reset, the schmitt triggers of I/Os are disabled so as to reduce power consumption. In addition, when the reset source is internal, the built-in pull-up resistor on NRST pin is deactivated.

3.7.6 VBAT operation

The V_{BAT} power domain, consuming very little energy, includes RTC, and LSE oscillator and backup registers.

In VBAT mode, the RTC domain is supplied from VBAT pin. The power source can be, for example, an external battery or an external supercapacitor. Two anti-tamper detection pins are available.

The RTC domain can also be supplied from VDD/VDDA pin.

By means of a built-in switch, an internal voltage supervisor allows automatic switching of RTC domain powering between V_{DD} and voltage from VBAT pin to ensure that the supply voltage of the RTC domain (V_{BAT}) remains within valid operating conditions. If both voltages are valid, the RTC domain is supplied from VDD/VDDA pin.

An internal circuit for charging the battery on VBAT pin can be activated if the V_{DD} voltage is within a valid range.

Note: External interrupts and RTC alarm/events cannot cause the microcontroller to exit the VBAT mode, as in that mode the V_{DD} *is not within a valid range.*

3.8 Interconnect of peripherals

Several peripherals have direct connections between them. This allows autonomous communication between peripherals, saving CPU resources thus power supply consumption. In addition, these hardware connections allow fast and predictable latency.

Depending on peripherals, these interconnections can operate in Run, Sleep and Stop modes.

Table 4. Interconnect of peripherals

Interconnect source	Interconnect destination	Interconnect action	Run Low-power run	Sleep Low-power sleep	Stop
TIMx	TIMx	Timer synchronization or chaining	Y	Y	-
	ADCx	Conversion triggers	Y	Y	-
	DMA	Memory-to-memory transfer trigger	Y	Y	-
ADCx	TIM1	Timer triggered by analog watchdog	Y	Y	-
RTC	TIM16	Timer input channel from RTC events	Y	Y	-
All clock sources (internal and external)	TIM14,16,17	Clock source used as input channel for RC measurement and trimming	Y	Y	-
CSS RAM (parity error) Flash memory (ECC error)	TIM1,16,17	Timer break	Y	Y	-

Table 4. Interconnect of peripherals (continued)

Interconnect source	Interconnect destination	Interconnect action	Run Low-power run	Sleep Low-power sleep	Stop
CPU (hard fault)	TIM1,16,17	Timer break	Y	-	-
GPIO	TIMx	External trigger	Y	Y	-
	ADC	Conversion external trigger	Y	Y	-

3.9 Clocks and startup

The clock controller distributes the clocks coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness. It features:

- **Clock prescaler:** to get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler
- **Safe clock switching:** clock sources can be changed safely on the fly in run mode through a configuration register.
- **Clock management:** to reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock source:** three different sources can deliver SYSCLK system clock:
  - 4-48 MHz high-speed oscillator with external crystal or ceramic resonator (HSE). It can supply clock to system PLL. The HSE can also be configured in bypass mode for an external clock.
  - 16 MHz high-speed internal RC oscillator (HSI16), trimmable by software. It can supply clock to system PLL.
  - System PLL with maximum output frequency of 64 MHz. It can be fed with HSE or HSI16 clocks.
- **Auxiliary clock source:** two ultra-low-power clock sources for the real-time clock (RTC):
  - 32.768 kHz low-speed oscillator with external crystal (LSE), supporting four drive capability modes. The LSE can also be configured in bypass mode for using an external clock.
  - 32 kHz low-speed internal RC oscillator (LSI) with ±5% accuracy, also used to clock an independent watchdog.
- **Peripheral clock sources:** several peripherals (I2S, USARTs, I2Cs, ADC) have their own clock independent of the system clock.
- **Clock security system (CSS):** in the event of HSE clock failure, the system clock is automatically switched to HSI16 and, if enabled, a software interrupt is generated. LSE

clock failure can also be detected and generate an interrupt. The CCS feature can be enabled by software.

- **Clock output:**
  - **MCO (microcontroller clock output)** provides one of the internal clocks for external use by the application
  - **LSCO (low speed clock output)** provides LSI or LSE in all low-power modes (except in VBAT operation).

Several prescalers allow the application to configure AHB and APB domain clock frequencies, 64 MHz at maximum.

3.10 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function (AF). Most of the GPIO pins are shared with special digital or analog functions.

Through a specific sequence, this special function configuration of I/Os can be locked, such as to avoid spurious writing to I/O control registers.

3.11 Direct memory access controller (DMA)

The direct memory access (DMA) controller is a bus master and system peripheral with single-AHB architecture.

With 5 channels, it performs data transfers between memory-mapped peripherals and/or memories, to offload the CPU.

Each channel is dedicated to managing memory access requests from one or more peripherals. The unit includes an arbiter for handling the priority between DMA requests.

Main features of the DMA controller:

- Single-AHB master
- Peripheral-to-memory, memory-to-peripheral, memory-to-memory and peripheral-to-peripheral data transfers
- Access, as source and destination, to on-chip memory-mapped devices such as Flash memory, SRAM, and AHB and APB peripherals
- All DMA channels independently configurable:
  - Each channel is associated either with a DMA request signal coming from a peripheral, or with a software trigger in memory-to-memory transfers. This configuration is done by software.
  - Priority between the requests is programmable by software (four levels per channel: very high, high, medium, low) and by hardware in case of equality (such as request to channel 1 has priority over request to channel 2).
  - Transfer size of source and destination are independent (byte, half-word, word), emulating packing and unpacking. Source and destination addresses must be aligned on the data size.
  - Support of transfers from/to peripherals to/from memory with circular buffer management

  - Programmable number of data to be transferred: 0 to $2^{16} - 1$
- Generation of an interrupt request per channel. Each interrupt request originates from any of the three DMA events: transfer complete, half transfer, or transfer error.

3.12 DMA request multiplexer (DMAMUX)

The DMAMUX request multiplexer enables routing a DMA request line between the peripherals and the DMA controller. Each channel selects a unique DMA request line, unconditionally or synchronously with events from its DMAMUX synchronization inputs. DMAMUX may also be used as a DMA request generator from programmable events on its input trigger signals.

3.13 Interrupts and events

The device flexibly manages events causing interrupts of linear program execution, called exceptions. The Cortex-M0+ processor core, a nested vectored interrupt controller (NVIC) and an extended interrupt/event controller (EXTI) are the assets contributing to handling the exceptions. Exceptions include core-internal events such as, for example, a division by zero and, core-external events such as logical level changes on physical lines. Exceptions result in interrupting the program flow, executing an interrupt service routine (ISR) then resuming the original program flow.

The processor context (contents of program pointer and status registers) is stacked upon program interrupt and unstacked upon program resume, by hardware. This avoids context stacking and unstacking in the interrupt service routines (ISRs) by software, thus saving time, code and power. The ability to abandon and restart load-multiple and store-multiple operations significantly increases the device's responsiveness in processing exceptions.

3.13.1 Nested vectored interrupt controller (NVIC)

The configurable nested vectored interrupt controller is tightly coupled with the core. It handles physical line events associated with a non-maskable interrupt (NMI) and maskable interrupts, and Cortex-M0+ exceptions. It provides flexible priority management.

The tight coupling of the processor core with NVIC significantly reduces the latency between interrupt events and start of corresponding interrupt service routines (ISRs). The ISR vectors are listed in a vector table, stored in the NVIC at a base address. The vector address of an ISR to execute is hardware-built from the vector table base address and the ISR order number used as offset.

If a higher-priority interrupt event happens while a lower-priority interrupt event occurring just before is waiting for being served, the later-arriving higher-priority interrupt event is served first. Another optimization is called tail-chaining. Upon a return from a higher-priority ISR then start of a pending lower-priority ISR, the unnecessary processor context unstacking and stacking is skipped. This reduces latency and contributes to power efficiency.

Features of the NVIC:

- Low-latency interrupt processing
- 4 priority levels
- Handling of a non-maskable interrupt (NMI)
- Handling of 32 maskable interrupt lines
- Handling of 10 Cortex-M0+ exceptions
- Later-arriving higher-priority interrupt processed first
- Tail-chaining
- Interrupt vector retrieval by hardware

3.13.2 Extended interrupt/event controller (EXTI)

The extended interrupt/event controller adds flexibility in handling physical line events and allows identifying wake-up events at processor wakeup from Stop mode.

The EXTI controller has a number of channels, of which some with rising, falling or rising, and falling edge detector capability. Any GPIO and a few peripheral signals can be connected to these channels.

The channels can be independently masked.

The EXTI controller can capture pulses shorter than the internal clock period.

A register in the EXTI controller latches every event even in Stop mode, which allows the software to identify the origin of the processor's wake-up from Stop mode or, to identify the GPIO and the edge event having caused an interrupt.

3.14 Analog-to-digital converter (ADC)

A native 12-bit analog-to-digital converter is embedded into STM32G030x6/x8 devices. It can be extended to 16-bit resolution through hardware oversampling. The ADC has up to 16 external channels and 3 internal channels (temperature sensor, voltage reference, V_{BAT} monitoring). It performs conversions in single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC frequency is independent from the CPU frequency, allowing maximum sampling rate of ~2 MSps even with a low CPU speed. An auto-shutdown function guarantees that the ADC is powered off except during the active conversion phase.

The ADC can be served by the DMA controller. It can operate in the whole V_{DD} supply range.

The ADC features a hardware oversampler up to 256 samples, improving the resolution to 16 bits (refer to AN2668).

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all scanned channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) can be internally connected to the ADC start triggers, to allow the application to synchronize A/D conversions with timers.

3.14.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{TS} that varies linearly with temperature.

The temperature sensor is internally connected to an ADC input to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor may vary from part to part due to process variation, the uncalibrated internal temperature sensor is suitable only for relative temperature measurements.

To improve the accuracy of the temperature sensor, each part is individually factory-calibrated by ST. The resulting calibration data are stored in the part's engineering bytes, accessible in read-only mode.

Table 5. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at a temperature of 30 °C (± 5 °C), $V_{DDA} = V_{REF+} = 3.0$ V (± 10 mV)	0x1FFF 75A8 - 0x1FFF 75A9

3.14.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC. V_{REFINT} is internally connected to an ADC input. The V_{REFINT} voltage is individually precisely measured for each part by ST during production test and stored in the part's engineering bytes. It is accessible in read-only mode.

Table 6. Internal voltage reference calibration values

Calibration value name	Description	Memory address
V_{REFINT}	Raw data acquired at a temperature of 30 °C (± 5 °C), $V_{DDA} = V_{REF+} = 3.0$ V (± 10 mV)	0x1FFF 75AA - 0x1FFF 75AB

3.14.3 V_{BAT} battery voltage monitoring

This embedded hardware feature allows the application to measure the V_{BAT} battery voltage using an internal ADC input. As the V_{BAT} voltage may be higher than V_{DDA} and thus outside the ADC input range, the VBAT pin is internally connected to a bridge divider by three. As a consequence, the converted digital value is one third the V_{BAT} voltage.

3.15 Timers and watchdogs

The device includes an advanced-control timer, four general-purpose timers, two watchdog timers and a SysTick timer. *Table 7* compares features of the advanced-control, general-purpose and basic timers.

Table 7. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Maximum operating frequency	Prescaler factor	DMA request generation	Capture/ compare channels	Comple-mentary outputs
Advanced-control	TIM1	16-bit	Up, down, up/down	64 MHz	Integer from 1 to 2^{16}	Yes	4	3
General-purpose	TIM3	16-bit	Up, down, up/down	64 MHz	Integer from 1 to 2^{16}	Yes	4	-
	TIM14	16-bit	Up	64 MHz	Integer from 1 to 2^{16}	No	1	-
	TIM16 TIM17	16-bit	Up	64 MHz	Integer from 1 to 2^{16}	Yes	1	1

3.15.1 Advanced-control timer (TIM1)

The advanced-control timer can be seen as a three-phase PWM unit multiplexed on 6 channels. It has complementary PWM outputs with programmable inserted dead-times. It can also be seen as a complete general-purpose timer. The four independent channels can be used for:

- input capture
- output compare
- PWM output (edge or center-aligned modes) with full modulation capability (0-100%)
- one-pulse mode output

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled, so as to turn off any power switches driven by these outputs.

Many features are shared with those of the general-purpose TIMx timers (described in *Section 3.15.2*) using the same architecture, so the advanced-control timers can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

3.15.2 General-purpose timers (TIM3, 14, 16, 17)

There are four synchronizable general-purpose timers embedded in the device (refer to *Table 7* for comparison). Each general-purpose timer can be used to generate PWM outputs or act as a simple timebase.

- TIM3

  This is a full-featured general-purpose timer with 16-bit auto-reload up/downcounter and 16-bit prescaler.

  It has four independent channels for input capture/output compare, PWM or one-pulse mode output. It can operate in combination with other general-purpose timers via the Timer Link feature for synchronization or event chaining. It can generate independent

DMA request and support quadrature encoders. Its counter can be frozen in debug mode.

- TIM14

  This timer is based on a 16-bit auto-reload upcounter and a 16-bit prescaler. It has one channel for input capture/output compare, PWM output or one-pulse mode output. Its counter can be frozen in debug mode.

- TIM16, TIM17

  These are general-purpose timers featuring:

  - 16-bit auto-reload upcounter and 16-bit prescaler
  - 1 channel and 1 complementary channel

  All channels can be used for input capture/output compare, PWM or one-pulse mode output. The timers can operate together via the Timer Link feature for synchronization or event chaining. They can generate independent DMA request. Their counters can be frozen in debug mode.

3.15.3 Independent watchdog (IWDG)

The independent watchdog is based on an 8-bit prescaler and 12-bit downcounter with user-defined refresh window. It is clocked from an independent 32 kHz internal RC (LSI). Independent of the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes. Its counter can be frozen in debug mode.

3.15.4 System window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked by the system clock. It has an early-warning interrupt capability. Its counter can be frozen in debug mode.

3.15.5 SysTick timer

This timer is dedicated to real-time operating systems, but it can also be used as a standard down counter.

Features of SysTick timer:

- 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

3.16 Real-time clock (RTC), tamper (TAMP) and backup registers

The device embeds an RTC and five 32-bit backup registers, located in the RTC domain of the silicon die.

The ways of powering the RTC domain are described in *Section 3.7.6*.

The RTC is an independent BCD timer/counter.

Features of the RTC:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month
- Programmable alarm
- On-the-fly correction from 1 to 32767 RTC clock pulses, usable for synchronization with a master clock
- Reference clock detection - a more precise second-source clock (50 or 60 Hz) can be used to improve the calendar precision
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy
- Two anti-tamper detection pins with programmable filter
- Timestamp feature to save a calendar snapshot, triggered by an event on the timestamp pin or a tamper event, or by switching to VBAT mode
- 17-bit auto-reload wakeup timer (WUT) for periodic events, with programmable resolution and period
- Multiple clock sources and references:
  - A 32.768 kHz external crystal (LSE)
  - An external resonator or oscillator (LSE)
  - The internal low-power RC oscillator (LSI, with typical frequency of 32 kHz)
  - The high-speed external clock (HSE) divided by 32

When clocked by LSE, the RTC operates in VBAT mode and in all low-power modes. When clocked by LSI, the RTC does not operate in VBAT mode, but it does in low-power modes.

All RTC events (Alarm, WakeUp Timer, Timestamp or Tamper) can generate an interrupt and wake the device up from the low-power modes.

The backup registers allow keeping 20 bytes of user application data in the event of V_{DD} failure, if a valid backup supply voltage is provided on VBAT pin. They are not affected by the system reset, power reset, and upon the device’s wakeup from Standby mode.

3.17 Inter-integrated circuit interface (I2C)

The device embeds two I2C peripherals. Refer to *Table 8* for the features.

The I^2C-bus interface handles communication between the microcontroller and the serial I^2C-bus. It controls all I^2C-bus-specific sequencing, protocol, arbitration and timing.

Features of the I2C peripheral:

- I^{2}C-bus specification and user manual rev. 5 compatibility:
  - Slave and master modes, multimaster capability
  - Standard-mode (Sm), with a bitrate up to 100 kbit/s
  - Fast-mode (Fm), with a bitrate up to 400 kbit/s
  - Fast-mode Plus (Fm+), with a bitrate up to 1 Mbit/s and extra output drive I/Os
  - 7-bit and 10-bit addressing mode, multiple 7-bit slave addresses
  - Programmable setup and hold times
  - Clock stretching
- SMBus specification rev 3.0 compatibility:
  - Hardware PEC (packet error checking) generation and verification with ACK control
  - Command and data acknowledge control
  - Address resolution protocol (ARP) support
  - Host and Device support
  - SMBus alert
  - Timeouts and idle condition detection
- PMBus rev 1.3 standard compatibility
- Independent clock: a choice of independent clock sources allowing the I2C communication speed to be independent of the PCLK reprogramming
- Wakeup from Stop mode on address match
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

Table 8. I^{2}C implementation

I^{2}C features[1]	I2C1	I2C2
Standard mode (up to 100 kbit/s)	X	X
Fast mode (up to 400 kbit/s)	X	X
Fast Mode Plus (up to 1 Mbit/s) with extra output drive I/Os	X	X
Programmable analog and digital noise filters	X	X
SMBus/PMBus hardware support	X	-
Independent clock	X	-
Wakeup from Stop mode on address match	X	-

1. X: supported

3.18 Universal synchronous/asynchronous receiver transmitter (USART)

The device embeds universal synchronous/asynchronous receivers/transmitters that communicate at speeds of up to 8 Mbit/s.

They provide hardware management of the CTS, RTS and RS485 DE signals, multiprocessor communication mode, master synchronous communication and single-wire half-duplex communication mode. Some can also support SmartCard communication (ISO 7816), IrDA SIR ENDEC, LIN Master/Slave capability and auto baud rate feature, and have a clock domain independent of the CPU clock, which allows them to wake up the MCU from Stop mode. The wakeup events from Stop mode are programmable and can be:

- start bit detection
- any received data frame
- a specific programmed data frame

All USART interfaces can be served by the DMA controller.

Table 9. USART implementation

USART modes/features[1]	USART1	USART2
Hardware flow control for modem	X	X
Continuous communication using DMA	X	X
Multiprocessor communication	X	X
Synchronous mode	X	X
Smartcard mode	X	-
Single-wire half-duplex communication	X	X
IrDA SIR ENDEC block	X	-
LIN mode	X	-
Dual clock domain and wakeup from Stop mode	X	-
Receiver timeout interrupt	X	-
Modbus communication	X	-
Auto baud rate detection	X	-
Driver Enable	X	X

1. X: supported

3.19 Serial peripheral interface (SPI)

The device contains two SPIs running at up to 32 Mbits/s in master and slave modes. It supports half-duplex, full-duplex and simplex communications. A 3-bit prescaler gives eight master mode frequencies. The frame size is configurable from 4 bits to 16 bits. The SPI peripherals support NSS pulse mode, TI mode and hardware CRC calculation.

The SPI peripherals can be served by the DMA controller.

The I^{2}S interface mode of the SPI peripheral (if supported, see the following table) supports four different audio standards can operate as master or slave, in half-duplex communication mode. It can be configured to transfer 16 and 24 or 32 bits with 16-bit or 32-bit data resolution and synchronized by a specific signal. Audio sampling frequency from 8 kHz up to 192 kHz can be set by an 8-bit programmable linear prescaler. When operating in master mode, it can output a clock for an external audio component at 256 times the sampling frequency.

Table 10. SPI/I2S implementation

SPI features(1)	SPI1	SPI2
Hardware CRC calculation	X	X
Rx/Tx FIFO	X	X
NSS pulse mode	X	X
I^2S mode	X	-
TI mode	X	X

1. X = supported.

3.20 Development support

3.20.1 Serial wire debug port (SW-DP)

An Arm SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.

4 Pinouts, pin description and alternate functions

Figure 3. STM32G030CxT LQFP48 pinout

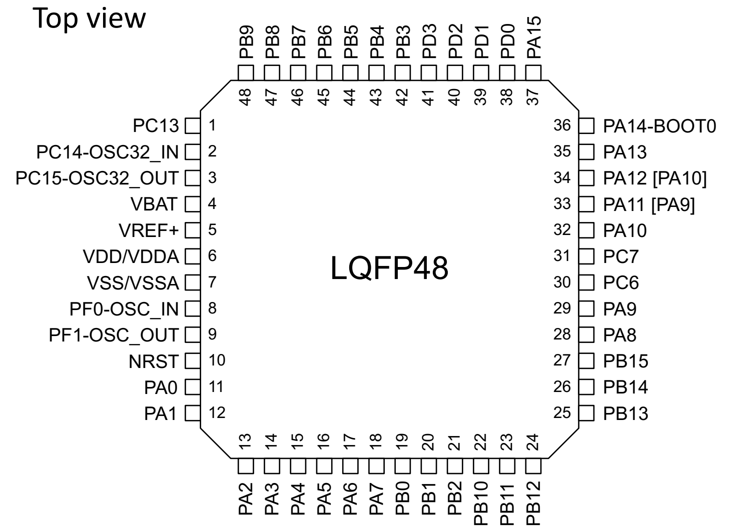


Figure 4. STM32G030KxT LQFP32 pinout

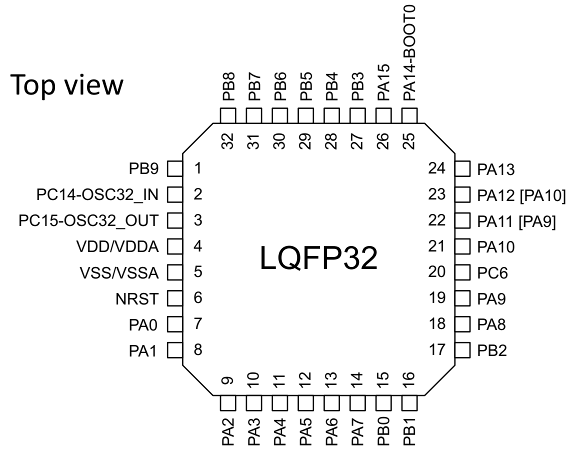


Figure 5. STM32G030Fx TSSOP20 pinout

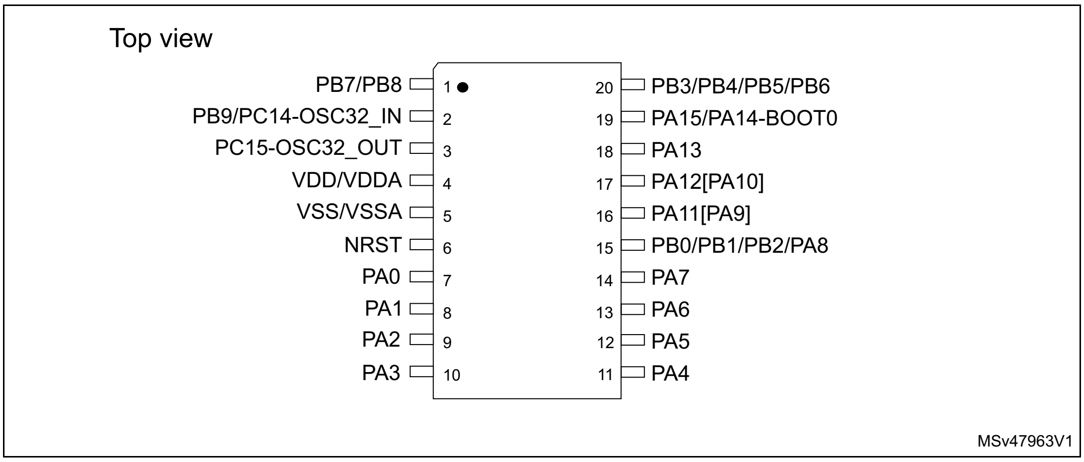


Figure 6. STM32G030Jx SO8N pinout

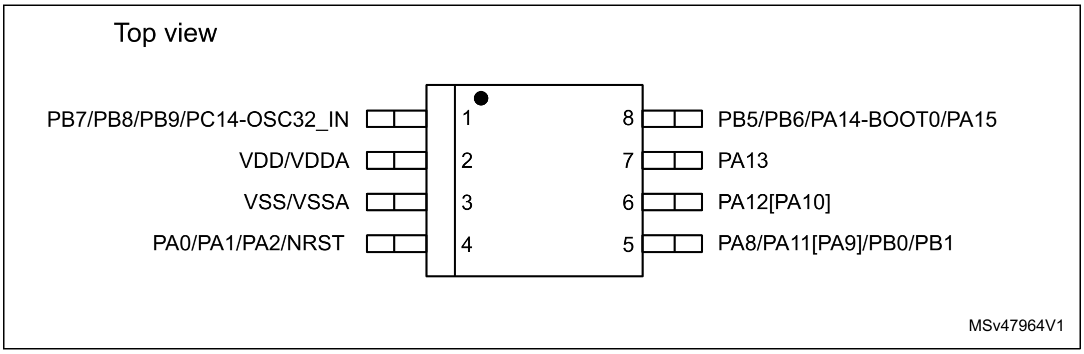


Table 11. Terms and symbols used in *Table 12*

Column	Symbol	Definition
Pin name	Terminal name corresponds to its by-default function at reset, unless otherwise specified in parenthesis under the pin name.	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input / output pin
I/O structure	FT	5 V tolerant I/O
	RST	Bidirectional reset pin with embedded weak pull-up resistor
	Options for FT I/Os	
	_f	I/O, Fm+ capable
	_a	I/O, with analog switch function
	_e	I/O, with switchable diode to V_{DDIOx}
Note	Upon reset, all I/Os are set as analog inputs, unless otherwise specified.	

Table 11. Terms and symbols used in *Table 12* (continued)

Column		Symbol	Definition
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

Table 12. Pin assignment and description

Pin				Pin name (function upon reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
SO8N	TSSOP20	LQFP32	LQFP48						
-	-	-	1	PC13	I/O	FT	(1)(2)	TIM1_BK	TAMP_IN1, RTC_TS, RTC_OUT1, WKUP2
-	-	-	2	PC14-OSC32_IN (PC14)	I/O	FT	(1)(2)	TIM1_BK2	OSC32_IN
1	2	2	-	PC14-OSC32_IN (PC14)	I/O	FT	(1)(2)	TIM1_BK2	OSC32_IN, OSC_IN
-	3	3	3	PC15-OSC32_OUT (PC15)	I/O	FT	(1)(2)	OSC32_EN, OSC_EN	OSC32_OUT
-	-	-	4	VBAT	S	-	-	-	VBAT
-	-	-	5	VREF+	S	-	-	-	-
2	4	4	6	VDD/VDDA	S	-	-	-	-
3	5	5	7	VSS/VSSA	S	-	-	-	-
-	-	-	8	PF0-OSC_IN (PF0)	I/O	FT	-	TIM14_CH1	OSC_IN
-	-	-	9	PF1-OSC_OUT (PF1)	I/O	FT	-	OSC_EN	OSC_OUT
4	6	6	10	NRST	I/O	FT	-	-	NRST
4	7	7	11	PA0	I/O	FT_a	(3)	SPI2_SCK, USART2_CTS,	ADC_IN0, TAMP_IN2,WKUP1
4	8	8	12	PA1	I/O	FT_ea	(3)	SPI1_SCK/I2S1_CK, USART2_RTS_DE_CK, I2C1_SMBA, EVENTOUT	ADC_IN1

Table 12. Pin assignment and description (continued)

Pin				Pin name (function upon reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
SO8N	TSSOP20	LQFP32	LQFP48						
4	9	9	13	PA2	I/O	FT_a	(3)	SPI1_MOSI/I2S1_SD, USART2_TX,	ADC_IN2, WKUP4,LSCO
-	10	10	14	PA3	I/O	FT_ea	-	SPI2_MISO, USART2_RX, EVENTOUT	ADC_IN3
-	-	-	15	PA4	I/O	FT_a	-	SPI1_NSS/I2S1_WS, SPI2_MOSI, TIM14_CH1, EVENTOUT	ADC_IN4, RTC_OUT2
-	11	11	-	PA4	I/O	FT_a	-	SPI1_NSS/I2S1_WS, SPI2_MOSI, TIM14_CH1, EVENTOUT	ADC_IN4, TAMP_IN1, RTC_TS, RTC_OUT1, WKUP2
-	12	12	16	PA5	I/O	FT_ea	-	SPI1_SCK/I2S1_CK, EVENTOUT	ADC_IN5
-	13	13	17	PA6	I/O	FT_ea	-	SPI1_MISO/I2S1_MCK, TIM3_CH1, TIM1_BK, TIM16_CH1	ADC_IN6
-	14	14	18	PA7	I/O	FT_a	-	SPI1_MOSI/I2S1_SD, TIM3_CH2, TIM1_CH1N, TIM14_CH1, TIM17_CH1	ADC_IN7
5	15	15	19	PB0	I/O	FT_ea	-	SPI1_NSS/I2S1_WS, TIM3_CH3, TIM1_CH2N	ADC_IN8
5	15	16	20	PB1	I/O	FT_ea	-	TIM14_CH1, TIM3_CH4, TIM1_CH3N, EVENTOUT	ADC_IN9
-	15	17	21	PB2	I/O	FT_ea	-	SPI2_MISO, EVENTOUT	ADC_IN10
-	-	-	22	PB10	I/O	FT_fa	-	SPI2_SCK, I2C2_SCL	ADC_IN11
-	-	-	23	PB11	I/O	FT_fa	-	SPI2_MOSI, I2C2_SDA	ADC_IN15
-	-	-	24	PB12	I/O	FT_a	-	SPI2_NSS, TIM1_BK, EVENTOUT	ADC_IN16
-	-	-	25	PB13	I/O	FT_f	-	SPI2_SCK, TIM1_CH1N, I2C2_SCL, EVENTOUT	-
-	-	-	26	PB14	I/O	FT_f	-	SPI2_MISO, TIM1_CH2N, I2C2_SDA, EVENTOUT	-
-	-	-	27	PB15	I/O	FT	-	SPI2_MOSI, TIM1_CH3N, EVENTOUT	RTC_REFIN
5	15	18	28	PA8	I/O	FT	-	MCO, SPI2_NSS, TIM1_CH1, EVENTOUT	-

Table 12. Pin assignment and description (continued)

Pin				Pin name (function upon reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
SO8N	TSSOP20	LQFP32	LQFP48						
-	-	19	29	PA9	I/O	FT_f	-	MCO, USART1_TX, TIM1_CH2, SPI2_MISO, I2C1_SCL, EVENTOUT	-
-	-	20	30	PC6	I/O	FT	-	TIM3_CH1	-
-	-	-	31	PC7	I/O	FT	-	TIM3_CH2	-
-	-	21	32	PA10	I/O	FT_f	-	SPI2_MOSI, USART1_RX, TIM1_CH3, TIM17_BK, I2C1_SDA, EVENTOUT	-
-	-	-	33	PA11 [PA9]	I/O	FT_f	(4)	SPI1_MISO/I2S1_MCK, USART1_CTS, TIM1_CH4, TIM1_BK2, I2C2_SCL	-
5	16	22	-	PA11 [PA9]	I/O	FT_fa	(4)	SPI1_MISO/I2S1_MCK, USART1_CTS, TIM1_CH4, TIM1_BK2, I2C2_SCL	ADC_IN15
-	-	-	34	PA12 [PA10]	I/O	FT_f	(4)	SPI1_MOSI/I2S1_SD, USART1_RTS_DE_CK, TIM1_ETR, I2S_CKIN, I2C2_SDA	-
6	17	23	-	PA12 [PA10]	I/O	FT_fa	(4)	SPI1_MOSI/I2S1_SD, USART1_RTS_DE_CK, TIM1_ETR, I2S_CKIN, I2C2_SDA	ADC_IN16
7	18	24	35	PA13	I/O	FT_ea	(5)	SWDIO, IR_OUT, EVENTOUT	ADC_IN17
8	19	25	36	PA14-BOOT0	I/O	FT_a	(5)	SWCLK, USART2_TX, EVENTOUT	ADC_IN18, BOOT0
8	19	26	37	PA15	I/O	FT	-	SPI1_NSS/I2S1_WS, USART2_RX, EVENTOUT	-
-	-	-	38	PD0	I/O	FT	-	EVENTOUT, SPI2_NSS, TIM16_CH1	-
-	-	-	39	PD1	I/O	FT	-	EVENTOUT, SPI2_SCK, TIM17_CH1	-
-	-	-	40	PD2	I/O	FT	-	TIM3_ETR, TIM1_CH1N	-
-	-	-	41	PD3	I/O	FT	-	USART2_CTS, SPI2_MISO, TIM1_CH2N	-

Table 12. Pin assignment and description (continued)

Pin				Pin name (function upon reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
SO8N	TSSOP20	LQFP32	LQFP48						
-	20	27	42	PB3	I/O	FT	-	SPI1_SCK/I2S1_CK, TIM1_CH2, USART1_RTS_DE_CK, EVENTOUT	-
-	20	28	43	PB4	I/O	FT	-	SPI1_MISO/I2S1_MCK, TIM3_CH1, USART1_CTS, TIM17_BK, EVENTOUT	-
8	20	29	44	PB5	I/O	FT	-	SPI1_MOSI/I2S1_SD, TIM3_CH2, TIM16_BK, I2C1_SMBA	WKUP6
8	20	30	45	PB6	I/O	FT_f	-	USART1_TX, TIM1_CH3, TIM16_CH1N, SPI2_MISO, I2C1_SCL, EVENTOUT	-
-	-	-	46	PB7	I/O	FT_f	-	USART1_RX, SPI2_MOSI, TIM17_CH1N, I2C1_SDA, EVENTOUT	-
1	1	31	-	PB7	I/O	FT_fa	-	USART1_RX, SPI2_MOSI, TIM17_CH1N, I2C1_SDA, EVENTOUT	ADC_IN11
1	1	32	47	PB8	I/O	FT_f	-	SPI2_SCK, TIM16_CH1, I2C1_SCL, EVENTOUT	-
1	2	1	48	PB9	I/O	FT_f	-	IR_OUT, TIM17_CH1, SPI2_NSS, I2C1_SDA, EVENTOUT	-

1. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF
   - These GPIOs must not be used as current sources (for example to drive a LED).
2. After an RTC domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the RTC registers. The RTC registers are not reset upon system reset. For details on how to manage these GPIOs, refer to the RTC domain and RTC register descriptions in the RM0444 reference manual.
3. As in SO8N device, the PA0, PA1, and PA2 GPIOs are bonded with NRST on the pin 4, low level applied to any of these GPIOs provokes the device reset. To prevent the risk of spurious resets, keep these GPIOs configured at all times as analog or digital inputs (as opposed to output or alternate function).
4. Pins PA9 and PA10 can be remapped in place of pins PA11 and PA12 (default mapping), using SYSCFG_CFGR1 register.
5. Upon reset, these pins are configured as SW debug alternate functions, and the internal pull-up on PA13 pin and the internal pull-down on PA14 pin are activated.

Table 13. Port A alternate function mapping

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0	SPI2_SCK	USART2_CTS	-	-	-	-	-	-
PA1	SPI1_SCK/I2S1_CK	USART2_RTS_DE_CK	-	-	-	-	I2C1_SMBA	EVENTOUT
PA2	SPI1_MOSI/I2S1_SD	USART2_TX	-	-	-	-	-	-
PA3	SPI2_MISO	USART2_RX	-	-	-	-	-	EVENTOUT
PA4	SPI1_NSS/I2S1_WS	SPI2_MOSI	-	-	TIM14_CH1	-	-	EVENTOUT
PA5	SPI1_SCK/I2S1_CK	-	-	-	-	-	-	EVENTOUT
PA6	SPI1_MISO/I2S1_MCK	TIM3_CH1	TIM1_BKIN	-	-	TIM16_CH1	-	-
PA7	SPI1_MOSI/I2S1_SD	TIM3_CH2	TIM1_CH1N	-	TIM14_CH1	TIM17_CH1	-	-
PA8	MCO	SPI2_NSS	TIM1_CH1	-	-	-	-	EVENTOUT
PA9	MCO	USART1_TX	TIM1_CH2	-	SPI2_MISO	-	I2C1_SCL	EVENTOUT
PA10	SPI2_MOSI	USART1_RX	TIM1_CH3	-	-	TIM17_BKIN	I2C1_SDA	EVENTOUT
PA11	SPI1_MISO/I2S1_MCK	USART1_CTS	TIM1_CH4	-	-	TIM1_BKIN2	I2C2_SCL	-
PA12	SPI1_MOSI/I2S1_SD	USART1_RTS_DE_CK	TIM1_ETR	-	-	I2S_CKIN	I2C2_SDA	-
PA13	SWDIO	IR_OUT	-	-	-	-	-	EVENTOUT
PA14	SWCLK	USART2_TX	-	-	-	-	-	EVENTOUT
PA15	SPI1_NSS/I2S1_WS	USART2_RX	-	-	-	-	-	EVENTOUT

Table 14. Port B alternate function mapping

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB0	SPI1_NSS/ I2S1_WS	TIM3_CH3	TIM1_CH2N	-	-	-	-	-
PB1	TIM14_CH1	TIM3_CH4	TIM1_CH3N	-	-	-	-	EVENTOUT
PB2	-	SPI2_MISO	-	-	-	-	-	EVENTOUT
PB3	SPI1_SCK/ I2S1_CK	TIM1_CH2	-	-	USART1_RTS _DE_CK	-	-	EVENTOUT
PB4	SPI1_MISO/ I2S1_MCK	TIM3_CH1	-	-	USART1_CTS	TIM17_BKIN	-	EVENTOUT
PB5	SPI1_MOSI/ I2S1_SD	TIM3_CH2	TIM16_BKIN	-	-	-	I2C1_SMBA	-
PB6	USART1_TX	TIM1_CH3	TIM16_CH1N	-	SPI2_MISO	-	I2C1_SCL	EVENTOUT
PB7	USART1_RX	SPI2_MOSI	TIM17_CH1N	-	-	-	I2C1_SDA	EVENTOUT
PB8	-	SPI2_SCK	TIM16_CH1	-	-	-	I2C1_SCL	EVENTOUT
PB9	IR_OUT	-	TIM17_CH1	-	-	SPI2_NSS	I2C1_SDA	EVENTOUT
PB10	-	-	-	-	-	SPI2_SCK	I2C2_SCL	-
PB11	SPI2_MOSI	-	-	-	-	-	I2C2_SDA	-
PB12	SPI2_NSS	-	TIM1_BKIN	-	-	-	-	EVENTOUT
PB13	SPI2_SCK	-	TIM1_CH1N	-	-	-	I2C2_SCL	EVENTOUT
PB14	SPI2_MISO	-	TIM1_CH2N	-	-	-	I2C2_SDA	EVENTOUT
PB15	SPI2_MOSI	-	TIM1_CH3N	-	-	-	-	EVENTOUT

Table 15. Port C alternate function mapping

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PC6	-	TIM3_CH1	-	-	-	-	-	-
PC7	-	TIM3_CH2	-	-	-	-	-	-
PC13	-	-	TIM1_BKIN	-	-	-	-	-
PC14	-	-	TIM1_BKIN2	-	-	-	-	-
PC15	OSC32_EN	OSC_EN	-	-	-	-	-	-

Table 16. Port D alternate function mapping

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PD0	EVENTOUT	SPI2_NSS	TIM16_CH1	-	-	-	-	-
PD1	EVENTOUT	SPI2_SCK	TIM17_CH1	-	-	-	-	-
PD2	-	TIM3_ETR	TIM1_CH1N	-	-	-	-	-
PD3	USART2_CTS	SPI2_MISO	TIM1_CH2N	-	-	-	-	-

Table 17. Port F alternate function mapping

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PF0	-	-	TIM14_CH1	-	-	-	-	-
PF1	OSC_EN	-	-	-	-	-	-	-

5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

Parameter values defined at temperatures or in temperature ranges out of the ordering information scope are to be ignored.

Packages used for characterizing certain electrical parameters may differ from the commercial packages as per the ordering information.

5.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and $T_A = T_A(\text{max})$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3σ).

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, $V_{DD} = V_{DDA}$ = 3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ±2σ).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 7*.

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 8*.

Figure 7. Pin loading conditions

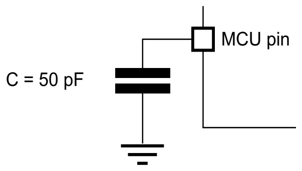
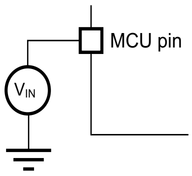
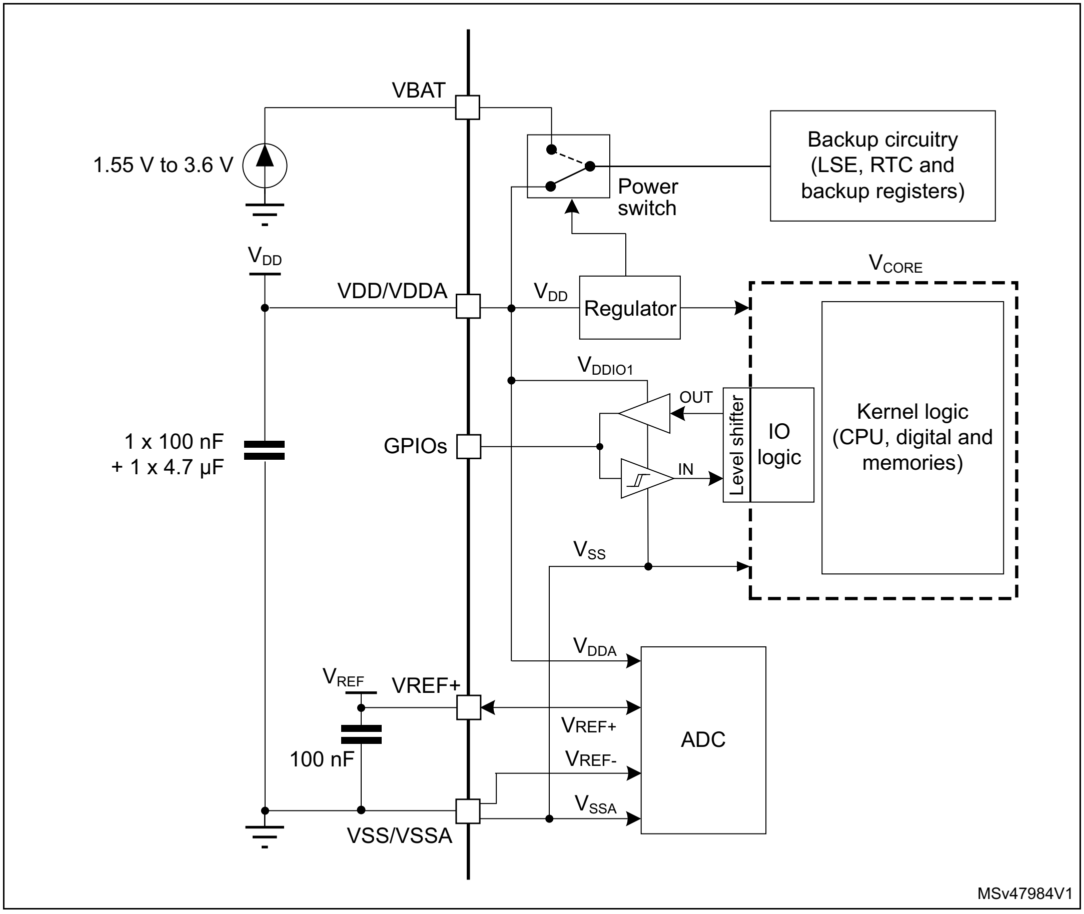


Figure 8. Pin input voltage



5.1.6 Power supply scheme

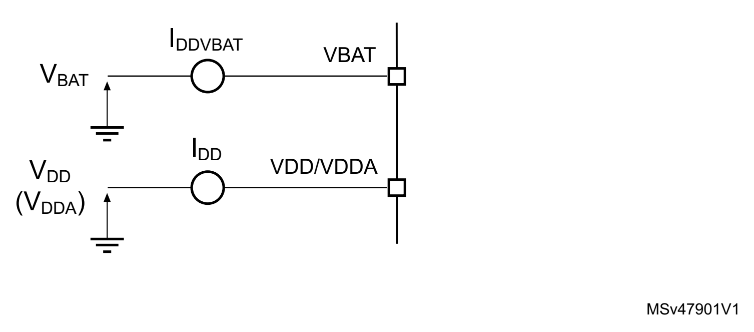
Figure 9. Power supply scheme



Caution: Power supply pin pair (VDD/VDDA and VSS/VSSA) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

5.1.7 Current consumption measurement

Figure 10. Current consumption measurement scheme



5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 18*, *Table 19* and *Table 20* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

All voltages are defined with respect to V_{SS}.

Table 18. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD}	External supply voltage	- 0.3	4.0	V
V_{BAT}	External supply voltage on VBAT pin	- 0.3	4.0	
V_{REF+}	External voltage on VREF+ pin	- 0.3	Min(V_{DD} + 0.4, 4.0)	
V_{IN}(1)	Input voltage on FT_xx	- 0.3	V_{DD} + 4.0(2)	
	Input voltage on any other pin	- 0.3	4.0	

1. Refer to *Table 19* for the maximum allowed injected current values.
2. To sustain a voltage higher than 4 V the internal pull-up/pull-down resistors must be disabled.

Table 19. Current characteristics

Symbol	Ratings	Max	Unit
$I_{VDD/VDDA}$	Current into VDD/VDDA power pin (source)(1)	100	mA
$I_{VSS/VSSA}$	Current out of VSS/VSSA ground pin (sink)(1)	100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin except FT_f	15	
	Output current sunk by any FT_f pin	20	
	Output current sourced by any I/O and control pin	15	
$\sum I_{IO(PIN)}$	Total output current sunk by sum of all I/Os and control pins	80	
	Total output current sourced by sum of all I/Os and control pins	80	
$I_{INJ(PIN)}$(2)	Injected current on a FT_xx pin	-5 / NA(3)	
$\sum\|I_{INJ(PIN)}\|$	Total injected current (sum of all I/Os and control pins)(4)	25	

1. All main power (VDD/VDDA, VBAT) and ground (VSS/VSSA) pins must always be connected to the external power supplies, in the permitted range.
2. A positive injection is induced by $V_{IN} > V_{DDIOx}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer also to *Table 18: Voltage characteristics* for the maximum allowed input voltage values.
3. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. When several inputs are submitted to a current injection, the maximum $\sum|I_{INJ(PIN)}|$ is the absolute sum of the negative injected currents (instantaneous values).

Table 20. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

5.3 Operating conditions

5.3.1 General operating conditions

Table 21. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	64	MHz
f_{PCLK}	Internal APB clock frequency	-	0	64	
$V_{DD/DDA}$	Supply voltage	-	2.0[1]	3.6	V
V_{BAT}	Backup operating voltage	-	1.55	3.6	V
V_{IN}	I/O input voltage	-	-0.3	Min(V_{DD} + 3.6, 5.5)[2]	V
T_A	Ambient temperature[3]	-	-40	85	°C
T_J	Junction temperature	-	-40	105	°C

1. When RESET is released functionality is guaranteed down to V_{PDR} min.
2. For operation with voltage higher than V_{DD} +0.3 V, the internal pull-up and pull-down resistors must be disabled.
3. The T_A(max) applies to P_D(max). At $P_D < P_D$(max) the ambient temperature is allowed to go higher than T_A(max) provided that the junction temperature T_J does not exceed T_J(max). Refer to *Section 6.5: Thermal characteristics*.

5.3.2 Operating conditions at power-up / power-down

The parameters given in *Table 22* are derived from tests performed under the ambient temperature condition summarized in *Table 21*.

Table 22. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} slew rate	V_{DD} rising	-	∞	µs/V
		V_{DD} falling	10	∞	

5.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 23* are derived from tests performed under the ambient temperature conditions summarized in *Table 21*.

Table 23. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
$t_{RSTTEMPO}$[2]	POR temporization when V_{DD} crosses V_{POR}	V_{DD} rising	-	250	400	µs
V_{POR}[2]	Power-on reset threshold	-	2.06	2.10	2.14	V
V_{PDR}[2]	Power-down reset threshold	-	1.960	2.00	2.04	V
$V_{hyst\_POR\_PDR}$	Hysteresis of V_{POR} and V_{PDR}	Hysteresis in continuous mode	-	20	-	mV
		Hysteresis in other mode	-	30	-	

1. Continuous mode means Run/Sleep modes, or temperature sensor enable in Low-power run/Low-power sleep modes.
2. Guaranteed by design.

5.3.4 Embedded voltage reference

The parameters given in *Table 24* are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 21: General operating conditions*.

Table 24. Embedded internal voltage reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	-40°C < T_J < 105°C	1.182	1.212	1.232	V
$t_{S\_vrefint}$ (1)	ADC sampling time when reading the internal reference voltage	-	4(2)	-	-	µs
$t_{start\_vrefint}$	Start time of reference voltage buffer when ADC is enable	-	-	8	12(2)	µs
$I_{DD(VREFINTBUF)}$	V_{REFINT} buffer consumption from V_{DD} when converted by ADC	-	-	12.5	20(2)	µA
ΔV_{REFINT}	Internal reference voltage spread over the temperature range	V_{DD} = 3 V	-	5	7.5(2)	mV
$T_{Coeff\_vrefint}$	Temperature coefficient	-	-	30	50(2)	ppm/°C
A_{Coeff}	Long term stability	1000 hours, T = 25 °C	-	300	1000(2)	ppm
$V_{DDCoeff}$	Voltage coefficient	3.0 V < V_{DD} < 3.6 V	-	250	1200(2)	ppm/V
V_{REFINT_DIV1}	1/4 reference voltage	-	24	25	26	% V_{REFINT}
V_{REFINT_DIV2}	1/2 reference voltage		49	50	51	
V_{REFINT_DIV3}	3/4 reference voltage		74	75	76	

1. The shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design.

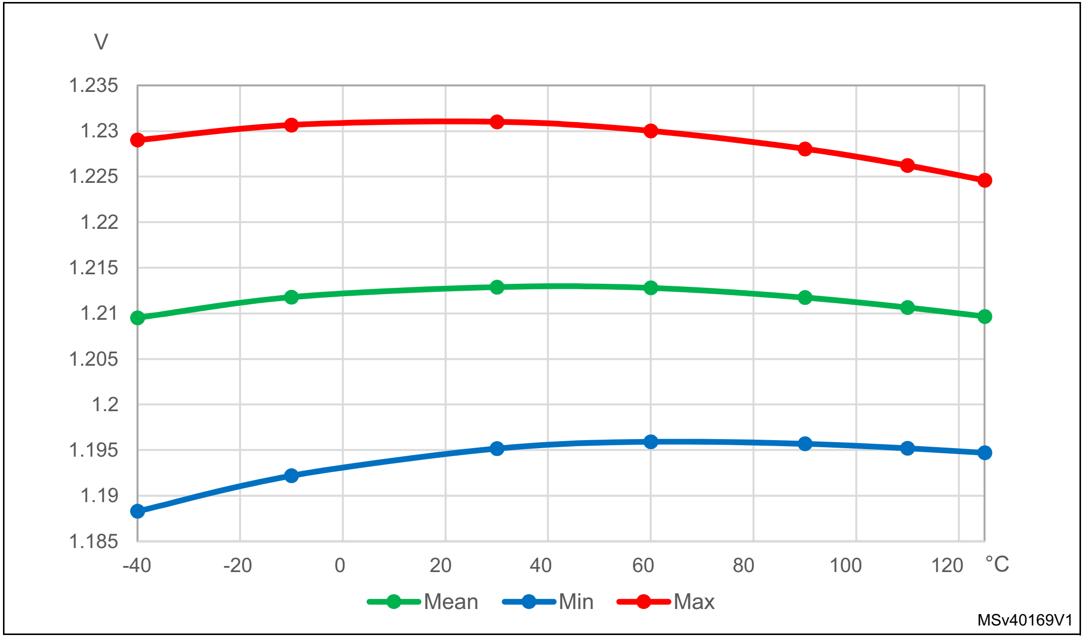


Figure 11. V_{REFINT} vs. temperature

5.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in *Figure 10: Current consumption measurement scheme*.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted with the minimum wait states number, depending on the f_{HCLK} frequency (refer to the table “Number of wait states according to CPU clock (HCLK) frequency” available in the RM0454 reference manual).
- When the peripherals are enabled $f_{PCLK} = f_{HCLK}$
- For Flash memory and shared peripherals $f_{PCLK} = f_{HCLK} = f_{HCLKS}$

Unless otherwise stated, values given in *Table 25* through *Table 31* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 21: General operating conditions*.

Table 25. Current consumption in Run and Low-power run modes at different die temperatures

Symbol	Parameter	Conditions			Typ		Max[1]		Unit
		General	f_{HCLK}	Fetch from[2]	25°C	85°C	25°C	85°C	
$I_{DD(Run)}$	Supply current in Run mode	Range 1; PLL enabled; f_{HCLK} = f_{HSI} bypass (≤16 MHz), f_{HCLK} = $f_{PLLRCLK}$ (>16 MHz); (3)	64 MHz	Flash memory	5.7	5.9	8.0	8.3	mA
			56 MHz		5.1	5.2	7.1	7.1	
			48 MHz		4.6	4.7	5.7	6.0	
			32 MHz		3.2	3.3	4.6	4.9	
			24 MHz		2.5	2.6	3.5	3.8	
			16 MHz		1.6	1.7	2.5	2.9	
			64 MHz	SRAM	4.7	4.8	7.2	7.5	
			56 MHz		4.2	4.3	6.5	6.7	
			48 MHz		3.7	3.9	5.7	6.0	
			32 MHz		2.6	2.7	4.1	4.3	
			24 MHz		2.0	2.1	3.2	3.5	
			16 MHz		1.3	1.3	2.3	2.4	
		Range 2; PLL enabled; f_{HCLK} = f_{HSI} bypass (≤16 MHz), f_{HCLK} = $f_{PLLRCLK}$ (>16 MHz); (3)	16 MHz	Flash memory	1.3	1.3	2.0	2.3	
			8 MHz		0.7	0.8	1.4	1.5	
			2 MHz		0.3	0.3	0.6	0.9	
			16 MHz	SRAM	1.1	1.1	1.9	2.1	
			8 MHz		0.6	0.6	1.2	1.4	
			2 MHz		0.2	0.3	0.6	0.9	
$I_{DD(LPRun)}$	Supply current in Low-power run mode	PLL disabled; f_{HCLK} = f_{HSE} bypass (> 32 kHz), f_{HCLK} = f_{LSE} bypass (= 32 kHz); (3)	2 MHz	Flash memory	182	226	570	790	µA
			1 MHz		99	132	480	700	
			500 kHz		58	89	430	630	
			125 kHz		25	56	370	600	
			32 kHz		17	47	330	480	
			2 MHz	SRAM	161	191	550	800	
			1 MHz		91	114	470	750	
			500 kHz		48	81	410	710	
			125 kHz		21	51	360	500	
			32 kHz		15	37	310	400	

1. Based on characterization results, not tested in production.
2. Prefetch and cache enabled when fetching from Flash. Code compiled with high optimization for space in SRAM.
3. V_{DD} = 3.0 V for values in Typ columns and 3.6 V for values in Max columns, all peripherals disabled, cache enabled, prefetch disabled for code and data fetch from Flash and enabled from SRAM

Table 26. Current consumption in Sleep and Low-power sleep modes

Symbol	Parameter	Conditions			Typ		Max[1]		Unit
		General	Voltage scaling	f_{HCLK}	25°C	85°C	25°C	85°C	
$I_{DD(Sleep)}$	Supply current in Sleep mode	Flash memory enabled; f_{HCLK} = f_{HSE} bypass (≤16 MHz; PLL disabled), f_{HCLK} = $f_{PLLRCLK}$ (>16 MHz; PLL enabled); All peripherals disabled	Range 1	64 MHz	1.4	1.5	2.2	2.4	mA
				56 MHz	1.3	1.4	1.9	2.1	
				48 MHz	1.2	1.2	1.9	1.9	
				32 MHz	0.9	0.9	1.4	1.5	
				24 MHz	0.7	0.8	1.1	1.3	
				16 MHz	0.4	0.4	0.7	0.8	
			Range 2	16 MHz	0.3	0.4	0.6	0.7	
				8 MHz	0.2	0.3	0.3	0.6	
				2 MHz	0.1	0.2	0.2	0.5	
$I_{DD(LPSleep)}$	Supply current in Low-power sleep mode	Flash memory disabled; PLL disabled; f_{HCLK} = f_{HSE} bypass (> 32 kHz), f_{HCLK} = f_{LSE} bypass (= 32 kHz); All peripherals disabled		2 MHz	43	77	175	410	µA
				1 MHz	29	60	150	375	
				500 kHz	23	52	145	285	
				125 kHz	16	46	130	270	
				32 kHz	13	44	125	260	

1. Based on characterization results, not tested in production.

Table 27. Current consumption in Stop 0 mode

Symbol	Parameter	Conditions		Typ		Max[1]		Unit
		V_{DD}		25°C	85°C	25°C	85°C	
$I_{DD(Stop\ 0)}$	Supply current in Stop 0 mode	HSI kernel ON	2.4 V	290	320	395	540	µA
			3 V	295	325	415	580	
			3.6 V	295	325	445	595	
		HSI kernel OFF	2.4 V	105	145	145	265	
			3 V	105	150	150	285	
			3.6 V	110	150	150	295	

1. Based on characterization results, not tested in production.

Table 28. Current consumption in Stop 1 mode

Symbol	Parameter	Conditions			Typ		Max(1)		Unit
			RTC	V_{DD}	25°C	85°C	25°C	85°C	
$I_{DD(Stop\ 1)}$	Supply current in Stop 1 mode	Flash memory not powered	Disabled	2.4 V	3.4	28	17	130	µA
				3 V	3.6	28	22	140	
				3.6 V	3.9	29	28	155	
			Enabled (clocked by LSE bypass)	2.4 V	3.9	28	22	140	
				3 V	4.1	29	23	155	
				3.6 V	4.6	29	28	160	

1. Based on characterization results, not tested in production.

Table 29. Current consumption in Standby mode

Symbol	Parameter	Conditions		Typ		Max(1)		Unit
		General	V_{DD}	25°C	85°C	25°C	85°C	
$I_{DD(Standby)}$	Supply current in Standby mode	RTC disabled	2.4 V	1.0	1.8	2.1	14	µA
			3.0 V	1.2	2.1	2.7	16	
			3.6 V	1.4	2.5	3.0	19	
		RTC enabled, clocked by LSI	2.4 V	1.3	2.1	2.2	17	
			3.0 V	1.7	2.5	2.9	19	
			3.6 V	2.1	3.0	3.8	19	

1. Based on characterization results, not tested in production.

Table 30. Current consumption in VBAT mode

Symbol	Parameter	Conditions		Typ		Unit
		RTC	V_{BAT}	25°C	85°C	
I_{DD_VBAT}	Supply current in VBAT mode	Enabled, clocked by LSE bypass at 32.768 kHz	2.4 V	270	360	nA
			3.0 V	360	460	
			3.6 V	470	600	
		Enabled, clocked by LSE crystal at 32.768 kHz	2.4 V	410	440	
			3.0 V	510	530	
			3.6 V	630	770	

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 48: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption measured previously (see *Table 31: Current consumption of peripherals*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the I/O supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DDIO1} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DDIO1} is the I/O supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$

C_S is the PCB board capacitance including the pad pin.

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in the following table. The MCU is placed under the following conditions:

- All I/O pins are in Analog mode
- The given value is calculated by measuring the difference of the current consumptions:
  - when the peripheral is clocked on
  - when the peripheral is clocked off
- Ambient operating temperature and supply voltage conditions summarized in *Table 18: Voltage characteristics*
- The power consumption of the digital part of the on-chip peripherals is given in the following table. The power consumption of the analog part of the peripherals (where applicable) is indicated in each related section of the datasheet.

Table 31. Current consumption of peripherals

Peripheral	Bus	Consumption in µA/MHz		
		Range 1	Range 2	Low-power run and sleep
IOPORT Bus	IOPORT	0.5	0.4	0.3
GPIOA	IOPORT	3.1	2.4	3.0
GPIOB	IOPORT	2.9	2.3	3.0
GPIOC	IOPORT	0.9	0.8	1.0
GPIOD	IOPORT	0.7	0.6	1.0
GPIOF	IOPORT	0.5	0.5	1.0
Bus matrix	AHB	3.2	2.2	2.8
All AHB Peripherals	AHB	9.8	8.2	8.5
DMA1/DMAMUX	AHB	3.4	2.9	3.0
CRC	AHB	0.5	0.4	0.5
FLASH	AHB	4.3	3.6	3.5
All APB peripherals	APB	23.5	20.0	20.5
AHB to APB bridge(1)	APB	0.2	0.2	0.1
PWR	APB	0.4	0.3	0.5
SYSCFG	APB	0.4	0.4	0.5
WWDG	APB	0.2	0.3	0.5
TIM1	APB	7.0	5.9	6.5
TIM3	APB	3.6	3.1	3.5
TIM14	APB	1.5	1.3	1.5
TIM16	APB	2.3	2.0	2.5
TIM17	APB	1.0	0.8	0.3
I2C1	APB	3.2	2.7	3.0
I2C2	APB	0.7	0.6	1.0
SPI1	APB	2.2	1.8	2.0
SPI2	APB	1.3	1.1	1.5
USART1	APB	6.6	5.6	6.0
USART2	APB	1.8	1.5	2.0
ADC	APB	1.6	1.5	1.5

1. The AHB to APB Bridge is automatically active when at least one peripheral is ON on the APB.

5.3.6 Wakeup time from low-power modes and voltage scaling transition times

The wakeup times given in *Table 32* are the latency between the event and the execution of the first user instruction.

Table 32. Low-power mode wakeup times(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WUSLEEP}$	Wakeup time from Sleep to Run mode	-	11	11	CPU cycles
$t_{WULPSLEEP}$	Wakeup time from Low-power sleep mode	Transiting to Low-power-run-mode execution in Flash memory not powered in Low-power sleep mode; HCLK = HSI16 / 8 = 2 MHz	11	14	
$t_{WUSTOP0}$	Wakeup time from Stop 0	Transiting to Run-mode execution in Flash memory not powered in Stop 0 mode; HCLK = HSI16 = 16 MHz; Regulator in Range 1 or Range 2	5.6	6	µs
		Transiting to Run-mode execution in SRAM or in Flash memory powered in Stop 0 mode; HCLK = HSI16 = 16 MHz; Regulator in Range 1 or Range 2	2	2.4	
$t_{WUSTOP1}$	Wakeup time from Stop 1	Transiting to Run-mode execution in Flash memory not powered in Stop 1 mode; HCLK = HSI16 = 16 MHz; Regulator in Range 1 or Range 2	9.0	11.2	µs
		Transiting to Run-mode execution in SRAM or in Flash memory powered in Stop 1 mode; HCLK = HSI16 = 16 MHz; Regulator in Range 1 or Range 2	5	7.5	
		Transiting to Low-power-run-mode execution in Flash memory not powered in Stop 1 mode; HCLK = HSI16/8 = 2 MHz; Regulator in low-power mode (LPR = 1 in PWR_CR1)	22	25.3	
		Transiting to Low-power-run-mode execution in SRAM or in Flash memory powered in Stop 1 mode; HCLK = HSI16 / 8 = 2 MHz; Regulator in low-power mode (LPR = 1 in PWR_CR1)	18	23.5	
t_{WUSTBY}	Wakeup time from Standby mode	Transiting to Run mode; HCLK = HSI16 = 16 MHz; Regulator in Range 1	14.5	30	µs
$t_{WULPRUN}$	Wakeup time from Low-power run mode(2)	Transiting to Run mode; HSISYS = HSI16/8 = 2 MHz	5	7	µs

1. Based on characterization results, not tested in production.
2. Time until REGLPF flag is cleared in PWR_SR2.

Table 33. Regulator mode transition times[(1)]

Symbol	Parameter	Conditions	Typ	Max	Unit
t_{VOST}	Transition times between regulator Range 1 and Range 2[(2)]	HSISYS = HSI16	20	40	µs

1. Based on characterization results, not tested in production.
2. Time until VOSF flag is cleared in PWR_SR2.

5.3.7 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.

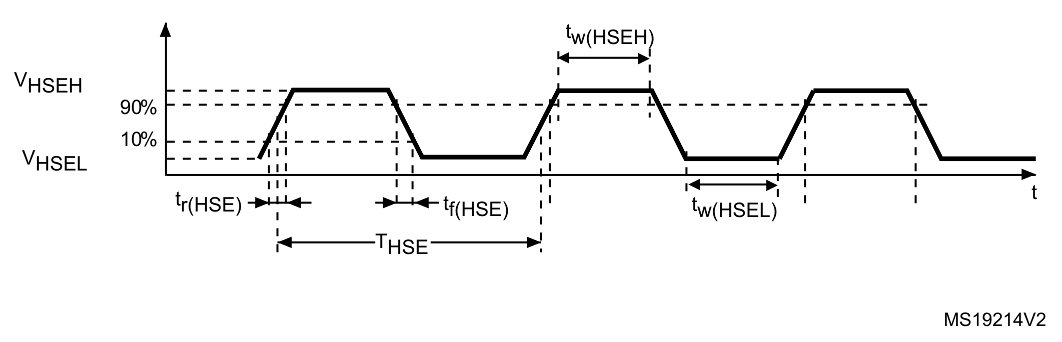
The external clock signal has to respect the I/O characteristics in *Section 5.3.14*. See *Figure 12* for recommended clock input waveform.

Table 34. High-speed external user clock characteristics[(1)]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	Voltage scaling Range 1	-	8	48	MHz
		Voltage scaling Range 2	-	8	26	
V_{HSEH}	OSC_IN input pin high level voltage	-	0.7 V_{DDIO1}	-	V_{DDIO1}	V
V_{HSEL}	OSC_IN input pin low level voltage	-	V_{SS}	-	0.3 V_{DDIO1}	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time	Voltage scaling Range 1	7	-	-	ns
		Voltage scaling Range 2	18	-	-	

1. Guaranteed by design.

Figure 12. High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO.

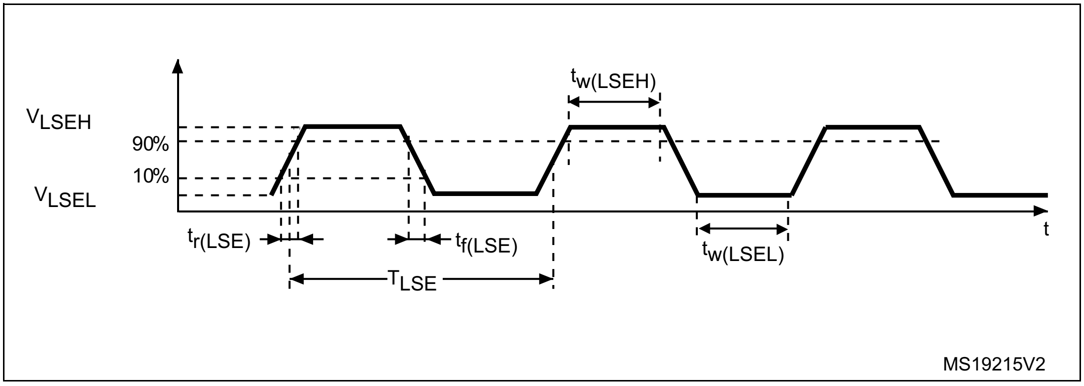
The external clock signal has to respect the I/O characteristics in *Section 5.3.14*. See *Figure 13* for recommended clock input waveform.

Table 35. Low-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	-	0.7 V_{DDIO1}	-	V_{DDIO1}	V
V_{LSEL}	OSC32_IN input pin low level voltage	-	V_{SS}	-	0.3 V_{DDIO1}	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time	-	250	-	-	ns

1. Guaranteed by design.

Figure 13. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 48 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 36*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 36. HSE oscillator characteristics(1)

Symbol	Parameter	Conditions(2)	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	48	MHz
R_F	Feedback resistor	-	-	200	-	kΩ

Table 36. HSE oscillator characteristics[1] (continued)

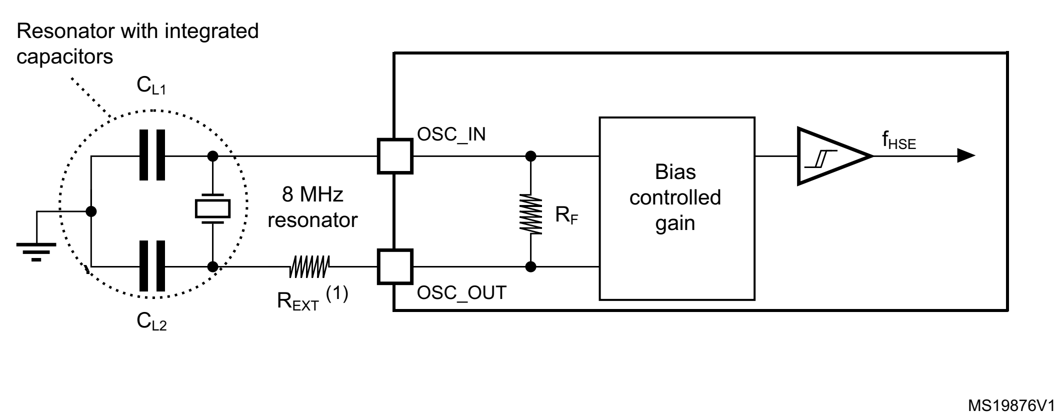
Symbol	Parameter	Conditions[2]	Min	Typ	Max	Unit
$I_{DD(HSE)}$	HSE current consumption	During startup[3]	-	-	5.5	mA
		V_{DD} = 3 V, Rm = 30 Ω, CL = 10 pF@8 MHz	-	0.58	-	
		V_{DD} = 3 V, Rm = 45 Ω, CL = 10 pF@8 MHz	-	0.59	-	
		V_{DD} = 3 V, Rm = 30 Ω, CL = 5 pF@48 MHz	-	0.89	-	
		V_{DD} = 3 V, Rm = 30 Ω, CL = 10 pF@48 MHz	-	1.14	-	
		V_{DD} = 3 V, Rm = 30 Ω, CL = 20 pF@48 MHz	-	1.94	-	
G_m	Maximum critical crystal transconductance	Startup	-	-	1.5	mA/V
$t_{SU(HSE)}$[4]	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Guaranteed by design.
2. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 20 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 14*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 14. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 37*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 37. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)(1)

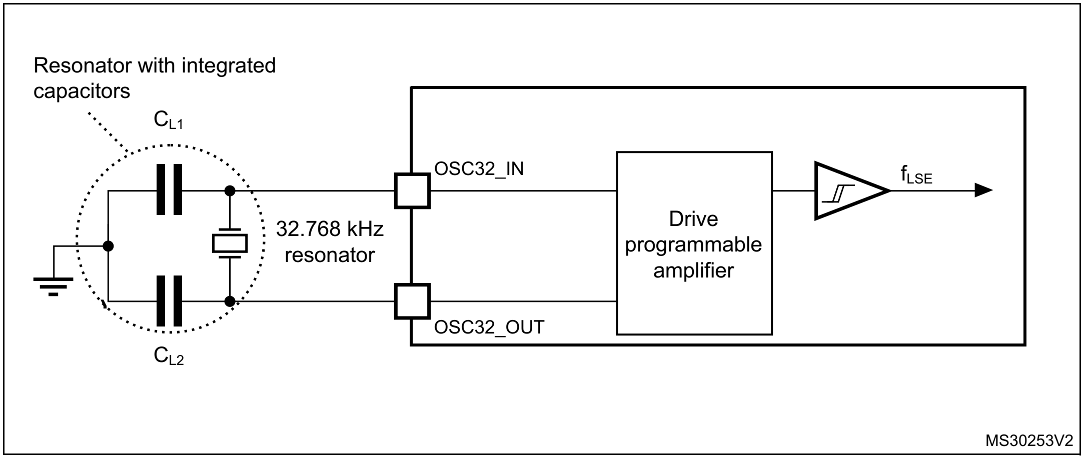
Symbol	Parameter	Conditions(2)	Min	Typ	Max	Unit
$I_{DD(LSE)}$	LSE current consumption	LSEDRV[1:0] = 00 Low drive capability	-	250	-	nA
		LSEDRV[1:0] = 01 Medium low drive capability	-	315	-	
		LSEDRV[1:0] = 10 Medium high drive capability	-	500	-	
		LSEDRV[1:0] = 11 High drive capability	-	630	-	
$Gm_{critmax}$	Maximum critical crystal gm	LSEDRV[1:0] = 00 Low drive capability	-	-	0.5	µA/V
		LSEDRV[1:0] = 01 Medium low drive capability	-	-	0.75	
		LSEDRV[1:0] = 10 Medium high drive capability	-	-	1.7	
		LSEDRV[1:0] = 11 High drive capability	-	-	2.7	
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	-	2	-	s

1. Guaranteed by design.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.

3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 15. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

5.3.8 Internal clock source characteristics

The parameters given in *Table 38* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 21: General operating conditions*. The provided curves are characterization results, not tested in production.

High-speed internal (HSI16) RC oscillator

Table 38. HSI16 oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI16}	HSI16 Frequency	V_{DD}=3.0 V, T_A=30 °C	15.88	-	16.08	MHz
$\Delta_{Temp(HSI16)}$	HSI16 oscillator frequency drift over temperature	T_A= 0 to 85 °C	-1	-	1	%
		T_A= -40 to 85 °C	-2	-	1.5	%
$\Delta_{VDD(HSI16)}$	HSI16 oscillator frequency drift over V_{DD}	V_{DD}=V_{DD}(min) to 3.6 V	-0.1	-	0.05	%
TRIM	HSI16 frequency user trimming step	From code 127 to 128	-8	-6	-4	%
		From code 63 to 64 From code 191 to 192	-5.8	-3.8	-1.8	
		For all other code increments	0.2	0.3	0.4	
D_{HSI16}(2)	Duty Cycle	-	45	-	55	%
$t_{su(HSI16)}$(2)	HSI16 oscillator start-up time	-	-	0.8	1.2	μs

Table 38. HSI16 oscillator characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{stab(HSI16)}$(2)	HSI16 oscillator stabilization time	-	-	3	5	µs
$I_{DD(HSI16)}$(2)	HSI16 oscillator power consumption	-	-	155	190	µA

1. Based on characterization results, not tested in production.
2. Guaranteed by design.

Low-speed internal (LSI) RC oscillator

Table 39. LSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	LSI frequency	V_{DD} = 3.0 V, T_A = 30 °C	31.04	-	32.96	kHz
		V_{DD} = V_{DD}(min) to 3.6 V, T_A = -40 to 85 °C	29.5	-	34	
$t_{SU(LSI)}$(2)	LSI oscillator start-up time	-	-	80	130	µs
$t_{STAB(LSI)}$(2)	LSI oscillator stabilization time	5% of final frequency	-	125	180	µs
$I_{DD(LSI)}$(2)	LSI oscillator power consumption	-	-	110	180	nA

1. Based on characterization results, not tested in production.
2. Guaranteed by design.

5.3.9 PLL characteristics

The parameters given in *Table 40* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 21: General operating conditions*.

Table 40. PLL characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock frequency(2)	-	2.66	-	16	MHz
D_{PLL_IN}	PLL input clock duty cycle	-	45	-	55	%
$f_{PLL\_P\_OUT}$	PLL multiplier output clock P	Voltage scaling Range 1	3.09	-	122	MHz
		Voltage scaling Range 2	3.09	-	40	
$f_{PLL\_R\_OUT}$	PLL multiplier output clock R	Voltage scaling Range 1	12	-	64	MHz
		Voltage scaling Range 2	12	-	16	
f_{VCO_OUT}	PLL VCO output	Voltage scaling Range 1	96	-	344	MHz
		Voltage scaling Range 2	96	-	128	
t_{LOCK}	PLL lock time	-	-	15	40	µs
Jitter	RMS cycle-to-cycle jitter	System clock 56 MHz	-	50	-	±ps
	RMS period jitter		-	40	-	

Table 40. PLL characteristics[1] (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DD(PLL)}$	PLL power consumption on V_{DD}[1]	VCO freq = 96 MHz	-	200	260	μA
		VCO freq = 192 MHz	-	300	380	
		VCO freq = 344 MHz	-	520	650	

1. Guaranteed by design.
2. Make sure to use the appropriate division factor M to obtain the specified PLL input clock values.

5.3.10 Flash memory characteristics

Table 41. Flash memory characteristics[1]

Symbol	Parameter	Conditions	Typ	Max	Unit
t_{prog}	64-bit programming time	-	85	125	μs
t_{prog_row}	Row (32 double word) programming time	Normal programming	2.7	4.6	ms
		Fast programming	1.7	2.8	
t_{prog_page}	Page (2 Kbyte) programming time	Normal programming	21.8	36.6	
		Fast programming	13.7	22.4	
t_{ERASE}	Page (2 Kbyte) erase time	-	22.0	40.0	
t_{prog_bank}	Bank (64 Kbyte[2]) programming time	Normal programming	0.7	1.2	s
		Fast programming	0.4	0.7	
t_{ME}	Mass erase time	-	22.1	40.1	ms
$I_{DD(FlashA)}$	Average consumption from V_{DD}	Programming	3	-	mA
		Page erase	3	-	
		Mass erase	5	-	
$I_{DD(FlashP)}$	Maximum current (peak)	Programming, 2 μs peak duration	7	-	mA
		Erase, 41 μs peak duration	7	-	

1. Guaranteed by design.
2. Values provided also apply to devices with less Flash memory than one 64 Kbyte bank

Table 42. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Min[1]	Unit
N_{END}	Endurance	T_A = -40 to +85 °C	1	kcycles
t_{RET}	Data retention	1 kcycle[2] at T_A = 85 °C	15	Years

1. Guaranteed by characterization results.
2. Cycling performed over the whole temperature range.

5.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 43*. They are based on the EMS levels and classes defined in application note AN1709.

Table 43. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 64 MHz, LQFP48, conforming to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 64 MHz, LQFP48, conforming to IEC 61000-4-4	5A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- corrupted program counter
- unexpected reset
- critical data corruption (for example control registers)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 44. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]	Unit
				8 MHz / 64 MHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = 25 °C, LQFP64 package compliant with IEC 61967-2	0.1 MHz to 30 MHz	-4	dBµV
			30 MHz to 130 MHz	1	
			130 MHz to 1 GHz	3	
			1 GHz to 2 GHz	8	
			EMI level	2.5	-

5.3.12 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/JEDEC standard.

Table 45. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to ANSI/ESDA/JEDEC JS-001	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to ANSI/ESDA/JEDEC JS-002	C2a	500	

1. Based on characterization results, not tested in production.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current is injected to each input, output and configurable I/O pin.

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 46. Electrical sensitivity

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +85 °C conforming to JESD78	II Level A

5.3.13 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DDIO1} (for standard, 3.3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out-of-range parameter: ADC error above a certain limit (higher than 5 LSB TUE), induced leakage current on adjacent pins out of conventional limits (-5 µA/+0 µA range) or other functional failure (for example reset occurrence or oscillator frequency deviation).

Negative induced leakage current is caused by negative injection and positive induced leakage current is caused by positive injection.

Table 47. I/O current injection susceptibility(1)

Symbol	Description		Functional susceptibility		Unit
			Negative injection	Positive injection	
I_{INJ}	Injected current on pin	All except PA1, PA3, PA5, PA6, PA13, PB0, PB1, PB2, and PB8	-5	N/A	mA
		PA1, PA5, PA13, PB1, PB2	0	+5 / N/A(2)	
		PA3, PA6, PB0	-5	+5 / N/A(2)	
		PB8	0	N/A	

1. Based on characterization results, not tested in production.
2. The injection current value is applicable when the switchable diode is activated, N/A when not activated.

5.3.14 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 48* are derived from tests performed under the conditions summarized in *Table 21: General operating conditions*. All I/Os are designed as CMOS- and TTL-compliant.

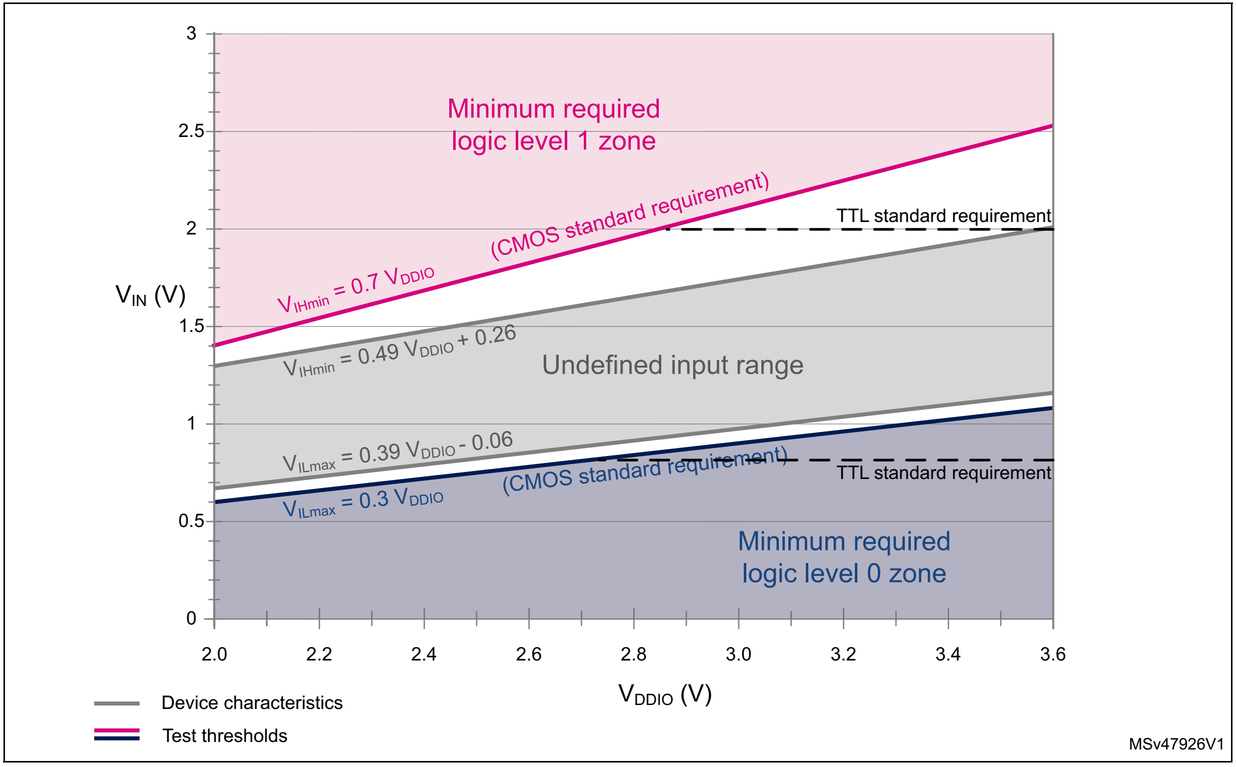
Table 48. I/O static characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IL}(1)	I/O input low level voltage	All	$V_{DD}(min) < V_{DDIO1} < 3.6$ V	-	-	0.3 x V_{DDIO1} (2)	V
						0.39 x V_{DDIO1} - 0.06 (3)	
V_{IH}(1)	I/O input high level voltage	All	$V_{DD}(min) < V_{DDIO1} < 3.6$ V	0.7 x V_{DDIO1}(2)	-	-	V
				0.49 x V_{DDIO1} + 0.26(3)	-	-	
V_{hys}(3)	I/O input hysteresis	FT_xx, NRST	$V_{DD}(min) < V_{DDIO1} < 3.6$ V	-	200	-	mV
I_{lkg}	Input leakage current(3)	All except FT_e	$0 < V_{IN} \leq V_{DDIO1}$	-	-	±70	nA
			$V_{DDIO1} \leq V_{IN} \leq V_{DDIO1}+1$ V	-	-	600(4)	
			$V_{DDIO1} +1$ V $< V_{IN} \leq$ 5.5 V(3)	-	-	150(4)	
		FT_e (5)	$0 < V_{IN} < V_{DDIO1}$	-	-	5	μA
R_{PU}	Weak pull-up equivalent resistor (6)	$V_{IN} = V_{SS}$		25	40	55	kΩ
R_{PD}	Weak pull-down equivalent resistor(6)	$V_{IN} = V_{DDIO1}$		25	40	55	kΩ
C_{IO}	I/O pin capacitance	-		-	5	-	pF

1. Refer to *Figure 16: I/O input characteristics*.
2. Tested in production.
3. Guaranteed by design.
4. This value represents the pad leakage of the I/O itself. The total product pad leakage is provided by this formula: $I_{Total\_Ileak\_max}$ = 10 μA + [number of I/Os where V_{IN} is applied on the pad] x I_{lkg}(Max).
5. FT_e with diode enabled. Input leakage current of FT_e I/Os with the diode disabled is the same as standard I/Os.
6. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters, as shown in *Figure 16*.

Figure 16. I/O input characteristics



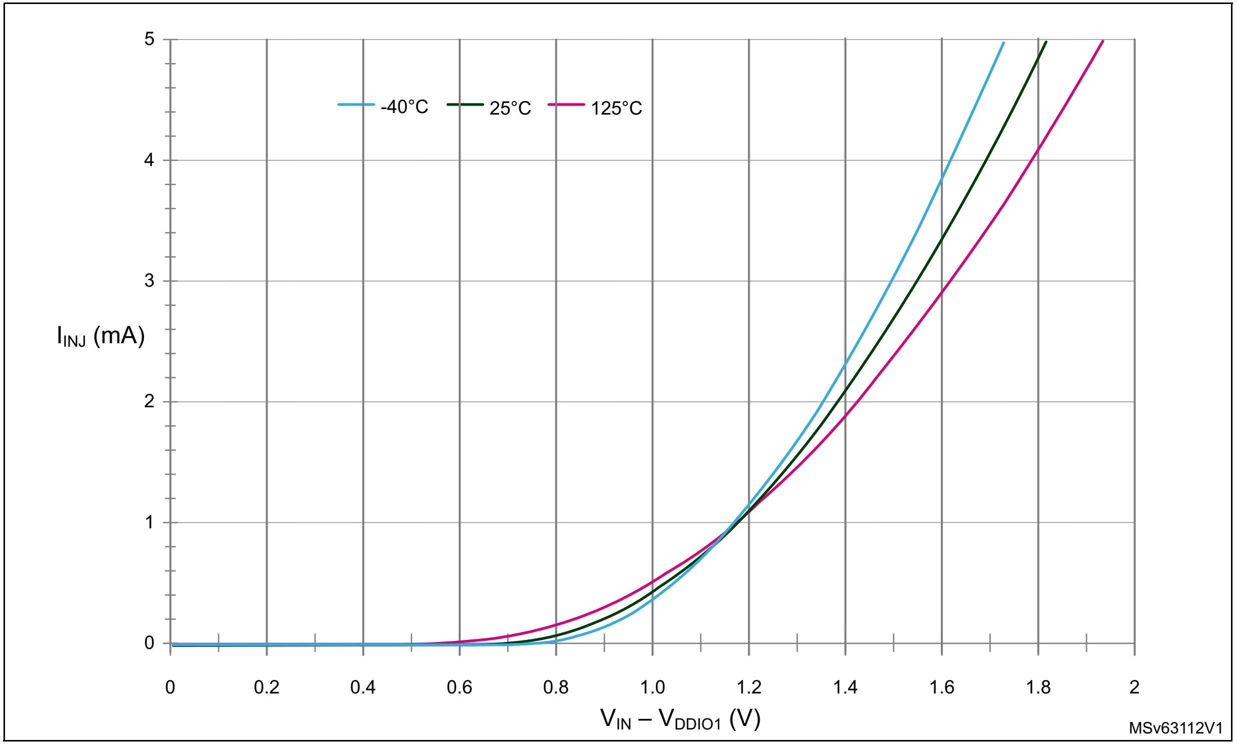
Characteristics of FT_e I/Os

The following table and figure specify input characteristics of FT_e I/Os.

Table 49. Input characteristics of FT_e I/Os

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{INJ}	Injected current on pin	-	-	-	5	mA
V_{DDIO1}-V_{IN}	Voltage over V_{DDIO1}	I_{INJ} = 5 mA	-	-	2	V
R_d	Diode dynamic serial resistor	I_{INJ} = 5 mA	-	-	300	Ω

Figure 17. Current injection into FT_e input with diode active



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±6 mA, and up to ±15 mA with relaxed V_{OL}/V_{OH}.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 5.2*:

- The sum of the currents sourced by all the I/Os on V_{DDIO1}, plus the maximum consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating I_{VDD} (see *Table 18: Voltage characteristics*).
- The sum of the currents sunk by all the I/Os on V_{SS}, plus the maximum consumption of the MCU sunk on V_{SS}, cannot exceed the absolute maximum rating I_{VSS} (see *Table 18: Voltage characteristics*).

Output voltage levels

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 21: General operating conditions*. All I/Os are CMOS- and TTL-compliant (FT OR TT unless otherwise specified).

Table 50. Output voltage characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level voltage for an I/O pin	CMOS port(2) $\|I_{IO}\|$ 6 mA $V_{DDIO1} \geq 2.7$ V	-	0.4	V
V_{OH}	Output high level voltage for an I/O pin		V_{DDIO1} - 0.4	-	
V_{OL}(3)	Output low level voltage for an I/O pin	TTL port(2) $\|I_{IO}\| = 6$ mA $V_{DDIO1} \geq 2.7$ V	-	0.4	
V_{OH}(3)	Output high level voltage for an I/O pin		2.4	-	
V_{OL}(3)	Output low level voltage for an I/O pin	All I/Os $\|I_{IO}\| = 15$ mA $V_{DDIO1} \geq 2.7$ V	-	1.3	
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DDIO1} - 1.3	-	
V_{OL}(3)	Output low level voltage for an I/O pin	$\|I_{IO}\| = 3$ mAV_{DDIO1}	-	0.4	
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DDIO1} - 0.45	-	
V_{OLFM+}(3)	Output low level voltage for an FT I/O pin in FM+ mode (FT I/O with _f option)	$\|I_{IO}\| = 20$ mA $V_{DDIO1} \geq 2.7$ V	-	0.4	
		$\|I_{IO}\| = 9$ mAV_{DDIO1}	-	0.4	

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 18: Voltage characteristics*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣI_{IO}.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Guaranteed by design.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 18* and *Table 51*, respectively.

Unless otherwise specified, the parameters given are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 21: General operating conditions*.

Table 51. I/O AC characteristics(1)(2)

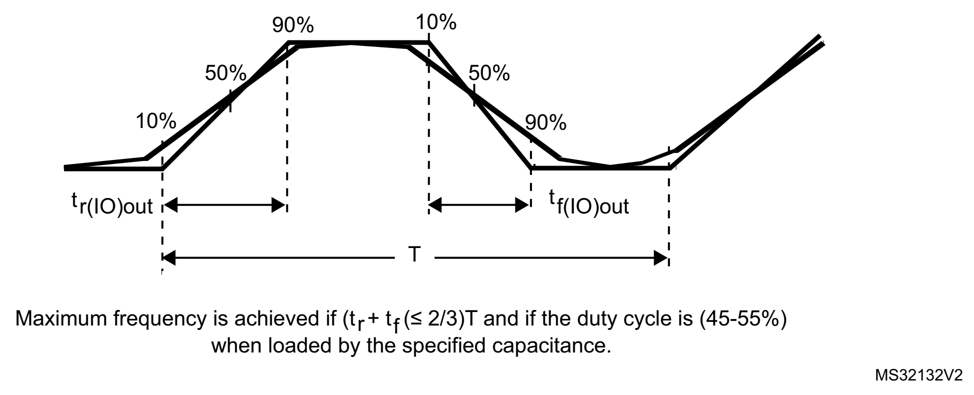
Speed	Symbol	Parameter	Conditions	Min	Max	Unit
00	Fmax	Maximum frequency	C=50 pF, 2.7 V ≤ V_{DDIO1} ≤ 3.6 V	-	2	MHz
			C=50 pF, 2.0 V ≤ V_{DDIO1} ≤ 2.7 V	-	0.35	
			C=10 pF, 2.7 V ≤ V_{DDIO1} ≤ 3.6 V	-	3	
			C=10 pF, 2.0 V ≤ V_{DDIO1} ≤ 2.7 V	-	0.45	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V ≤ V_{DDIO1} ≤ 3.6 V	-	100	ns
			C=50 pF, 2.0 V ≤ V_{DDIO1} ≤ 2.7 V	-	225	
			C=10 pF, 2.7 V ≤ V_{DDIO1} ≤ 3.6 V	-	75	
			C=10 pF, 2.0 V ≤ V_{DDIO1} ≤ 2.7 V	-	150	

Table 51. I/O AC characteristics[1][2] (continued)

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
01	Fmax	Maximum frequency	C=50 pF, 2.7 V ≤ V_{DDIO1} ≤ 3.6 V	-	10	MHz
			C=50 pF, 1.6 V ≤ V_{DDIO1} ≤ 2.7 V	-	2	
			C=10 pF, 2.7 V ≤ V_{DDIO1} ≤ 3.6 V	-	15	
			C=10 pF, 1.6 V ≤ V_{DDIO1} ≤ 2.7 V	-	2.5	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V ≤ V_{DDIO1} ≤ 3.6 V	-	30	ns
			C=50 pF, 1.6 V ≤ V_{DDIO1} ≤ 2.7 V	-	60	
			C=10 pF, 2.7 V ≤ V_{DDIO1} ≤ 3.6 V	-	15	
			C=10 pF, 1.6 V ≤ V_{DDIO1} ≤ 2.7 V	-	30	
10	Fmax	Maximum frequency	C=50 pF, 2.7 V ≤ V_{DDIO1} ≤ 3.6 V	-	30	MHz
			C=50 pF, 1.6 V ≤ V_{DDIO1} ≤ 2.7 V	-	15	
			C=10 pF, 2.7 V ≤ V_{DDIO1} ≤ 3.6 V	-	60	
			C=10 pF, 1.6 V ≤ V_{DDIO1} ≤ 2.7 V	-	30	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V ≤ V_{DDIO1} ≤ 3.6 V	-	11	ns
			C=50 pF, 1.6 V ≤ V_{DDIO1} ≤ 2.7 V	-	22	
			C=10 pF, 2.7 V ≤ V_{DDIO1} ≤ 3.6 V	-	4	
			C=10 pF, 1.6 V ≤ V_{DDIO1} ≤ 2.7 V	-	8	
11	Fmax	Maximum frequency	C=30 pF, 2.7 V ≤ V_{DDIO1} ≤ 3.6 V	-	60	MHz
			C=30 pF, 1.6 V ≤ V_{DDIO1} ≤ 2.7 V	-	30	
			C=10 pF, 2.7 V ≤ V_{DDIO1} ≤ 3.6 V	-	80[3]	
			C=10 pF, 1.6 V ≤ V_{DDIO1} ≤ 2.7 V	-	40	
	Tr/Tf	Output rise and fall time	C=30 pF, 2.7 V ≤ V_{DDIO1} ≤ 3.6 V	-	5.5	ns
			C=30 pF, 1.6 V ≤ V_{DDIO1} ≤ 2.7 V	-	11	
			C=10 pF, 2.7 V ≤ V_{DDIO1} ≤ 3.6 V	-	2.5	
			C=10 pF, 1.6 V ≤ V_{DDIO1} ≤ 2.7 V	-	5	
Fm+	Fmax	Maximum frequency	C=50 pF, 1.6 V ≤ V_{DDIO1} ≤ 3.6 V	-	1	MHz
	Tf	Output fall time[4]		-	5	ns

1. The I/O speed is configured using the OSPEEDRy[1:0] bits. The Fm+ mode is configured in the SYSCFG_CFGR1 register. Refer to the RM0454 reference manual for a description of GPIO Port configuration register.
2. Guaranteed by design.
3. This value represents the I/O capability but the maximum system frequency is limited to 64 MHz.
4. The fall time is defined between 70% and 30% of the output waveform, according to I^2C specification.

Figure 18. I/O AC characteristics definition(1)



1. Refer to *Table 51: I/O AC characteristics*.

5.3.15 NRST input characteristics

The NRST input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU}.

Unless otherwise specified, the parameters given in the following table are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 21: General operating conditions*.

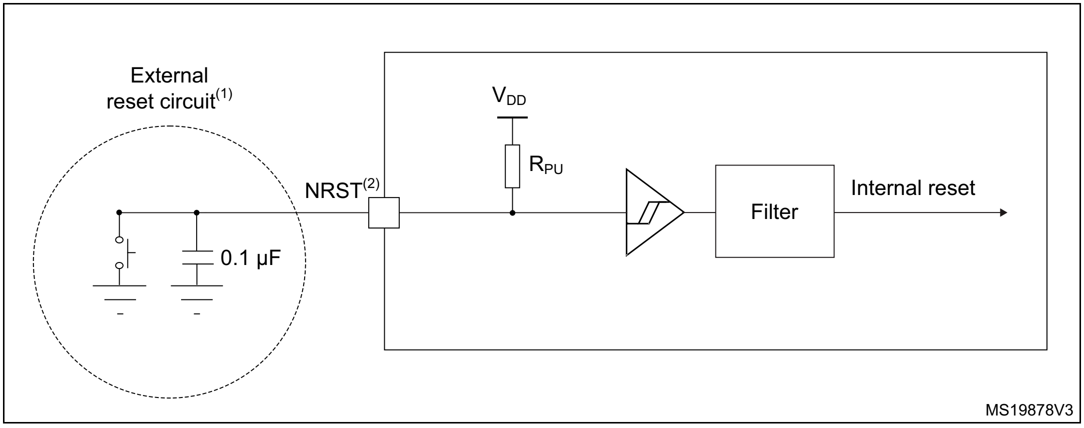
Table 52. NRST pin characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage	-	-	-	0.3 x V_{DDIO1}	V
$V_{IH(NRST)}$	NRST input high level voltage	-	0.7 x V_{DDIO1}	-	-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	25	40	55	kΩ
$V_{F(NRST)}$	NRST input filtered pulse	-	-	-	70	ns
$V_{NF(NRST)}$	NRST input not filtered pulse	2.0 V ≤ V_{DD} ≤ 3.6 V	350	-	-	ns

1. Guaranteed by design.

2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10% order).

Figure 19. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 52: NRST pin characteristics*. Otherwise the reset will not be taken into account by the device.
3. The external capacitor on NRST must be placed as close as possible to the device.

5.3.16 Analog switch booster

Table 53. Analog switch booster characteristics[1]

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply voltage	V_{DD}(min)	-	3.6	V
$t_{SU(BOOST)}$	Booster startup time	-	-	240	µs
	Booster consumption for $V_{DD} \leq 2.7$ V	-	-	500	
	Booster consumption for $2.7\text{ V} \leq V_{DD} \leq 3.6$ V	-	-	900	

1. Guaranteed by design.

5.3.17 Analog-to-digital converter characteristics

Unless otherwise specified, the parameters given in *Table 54* are preliminary values derived from tests performed under ambient temperature, f_{PCLK} frequency and V_{DDA} supply voltage conditions summarized in *Table 21: General operating conditions*.

Note: It is recommended to perform a calibration after each power-up.

Table 54. ADC characteristics[1]

Symbol	Parameter	Conditions[2]	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	2.0	-	3.6	V
V_{REF+}	Positive reference voltage	-	2	-	V_{DDA}	V
f_{ADC}	ADC clock frequency	Range 1	0.14	-	35	MHz
		Range 2	0.14	-	16	

Table 54. ADC characteristics[1] (continued)

Symbol	Parameter	Conditions[2]	Min	Typ	Max	Unit
f_s	Sampling rate	12 bits	-	-	2.50	MSps
		10 bits	-	-	2.92	
		8 bits	-	-	3.50	
		6 bits	-	-	4.38	
f_{TRIG}	External trigger frequency	f_{ADC} = 35 MHz; 12 bits	-	-	2.33	MHz
		12 bits	-	-	$f_{ADC}/15$	
V_{AIN} [3]	Conversion voltage range	-	V_{SSA}	-	V_{REF+}	V
R_{AIN}	External input impedance	-	-	-	50	kΩ
C_{ADC}	Internal sample and hold capacitor	-	-	5	-	pF
t_{STAB}	ADC power-up time	-		2		Conversion cycle
t_{CAL}	Calibration time	f_{ADC} = 35 MHz		2.35		µs
		-		82		$1/f_{ADC}$
t_{LATR}	Trigger conversion latency	CKMODE = 00	2	-	3	$1/f_{ADC}$
		CKMODE = 01		6.5		$1/f_{PCLK}$
		CKMODE = 10		12.5		
		CKMODE = 11		3.5		
t_s	Sampling time	f_{ADC} = 35 MHz	0.043	-	4.59	µs
			1.5	-	160.5	$1/f_{ADC}$
$t_{ADCVREG\_STUP}$	ADC voltage regulator start-up time	-	-	-	20	µs
t_{CONV}	Total conversion time (including sampling time)	f_{ADC} = 35 MHz Resolution = 12 bits	0.40	-	4.95	µs
		Resolution = 12 bits		t_s + 12.5 cycles for successive approximation = 14 to 173		$1/f_{ADC}$
t_{IDLE}	Laps of time allowed between two conversions without rearm	-	-	-	100	µs
$I_{DDA(ADC)}$	ADC consumption from V_{DDA}	f_s = 2.5 MSps	-	410	-	µA
		f_s = 1 MSps	-	164	-	
		f_s = 10 kSps	-	17	-	
$I_{DDV(ADC)}$	ADC consumption from V_{REF+}	f_s = 2.5 MSps	-	65	-	µA
		f_s = 1 MSps	-	26	-	
		f_s = 10 kSps	-	0.26	-	

1. Guaranteed by design
2. I/O analog switch voltage booster must be enabled (BOOSTEN = 1 in the SYSCFG_CFGR1) when V_{DDA} < 2.4 V and disabled when $V_{DDA} \geq 2.4$ V.
3. V_{REF+} is internally connected to V_{DDA} on some packages.Refer to *Section 4: Pinouts, pin description and alternate functions* for further details.

Table 55. Maximum ADC R_{AIN}

Resolution	Sampling cycle at 35 MHz	Sampling time at 35 MHz [ns]	Max. R_{AIN}[1][2] (Ω)
12 bits	1.5	43	50
	3.5	100	680
	7.5	214	2200
	12.5	357	4700
	19.5	557	8200
	39.5	1129	15000
	79.5	2271	33000
	160.5	4586	50000
10 bits	1.5	43	68
	3.5	100	820
	7.5	214	3300
	12.5	357	5600
	19.5	557	10000
	39.5	1129	22000
	79.5	2271	39000
	160.5	4586	50000
8 bits	1.5	43	82
	3.5	100	1500
	7.5	214	3900
	12.5	357	6800
	19.5	557	12000
	39.5	1129	27000
	79.5	2271	50000
	160.5	4586	50000

Table 55. Maximum ADC R_{AIN} (continued)

Resolution	Sampling cycle at 35 MHz	Sampling time at 35 MHz [ns]	Max. R_{AIN}(1)(2) (Ω)
6 bits	1.5	43	390
	3.5	100	2200
	7.5	214	5600
	12.5	357	10000
	19.5	557	15000
	39.5	1129	33000
	79.5	2271	50000
	160.5	4586	50000

1. Guaranteed by design.
2. I/O analog switch voltage booster must be enabled (BOOSTEN = 1 in the SYSCFG_CFGR1) when V_{DDA} < 2.4 V and disabled when V_{DDA} ≥ 2.4 V.

Table 56. ADC accuracy(1)(2)(3)

Symbol	Parameter	Conditions(4)	Min	Typ	Max	Unit
ET	Total unadjusted error	V_{DDA}=V_{REF+} < 3.6 V; f_{ADC} = 35 MHz; f_s ≤ 2.5 MSps; T_A = entire range	-	3	6.5	LSB
EO	Offset error	V_{DDA}=V_{REF+} < 3.6 V; f_{ADC} = 35 MHz; f_s ≤ 2.5 MSps; T_A = entire range	-	1.5	4.5	LSB
EG	Gain error	V_{DDA}=V_{REF+} < 3.6 V; f_{ADC} = 35 MHz; f_s ≤ 2.5 MSps; T_A = entire range	-	3	5	LSB
ED	Differential linearity error	V_{DDA}=V_{REF+} < 3.6 V; f_{ADC} = 35 MHz; f_s ≤ 2.5 MSps; T_A = entire range	-	1.2	1.5	LSB
EL	Integral linearity error	V_{DDA}=V_{REF+} < 3.6 V; f_{ADC} = 35 MHz; f_s ≤ 2.5 MSps; T_A = entire range	-	2.5	3	LSB
ENOB	Effective number of bits	V_{DDA}=V_{REF+} < 3.6 V; f_{ADC} = 35 MHz; f_s ≤ 2.5 MSps; T_A = entire range	9.6	10.2	-	bit
SINAD	Signal-to-noise and distortion ratio	V_{DDA}=V_{REF+} < 3.6 V; f_{ADC} = 35 MHz; f_s ≤ 2.5 MSps; T_A = entire range	59.5	63	-	dB
SNR	Signal-to-noise ratio	V_{DDA}=V_{REF+} < 3.6 V; f_{ADC} = 35 MHz; f_s ≤ 2.5 MSps; T_A = entire range	60	64	-	dB
THD	Total harmonic distortion	V_{DDA}=V_{REF+} < 3.6 V; f_{ADC} = 35 MHz; f_s ≤ 2.5 MSps; T_A = entire range	-	-74	-70	dB

1. Based on characterization results, not tested in production.
2. ADC DC accuracy values are measured after internal calibration.
3. Injecting negative current on any analog input pin significantly reduces the accuracy of A-to-D conversion of signal on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins susceptible to receive negative current.
4. I/O analog switch voltage booster enabled (BOOSTEN = 1 in the SYSCFG_CFGR1) when $V_{DDA} < 2.4$ V and disabled when $V_{DDA} \geq 2.4$ V.

Figure 20. ADC accuracy characteristics

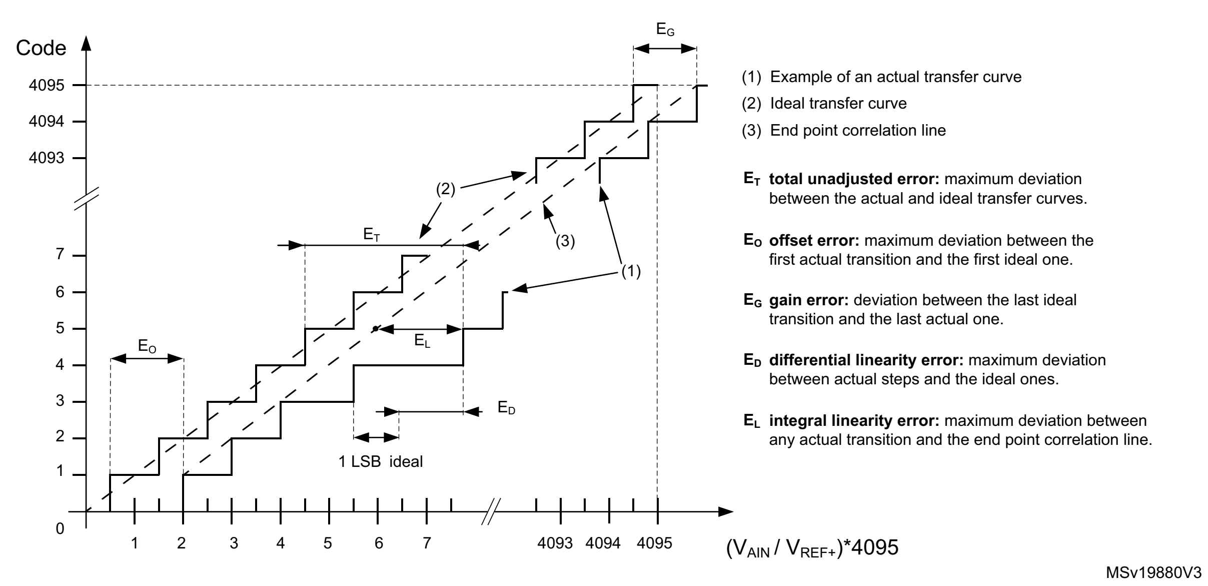
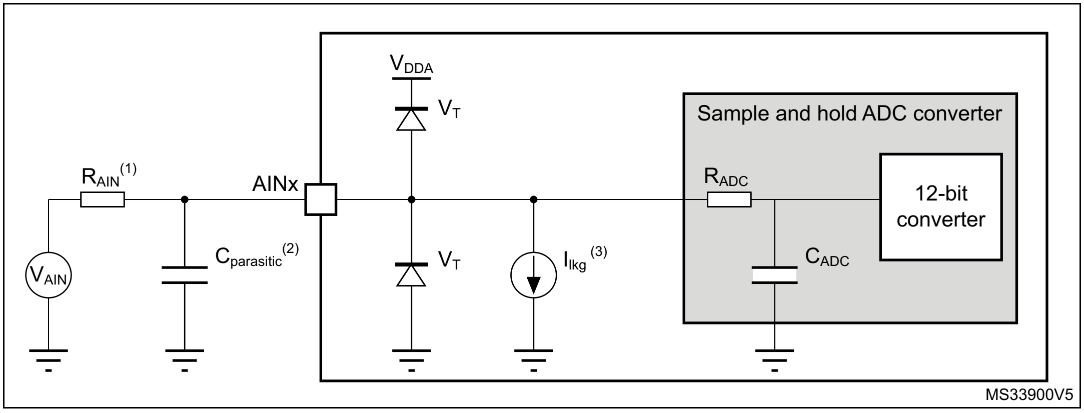


Figure 21. Typical connection diagram using the ADC



1. Refer to *Table 54: ADC characteristics* for the values of R_{AIN} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (refer to *Table 48: I/O static characteristics* for the value of the pad capacitance). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.
3. Refer to *Table 48: I/O static characteristics* for the values of Ilkg.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 9: Power supply scheme*. The 100 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

5.3.18 Temperature sensor characteristics

Table 57. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L[1]	V_{TS} linearity with temperature	-	±1	±2	°C
Avg_Slope[2]	Average slope	2.3	2.5	2.7	mV/°C
V_{30}	Voltage at 30°C (±5 °C)[3]	0.742	0.76	0.785	V
$t_{START(TS\_BUF)}$[1]	Sensor Buffer Start-up time in continuous mode[4]	-	8	15	µs
t_{START}[1]	Start-up time when entering in continuous mode[4]	-	70	120	µs
t_{S_temp}[1]	ADC sampling time when reading the temperature	5	-	-	µs
$I_{DD(TS)}$[1]	Temperature sensor consumption from V_{DD}, when selected by ADC	-	4.7	7	µA

1. Guaranteed by design.
2. Based on characterization results, not tested in production.
3. Measured at V_{DDA} = 3.0 V ±10 mV. The V_{30} ADC conversion result is stored in the TS_CAL1 byte.
4. Continuous mode means Run/Sleep modes, or temperature sensor enable in Low-power run/Low-power sleep modes.

5.3.19 V_{BAT} monitoring characteristics

Table 58. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	39	-	kΩ
Q	Ratio on V_{BAT} measurement	-	3	-	-
Er[1]	Error on Q	-10	-	10	%
t_{S_vbat}[1]	ADC sampling time when reading the VBAT	12	-	-	µs

1. Guaranteed by design.

Table 59. V_{BAT} charging characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{BC}	Battery charging resistor	VBRS = 0	-	5	-	kΩ
		VBRS = 1	-	1.5	-	

5.3.20 Timer characteristics

The parameters given in the following tables are guaranteed by design. Refer to *Section 5.3.14: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 60. TIMx[1] characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 64 MHz	15.625	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 64 MHz	0	40	
Res_{TIM}	Timer resolution	TIMx	-	16	bit
$t_{COUNTER}$	16-bit counter clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 64 MHz	0.015625	1024	µs
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 64 MHz	-	67.10	s

1. TIMx, is used as a general term in which x stands for 1,, 3, 4, 5, 6, 7, 8, 15, 16 or 17.

Table 61. IWDG min/max timeout period at 32 kHz LSI clock[1]

Prescaler divider	PR[2:0] bits	Min timeout RL[11:0]= 0x000	Max timeout RL[11:0]= 0xFFF	Unit
/4	0	0.125	512	ms
/8	1	0.250	1024	
/16	2	0.500	2048	
/32	3	1.0	4096	
/64	4	2.0	8192	
/128	5	4.0	16384	
/256	6 or 7	8.0	32768	

1. The exact timings further depend on the phase of the APB interface clock versus the LSI clock, which causes an uncertainty of one RC period.

5.3.21 Characteristics of communication interfaces

I²C-bus interface characteristics

The I²C-bus interface meets timing requirements of the I²C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The timings are guaranteed by design as long as the I2C peripheral is properly configured (refer to the reference manual RM0454) and when the I2CCLK frequency is greater than the minimum shown in the following table.

Table 62. Minimum I2CCLK frequency

Symbol	Parameter	Condition		Typ	Unit
$f_{I2CCLK(min)}$	Minimum I2CCLK frequency for correct operation of I2C peripheral	Standard-mode		2	MHz
		Fast-mode	Analog filter enabled DNF = 0	9	
			Analog filter disabled DNF = 1	9	
		Fast-mode Plus	Analog filter enabled DNF = 0	18	
			Analog filter disabled DNF = 1	16	

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DDIO1} is disabled, but is still present. Only FT_f I/O pins support Fm+ low-level output current maximum requirement. Refer to *Section 5.3.14: I/O port characteristics* for the I2C I/Os characteristics.

All I2C SDA and SCL I/Os embed an analog filter. Refer to the following table for its characteristics:

Table 63. I2C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Limiting duration of spikes suppressed by the filter(2)	50	260	ns

1. Based on characterization results, not tested in production.
2. Spikes shorter than the limiting duration are suppressed.

SPI/I^{2}S characteristics

Unless otherwise specified, the parameters given in *Table 64* for SPI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and supply voltage conditions summarized in *Table 21: General operating conditions*. The additional general conditions are:

- OSPEEDRy[1:0] set to 11 (output speed)
- capacitive load C = 30 pF
- measurement points at CMOS levels: 0.5 x V_{DD}

Refer to *Section 5.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

Table 64. SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode $V_{DD}(min) < V_{DD} < 3.6$ V Range 1	-	-	32	MHz
		Master transmitter $V_{DD}(min) < V_{DD} < 3.6$ V Range 1			32	
		Slave receiver $V_{DD}(min) < V_{DD} < 3.6$ V Range 1			32	
		Slave transmitter/full duplex $2.7 < V_{DD} < 3.6$ V Range 1			32	
		Slave transmitter/full duplex $V_{DD}(min) < V_{DD} < 3.6$ V Range 1			25	
		$V_{DD}(min) < V_{DD} < 3.6$ V Range 2			8	
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI prescaler = 2	4 x T_{PCLK}	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI prescaler = 2	2 x T_{PCLK}	-	-	ns
$t_{w(SCKH)}$	SCK high time	Master mode	T_{PCLK} - 1.5	T_{PCLK}	T_{PCLK} + 1	ns
$t_{w(SCKL)}$	SCK low time	Master mode	T_{PCLK} - 1.5	T_{PCLK}	T_{PCLK} + 1	ns
$t_{su(MI)}$	Master data input setup time	-	1	-	-	ns
$t_{su(SI)}$	Slave data input setup time	-	3	-	-	ns
$t_{h(MI)}$	Master data input hold time	-	5	-	-	ns
$t_{h(SI)}$	Slave data input hold time	-	2	-	-	ns
$t_{a(SO)}$	Data output access time	Slave mode	9	-	34	ns
$t_{dis(SO)}$	Data output disable time	Slave mode	9	-	16	ns
$t_{v(SO)}$	Slave data output valid time	$2.7 < V_{DD} < 3.6$ V Range 1	-	9	12	ns
		$V_{DD}(min) < V_{DD} < 3.6$ V Range 1	-	9	19.5	
		$V_{DD}(min) < V_{DD} < 3.6$ V Voltage Range 2	-	11	24	
$t_{v(MO)}$	Master data output valid time	-	-	3	5	ns

Table 64. SPI characteristics[1] (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{h(SO)}$	Slave data output hold time	-	5	-	-	ns
$t_{h(MO)}$	Master data output hold time	-	1	-	-	ns

1. Based on characterization results, not tested in production.

Figure 22. SPI timing diagram - slave mode and CPHA = 0

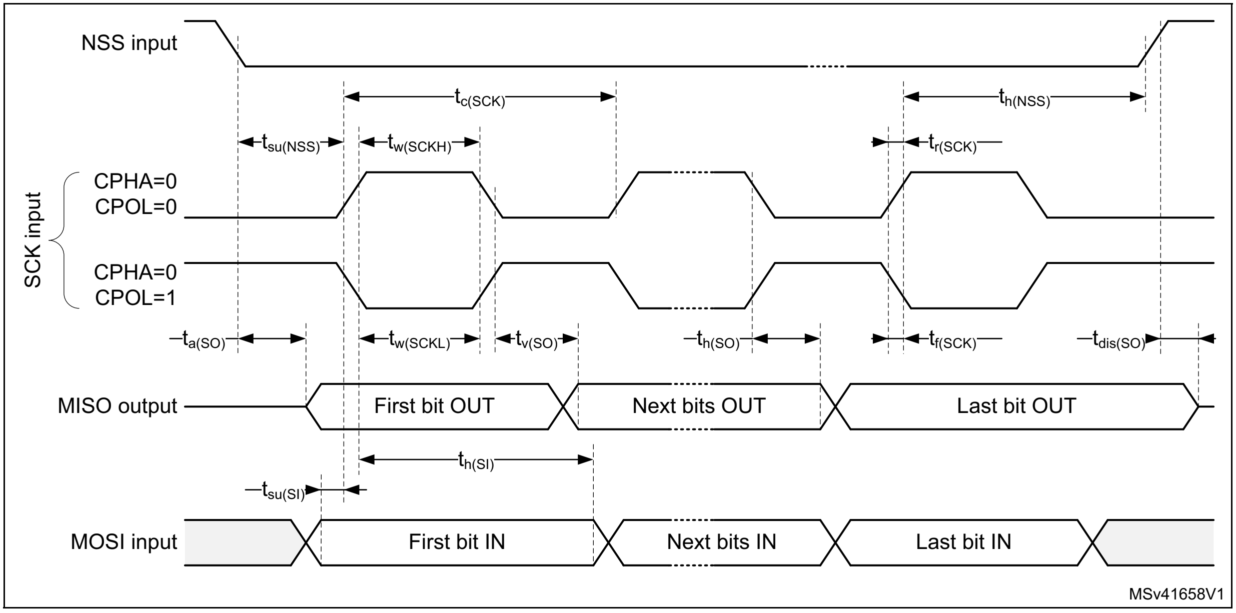
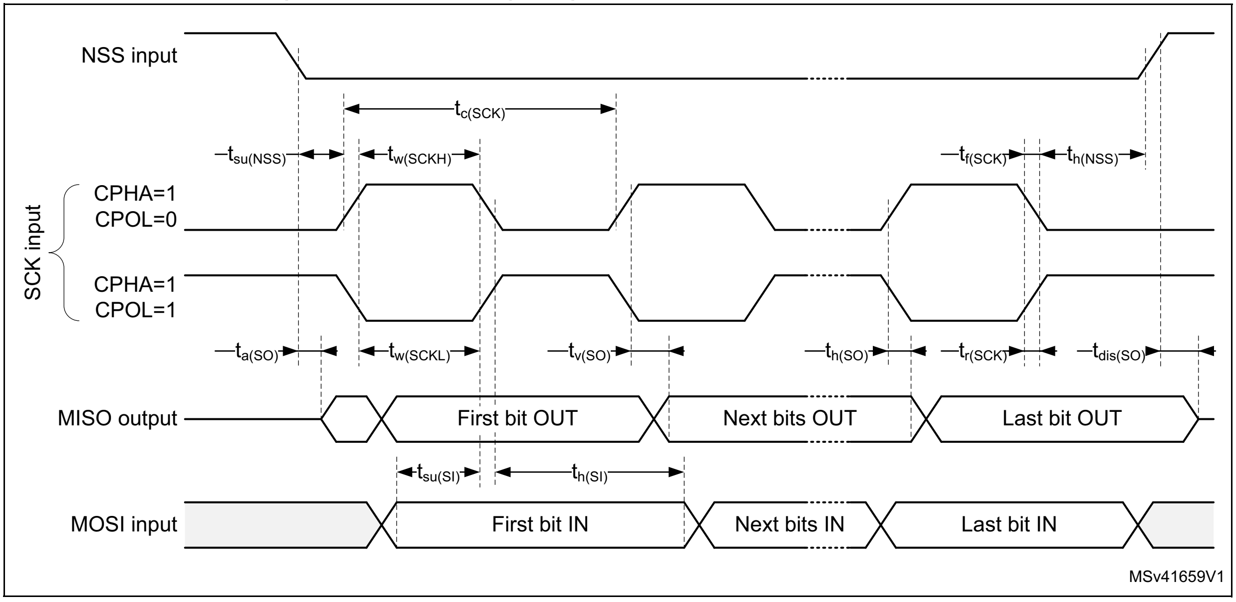
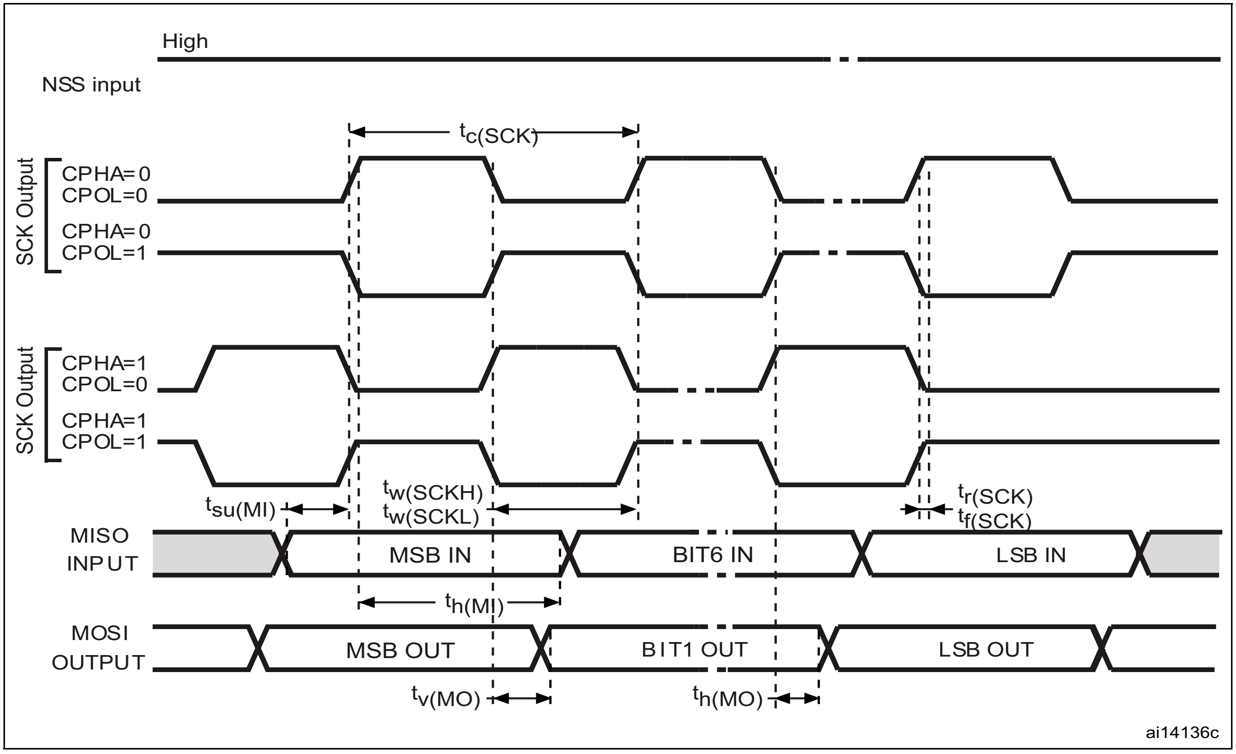


Figure 23. SPI timing diagram - slave mode and CPHA = 1



1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Figure 24. SPI timing diagram - master mode



1. Measurement points are set at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Table 65. I^2S characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	I2S main clock output	f_{MCK}= 256 x Fs; (Fs = audio sampling frequency) Fs_{min} = 8 kHz; Fs_{max} = 192 kHz;	2.048	49.152	MHz
f_{CK}	I2S clock frequency	Master data	-	64xFs	MHz
		Slave data	-	64xFs	
D_{CK}	I2S clock frequency duty cycle	Slave receiver	30	70	%

Table 65. I^{2}S characteristics$^{(1)}$ (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{v(WS)}$	WS valid time	Master mode	-	6	ns
$t_{h(WS)}$	WS hold time	Master mode	3	-	
$t_{su(WS)}$	WS setup time	Slave mode	3	-	
$t_{h(WS)}$	WS hold time	Slave mode	2	-	
$t_{su(SD\_MR)}$	Data input setup time	Master receiver	4	-	
$t_{su(SD\_SR)}$		Slave receiver	5	-	
$t_{h(SD\_MR)}$	Data input hold time	Master receiver	4.5	-	
$t_{h(SD\_SR)}$		Slave receiver	2	-	
$t_{v(SD\_ST)}$	Data output valid time - slave transmitter	after enable edge; 2.7 < V_{DD} < 3.6V	-	10	
		after enable edge; V_{DD}(min) < V_{DD} < 3.6V		15	
$t_{v(SD\_MT)}$	Data output valid time - master transmitter	after enable edge	-	5.5	
$t_{h(SD\_ST)}$	Data output hold time - slave transmitter	after enable edge	7	-	
$t_{h(SD\_MT)}$	Data output hold time - master transmitter	after enable edge	1	-	

1. Based on characterization results, not tested in production.

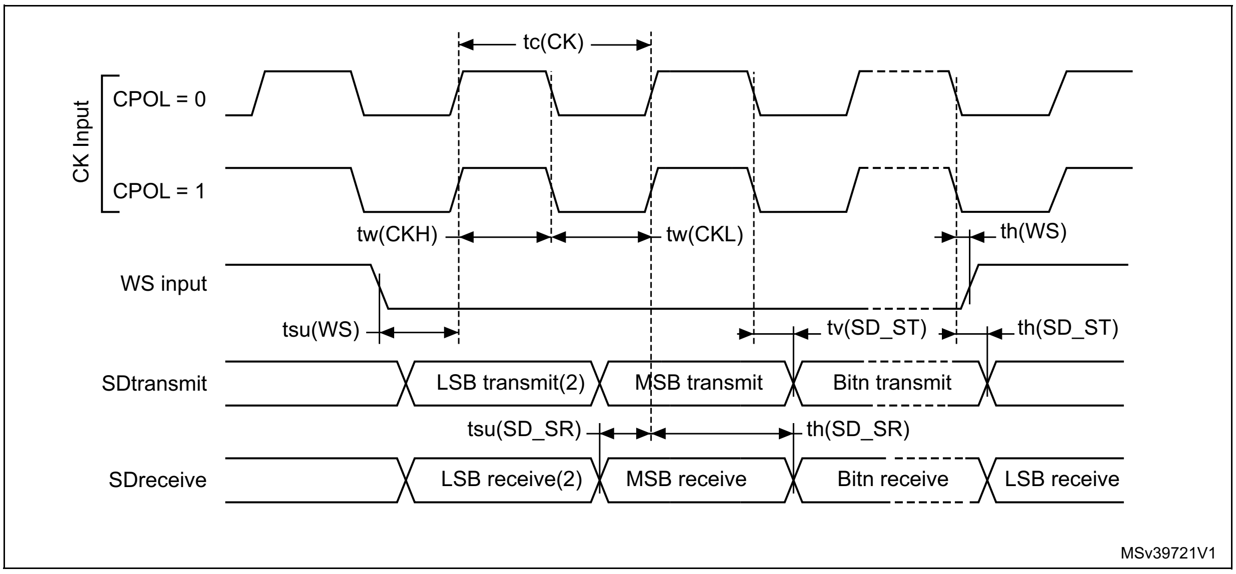
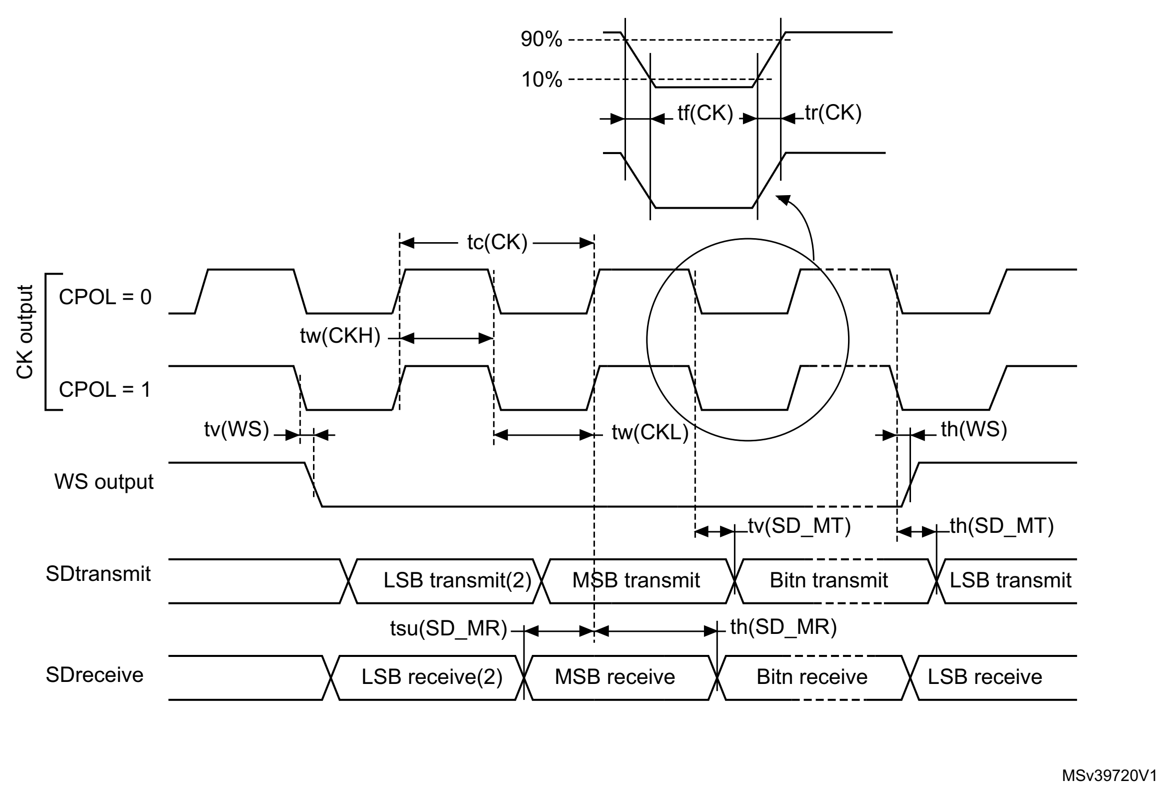


Figure 25. I^{2}S slave timing diagram (Philips protocol)

1. Measurement points are done at CMOS levels: 0.3 V_{DDIO1} and 0.7 V_{DDIO1}.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 26. I^{2}S master timing diagram (Philips protocol)



1. Based on characterization results, not tested in production.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

USART characteristics

Unless otherwise specified, the parameters given in *Table 66* for USART are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and supply voltage conditions summarized in *Table 21: General operating conditions*. The additional general conditions are:

- OSPEEDRy[1:0] set to 10 (output speed)
- capacitive load C = 30 pF
- measurement points at CMOS levels: 0.5 x V_{DD}

Refer to *Section 5.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, CK, TX, and RX for USART).

Table 66. USART characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CK}	USART clock frequency	Master mode	-	-	8	MHz
		Slave mode	-	-	21	

Table 66. USART characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{su(NSS)}$	NSS setup time	Slave mode	t_{ker} + 2	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	2	-	-	
$t_{w(CKH)}$	CK high time	Master mode	1 / f_{CK} / 2 - 1	1 / f_{CK} / 2	1 / f_{CK} / 2 + 1	
$t_{w(CKL)}$	CK low time					
$t_{su(RX)}$	Data input setup time	Master mode	t_{ker} + 2	-	-	
		Slave mode	3	-	-	
$t_{h(RX)}$	Data input hold time	Master mode	2	-	-	
		Slave mode	1	-	-	
$t_{v(TX)}$	Data output valid time	Master mode	-	1	2	
		Slave mode	-	10	19	
$t_{h(TX)}$	Data output hold time	Master mode	0	-	-	
		Slave mode	7	-	-	

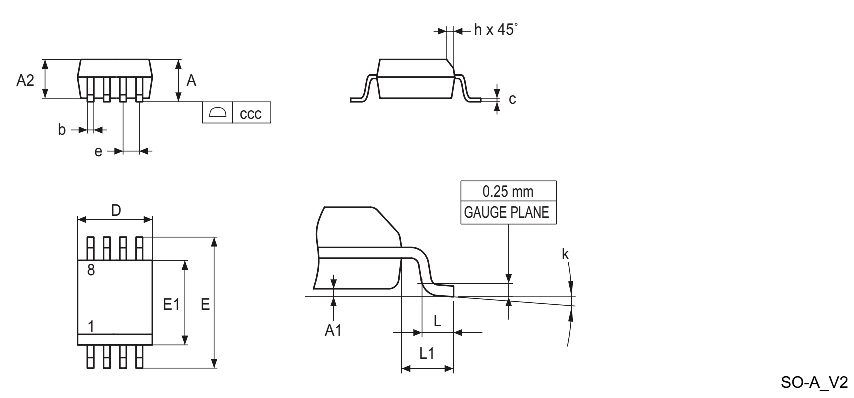
6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

6.1 SO8N package information

SO8N is an 8-lead 4.9 x 6 mm plastic small-outline package with 150 mils body width.

Figure 27. SO8N package outline



1. Drawing is not to scale.

Table 67. SO8N package mechanical data

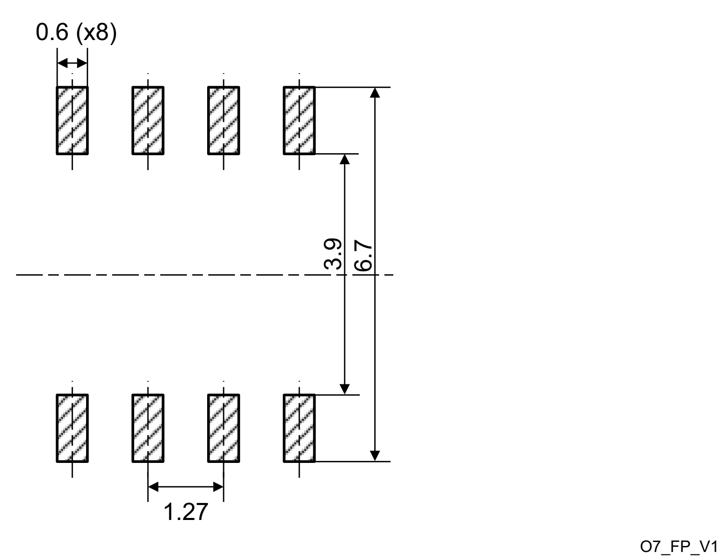
Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.750	-	-	0.0689
A1	0.100	-	0.250	0.0039	-	0.0098
A2	1.250	-	-	0.0492	-	-
b	0.280	-	0.480	0.0110	-	0.0189
c	0.170	-	0.230	0.0067	-	0.0091
D	4.800	4.900	5.000	0.1890	0.1929	0.1969
E	5.800	6.000	6.200	0.2283	0.2362	0.2441
E1	3.800	3.900	4.000	0.1496	0.1535	0.1575
e	-	1.270	-	-	0.0500	-
h	0.250	-	0.500	0.0098	-	0.0197
k	0°	-	8°	0°	-	8°
L	0.400	-	1.270	0.0157	-	0.0500

Table 67. SO8N package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
L1	-	1.040	-	-	0.0409	-
ccc	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to four decimal digits.

Figure 28. SO8N package recommended footprint



1. Dimensions are expressed in millimeters.

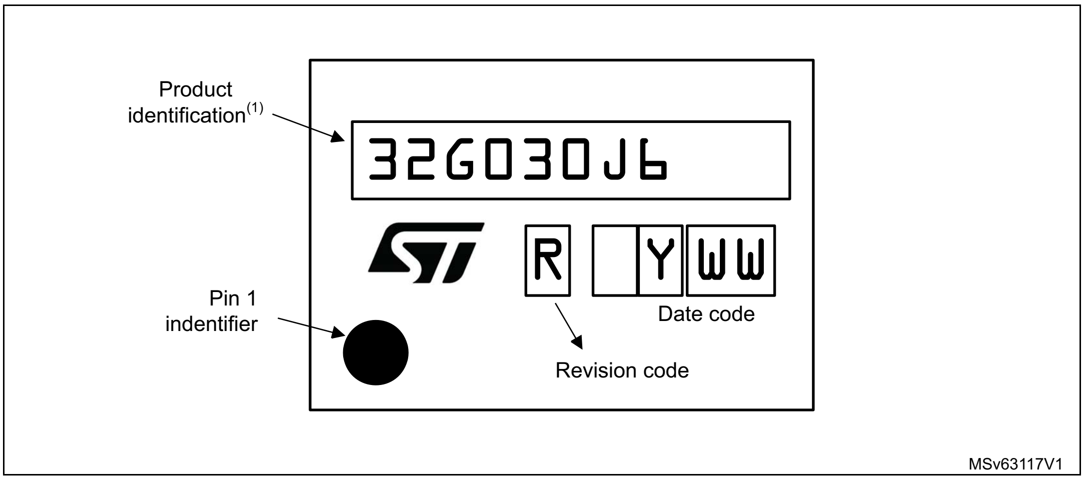
Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks that identify the parts throughout supply chain operations, are not indicated below.

Figure 29. SO8N package marking example

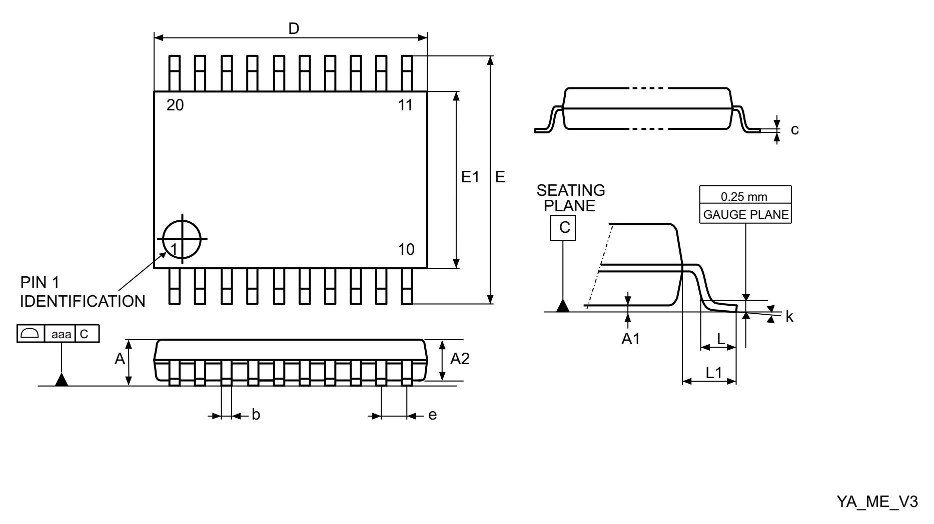


1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

6.2 TSSOP20 package information

TSSOP20 is a 20-lead, 6.5 x 4.4 mm thin small-outline package with 0.65 mm pitch.

Figure 30. TSSOP20 package outline



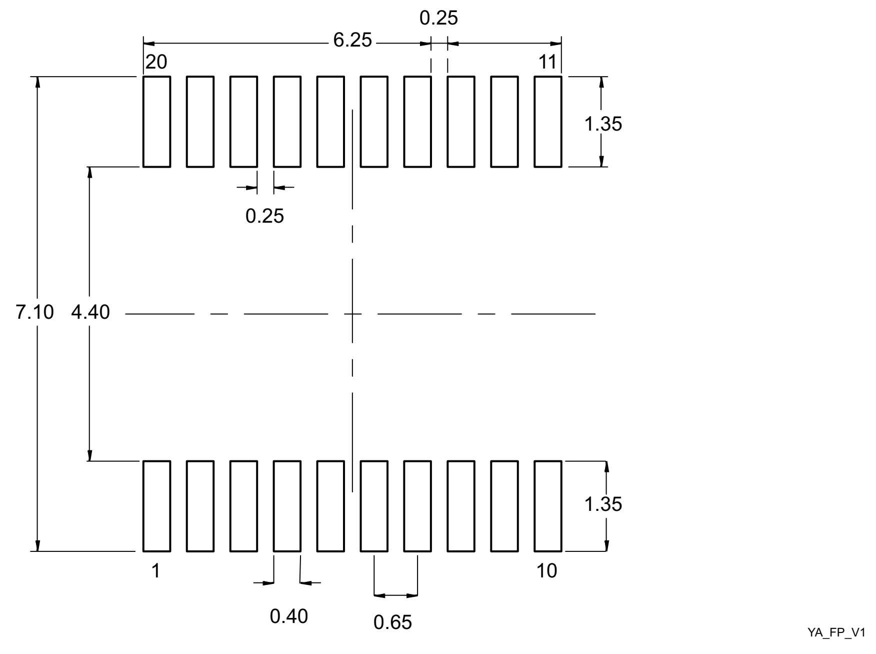
1. Drawing is not to scale.

Table 68. TSSOP20 package mechanical data

Symbol	millimeters			inches(1)		
	Min.	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**
A	-	-	1.200	-	-	0.0472
A1	0.050	-	0.150	0.0020	-	0.0059
A2	0.800	1.000	1.050	0.0315	0.0394	0.0413
b	0.190	-	0.300	0.0075	-	0.0118
c	0.090	-	0.200	0.0035	-	0.0079
D(2)	6.400	6.500	6.600	0.2520	0.2559	0.2598
E	6.200	6.400	6.600	0.2441	0.2520	0.2598
E1(3)	4.300	4.400	4.500	0.1693	0.1732	0.1772
e	-	0.650	-	-	0.0256	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	-	8°	0°	-	8°
aaa	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to four decimal digits.
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
3. Dimension “E1” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25mm per side.

Figure 31. TSSOP20 package footprint



1. Dimensions are expressed in millimeters.

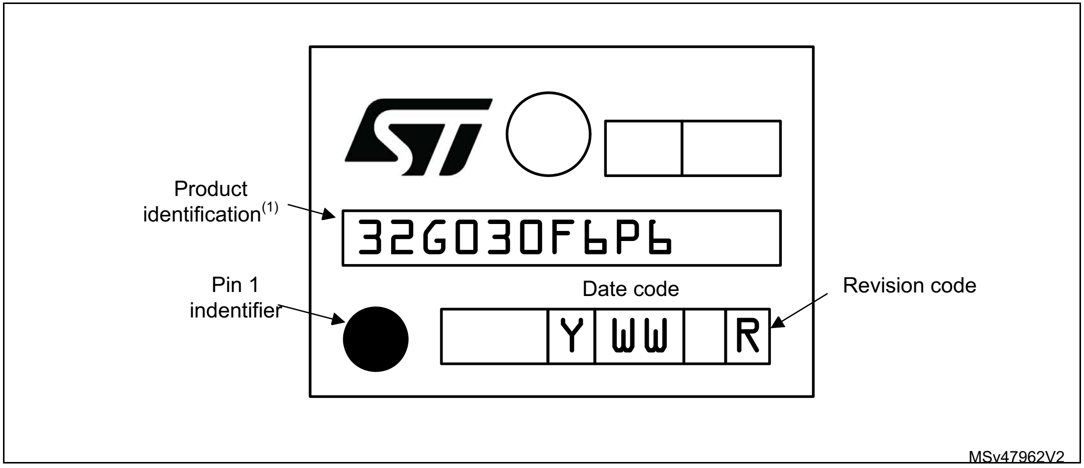
Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks that identify the parts throughout supply chain operations, are not indicated below.

Figure 32. TSSOP20 package marking example



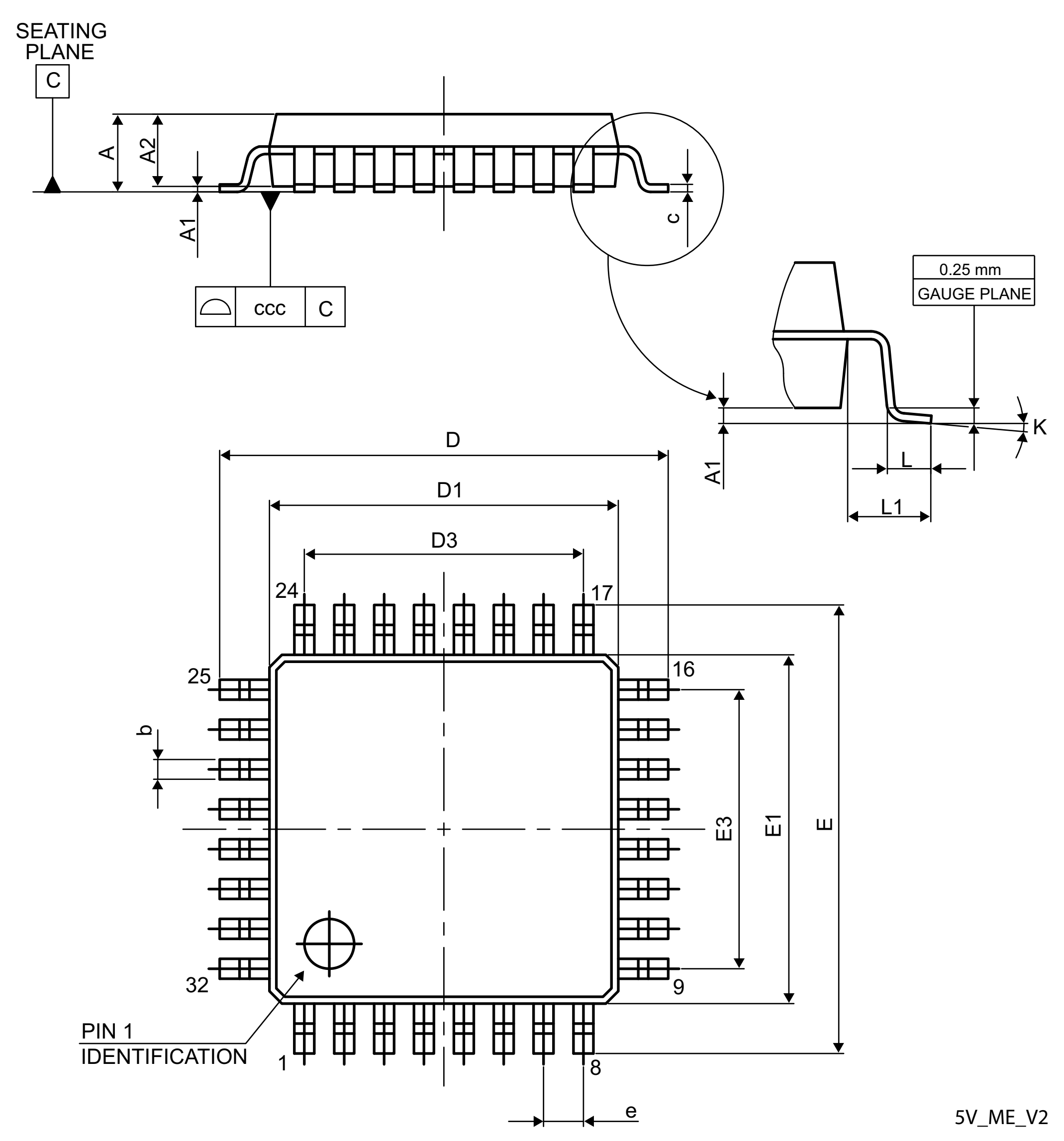
1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering

samples to run a qualification activity.

6.3 LQFP32 package information

LQFP32 is a 32-pin, 7 x 7 mm low-profile quad flat package.

Figure 33. LQFP32 package outline



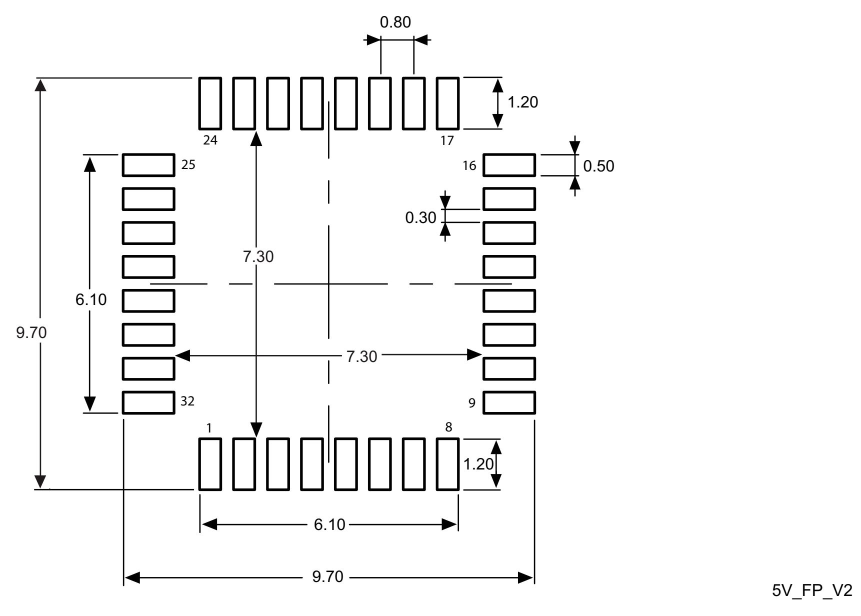
1. Drawing is not to scale.

Table 69. LQFP32 mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.300	0.370	0.450	0.0118	0.0146	0.0177
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.600	-	-	0.2205	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.600	-	-	0.2205	-
e	-	0.800	-	-	0.0315	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 34. Recommended footprint for LQFP32 package



1. Dimensions are expressed in millimeters.

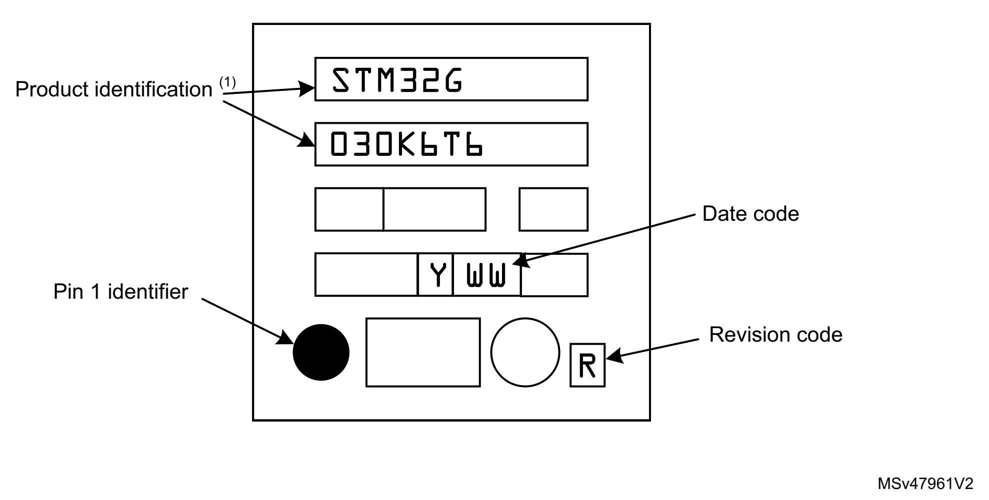
Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 35. LQFP32 package marking example

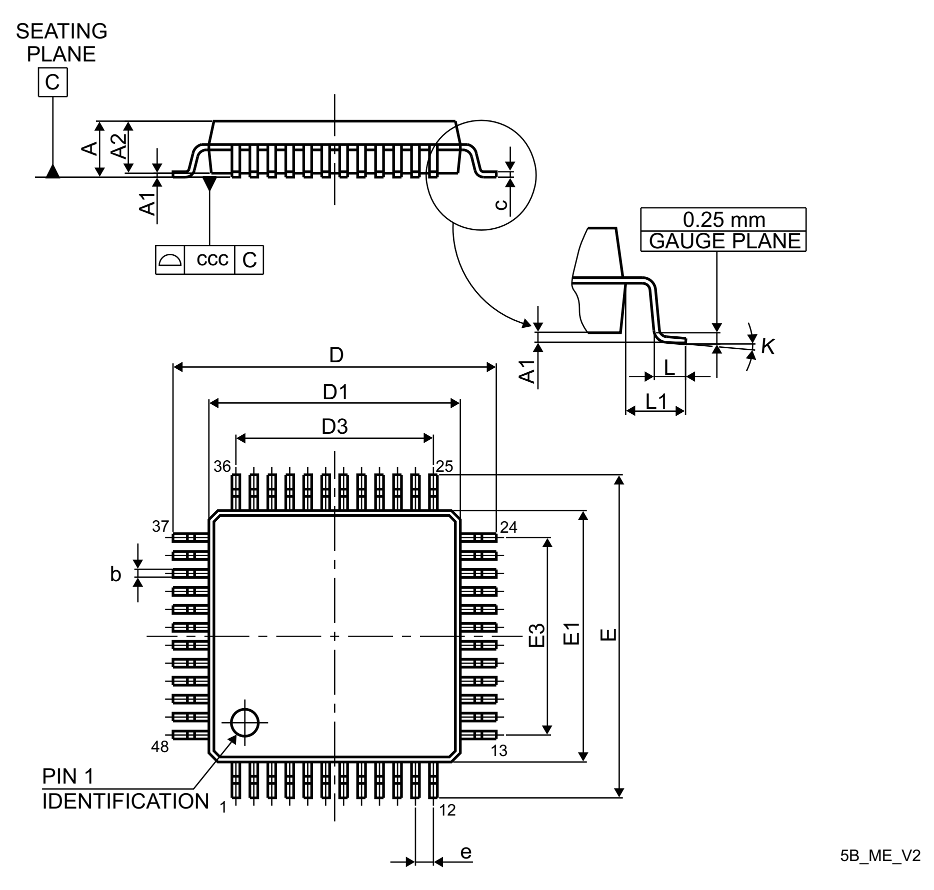


1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

6.4 LQFP48 package information

LQFP48 is a 48-pin, 7 x 7 mm low-profile quad flat package.

Figure 36. LQFP48 package outline



1. Drawing is not to scale.

Table 70. LQFP48 mechanical data

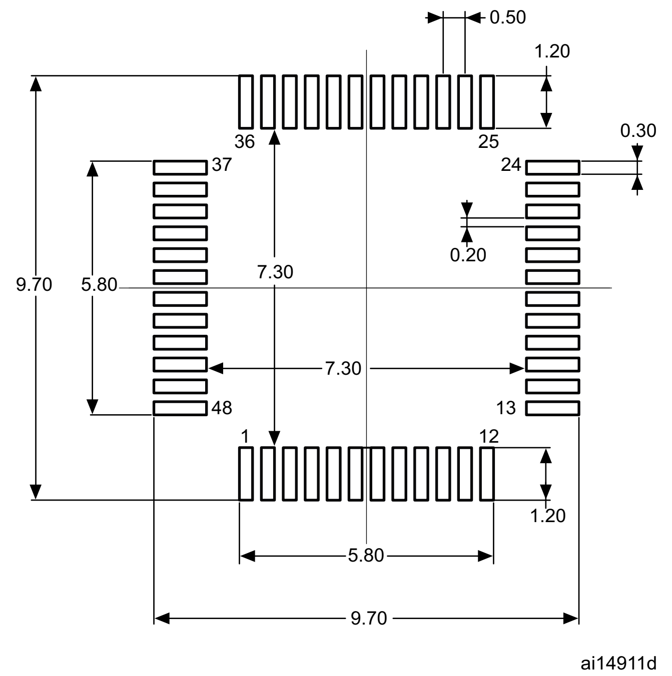
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-

Table 70. LQFP48 mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 37. Recommended footprint for LQFP48 package



1. Dimensions are expressed in millimeters.

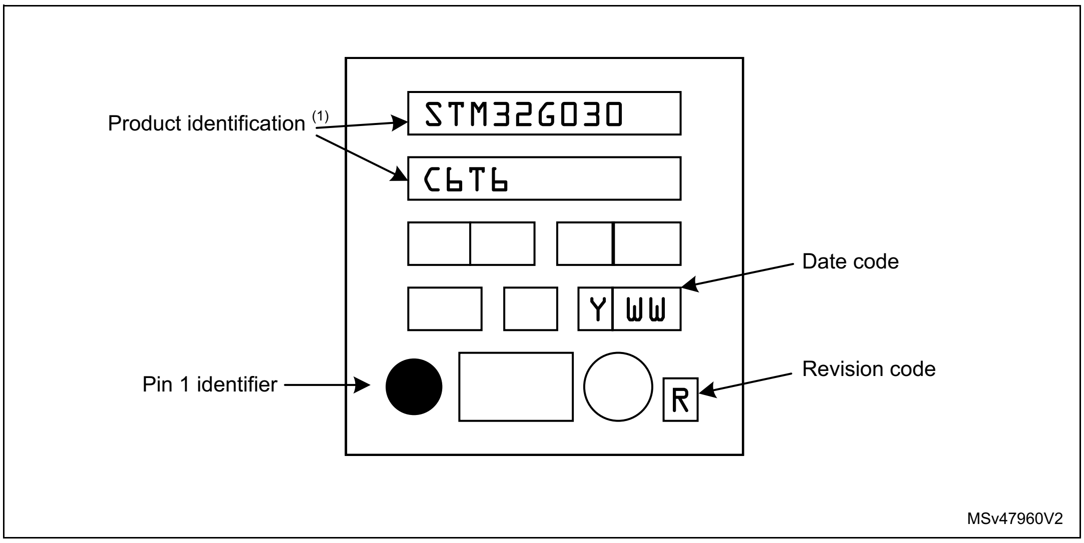
Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 38. LQFP48 package marking example



1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

6.5 Thermal characteristics

The operating junction temperature T_J must never exceed the maximum given in *Table 21: General operating conditions*

The maximum junction temperature in °C that the device can reach if respecting the operating conditions, is:

$$T_J(\max) = T_A(\max) + P_D(\max) \times \Theta_{JA}$$

where:

- $T_A(\max)$ is the maximum operating ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- $P_D = P_{INT} + P_{I/O}$,
  - P_{INT} is power dissipation contribution from product of I_{DD} and V_{DD}
  - $P_{I/O}$ is power dissipation contribution from output ports where:
    $P_{I/O} = \Sigma (V_{OL} \times I_{OL}) + \Sigma ((V_{DDIO1} - V_{OH}) \times I_{OH})$,
    taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 71. Package thermal characteristics

Symbol	Parameter	Package	Value			Unit
			Junction-to-ambient	Junction-to-board	Junction-to-case	
Θ	Thermal resistance	LQFP48 7 × 7 mm	84	76	42	°C/W
		LQFP32 7 × 7 mm	84	76	42	
		TSSOP20 6.4 × 4.4 mm	88	57	19	
		SO8N 4.9 × 6 mm	134	86	30	

6.5.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (still air). Available from www.jedec.org.

7 Ordering information

Example STM32 G 030 K 8 T 6 xyy

Device family

STM32 = Arm® based 32-bit microcontroller

Product type

G = general-purpose

Device subfamily

030 = STM32G030

Pin count

J = 8

F = 20

K = 32

C = 48

Flash memory size

6 = 32 Kbytes

8 = 64 Kbytes

Package type

T = LQFP

P = TSSOP

M = SO␣N

Temperature range

6 = -40 to 85°C (105°C junction)

Options

␣TR = tape and reel packing

␣␣␣ = tray packing

other = 3-character ID incl. custom Flash code and packing information

For a list of available options (memory, package, and so on) or for further information on any aspect of this device, please contact your nearest ST sales office.

8 Revision history

Table 72. Document revision history

Date	Revision	Changes
26-Jun-2019	1	Initial release
09-Dec-2019	2	Added *Section 3.12: DMA request multiplexer (DMAMUX)*. Corrected figures with package marking examples. Corrected I/O numbers in *Table 2: STM32G030x6/x8 family device features and peripheral counts*. Added I/O types in *Table 12: Pin assignment and description*.
22-Apr-2020	3	Cover page updated; *Section 2: Description* updated; *Table 18: Voltage characteristics* updated; *Table 19: Current characteristics*: Note 2 removed; *Table 54: ADC characteristics*: major update;
20-Jan-2022	4	Footnote *3.* of *Table 12: Pin assignment and description* updated; $V_{ESD(HBM)}$ updated in *Table 45: ESD absolute maximum ratings*. Packages in *Section 6: Package information* re-ordered from lowest to highest pin count.

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