SONY

CXD2023Q

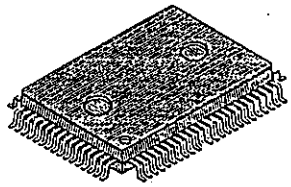
Digital Comb Filter (NTSC)

For the availability of this product, please contact the sales office.

Description

The CXD2023Q is an adaptive comb filter compatible with NTSC system, and can provide high-precision Y/C separation with a single-chip.

80 pin QFP (Plastic)



Features

- Y/C separation by adaptive processing
- High frequency compensation function
- Two 1H delay lines
- 8-bit A/D converter (1-channel)
- 8-bit D/A converter (2-channel)
- Clock 4 fsc
- Pin assignments are compatible with CXD2024Q (in NTSC mode)

Structure

Silicon gate CMOS IC

Applications

Y/C separation for color TVs and VCRs

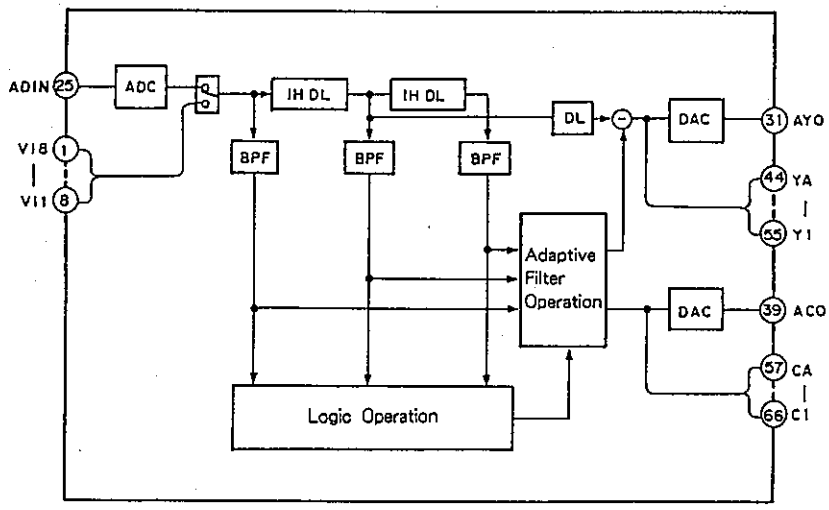
Absolute Maximum Ratings (Ta=25 °C, Vss=0V)

• Supply voltage	DV_{DD}, AAVD, ADVD, YV_{DD}, CV_{DD}	Vss to +7.0	V
• Input voltage	V_I	Vss to V_{DD}	V
• Output voltage	Vo	Vss–0.5 to V_{DD}+0.5	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–55 to +150	°C

Recommended Operating Conditions

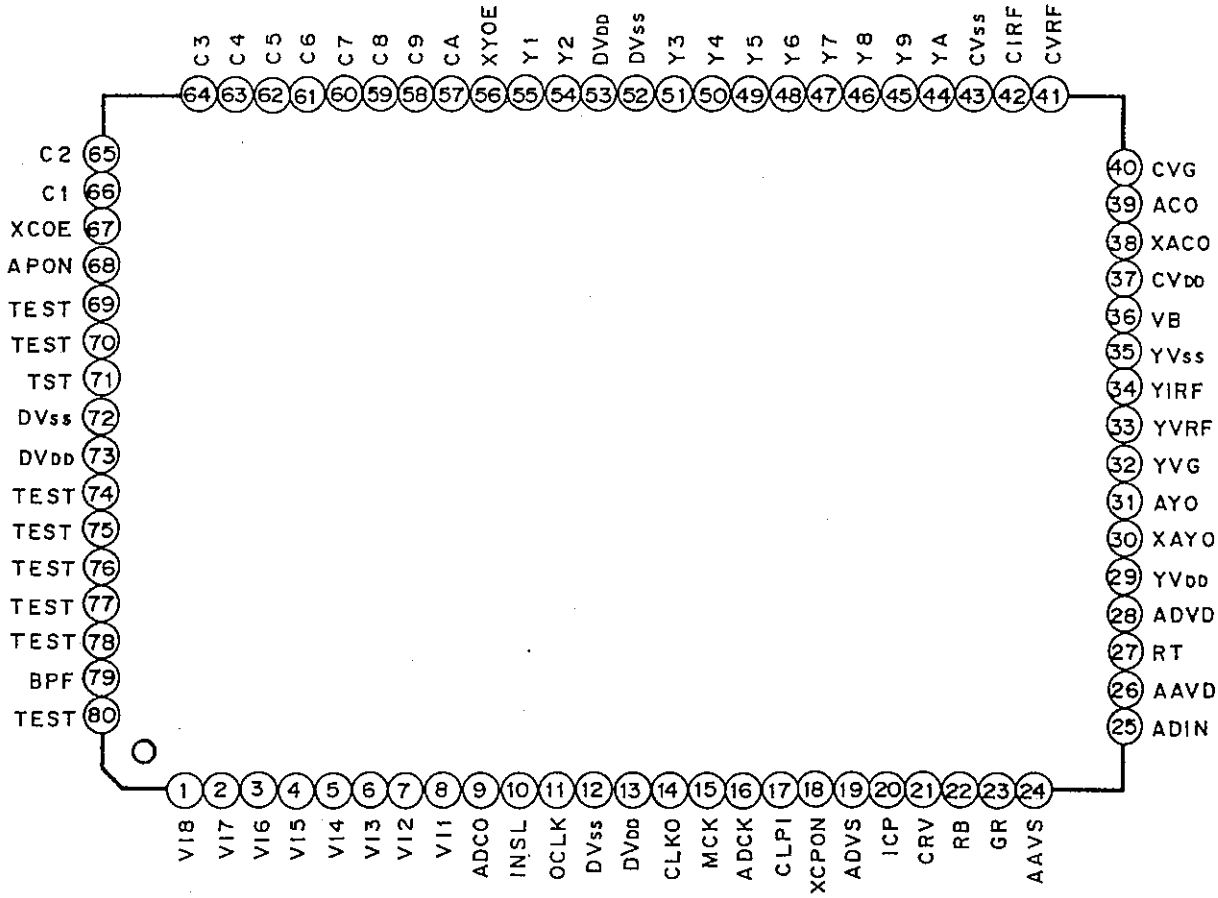
• Supply voltage	DV_{DD}, AAVD, ADVD, YV_{DD}, CV_{DD}	5.0 ± 0.25	V
• Analog input	ADIN	1.8	Vpp or greater
• Operating temperature	Topr	–20 to +75	°C

Block Diagram



E92902A14

Pin Configuration



Pin Description

Pin No.	Symbol	I/O	Description
1	VI8	I	Digital input (MSB) Connected to DVss or DVDD when not in use.
2	VI7	I	Digital input Connected to DVss or DVDD when not in use.
3	VI6	I	Digital input Connected to DVss or DVDD when not in use.
4	VI5	I	Digital input Connected to DVss or DVDD when not in use.
5	VI4	I	Digital input Connected to DVss or DVDD when not in use.
6	VI3	I	Digital input Connected to DVss or DVDD when not in use.
7	VI2	I	Digital input Connected to DVss or DVDD when not in use.
8	VI1	I	Digital input (LSB) Connected to DVss or DVDD when not in use.
9	ADCO	I	A/D converter output mode High: Video signals took in from A/D converter (input pin: ADIN) are output without change from the Y output pins (YA to Y3) as 8-bit digital data with a 3.5 clock delay. Low: Normal mode
10	INSL	I	Input switching. Switches comb filter input. Low: Analog input High: Digital input
11	OCLK	I	Clock amplifier input. Input at 0.8Vp-p or more with DC coupled at capacitor.
12	DVss	—	Digital ground
13	DVDD	—	Digital power supply (5V)
14	CLKO	O	Clock amplifier output

Pin No.	Symbol	I/O	Description
15	MCK	I	Clock input. Input 4 fsc clock locked to the color burst. Normally connected to clock amplifier output at Pin 14.
16	ADCK	I	Clock input for A/D converter. Input the same clock signal as MCK. Normally connected to clock amplifier output at Pin 14.
17	CLPI	I	Clamp pulse input for A/D converter. Clamps the signal voltage of the clamp pulse during the low interval. When the clamp function is off, connect to DV_{DD}.
18	XCPON	I	High: Clamp function is set to off, and only the normal A/D converter function is enabled. Low: Clamp function is enabled.
19	ADVS	—	Digital ground for A/D converter
20	ICP	I	Clamp control voltage integration pin. Connect capacitor of approximately 0.01 µF. (When not using clamp, connect to ground.)
21	CRV	I	Clamp reference voltage input. Operates the reference voltage and the clamp interval input voltage to be equal. (When not using clamp, connect to ground.)
22	RB	O	Reference voltage (bottom) 0.5V (typ.)
23	GR	—	Guard ring (Connect to analog ground.)
24	AAVS	—	Analog ground for A/D converter
25	ADIN	I	Comb filter analog input (A/D converter input)
26	AAVD	—	Analog power supply for A/D converter (5V)
27	RT	O	Reference voltage (top) 2.6V (typ.)
28	ADVD	—	Digital power supply for A/D converter (5V)
29	YV_{DD}	—	Power supply for Y/DA converter (5V)
30	XAYO	O	AYO inverted current output (Connect to analog ground YVss.)
31	AYO	O	Analog luminance signal output (Output can be obtained by connecting resistance.)
32	YVG	O	Connect capacitor of approximately 0.1 µF.
33	YVRF	I	Sets the full-scale value of the analog luminance signal.
34	YIRF	O	Connect a resistance of 16 times (16R) that of the output resistance "R" of AYO pin.
35	YVss	—	Analog ground for Y/DA converter
36	VB	O	Connect capacitor of approximately 0.1 µF.
37	CV_{DD}	—	Analog power supply for C/DA converter (5V)
38	XACO	I	ACO inverted current output (Connect to analog ground CVss.)
39	ACO	O	Analog chrominance signal output (Output can be obtained by connecting resistance.)
40	CVG	O	Connect capacitor of approximately 0.1 µF.
41	CVRF	I	Sets the full-scale value of the analog chrominance signal.
42	CIRF	O	Connect a resistance of 16 times (16R) that of the output resistance "R" of AYO pin.
43	CVss	—	Ground for C/DA converter
44	YA	O	Digital luminance signal output (MSB)
45	Y9	O	Digital luminance signal output
46	Y8	O	Digital luminance signal output
47	Y7	O	Digital luminance signal output
48	Y6	O	Digital luminance signal output

Pin No.	Symbol	I/O	Description
49	Y5		Digital luminance signal output
50	Y4	O	Digital luminance signal output
51	Y3	O	Digital luminance signal output
52	DVss	—	Digital ground
53	DV_{DD}	—	Digital power supply (5V)
54	Y2	O	Digital luminance signal output
55	Y1	O	Digital luminance signal output (LSB)
56	XYOE	I	Digital luminance signal output control High: High impedance Low: Enable
57	CA	O	Digital chrominance signal output (MSB)
58	C9	O	Digital chrominance signal output
59	C8	O	Digital chrominance signal output
60	C7	O	Digital chrominance signal output
61	C6	O	Digital chrominance signal output
62	C5	O	Digital chrominance signal output
63	C4	O	Digital chrominance signal output
64	C3	O	Digital chrominance signal output
65	C2	O	Digital chrominance signal output
66	C1	O	Digital chrominance signal output (LSB)
67	XCOE	I	Digital chrominance signal output control. High: High impedance Low: Enable
68	APCN	I	Aperture compensation. High: Compensates for the aperture-induced frequency characteristics degradation. Even in through mode (TST ON), aperture compensation is performed for the Y output. Low: Standard mode
69	TEST	I	Test Fixed to "Low"
70	TEST	I	Test Fixed to "Low"
71	TST	I	Y output through mode. High: Outputs the input composite video signal from the Y output. At this time, there is 1H+18 clock delay to the input (for digital input). For C output, Y/C separated C signal is output. Low: Y/C separation mode
72	DVss	—	Digital ground
73	DV_{DD}	—	Digital power supply (5V)
74	TEST	I	Test Fixed to "Low"
75	TEST	I	Test Fixed to "Low"
76	TEST	I	Test Fixed to "Low"
77	TEST	I	Test Fixed to "Low"
78	TEST	I	Test Fixed to "Low"
79	BPF	I	High: Fixed to BPF separation Low: Standard mode
80	TEST	I	Test Fixed to "Low"

Electrical Characteristics

1) DC Characteristics

(V_{DD}=5V ± 5%, Vss=0V, Topr=–20 to +75 °C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply current	I_{DD}	Clock 14MHz	—	—	80	mA
High level input voltage	V_{IH}	CMOS level	V_{DD}×0.7	—	V_{DD}	V
Low level input voltage	V_{IL}	CMOS level	Vss	—	V_{DD}×0.3	V
High level output voltage	V_{OH}	I_{OH}=–2mA	V_{DD}–0.5	—	V_{DD}	V
		I_{OH}=–4mA (14pin)	V_{DD}–0.5	—	V_{DD}	V
Low level output voltage	V_{OL}	I_{OL}=4mA	Vss	—	0.4	V
		I_{OL}=8mA (14pin)	Vss	—	0.4	V
Logical Vth	LVth	OCLK (11pin)	—	V_{DD}/2	—	V
Input voltage	V_{IN}		0.8	—	V_{DD}	Vp-p
Feedback resistor	R_{FB}		500K	2M	5M	Ω

2) AC Characteristics

(V_{DD}=5V ± 5%, Vss=0V, Topr=–20 to +75 °C, C_L=20pF)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Data setup time	tdsu	MCK→VI8 to VI1	20	—	—	ns
Data hold time	tdh	MCK→VI8 to VI1	10	—	—	ns
Propagation delay time	tpd	MCK→YA to Y1	—	—	45	ns
		MCK→CA to C1	—	—	45	ns
Clock frequency	f		14	4fsc	15	MHz

3) Pin Capacitance

(Ta=25 °C, f=1MHz, V_{IN}=0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}		—	—	9	pF
Output capacitance	C_{OUT}		—	—	11	pF

4) ADC Characteristics

(V_{DD}=5V, Ta=25°C, fc=10MHz)

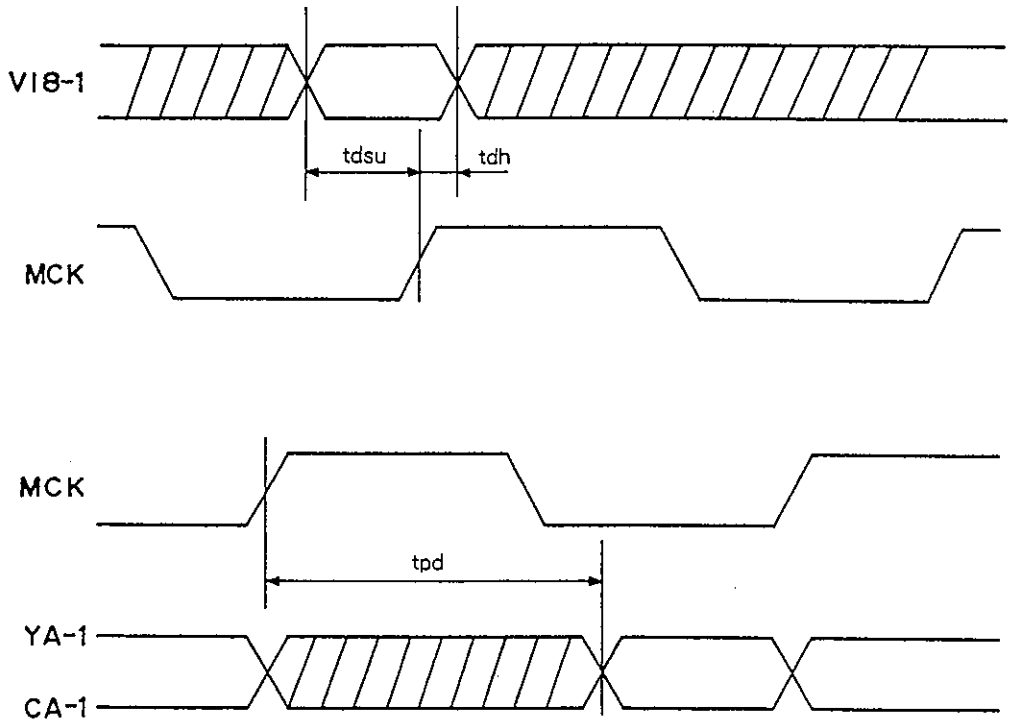
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n		—	8	—	bit
Max. conversion speed	fmax		14.3	—	—	MSPS
Analog input band width	BW	–3dB	—	18	—	MHz
Self bias	VRB		0.48	0.52	0.56	V
	VRT–VRB		1.96	2.08	2.22	V
Offset voltage	E_{OT}		–50	–30	–10	mV
	E_{OB}		+30	+50	+70	
Propagation delay time	tpd		—	—	45	ns
Differential linearity error	E_D		–1	—	+1	LSB
Integral linearity error	E_L		–2	—	+2	LSB
Clamp offset voltage	Eoc	V_{REF}=VRB	–20	0	+20	mV
		V_{REF}=VRT	–30	–10	+10	mV

5) DAC Characteristics

(V_{DD}=5V, V_{RF}=2V, R=200Ω, Ta=25°C, fc=10MHz)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n		—	8	—	bit
Max. conversion speed	fmax		14.3	—	—	MSPS
Differential linearity error	E_D		–0.5	—	+0.5	LSB
Integral linearity error	E_L		–1.5	—	+1.5	LSB
Output full-scale voltage	V_{FS}		1.9	2.0	2.1	V
Output full-scale current	I_{FS}		—	10	15	mA
Output offset voltage	Vos		—	—	1	mV
Precision guaranteed output voltage range	Voc		0.5	2.0	2.1	V
Glitch energy	G_E	When R=75Ω	—	30	—	pV-s

AC Characteristics Timing Chart



Description of Operation

The CXD2023Q is an NTSC compatible IC which, through adaptive (two-dimensional) processing, offers higher performance digital Y/C separation than conventional line combs. Moreover, two-dimensional processing permits systems to be implemented at a far lower cost than is possible with three-dimensional processing.

In the case of NTSC, the conventional simple line comb always causes an error in vertical non-correlated section because it calculates non-correlated signals together as shown in Fig. 1. In order to avoid the occurrences of calculating non-correlated signals together, the CXD2023Q is provided with two line combs for Y/C separation of a line signals. One line comb calculates its line signals and the signals of the line upper that one (referred to as the upper line comb for the sake of convenience), while the other line comb calculates its line signals and the signals of the line lower that one (contrastingly referred to as the lower line comb). Which line comb is used is dependent upon the signal correlation.

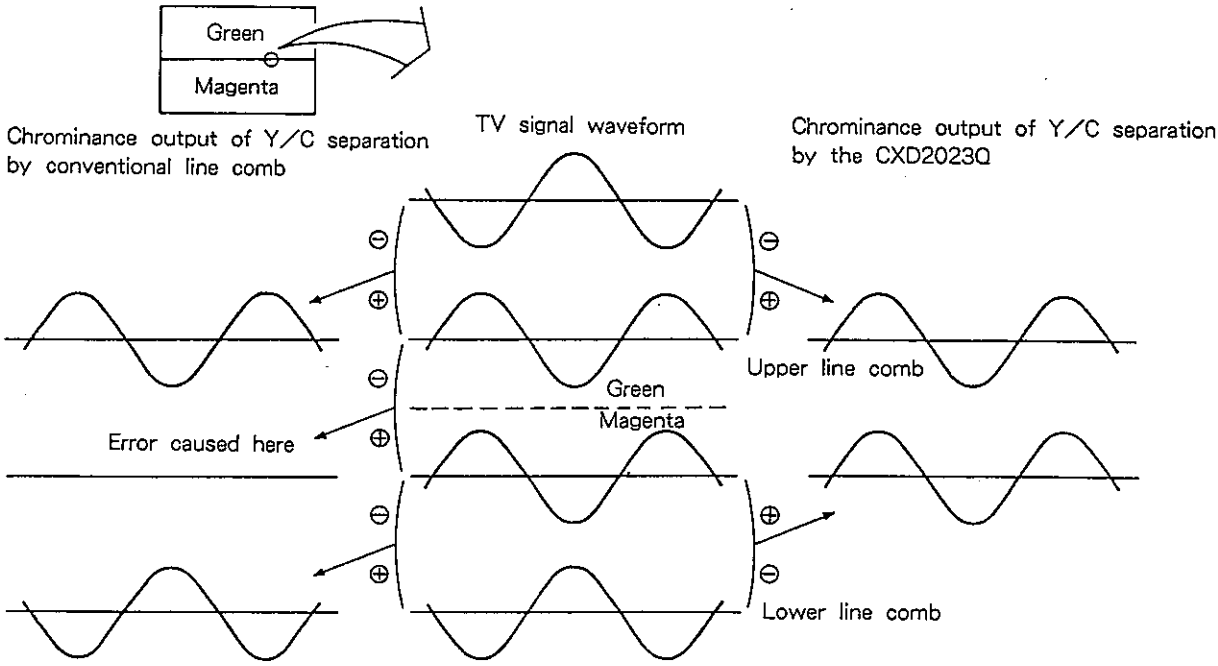


Fig. 1.

When, as is the case in Fig. 2 for example, only a single line is colored, an error is caused on both the upper and the lower line combs. In the case like this where the vertical frequency is high but the horizontal frequency is low, Y/C separation is performed by the band pass filter and trap.

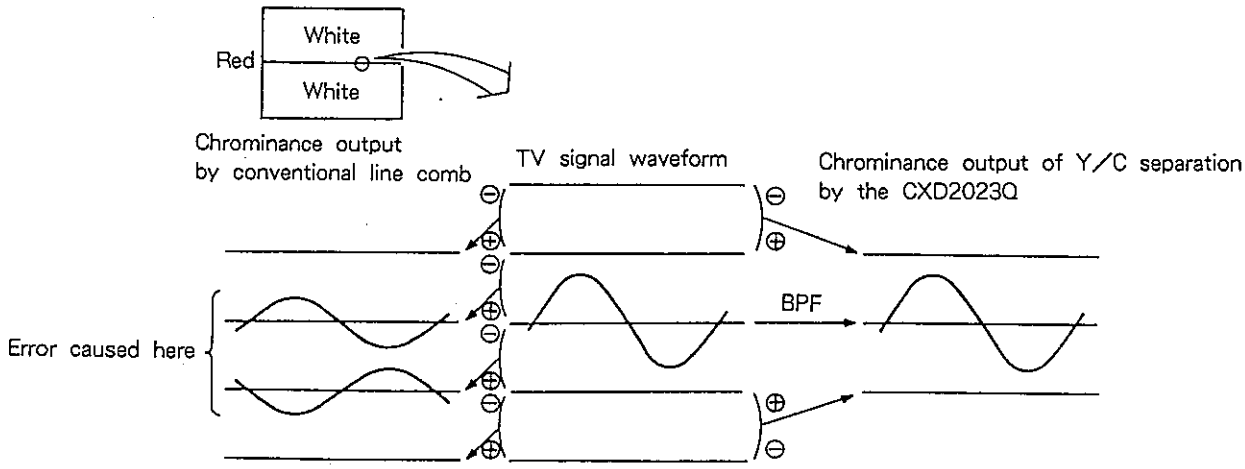


Fig. 2.

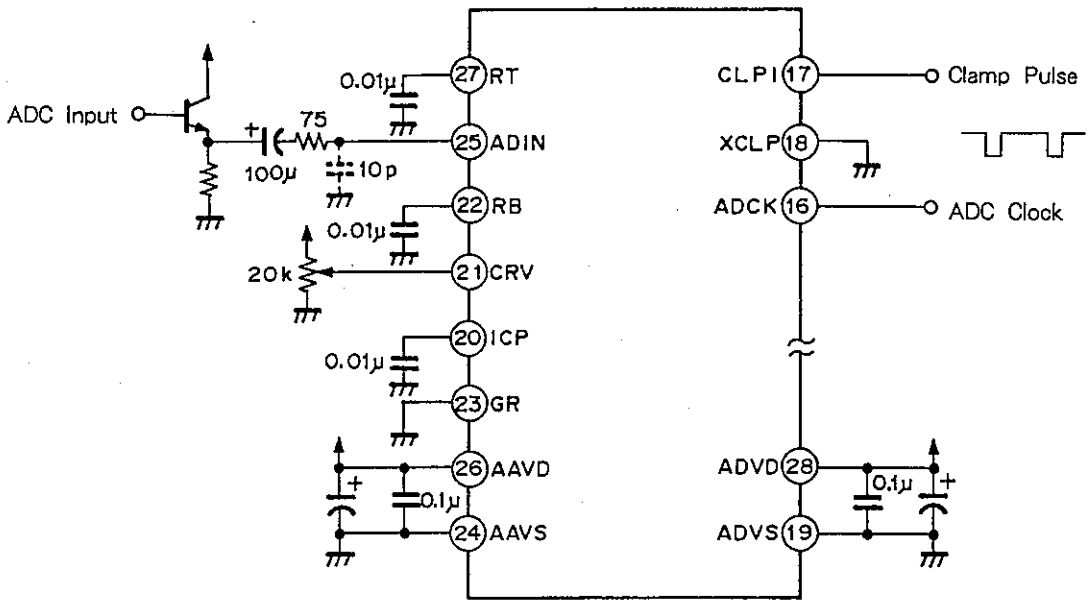
When both the vertical and horizontal frequencies are high, and the vertical correlation is strong, the 2H comb output is derived by averaging the upper and lower comb outputs.
In this manner, by determining and selecting the optimum output from among the upper comb, lower comb, 2H comb and band pass filter on the basis of signal correlation, a much higher precision in Y/C separation can be achieved than that in conventional line combs.
In addition, digital implementation eliminates ringing and others that used to occur in the conventional glass delay line.

Summary of Advantages Offered by the CXD2023Q

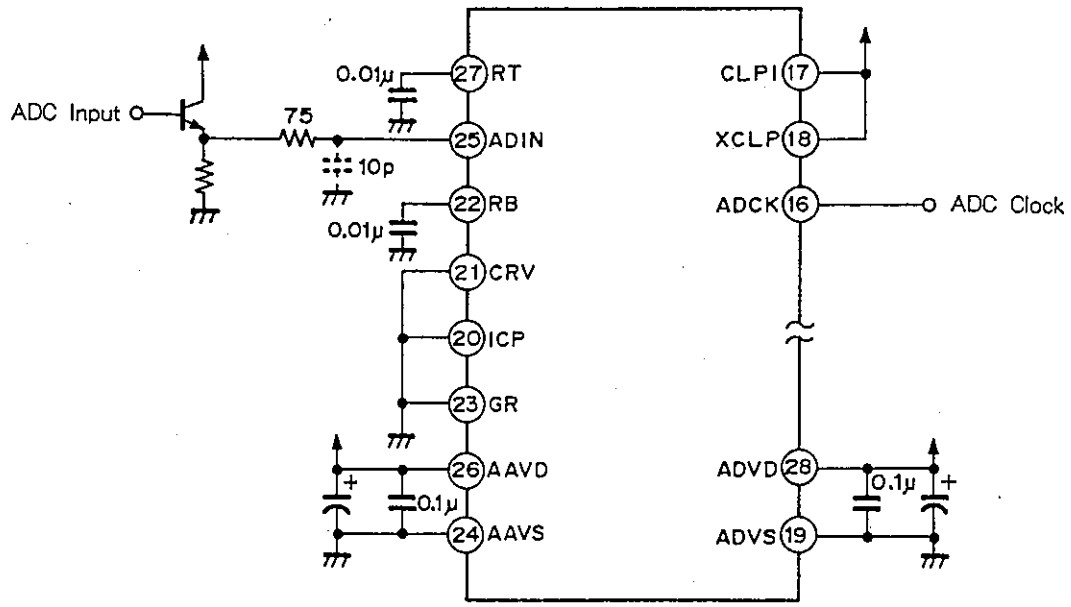
(1) Reduces the number of parts through the built-in A/D (one-channel) and D/A (two-channel) converters.
(2) Reduces cross color and improves frequency response characteristics when used with PAL.
(3) Pin assignments are compatible with CXD2024Q (comb filter for NTSC/PAL) in NTSC mode. (The external parts are the same.)
The edit for NTSC, PAL and NTSC/PAL systems can be done.
(4) Digital implementation eliminates ringing encountered in the glass delay lines.
(5) Lightens the load on manufacturing lines by eliminating the need for comb adjustment.

Application Circuit for A/D Converter

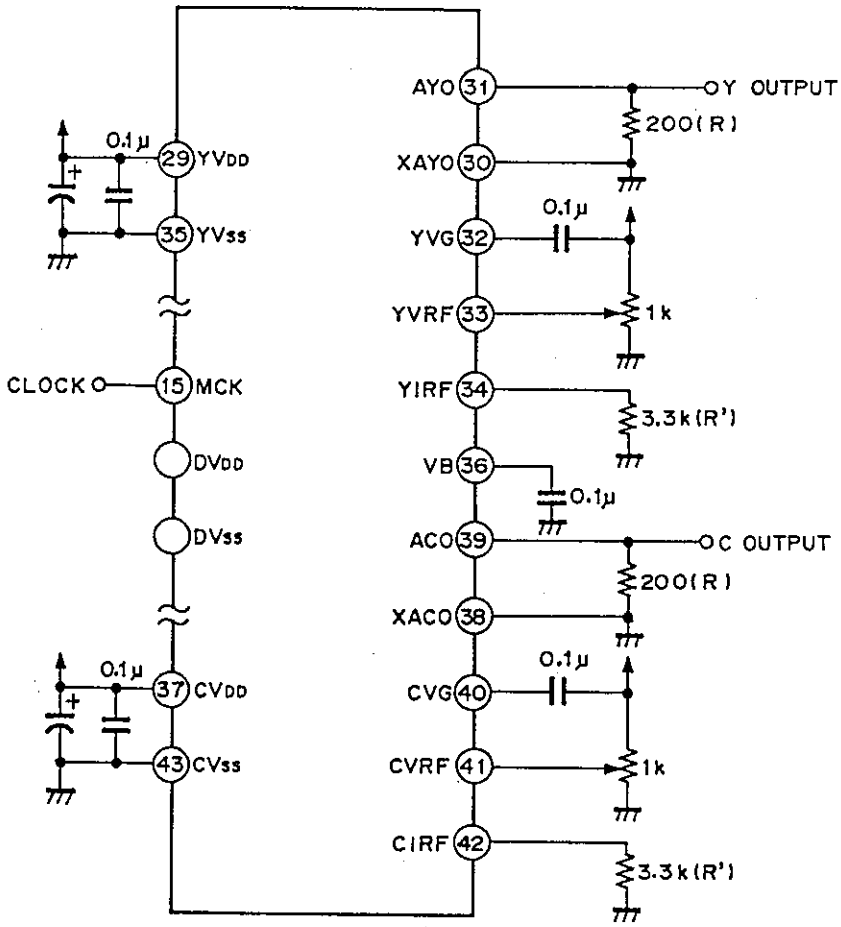
(1) In the case of input clamp pulse directly



(2) In the case of not using the internal clamp circuit



Application Circuit for D/A Converter



- Method of Selecting Output Resistance

  The CXD2023Q has a built-in current output type D/A converter. To obtain the output voltages, connect resistances to AYO and ACO pins.

  The voltage and current specs are:

  Output full-scale voltage: V_{FS}=0.5 to 2.0V

  Output full-scale current: I_{FS}=0 to 15mA

  Calculate the output resistance using the relationship $V_{FS}=I_{FS}\times R$. In addition, connect an output resistance of 16 times the output voltage to the reference current pin (I_{REF}). In the case where the value comes to that cannot exist practically, use a value of resistance as close to the value calculated as possible.

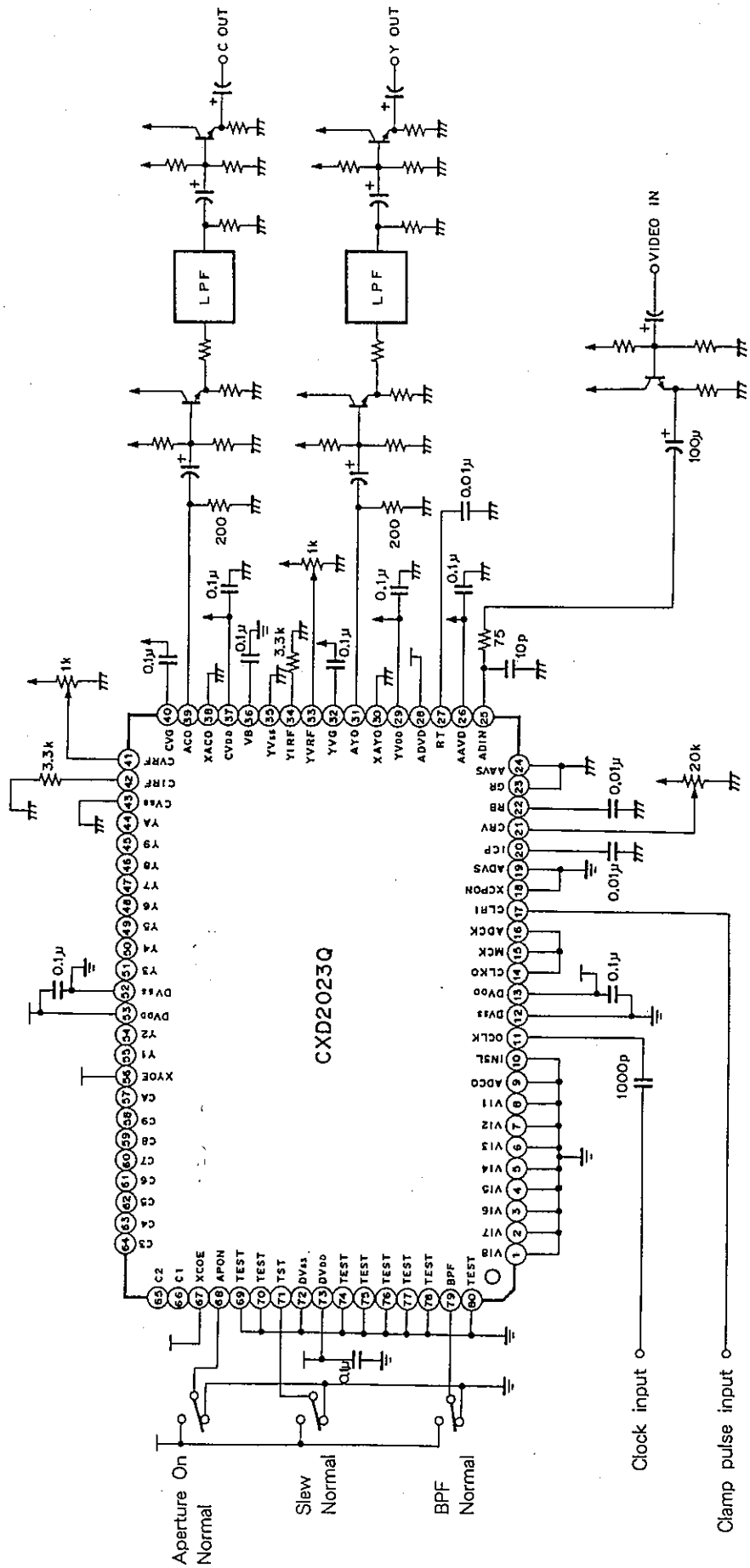
  Note that, at this time, $V_{FS}=V_{RF}\times 16R/R'$

  where R is the resistance connected to I/O, and R' is the resistance connected to I_{RF}. Power consumption can be reduced by using higher resistance values, but then glitch energy and data settling time increase contrastingly. Select the resistance values most suited to the system application.

- V_{DD}, Vss

  Separate the analog and digital systems around the device to effect noise. YV_{DD} and CV_{DD} are respectively by-passed to YVss and CVss as close to each other as possible through ceramic capacitor of about 0.1 μF.

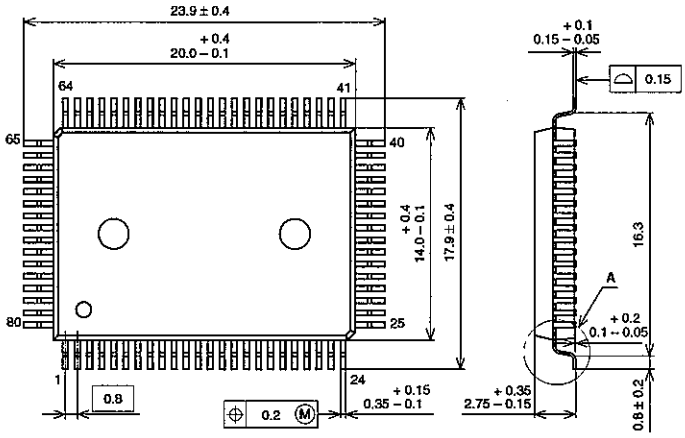
Application Circuit

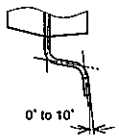


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit: mm

80PIN QFP (PLASTIC)





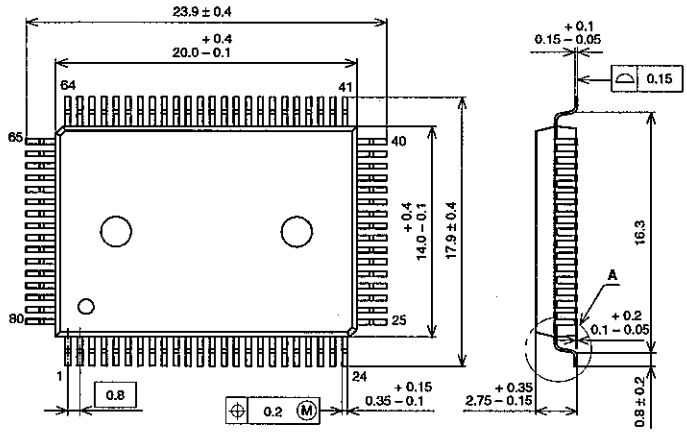
DETAIL A

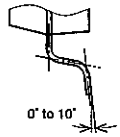
SONY CODE	QFP-80P-L01
EIAJ CODE	QFP080-P-1420
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.6g

80PIN QFP (PLASTIC)





DETAIL A

SONY CODE	QFP-80P-L01
EIAJ CODE	QFP080-P-1420
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.6g

LEAD SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	ALLOY 42
LEAD TREATMENT	Sn-Bi 2.5%
LEAD TREATMENT THICKNESS	5-18μm