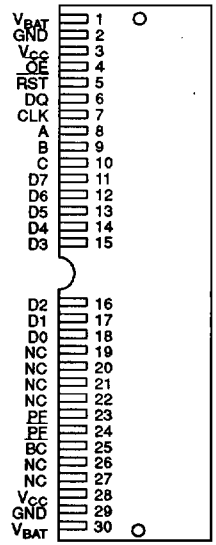
DALLAS SEMICONDUCTOR

DS2262
MegaStore Stik

FEATURES

- Solid-state mass storage subsystem using nonvolatile DRAM
- Versions with 4 and 8 megabits available
- DRAM timing and refresh control performed transparently to host
- Nonvolatile data retention using an external 6-9 volt backup supply
- Low-power data retention mode consumes less that 3 mA (4 megabit version)
- Backup supply can be switched off under host software control for conserving energy
- 3-wire serial port can access DRAM data at up to 1 megabit/second in burst mode
- Unique backup supply gas gauge continuously reports battery condition
- Power fail detect write-protects memory at either 5% or 10% of 5 volt main supply
- Mates with JEDEC-standard 30 pin SIMM edge connectors (right angle and vertical)

PIN ASSIGNMENT



PIN DESCRIPTION

V_{CC}	-	+5V Power Supply
V_{BAT}	-	Battery Supply
$\overline{OE}$	-	Option Enable
$\overline{RST}$	-	Reset
DQ	-	Serial Port Data I/O
CLK	-	Clock
A, B, C	-	DRAM Select
D7-D0	-	DRAM 0-7 Data Outputs
PF, $\overline{PF}$	-	Power Fail Outputs
$\overline{BC}$	-	Battery Condition Output
GND	-	Ground

DESCRIPTION

The DS2262 MegaStore Stik is an extremely compact solid-state mass storage device that provides up to 8 megabits of nonvolatile DRAM for data storage. The DRAM and internal control functions are accessed using a 3-wire serial interface (CLK, D/Q, $\overline{RST}$) which can hook directly to the serial port of popular microprocessor/microcontroller devices such as the DS5000T/2250T Time Microcontroller family. All necessary DRAM timing and refresh duties are performed automatically.

An external backup supply such as a 6-volt battery can be attached to enable DRAM data retention, creating in effect a solid state disk drive. An internal circuit monitors the main +5V supply. Upon its failure, the DRAM is write-protected and the backup supply switched on.

With an inexpensive 1300 mA/Hr lithium battery, a DS2262 with 4 megabits can provide up to 3 weeks of continuous nonvolatile operation. If the failure of the main supply is relatively infrequent, the DS2262 can extend its nonvolatile operation for years, especially if the backup source is a rechargeable battery. A unique gas gauge circuit continuously monitors and reports the backup supply condition, warning the host of impending battery failure.

OPERATION - $\overline{OE}$ (PIN 4) HIGH

The main elements of the DS2262 are shown in Figure 1. Six signals control sending or retrieval of data using the address converter circuit. The signals CLK, $\overline{RST}$, and DQ comprise the DS2262 serial port. The signals A, B, and C control which DRAM data is written to. To transfer data into the DS2262, $\overline{RST}$ is first driven high while CLK is low. After sufficient setup time from $\overline{RST}$, one bit of data is placed onto the DQ line. With valid data on DQ, the CLK line is then transitioned low to high. The CLK transition causes the first bit of data to be transferred to the DS2262. If data is to be written to or read from one of the DRAMs, that DRAM must be selected on the A, B, and C pins when $\overline{RST}$ is brought high, and must remain selected until $\overline{RST}$ is brought low again to reset the serial port (see Table 2).

Information is written to the serial port in the form of a 24 bit address field followed by an 8 bit function code. 24 address bits are required regardless of the density of Stick used. Function codes are listed in Table 1. After a function code has been correctly entered, one or more data bits can be written to or read from a DRAM or the control registers. Data is read from the control registers by driving CLK low while $\overline{RST}$ is high. Data becomes valid on the DQ line after sufficient time is allowed for access. Reading from a DRAM selected by the A, B and C pins will place the correct data on the corresponding data line (D0-D7) after time is allowed for access, as well as on the DQ line. A read cycle is terminated when $\overline{RST}$ is returned low.

OPERATION - $\overline{OE}$ (PIN 4) LOW

When the $\overline{OE}$ pin is tied low, the A, B and C pins are replaced with a serial interface controlled by $\overline{RST}$, CLK, and DQ. To load the DRAM to be written, the $\overline{RST}$ pin is brought low and the DRAM select signals are clocked in, in the order C, B then A on DQ on the rising edge of the CLK pin. $\overline{RST}$ is then brought high to enable the entry of addresses and function codes into the control registers as described above. When the DS2262 is to be used with the $\overline{OE}$ pin low, the A, B and C pins should be left unconnected.

BURST MODE

When it is necessary to retrieve or write multiple consecutive bits of data from the DRAM, burst read or burst write function codes can be used to minimize protocol overhead. In this mode, the starting memory address is entered in the address field. This field is then incremented for each new clock cycle. Burst mode is terminated when $\overline{RST}$ is driven low. Each clock cycle for read or write operations is exactly the same as single bit transfers.

OPERATION - POWER LOSS AND DATA RETENTION

When the 5-volt V_{CCI} power begins to drop, an internal precision band-gap reference and comparator senses this change. Depending on the level of the tolerance pin, a power fail signal will be generated if V_{CCI} falls below 4.75 volts or 4.5 volts. (See DC Electrical specifications for detail.) The power fail outputs (PF,$\overline{PF}$) are driven active at this time and will remain active until V_{CCI} is restored to a normal condition. When the data retention mode begins, the DS2262 isolates the 3-wire serial port. If an active DRAM read/write cycle is in progress when power loss occurs, the DS2262 will complete this cycle properly before isolating the 3-wire serial port ($\overline{RST}$, CLK, D/Q). The V_{CCI} input is then disconnected from the V_{CCO} output and the backup supply connected to the V_{BAT} pin is switched in. The V_{BAT} input is normally connected to either a rechargeable battery or super capacitor. However, any backup supply with a voltage output between the limits of 6 and 10 volts is suitable. If nonvolatile operation is not desired, the BKUP input should be tied to the V_{CCI} pin; do not tie this pin low when not using the battery-backup function.

BATTERY GAS GAUGE

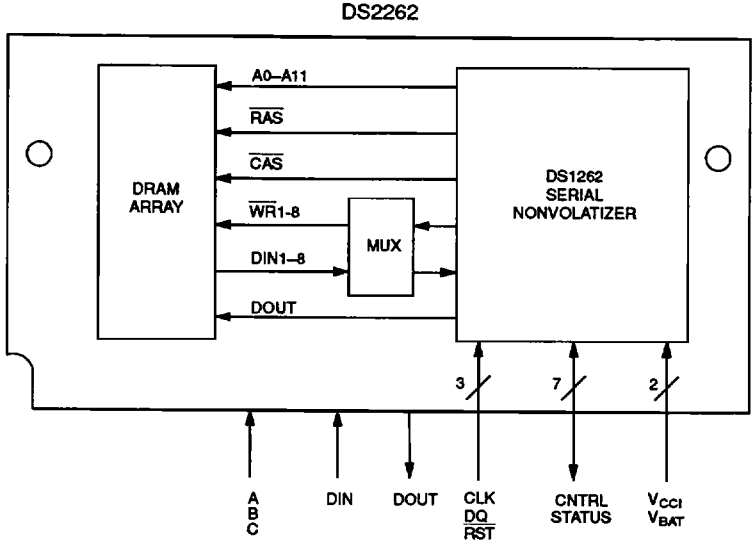
The DS2262 contains two features that provide information about the condition of the backup supply. First, the DS2262 monitors the backup supply input condition. If this input is below V_{CCI} the backup condition output pin ($\overline{BC}$) is driven active low and remains in this state until the backup supply voltage is restored to a level above V_{CCI}. This feature is active only while V_{CCI} is applied within nominal limits. Whenever the backup supply is providing power, the $\overline{BC}$ pin remains in a high impedance state.

The second feature for monitoring the condition of the backup supply is a gas gauge circuit, consisting of a counter that is decremented at 1 second intervals whenever the backup supply is providing power. This counter is initialized with a number by the user while V_{CCI} is within normal limits. The value of the counter is set by entering the desired binary value in the logic address field, followed by a write battery condition function code. The value is entered starting with the LSB of the address field and ending with the MSB of the address field followed by the correct function code. Information in the address field is automatically entered into the battery condition counter when $\overline{RST}$ is brought low to end the

cycle. The battery condition counter value can only be entered when V_{CCI} is within normal limits. No other action will take place when using the write battery condition function code.

The battery condition counter can be read by loading the address field with any value followed by a read battery condition function code. After this function code is entered, the next 24 clock cycles will output the value of the battery condition counter on the D/Q line. The value of the battery condition counter can only be read when V_{CCI} is within normal limits. No other action will take place when a read backup condition function code is used. The backup condition counter is a binary number representing the time allowed until the backup supply will be discharged. When the counter reaches zero, the $\overline{BC}$ pin will be driven low as soon as V_{CCI} is within normal limits. The $\overline{BC}$ pin will remain low until a new value is written into the battery condition counter. The correct value to enter into the counter can be calculated by dividing the capacity in ampere-hours of the backup supply by the average load current of the DRAM and converting this value into seconds.

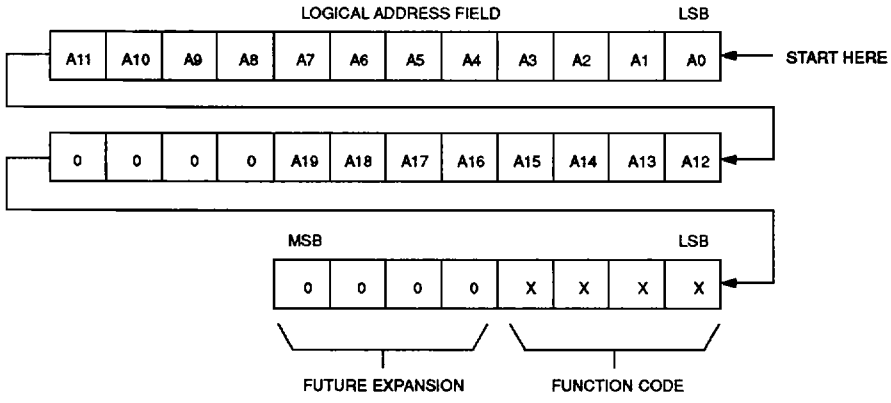
FUNCTIONAL DIAGRAM Figure 1



DRAM SELECTION Table 1

INPUTS			DRAM SELECTED
A	B	C	
0	0	0	0
1	0	0	1
0	1	0	2
1	1	0	3
0	0	1	4
1	0	1	5
0	1	1	6
1	1	1	7

SERIAL PORT PROTOCOL Figure 2



4

FUNCTION CODES Table 2

FUNCTION NAME	FUNCTION CODE (HEX)
BURST READ DRAM DATA READ DRAM DATA	00 01
READ BKUP COUNTER WRITE BKUP COUNTER	02 03
BACKUP SUPPLY ENABLED BACKUP SUPPLY DISABLED	0C 0D
WRITE DRAM DATA BURST WRITE DRAM DATA	0E 0F, FF

ABSOLUTE MAXIMUM RATINGS*

VOLTAGE ON ANY PIN RELATIVE TO GROUND	-0.3V TO +7.0V
VOLTAGE ON BKUP PIN RELATIVE TO GROUND	-0.3V TO +12V
OPERATING TEMPERATURE	0°C TO 70°C
STORAGE TEMPERATURE	-55°C TO 125°C
SOLDERING TEMPERATURE	260°C FOR 10 SECONDS

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Primary Power Supply	V_{CCI}	4.5	5.0	5.5	V	1
Input Logic High	V_{IH}	2.0		V_{CC}+0.3	V	1
Input Logic Low	V_{IL}	-0.3		+0.8	V	1
Backup Supply	V_{BAT}	5.5	8.0	10.0	V	1, 2

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CCI}=4.5V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}	-1.0		+1.0	µA	
DQ Leakage	I_{LO}	-1.0		+1.0	µA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	
Output Current @ 0.4V	I_{OL}	2.0			mA	
Input Supply Current	I_{CCI}		3.0	7.0	mA	
TOL Pin = V_{CCO}	V_{TP}	4.50	4.62	4.75	V	
TOL Pin = GND	T_{TP}	4.25	4.37	4.50	V	
Backup Supply Leakage	I_{BKUPL}		2	4	µA	
Backup Supply Quiescent	I_{BKUPQ}		2.0		MA	

CAPACITANCE

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	t_A=25°C	5	7	pF	
Output Capacitance	C_{OUT}	t_A=25°C	7	10	pF	
I/O Capacitance	$C_{I/O}$	t_A=25°C	7	10	pF	

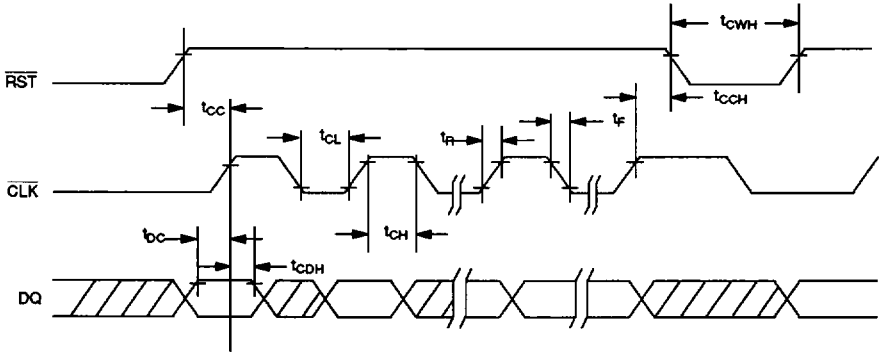
AC ELECTRICAL CHARACTERISTICS

(t_A=25°C, V_{CC}=5V ± 5%)

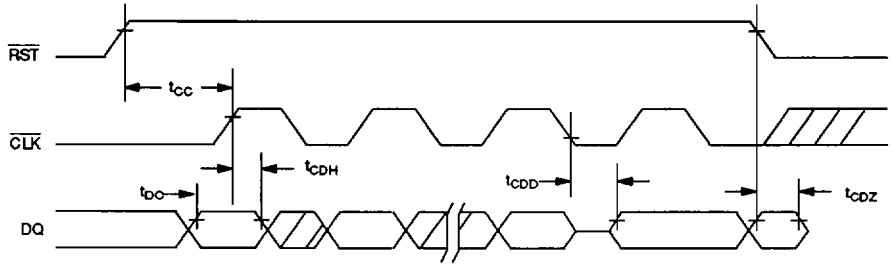
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
DQ to CLK Setup	t_{DC}	100			ns	
CLK to DQ Delay	t_{CDD}			200	ns	
CLK Low Time	t_{CL}	500			ns	
CLK High Time	t_{CH}	500			ns	
CLK Frequency	t_{CLK}	DC		1	MHz	
CLK Rise and Fall	t_R, t_F	3	10	20	ns	
$\overline{RST}$ to CLK Setup	t_{CC}	1			µs	
CLK to $\overline{RST}$ Hold	t_{CCH}	200			ns	
$\overline{RST}$ Inactive Time	t_{CWH}	1			µs	
$\overline{RST}$ to DQ in High Z	t_{CDZ}			100	ns	

4

WRITE DATA TRANSFER FROM SERIAL PORT



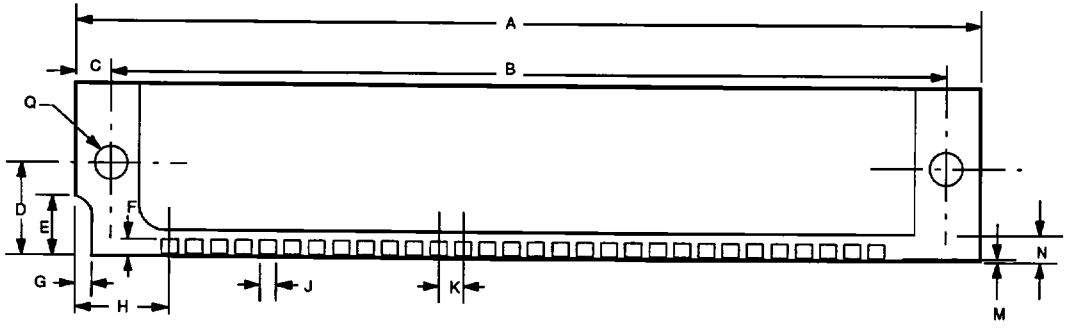
READ DATA TRANSFER FROM SERIAL PORT

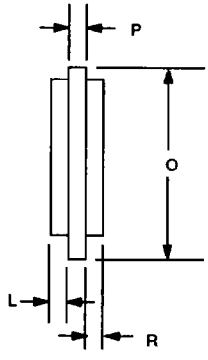


NOTES

1. All voltages are referenced to ground.
2. The $\overline{BC}$ pin will be driven active whenever V_{CCI} is within nominal limits and the backup supply is below V_{CCI}.
3. Load capacity is 100 pF.
4. Measured with all outputs open, $V_{CCI} = V_{IH} = 5.5$ V.
5. V_{TP} is the trip point where the internal switching circuits disconnects V_{CCI} and connects the internally regulated backup supply to the DRAMs.
6. Backup leakage current is the current into the BKUP pin when the backup supply has been disabled (via the 0D function code) and the DS2262 is in the data retention mode (V_{CCI}=0V).
7. Backup quiescent current is the current consumed by the DS2262 when in the data retention mode and the backup supply is enabled. Total current into the V_{BAT} pin in the data retention mode is this current plus the DRAM refresh current (see DRAM data sheet).

DS2262 MEGASTORE STIK





DIM	INCHES MIN
A	3.500
B	3.234
C	.0.133
D	.0.400
E	0.250
F	0.070 MIN.
G	.0.080
H	0.300
J	0.070
K	.0.100
L	.0.185 MAX.
M	.0.010 MAX.
N	0.100 MIN.
O	0.855 MAX.
P	0.054 MAX.
Q	0.125
R	0.185 MAX.