M65830P,FP
DIGITAL DELAY

DESCRIPTION

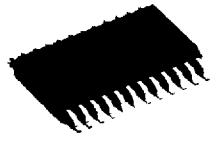
The M65830 is a CMOS IC developed to produce surround effects on TV sets and video disc players. Among the series, it has the highest degree of freedom in the selection of delay time, so it permits fine adjustments when mounted on a set.

FEATURES

- Selection of delay time in a range between 0.5msec and 32.0msec in 64 increments of 0.5msec
- Selection of delay time is controlled by serial data
- Built-in A-D, D-A converters, input/output low-pass filter, and 16K bit memory
- High sound quality is assured by simple system construction, due to A-D, D-A converters with ADM (Adaptive Delta Modulation) system
  - Output noise voltage : − 95.0dBV (typ)
  - Total harmonic distortion : 0.2% (typ)

Outline 24P4(P)

2.54mm pitch 600mil DIP
(13.0mm × 31.1mm × 3.8mm)



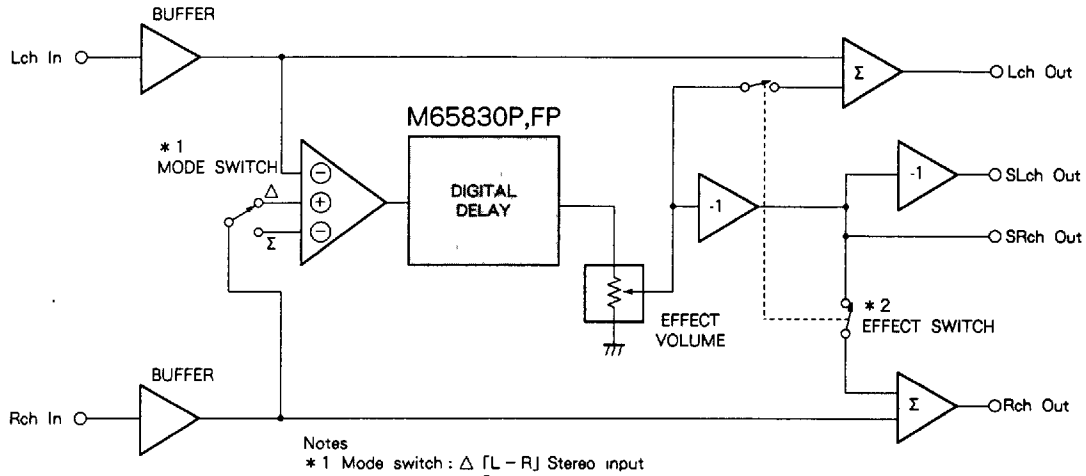
Outline 24P2W-A(FP)

1.27mm pitch 450mil SOP
(8.4mm × 15.0mm × 2.0mm)

RECOMMENDED OPERATING CONDITIONS

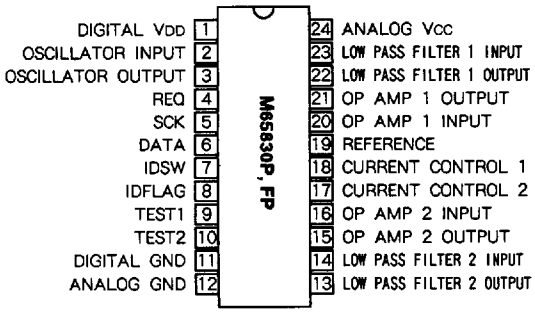
Supply voltage range ····· V_{CC}, V_{DD} = 4.5~5.5V
Rated supply voltage ····· V_{CC}, V_{DD} = 5V

SYSTEM CONFIGURATION



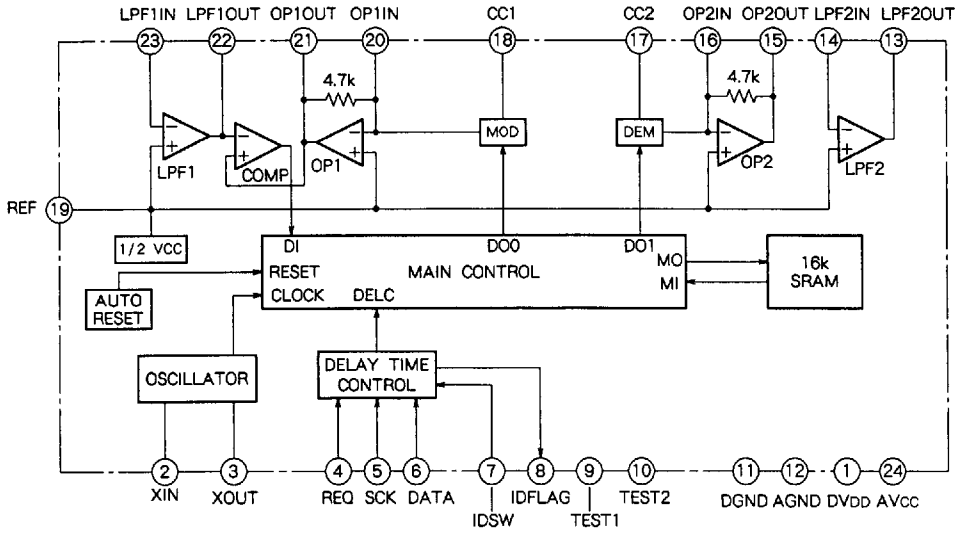
Notes
*1 Mode switch : Δ [L − R] Stereo input
Mode switch : Σ [L + R] Monaural input
*2 Effect switch ON : Surround output disabled (2 loudspeakers)
OFF : Surround output enabled (4 loudspeakers)

PIN CONFIGURATION



Outline 24P4(P)
24P2W-A(FP)

IC INTERNAL BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Symbol	Name	I/O	Function
①	V_{DD}	Digital power supply	–	
②	X_{IN}	Oscillator input	I	Connect a 2MHz ceramic oscillator
③	X_{OUT}	Oscillator output	O	Input an external clock, if used, to pin ②
④	REQ	Request	I	Data request input
⑤	SCK	Shift clock	I	Serial data shift clock input
⑥	DATA	Data	I	Serial data input
⑦	IDSW	ID switch	I	External input pin for 4th bit of ID code
⑧	IDFLAG	ID flag	O	Data input checking pulse and serial data output
⑨	TEST1	Test 1	–	L = normal mode
⑩	TEST2	Test 2	–	L = normal mode
⑪	D GND	Digital GND	–	
⑫	A GND	Analog GND	–	
⑬	LPF2 OUT	Low pass filter 2 output	O	Make up, with external C and R, a low pass filter on the output end
⑭	LPF2 IN	Low pass filter 2 input	I	
⑮	OP2 OUT	OP amp 2 output	O	Make up, with an external C, an integrator for demodulation
⑯	OP2 IN	OP amp 2 input	I	
⑰	CC2	Current control 2	–	Demodulator ADM control
⑱	CC1	Current control 1	–	Modulator ADM control
⑲	REF	Reference	–	Analog reference voltage = 1/2V_{CC}
⑳	OP1 IN	OP amp 1 input	I	Make up, with external C and R, an integrator for demodulation
㉑	OP1 OUT	OP amp 1 output	O	
㉒	LPF1 OUT	Low pass filter 1 output	O	Make up, with external C and R, a low pass filter on the input end
㉓	LPF1 IN	Low pass filter 1 input	I	
㉔	V_{CC}	Analog power supply	–	

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter		Ratings	Unit
V_{CC}	Supply voltage		6.5	V
I_{CC}	Circuit current		100	mA
P_d	Power dissipation	M65830P	1	W
		M65830FP	0.8	
T_{opr}	Operating temperature		−20∼+75	℃
T_{stg}	Storage temperature		−40∼+125	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Analog supply voltage		4.5	5	5.5	V
V_{DD}	Digital supply voltage		4.5	5	5.5	V
V_{CC}-V_{DD}	Voltage difference between V_{CC} and V_{DD}		−0.3	0	0.3	V
f_{ck}	Clock frequency		1	2	3	MHz
V_{IH}	Input voltage (H level)		0.7V_{DD}	–	V_{DD}	V
V_{IL}	Input voltage (L level)		0	–	0.3V_{DD}	V
f_{Sck}	Serial clock		–	–	4.0	MHz

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, f = 1kHz, Vo = 100mVrms, Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{CC}	Circuit current	No signal	–	16	35	mA
Gv	Input/output voltage gain	R_L = 47kΩ	−3.5	−0.5	2.5	dB
V_{Omax}	Max. output voltage	THD = 10%	0.7	1	–	Vrms
THD	Output distortion	30kHz LPF	–	0.2	1.0	%
No	Output noise voltage	DIN-AUDIO	–	−95	−75	dBV
SVRR	Power suppression ratio	△V_{CC} = −20dBV, f = 100Hz	–	−40	−25	dB
IccS	Sleep current	Current flowing under sleep mode condition	–	12	30	mA

FUNCTION DESCRIPTION

(1) Delay time

D6	D5	D4	D3	D2	D1	Delay time(ms)
L	L	L	L	L	L	0.5
					H	1.0
				H	L	1.5
					H	2.0
			H	L	L	2.6
					H	3.1
				H	L	3.6
					H	4.1
		H	L	L	L	4.6
					H	5.1
				H	L	5.6
					H	6.1
			H	L	L	6.7
					H	7.2
				H	L	7.7
					H	8.2
	H	L	L	L	L	8.7
					H	9.2
				H	L	9.7
					H	10.2
			H	L	L	10.8
					H	11.3
				H	L	11.8
					H	12.3
		H	L	L	L	12.8
					H	13.3
				H	L	13.8
					H	14.3
			H	L	L	14.8
					H	15.4
				H	L	15.9
					H	16.4

D6	D5	D4	D3	D2	D1	Delay time(ms)
H	L	L	L	L	L	16.9
					H	17.4
				H	L	17.9
					H	18.4
			H	L	L	18.9
					H	19.5
				H	L	20.0
					H	20.5
		H	L	L	L	21.0
					H	21.5
				H	L	22.0
					H	22.5
			H	L	L	23.0
					H	23.6
				H	L	24.1
					H	24.6
	H	L	L	L	L	25.1
					H	25.6
				H	L	26.1
					H	26.6
			H	L	L	27.1
					H	27.6
				H	L	28.2
					H	28.7
		H	L	L	L	29.2
					H	29.7
				H	L	30.2
					H	30.7
			H	L	L	31.2
					H	31.7
				H	L	32.3
					H	32.8

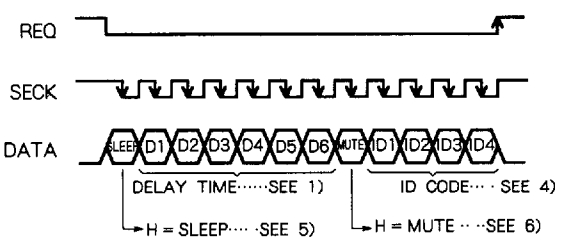
Note. D1~D6 for delay time setting correspond to D1~D6 in serial data (see (3))

(2) Sampling frequency fs

fs = 500kHz (if master clock frequency f_{ck} = 2MHz)

(3) Delay time setting

Delay time can be controlled by means of serial data inputted in the following timing from a microcomputer.



DATA is read at the negative-going edge of SCK. The last 12 bits are loaded at the positive-going edge of REQ.

(4) ID code and IDSW pins

ID code is used to control each IC in case more than one pieces of the M65830P, FP are used or other ICs are concurrently used.

IDSW is the control pin for reading serial data.

If an ID code inputted does not meet the following conditions 1 or 2, or an ID code is inputted to an external setting pin other than that indicated below (pin ⑦IDSE), the IC cannot read serial data, and the previous setting conditions remain in effect.

ID CODE SETTING TABLE

Condition	External setting pin	ID code				DATA READ
	Pin ⑦ IDSW	ID1	ID2	ID3	ID4	
1	L	L	L	H	L	Enabled
2	H	L	L	H	H	Enabled

(5) Sleep mode

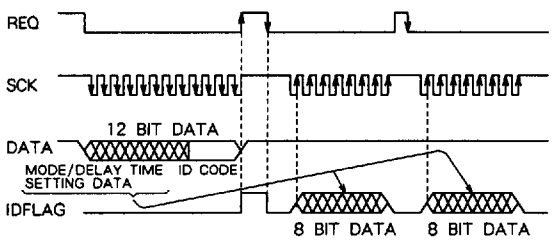
In sleep mode, ① the output is muted ; ② the internal input clock stops ; and ③ memory operation stops, so the IC becomes inactive. This mode is controlled by serial data SLEEP in the following manner : "H" : sleep mode ; "L" : normal mode.

(6) Muting

If serial data MUTE is "H," the IC compulsively performs the mute function ; if "L," muted condition is canceled.

(7) IDFLAG

The IDFLAG pin outputs a "H" signal if serial data from microcomputer or the like is correctly inputted. In addition, this pin, for checking purposes, outputs serial data containing information about the currently set operation mode.



(8) Reset

The IC is reset automatically when powered up. Then approximately 120msec later (provided that Vcc = 5V and C connected to pin ⑲ = 47μF), the reset state is automatically released. At this point delay time is set to 20.0msec.

※About reset time

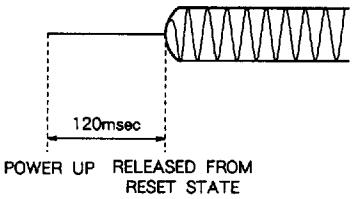
The factors that determine the IC's reset time is the internal resistance R of the IC and the value of capacitor C connected to pin ⑲(REF). The reset time is obtained by the following equation.

Reset time = 2.5 × C [μF]

Example : If external capacitor C connected to pin 19 = 47μF and Vcc = 5V :

Reset time = 2.5 × 47 = 117.5 [msec]

* Accordingly, reset time will be approximately 120msec.

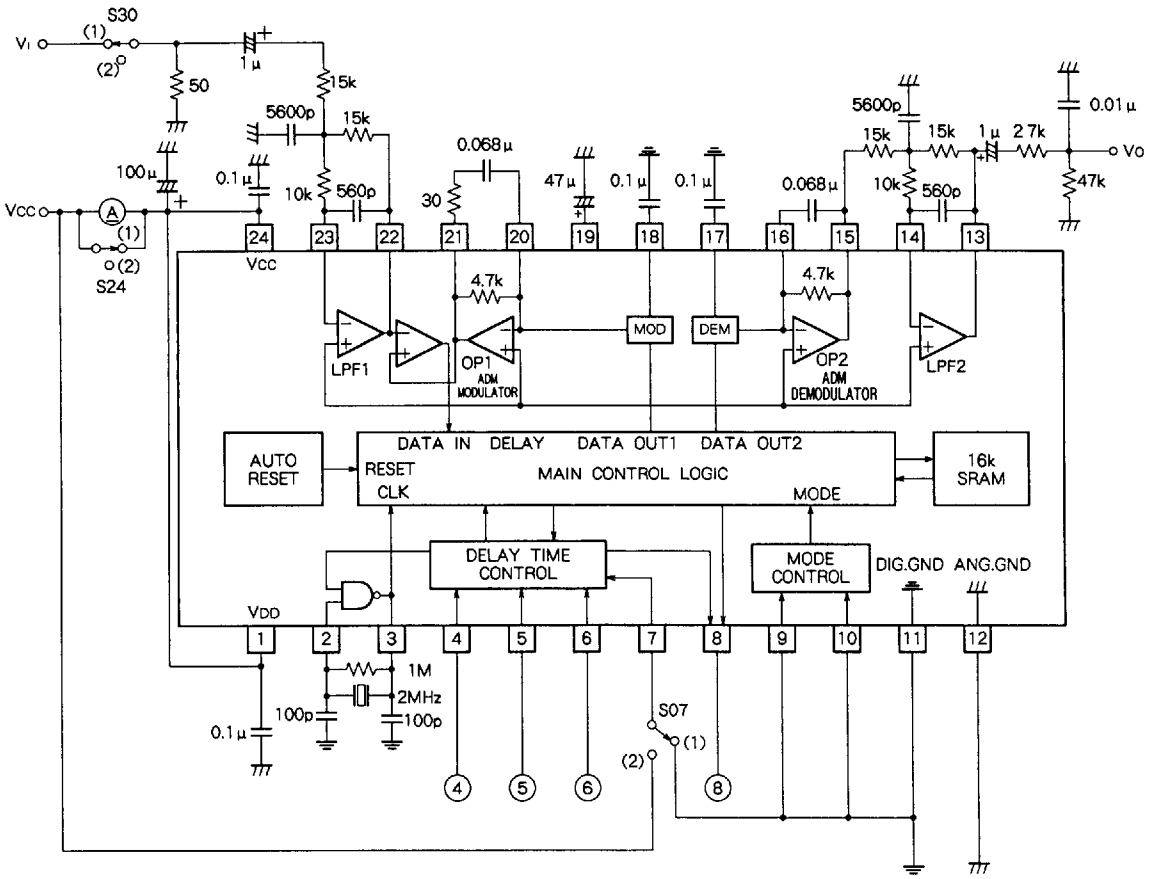


TEST CONDITIONS

Symbol	Parameter	Conditions	Pin			Switch			Remark
			4	5	6	S7	S24	S30	
Icco	Circuit current	No signal	*	*	*	#	2	2	
Gv	Voltage gain		*	*	*	#	1	1	Gv = 20log(Vo/Vi)
Td	Delay time		*	*	*	#	1	1	See 1)
Vomax	Max. output voltage	THD = 10% 30kHz L. P. F	*	*	*	#	1	1	
THD	Total high-harmonic distortion	30kHz L. P. F	*	*	*	#	1	1	
No	Output noise voltage	Vi = 0mVrms DIN AUDIO	*	*	*	#	1	2	
SVRR	Power suppression ratio	f = 100Hz ΔVcc = − 20dBV	*	*	*	#	1	2	
Iccs	Sleep current	Sleep mode selected	*	*	*	#	1	1	

* · ·Set to "L" or "H" after serial data is inputted (See 3)
#···1 or 2 (See the ID code setting table in (See 4))

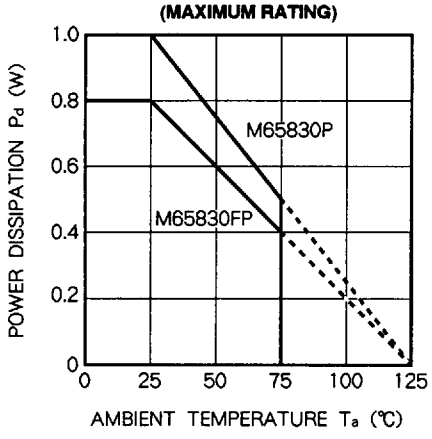
TEST CIRCUIT



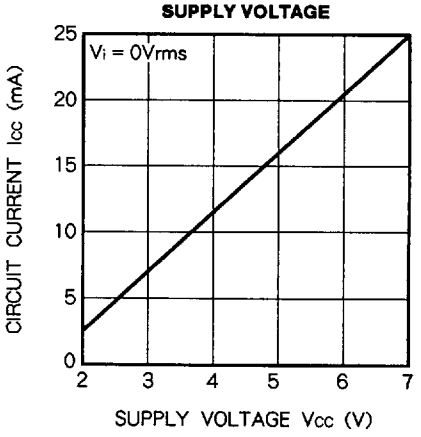
Units Resistance : Ω
Capacitance : F

TYPICAL CHARACTERISTICS

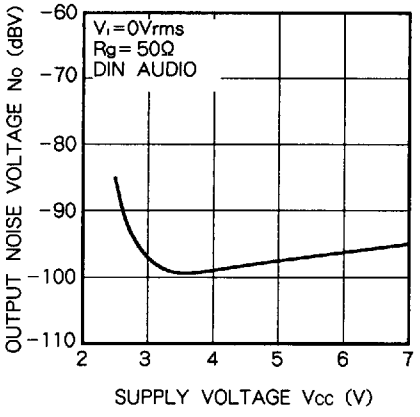
THERMAL DERATING (MAXIMUM RATING)



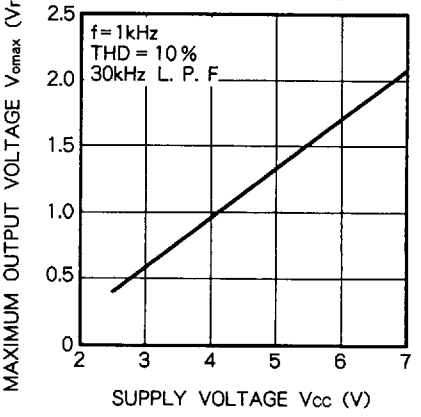
CIRCUIT CURRENT VS. SUPPLY VOLTAGE



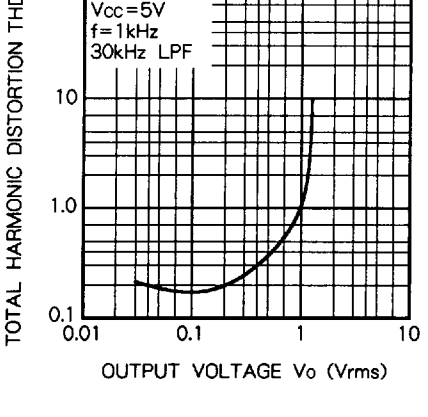
OUTPUT NOISE VOLTAGE VS. SUPPLY VOLTAGE



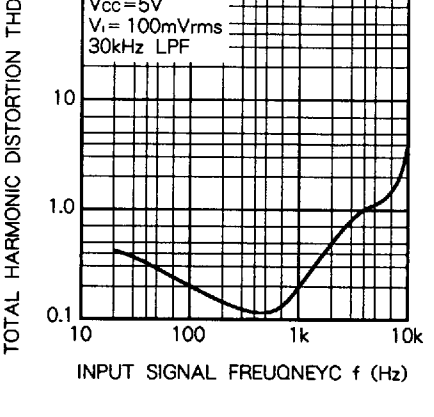
MAXIMUM OUTPUT VOLTAGE VS. SUPPLY VOLTAGE



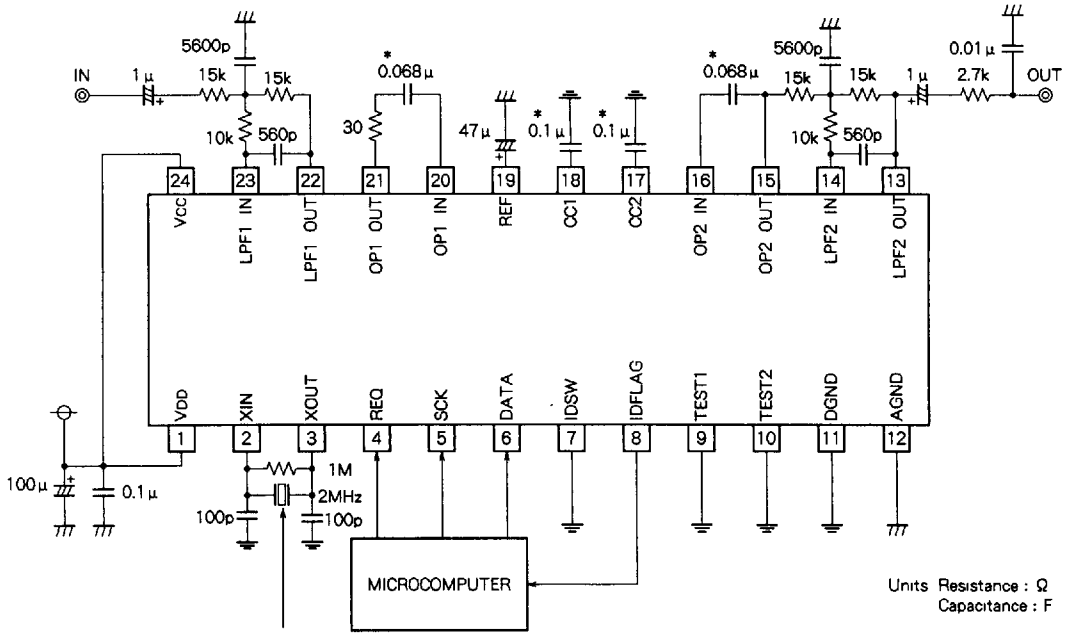
TOTAL HARMONIC DISTORTION VS. OUTPUT VOLTAGE



TOTAL HARMONIC DISTORTION VS. INPUT SIGNAL FREQUENCY



APPLICATION EXAMPLE



CERAMIC RESONATOR
MANUFACTURED BY MURATA
MFG CO., LTD.

* The relative precision of capacitors marked with a * should be within ± 5%