R8069
Line Interface Unit (LIU)

INTRODUCTION

The Rockwell R8069 Line Interface Unit (LIU) is a single chip CMOS device that interfaces the Rockwell R8070 T1/CEPT PCM Transceiver or RT9170 Intelligent T1 Controller to the physical T-1/CEPT PCM30 transmission medium.

The R8069 LIU device contains analog and digital circuits which are based on CMOS technology to support the line interface function required in ISDN primary rate transmission. The R8069 provides capabilities for 4-wire transmission of image, voice, or data signals; clock extraction; line equalization; bipolar violation detection; jitter accommodation; and AIS (Blue Alarm) generation and detection. In addition, the device operates at 1.544 or 2.048 Mbit/s and meets pulse shape and jitter requirements specified by T-1 or PCM30 standards, respectively.

The R8069 is ideally suited for image, voice, or data transmission required in ISDN primary rate applications. The device is highly integrated and requires minimal external components.

Internal LIU functions allow system designers to minimize their development cost and easily implement a T-1/PCM30 physical interface to primary rate lines without concern about most of the complex details normally associated with such a design. The R8069 also provides a high level of integration which increases system reliability, reduces space and achieves higher levels of performance and quality.

FEATURES

- Compatible with T-1 (1.544 Mbit/s) DSX-1 and PCM30 (2.048 Mbit/s) standards
- Selectable T-1 and PCM30 clock rates
- Directly compatible with Rockwell R8070 T-1/CEPT PCM Transceiver, RT9170 Intelligent T1 Controller, and R8071 ISDN/DMI Link Layer Controller devices
- Meets AT&T Technical Advisory No. 34 for T-1 and CCITT Recommendation G.703 for PCM30
- Meets jitter requirements specified in AT&T Publication 62411 (Oct. 1985) for T-1 and CCITT Recommendation G.823 for PCM30
- Phase locked loop for loop timing applications
- Provides line equalization for up to 660 feet of 100 Ω 22-gauge plastic insulated (ABAM) cable for T-1
- Accommodates pulse shape requirements for 75 Ω and 120 Ω lines in PCM30 application and 100 Ω T-1 lines
- Intrinsic jitter less than 0.05 UI
- Jitter attenuation roll off starts at 2 Hz
- Jitter tolerance above 0.4 UI for jitter frequency from 20 kHz to 100 kHz
- 44-bit receiver (RX) elastic store for input jitter and wander accommodation
- Provision to bypass RX elastic store
- Master/slave timing option
- Local and remote loopback modes
- AIS (Blue Alarm) generation and detection
- Bipolar violation detector
- Automatic detection of external line-rate clock (EXCLK)
- Automatic centering of phase-lock loop when timing reference is absent
- On-chip line drivers, pulse shaping, and TX equalizer
- Analog CMOS technology
- CMOS/TTL compatible inputs and outputs
- Operates from a single +5V power supply
- Packaging options
  - 28-pin plastic DIP
  - 28-pin CERDIP
  - 44-pin PLCC

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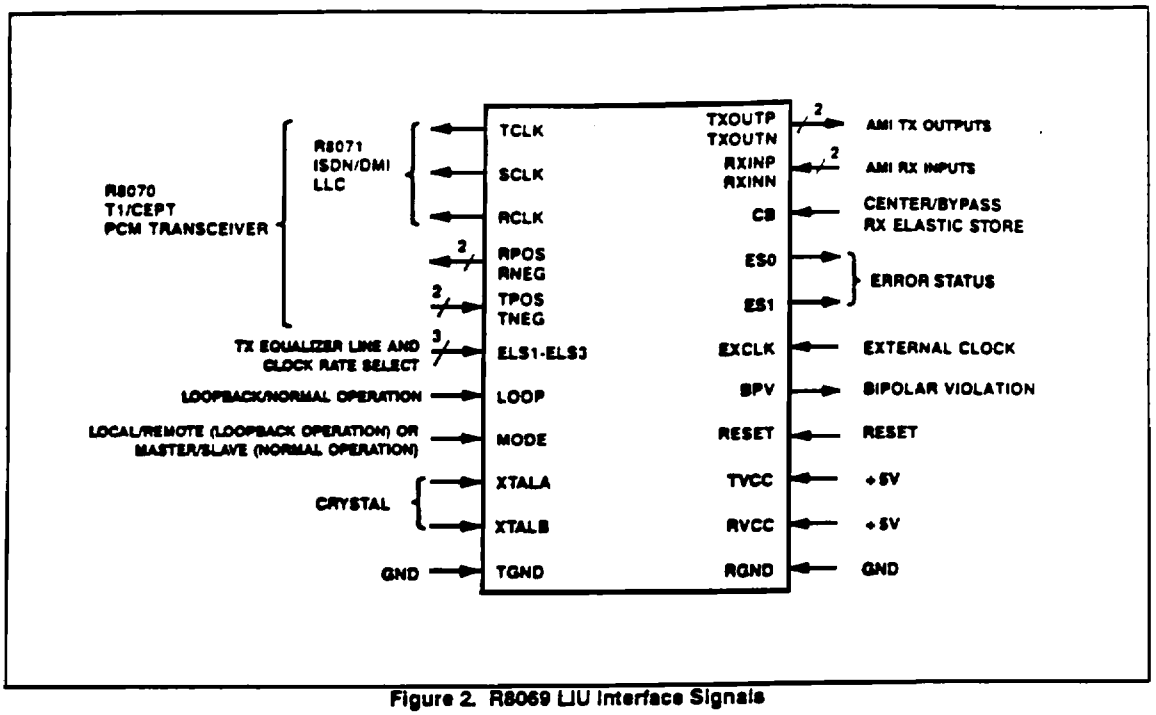


Figure 2. R8069 LIU Interface Signals

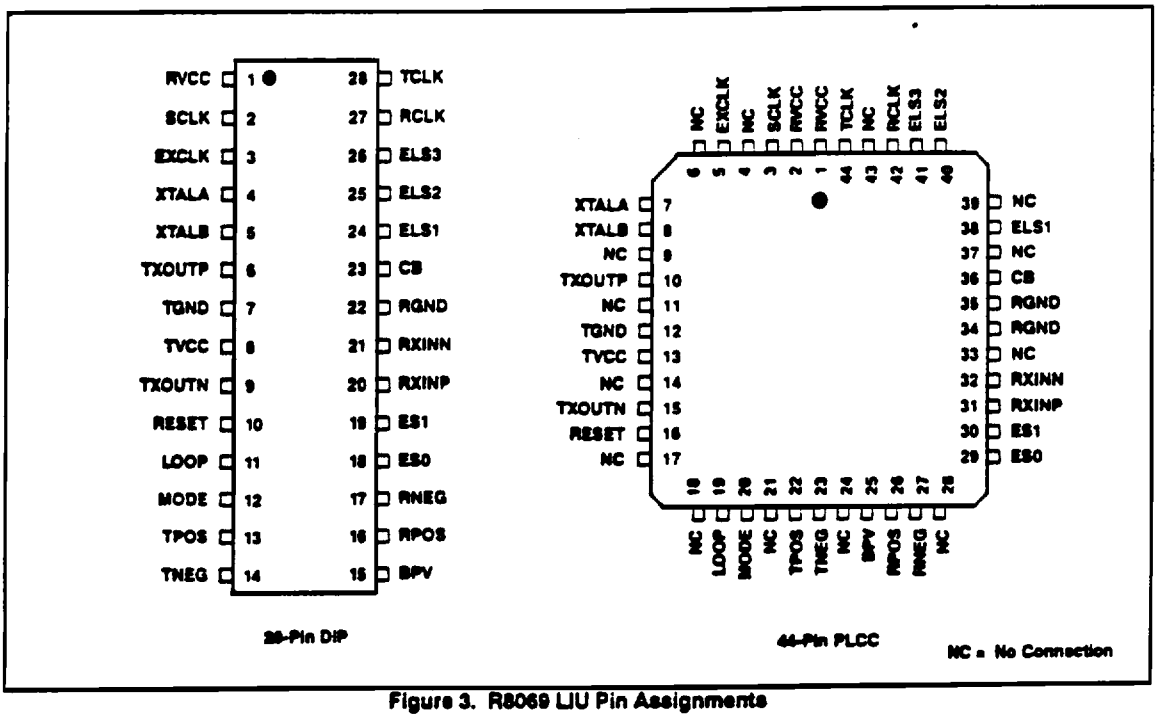


Figure 3. R8069 LIU Pin Assignments

Table 1. R8069 Interface Signal Descriptions (Cont'd)

Symbol	I/O	Name/Function
RESET	I	Reset. When Reset is asserted, the RX elastic store is centered, the VCO is trained to lock to EXCLK, or the crystal-based PLL2 if EXCLK is absent. This resetting mechanism is disabled when both LOOP and MODE inputs are high.
XTALA, XTALB	I	XTAL input pins. Connect an external, parallel resonant, 6.176 MHz or 8.192 MHz crystal to these pins for T-1 or PCM30 application, respectively. NOTE: Do not connect a TTL or CMOS clock source to these pins.
TVCC	I	Transmit Line Driver Power. +5V power supply for the transmit line driver.
TGND	I	Transmit Line Driver Ground. Ground for the transmit line driver.
RVCC	I	Power. +5V power supply.
RGND	I	Ground.

FUNCTIONAL DESCRIPTION

The R8069 LIU contains both analog and digital circuitry which independently process transmit and receive primary rate voice or data information. Circuitry to provide master, slave, local loopback, and remote loopback is also included. A simplified block diagram of the R8069 LIU is depicted in Figure 4. Typical R8069 LIU connections in CEPT and T-1 applications are shown in Figures 5, 6, and 7.

TRANSMIT SECTION

Unipolar transmit data (TPOS and TNEG) is clocked into the R8069 by the falling edge of TCLK. The transmit data goes to a line equalizer for pulse shaping and conditioning. The line equalizer will equalize up to 660 feet of 100 Ω ABAM cable (22-gauge plastic insulated cable with characteristics specified in Appendix B of the AT&T Technical Reference Number 34, September 1983)*.

Three encoded inputs, ELS1-ELS3, allow selection of cable length equalization and clock rates (Table 2). Equalization of cable length of 0-660 feet in increments of 110 feet is selectable for T-1 line. A 20 Ω resistor should to be connected in series with 75Ω coaxial cable connector (see Figure 5 and Table 2).

The equalized data is then provided to a line driver. In T-1 applications the driver can drive a twisted pair cable of up to 660 feet. The isolated pulse template at the end of the cable (at DSX-1) meets the pulse shape requirement specified by AT&T Technical Advisory No. 34. In PCM30 mode, the R8069 LIU provides a pulse shape which meets the requirements of CCITT Recommendation G.703. The pulse shape is measured at the output of the transmit transformer. The upper and lower limits of the T-1 or PCM30 pulse template were used to qualify the pulse shape.

* The R8069 was tested using AT&T ABAM cable part no. 606-6/22 R6900.

The DSX-1 pulse template for T-1 is specified by Table 3 and illustrated in Figure 8.

The output pulse waveform for PCM30 conforms to the template shown in Figure 9.

Table 2. ELS1 - ELS3 Encoding

ELS3	ELS2	ELS1	Cable Length/ Line Impedance	Clock Rate[1]
L	L	L	0 - 110 ft	T-1
L	L	H	110 - 220 ft	T-1
L	H	L	220 - 330 ft	T-1
L	H	H	330 - 440 ft	T-1
H	L	L	440 - 550 ft	T-1
H	L	H	550 - 660 ft	T-1
H	H	L	75/120 Ω[2,3]	PCM30

NOTES:

1. T-1 = 1.544 Mbits/s; PCM30 = 2.048 Mbits/s.
2. See Figures 5 and 6.
3. If the selected equalization line code is ELS3 = H, ELS2 = H, and ELS1 = L, then a 20 Ω resistor is required at the line side of the transmit transformer (see Figure 5). This is the recommended mode in a 75 Ω PCM30 application to ensure that the pulse shhape meets G.703.

   At the customer's option, the value ELS3 = H, ELS2 = H, and ELS1 = H may be selected and the 20Ω resistor can be deleted.. In this configuration, the pulse shape will normally conform to G.703, but is not guaranteed in every case.

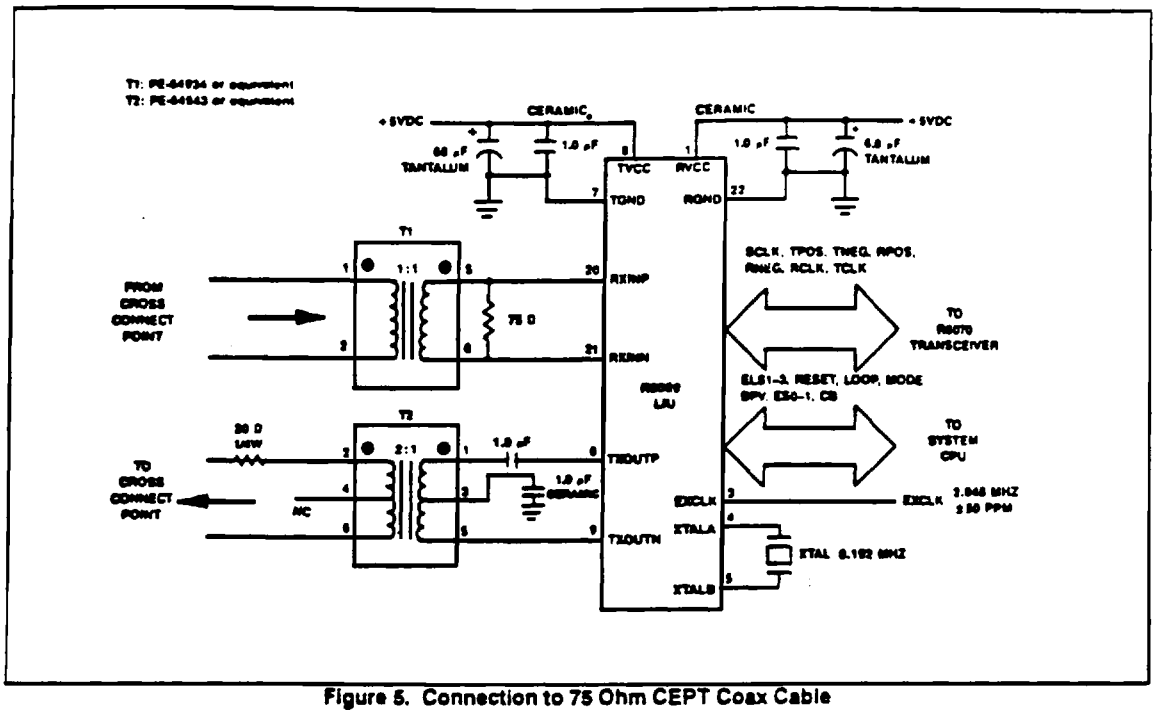


Figure 5. Connection to 75 Ohm CEPT Coax Cable

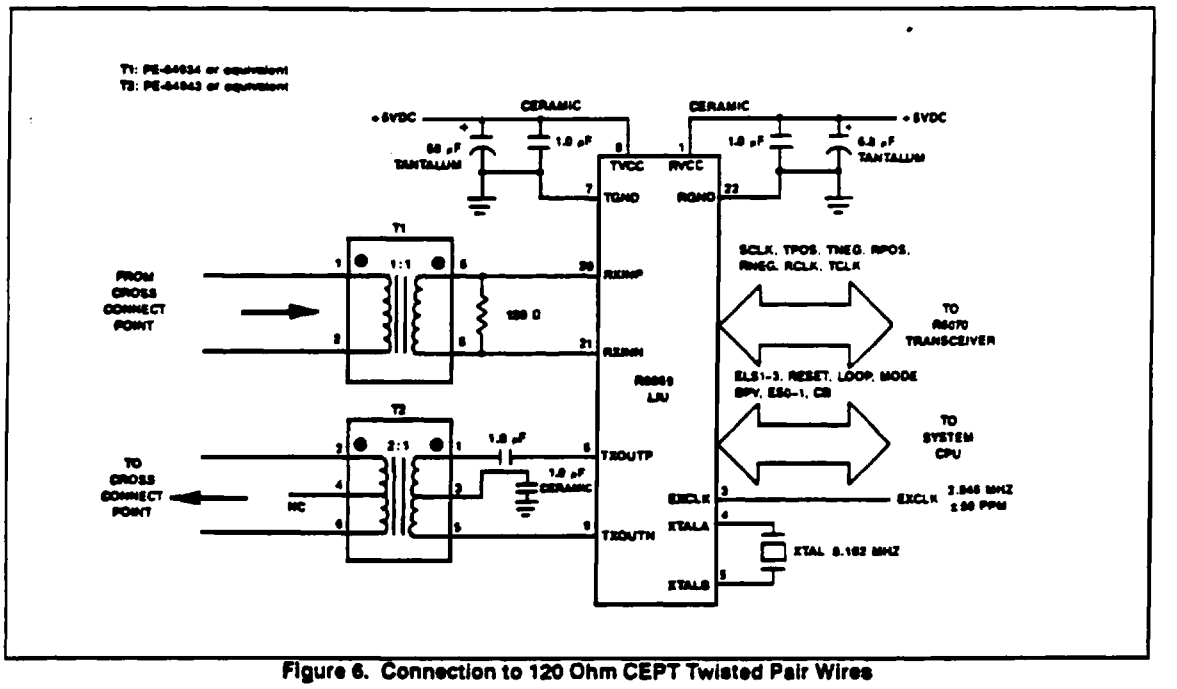
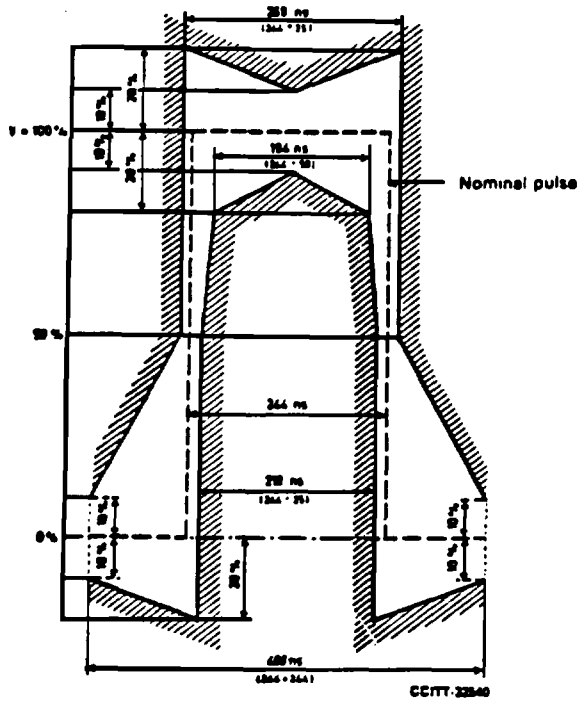


Figure 6. Connection to 120 Ohm CEPT Twisted Pair Wires



FOR
75 Ω LOAD IMPEDANCE: V = 2.37V
120 Ω LOAD IMPEDANCE: V = 3.00V
OPERATING FREQUENCY 2.048 MBPS
SOURCE: CCITT REC G.703

Figure 9. Isolated Pulse Template (PCM30)

MODE AND LOOP SELECTION

The basic modes of operation are as follows:

MODE	LOOP	Mode of Operation
Low	Low	Master Normal
High	Low	Slave Normal
Low	High	Local Loopback
High	High	Remote Loopback

MODE and LOOP signals are latched on the falling edge of EXCLK or TCLK (if no EXCLK is present) in master timing modes or on the falling edge of TCLK in slave timing modes.

MODE AND LOOP TIMING MODE

Mode and Loop modes are determined by the state of the MODE and LOOP pins. Refer to LOOP AND MODE SELECTION for selection details. For data alignment and clock sources, refer to Table 4.

Master Operation with EXCLK

TCLK and SCLK reference EXCLK while RCLK references RXINP/N or EXCLK. TPOS and TNEG are clocked in on the falling edge of TCLK. The source of TXOUTP/N is TPOS/TNEG. RPOS and RNEG are clocked out on the falling edge of RCLK (CB=1) or TCLK (CB=0). The source of RPOS/RNEG is RXINP/N.

Slave Operation with EXCLK

TCLK and SCLK reference the recovered clock while RCLK references RXINP/N. TPOS and TNEG are clocked in on the falling edge of TCLK. The source of TXOUTP/N is TPOS/TNEG. RPOS and RNEG are clocked out on the falling edge of RCLK (CB=1) or TCLK (CB=0). The source of RPOS/RNEG is RXINP/N.

Local Loopback with EXCLK

TCLK and SCLK reference EXCLK while RCLK references RXINP/N. TPOS and TNEG are clocked in on the falling edge of TCLK. TXOUTP/N transmit all ones. RPOS and RNEG are clocked out on the falling edge of TCLK. RPOS/RNEG are connected to TPOS/TNEG through the loopback circuit.

Remote Loopback with EXCLK

TCLK and SCLK reference EXCLK or RXINP/N while RCLK references RXINP/N or EXCLK. TPOS and TNEG are ignored. The source of TXOUTP/N is RXINP/N. RPOS and RNEG are clocked out on the falling edge of RCLK. The source of RPOS/RNEG is RXINP/N.

Master Operation without EXCLK

TCLK and SCLK reference the on-chip crystal oscillator nominal frequency while RCLK is based on RXINP/N or the crystal-based clock source. TPOS and TNEG are clocked in on the falling edge of TCLK. The source of TXOUTP/N is TPOS/TNEG. RPOS and RNEG are clocked out on the falling edge of RCLK (CB=1) or TCLK (CB=0). The source of RPOS/RNEG is RXINP/N.

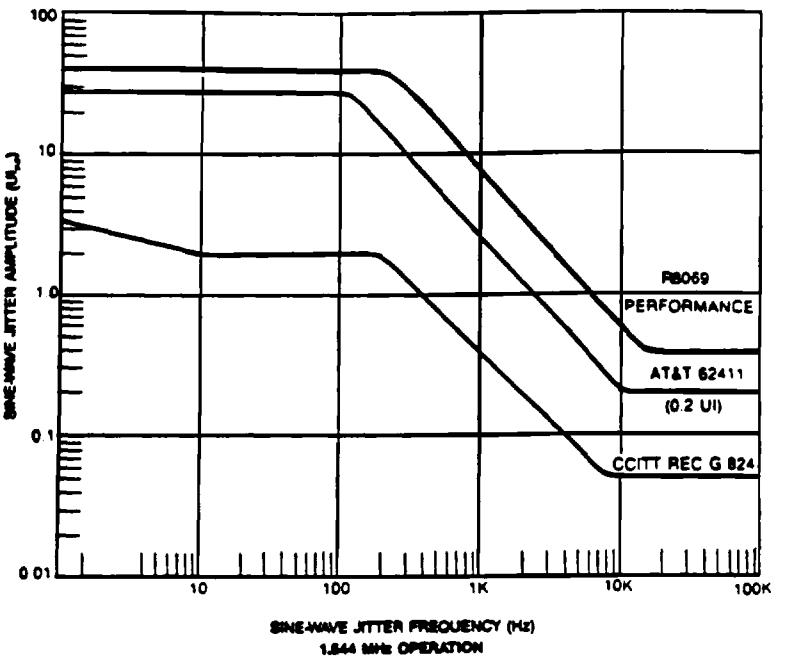
Slave Operation without EXCLK

TCLK, SCLK, and RCLK reference the on-chip crystal oscillator nominal frequency or RXINP/N. TPOS and TNEG are clocked in on the falling edge of TCLK. The source of TXOUTP/N is TPOS/TNEG. RPOS and RNEG are clocked out on the falling edge of RCLK (CB=1) or TCLK (CB=0). The source of RPOS/RNEG is RXINP/N.

Table 4. Data and Clock Sources

Timing/ Operation Mode	Input Pins* M	L	EXCLK Supplied?	Source of TCLK and SCLK: No Data on RXINP/N	Source of TCLK and SCLK: Data on RXINP/N	Source of TXOUTP/N	Source of RCLK: CB=0	Source of RCLK: CB=1 and Data on RXINP/N	Source of RCLK: CB=1 and No Data on RXINP/N	Source of RPOS/RNEG
With EXCLK										
Master	L	L	Y	EXCLK	EXCLK	TPOS/TNEG	RXINP/N	RXINP/N	EXCLK	RXINP/N
Slave	H	L	Y	EXCLK	RXINP/N	TPOS/TNEG	RXINP/N	RXINP/N	EXCLK	RXINP/N
Local Loopback	L	H	Y	EXCLK	EXCLK	All Ones	RXINP/N	RXINP/N	EXCLK	TPOS/TNEG
Remote Loopback	H	H	Y	EXCLK	RXINP/N	RXINP/N	RXINP/N	RXINP/N	EXCLK	RXINP/N
Without EXCLK										
Master	L	L	N	XTAL	XTAL	TPOS/TNEG	RXINP/N	RXINP/N	XTAL	RXINP/N
Slave	H	L	N	XTAL	RXINP/N	TPOS/TNEG	RXINP/N	RXINP/N	XTAL	RXINP/N
Local Loopback	L	H	N	XTAL	XTAL	All Ones	RXINP/N	RXINP/N	XTAL	TPOS/TNEG
Remote Loopback	H	H	N	XTAL	RXINP/N	RXINP/N	RXINP/N	RXINP/N	XTAL	RXINP/N

* M = MODE input; L = LOOP input.



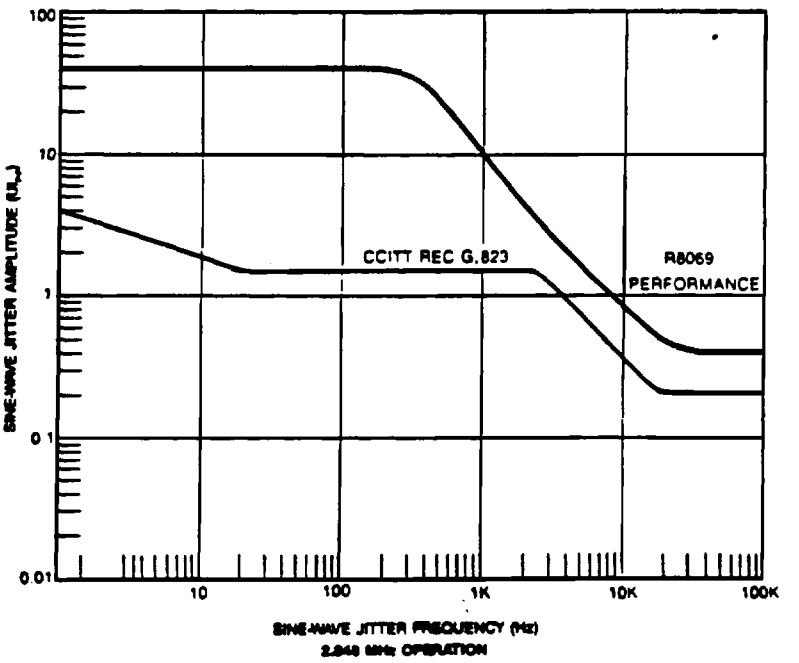


Figure 10. R8069 Input Data Jitter Tolerance

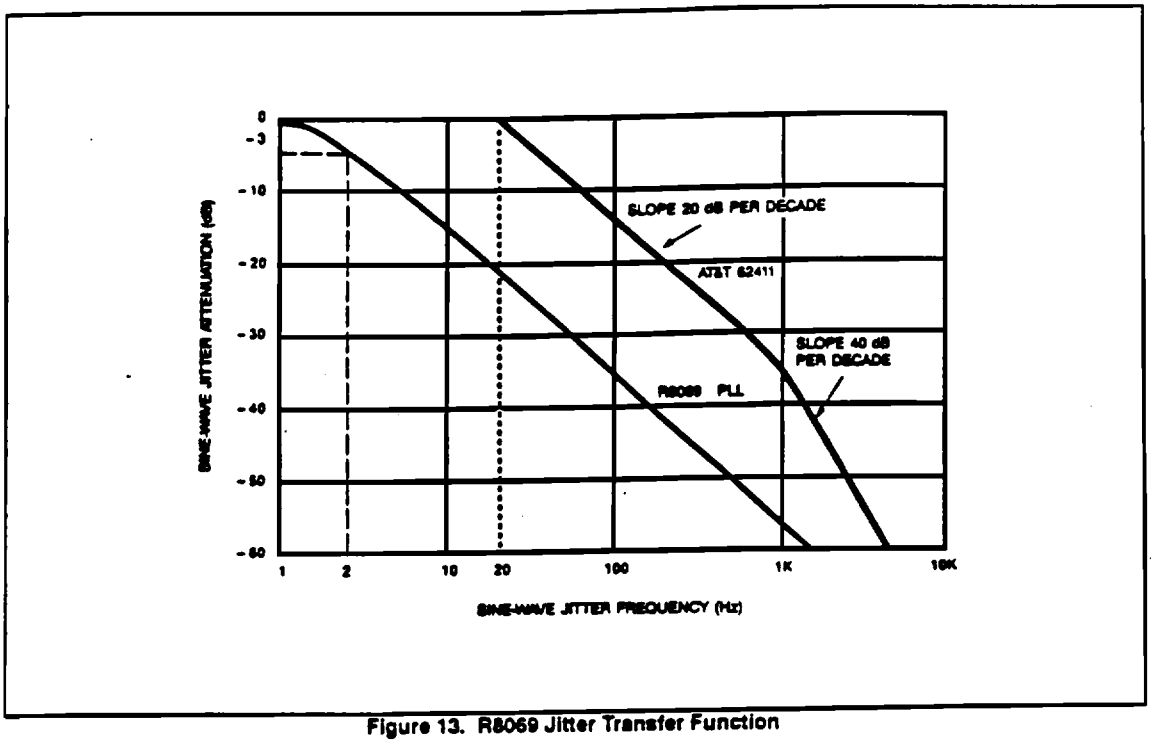


Figure 13. R8069 Jitter Transfer Function

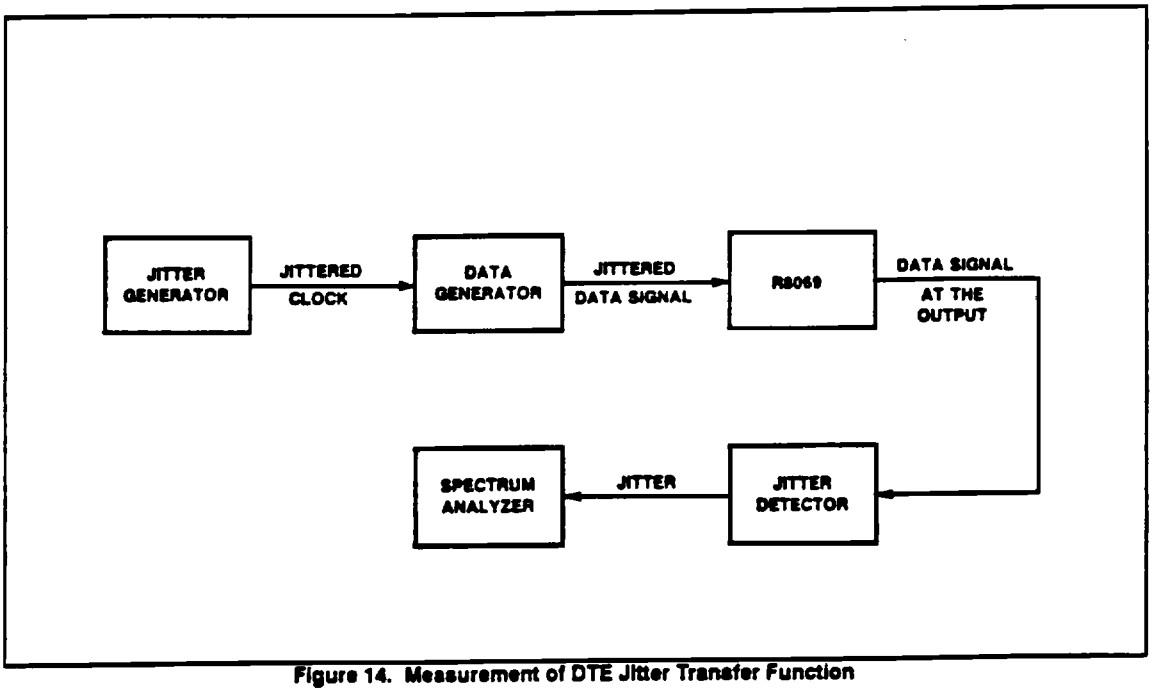


Figure 14. Measurement of DTE Jitter Transfer Function

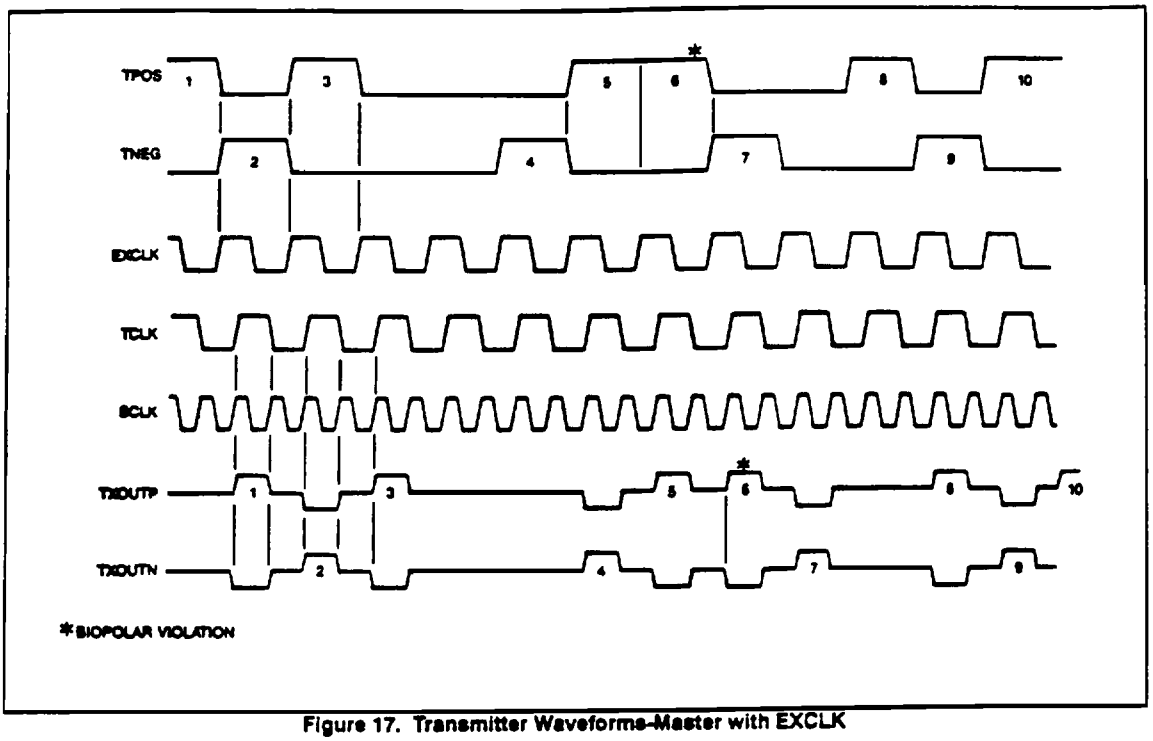


Figure 17. Transmitter Waveforms-Master with EXCLK

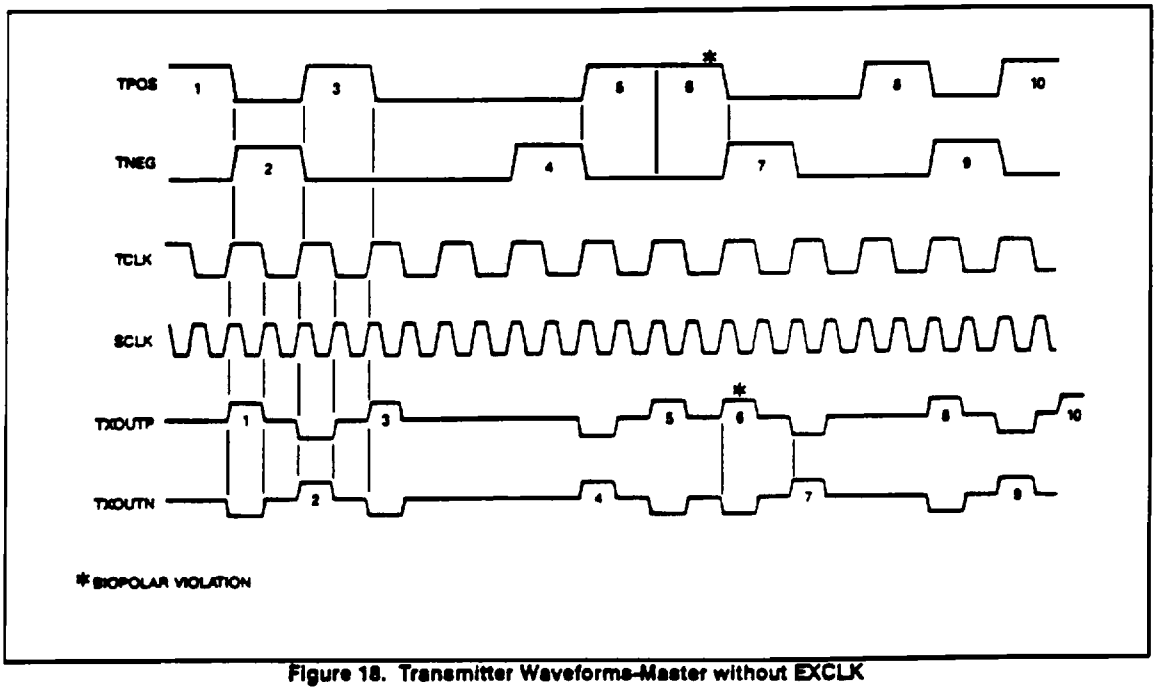


Figure 18. Transmitter Waveforms-Master without EXCLK

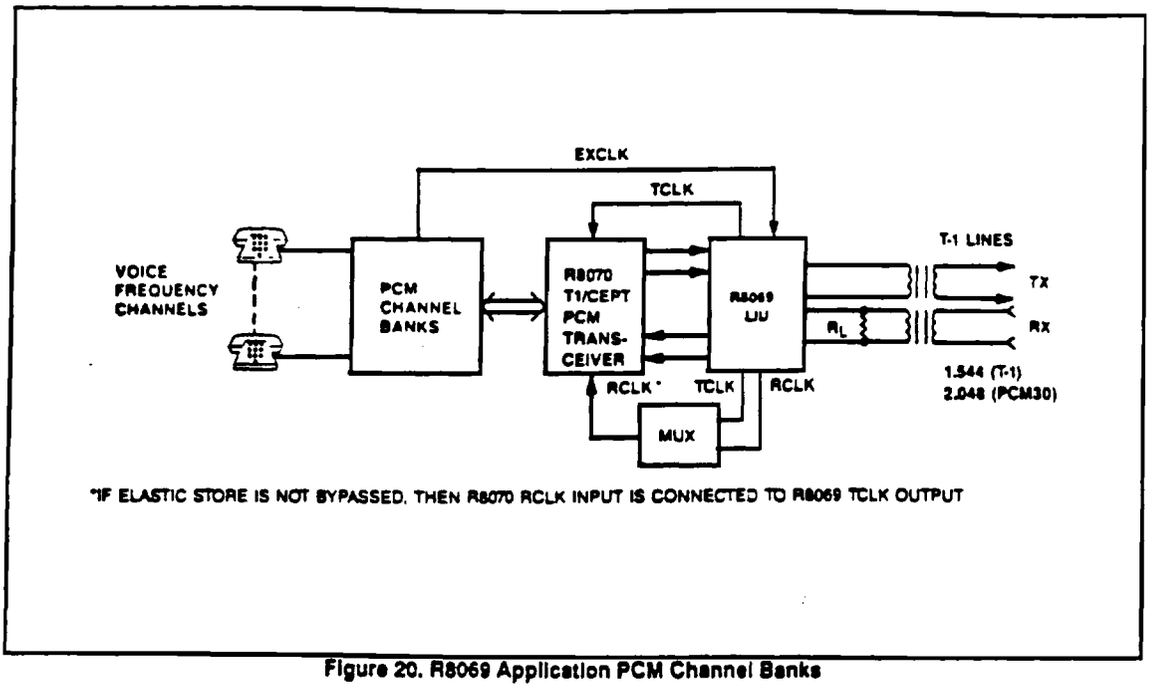


Figure 20. R8069 Application PCM Channel Banks

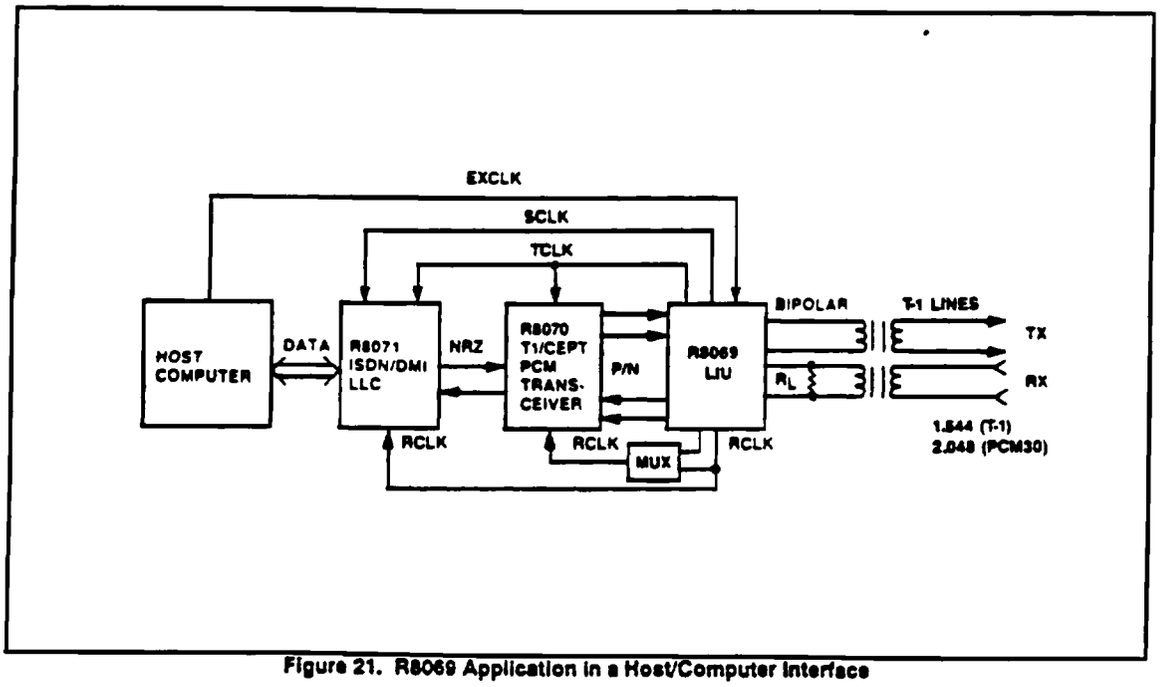


Figure 21. R8069 Application in a Host/Computer Interface

Table 6. Recommended Crystal Specifications

Parameter	Value
Nominal Frequency @ 25°C	
T-1	6.17600u MHz
PCM30	8.192000 MHz
Operating Temperature	0°C to 70°C
Storage Temperature	– 40°C to 85°C
Oscillator Mode	Fundamental
Resonance Mode	Parallel
Load Capacitance (C_L)	14 pF (see note 2)
Frequency Tolerance @ 25°C	± 0.001% (±10 ppm)
Temperature Stability @ 0°C to 70°C	± 0.003% (±30 ppm)
Pullability @ 25°C and C_L = 9.8 pF	
T-1	+200 ppm min.
PCM30	+120 ppm min.
Pullability @ 25°C and C_L = 23.0 pF	
T-1	–200 ppm min.
PCM30	–120 ppm min
Maximum Drive Level	2.5 mW
Series Resistance	50 Ω max.
Maximum Aging Per Year	2 ppm

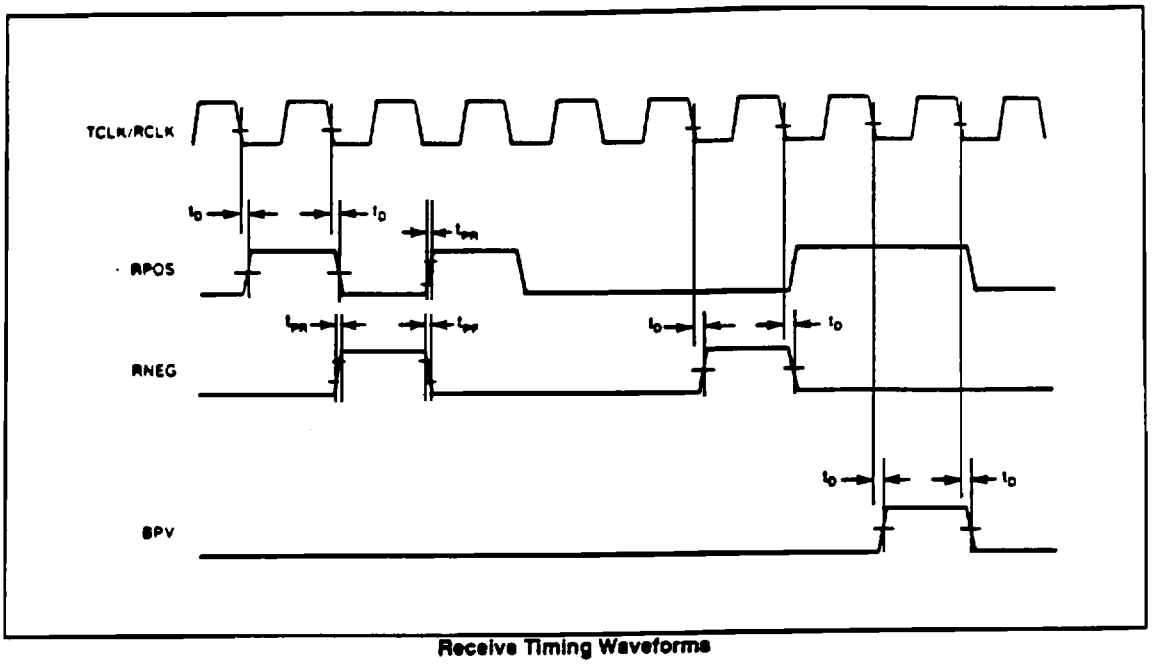
Notes:

1. This table is an example of typical crystal requirements for a system design with a pulling range of ± 130 ppm. For different pulling range requirements, refer to Application Note, R8069-Series Crystal Specifications, Order No. 355.
2. C_L includes typical 3.3 pF load capacitance due to board layout, crystal lead capacitance, and other stray capacitance, i.e.,
   $C_L = C_{UU\ LOAD} + C_{OTHER}$
   = 10.7 pF + 3.3 pF = 14 pF

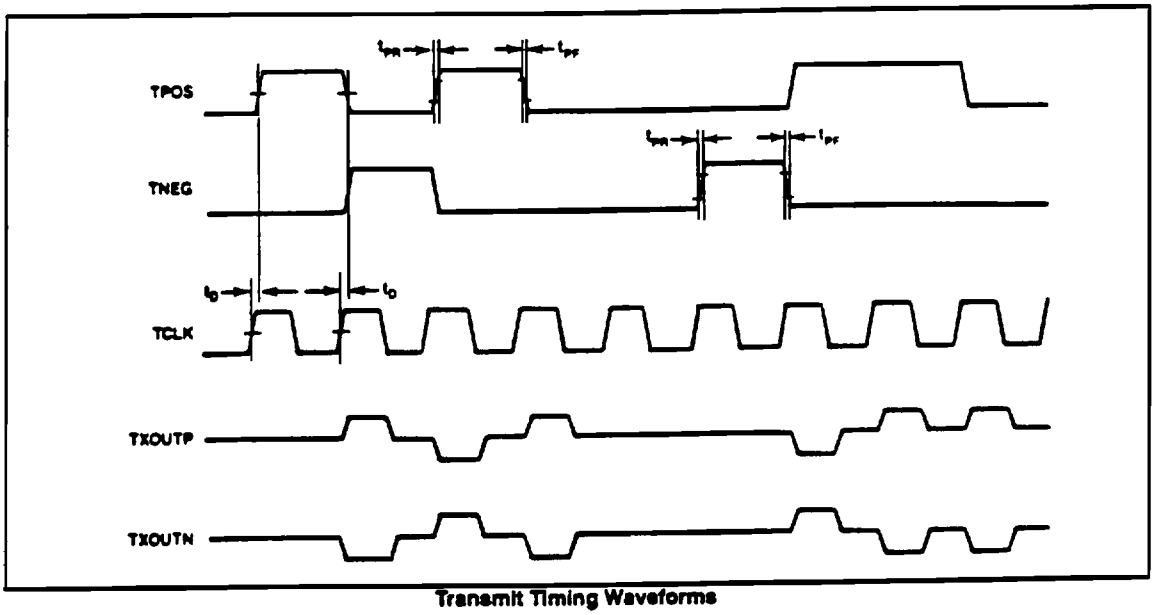
Table 7. Recommended R8069 Transformer

Parameter	Value
Transmit Transformer	
Turn Ratio	1CT:2CT
Rise/Fall Time	22 ns max.
Serial Resistance	0.7 Ω max.
Primary Inductance	1 mH min.
Isolation Voltage	1500 Vrms
Insulation Resistance	10,000 MΩ min.
Average Power Rating	500 mW
Leakage Inductance	0.30 µH - 0.55 µH
Receive Transformer	
Turn Ratio	1:1
Rise/Fall Time	22 ns max.
Serial Resistance	0.7 Ω max.
Primary Inductance	1 mH min.
Isolation Voltage	1500 Vrms
Insulation Resistance	10,000 MΩ min.
Average Power Rating	500 mW
Leakage Inductance	0.55 µH max.

SWITCHING CHARACTERISTICS - WAVEFORMS (CONT'D)



Receive Timing Waveforms



Transmit Timing Waveforms

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Units
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to V_{CC} + 0.3	Vdc
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{STG}	−55 to +150	°C

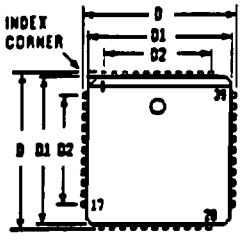
*NOTE: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL OPERATING CHARACTERISTICS[1]

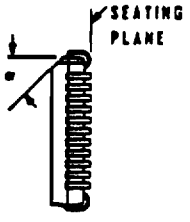
(V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0 Vdc, T_A = 0°C to 70°C, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Condition
Input Low Voltage	V_{IL}	−0.3	–	+0.8	V	
Input High Voltage	V_{IH}	+2.0	–	VCC +0.3	V	
Output Low Voltage	V_{OL}	–	–	0.4	V	I_{LOAD} = 1.6 mA
Output High Voltage						
TTL	V_{OH}	2.4	–	–	–	I_{LOAD} = −100 µA
CMOS	–	3.5	–	–	–	I_{LOAD} = −100 µA
Output Low Current	I_{OL}	+1.6	–	–	mA	V_{OL} = 0.4V
Output High Current	I_{OH}	−100	–	–	µA	V_{OH} = 3.5V
Input Capacitance	C_{IN}	–	–	5	pF	
Power Dissipation[2]	P_D				mW	
T-1 Mode						
Transmit Random Data						
330 ft.		–	270	305		
655 ft.		–	280	360		
Transmit All Ones						
330 ft.		–	350	430		
655 ft.		–	410	480		
PCM30 Mode						
Transmit Random Data		–	240	280		
Transmit All Ones		–	310	360		
Power Consumption[2]	P_C				mW	
T-1 Mode						
Transmit Random Data						
330 ft.		–	300	375		
655 ft.		–	340	410		
Transmit All Ones						
330 ft.		–	420	500		
655 ft.		–	500	570		
PCM30 Mode						
Transmit Random Data		–	260	300		
Transmit All Ones		–	350	400		
Parametric Tests						
Input High Current	I_{IH}	–	–	20	µA	V_{CC} = max., V_{IH} = 2.0V
Input Low Current	I_{IL}	–	–	20	µA	V_{CC} = max., V_{IL} = 0.8V

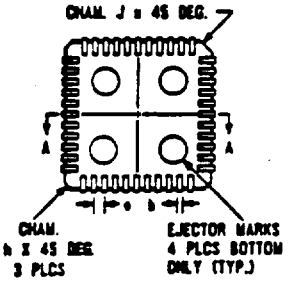
Notes: 1. Applies to all signals except TXOUTP, TXOUTN, RXINP and RXINN.
2. Power Consumption = Power dissipated in the device plus power delivered to the transmission line.



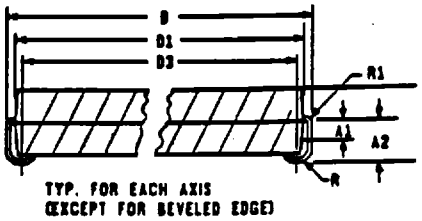
TOP VIEW



SIDE VIEW



BOTTOM VIEW



TYP. FOR EACH AXIS
(EXCEPT FOR BEVELED EDGE)

SECTION A-A

Dim.	Millimeters Min.	Millimeters Max.	Inches Min.	Inches Max.
A	4.14	4.39	0.163	0.173
A1	1.37	1.47	0.054	0.058
A2	2.31	2.46	0.091	0.097
b	0.457 TYP		0.018 TYP	
D	17.45	17.60	0.687	0.693
D1	16.46	16.56	0.648	0.652
D2	12.62	12.78	0.497	0.503
D3	15.75 REF		0.620 REF	
e	1.27 BSC		0.050 BSC	
h	0.254 TYP		0.010 TYP	
J	1.15 TYP		0.045 TYP	
α	45° TYP		45° TYP	
R	0.89 TYP		0.035 TYP	
R1	0.254 TYP		0.010 TYP	
Ref: PD44J/GP00-0166				

44-Pin PLCC