Am7970

Compression Expansion Processor (CEP)

DISTINCTIVE CHARACTERISTICS

- Compression/Expansion of digital two-tone image data using run-length and relative address coding.
  - Full-duplex capability for simultaneous independent compression and expansion.
  - High-performance 2 to 8 Mbps throughput with a 5-MHz clock.
- Compatible with CCITT recommendations T.4 and T.6 for Group 3 and Group 4 facsimile apparatus.
  - One-Dimensional, Modified Huffman Coding with optional Wraparound Mode.
  - Two-Dimensional, Modified READ (MR and MMR) coding with programmable K-Parameter.
- CPU Bus and optional local Document Store Bus with on-chip, dual-bus DMA controller.
  - 16-Mbyte physical addressing range on each bus.
- Transparent Mode transfer of unmodified data.
- Programmable paper width up to 16K picture elements and programmable top, left, and right margins.
- Optional Express Mode during compression and Granularity Mode during expansion.

GENERAL DESCRIPTION

The Am7970 Compression/Expansion Processor (CEP) is a high-performance peripheral which compresses and expands two-tone bit image data in accordance with internationally-accepted CCITT recommendations. These fully image-preserving compression protocols allow highly efficient storage and transmission of two-tone pictures and documents.

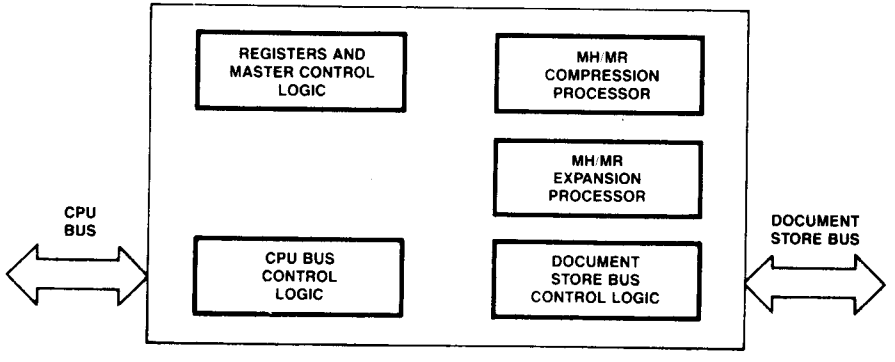
The CEP performs Modified Huffman One-Dimensional Coding or Modified READ Two-Dimensional Coding. This is compatible with CCITT recommendations T.4 and T.6 for Group 3 and Group 4 digital facsimile apparatus. Typical compression of the eight CCITT test documents is 5x to 50x. (The compression ratio is very dependent on the document, the compression mode, and the image resolution.)

The Am7970 has a standard Am8088-like microprocessor bus interface for easy implementation. CEP operation is set by programming internal control registers. CEP status is available through polled registers; exception conditions may be signalled using an external interrupt. The 38 on-chip registers allow very easy and highly flexible system implementation. After initialization, the CEP processes data with minimal intervention by the host processor.

The Compressor and Expander, which operate in full-duplex, can be independently programmed for One-Dimensional encoding/decoding, Two-Dimensional encoding/decoding, or Transparent data transfer.

In Two-Dimensional operation, the programmable K-Parameter defines the number of lines to be encoded in each Two-Dimensional coding sequence. For error-less systems (Group 4), "K=infinity" allows maximum compression.

Accelerated image processing is supported with a Compressor Express Mode, which compresses only every "Nth" line (N=1 to 255) and an Expander Granularity Mode which repeats each line "N" times (N=1 to 7).



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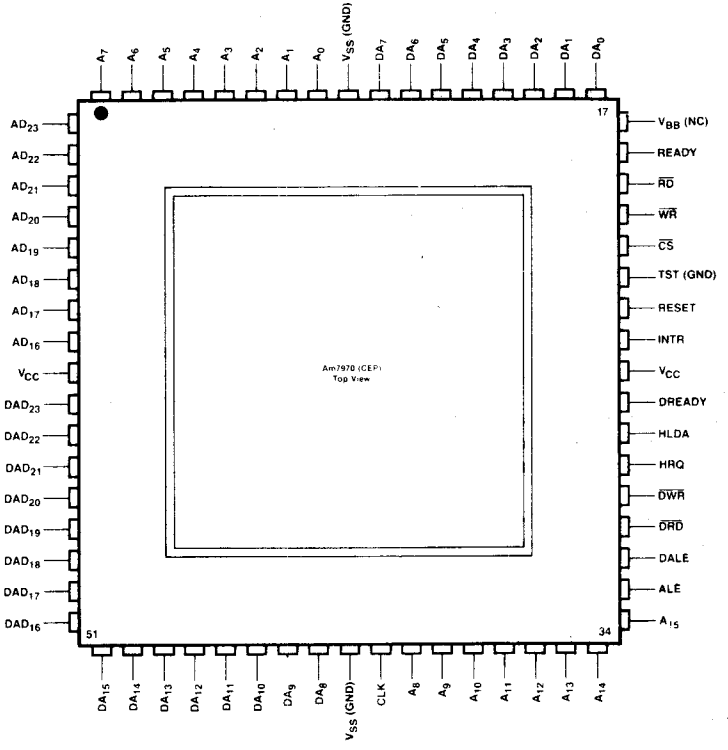
Document format controls include line length and margins. Line lengths or document widths of up to 16K picture elements may be selected. Programmable top, left, and right margins specify "white space" around image data, supporting normal margin requirements, and also "windowing," which is the overlaying of multiple image blocks or image blocks and character blocks.

The Am7970 CEP includes a secondary, local Document Store bus for optional use in conjunction with the CPU bus. The local storage buffer is highly desirable within many system architectures to optimize CPU bus performance. The CEP can linearly address up to 16 Mbytes of memory on each bus, for a total of 32 Mbytes. Starting address, buffer length, and current address for raw and processed data are stored within internal registers independently for both the Compressor and the Expander.

The Am7970 is packaged in a 68-pin LCC or Pin Grid Array and uses a single +5 V power supply.



Am7970 (CEP) Pin Out for LCC Package

Am7970 DL C

Device Type
Compression/Expansion Processor
(CEP)

Package
DL – 68-Pin Ceramic LCC
PL – 68-Pin Plastic LCC*
G – 68-Pin PGA*

Temperature (see Operating Range)
C – Commercial (0 to +70 C)

Valid Combinations

Am7970	DLC, PLC GC

*Package to be announced. Contact factory

ORDERING INFORMATION

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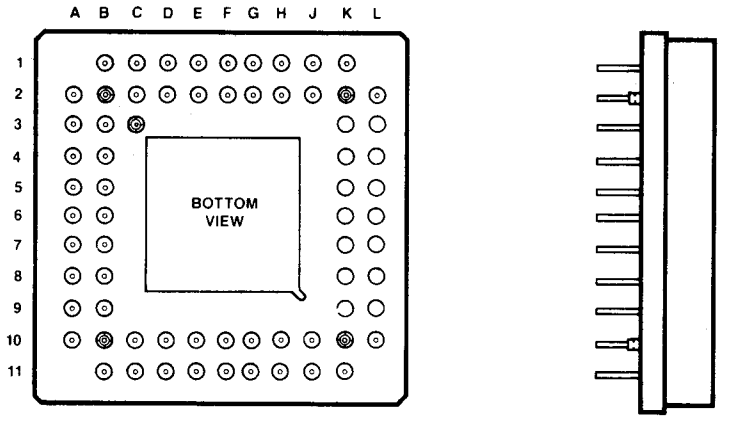
Refer to page 7-1 for Essential Information on Military Devices



Am7970 (CEP) Pin Out for PGA Package

Pin Number	Function
A_2	AD_{23}
A_3	AD_{21}
A_4	AD_{19}
A_5	AD_{17}
A_6	V_{CC}
A_7	DAD_{22}
A_8	DAD_{20}
A_9	DAD_{18}
A_{10}	DAD_{16}
B_1	A_7
B_2	A_6
B_3	AD_{22}
B_4	AD_{20}
B_5	AD_{18}
B_6	AD_{16}
B_7	DAD_{23}
B_8	DAD_{21}
B_9	DAD_{19}
B_{10}	DAD_{17}
B_{11}	DA_{15}
C_1	A_5
C_2	A_4
C_{10}	DA_{14}
C_{11}	DA_{13}
D_1	A_3
D_2	A_2
D_{10}	DA_{12}
D_{11}	DA_{11}
E_1	A_1
E_2	A_0
E_{10}	DA_{10}
E_{11}	DA_9
F_1	V_{SS}
F_2	DA_7
F_{10}	DA_8
F_{11}	V_{SS}

Pin Number	Function
G_1	DA_6
G_2	DA_5
G_{10}	CLK
G_{11}	A_8
H_1	DA_4
H_2	DA_3
H_{10}	A_9
H_{11}	A_{10}
J_1	DA_2
J_2	DA_1
J_{10}	A_{11}
J_{11}	A_{12}
K_1	DA_0
K_2	READY
K_3	WR
K_4	TST (NC)
K_5	INTR
K_6	DREADY
K_7	HRQ
K_8	DRD
K_9	ALE
K_{10}	A_{13}
K_{11}	A_{14}
L_2	V_{BB} (NC)
L_3	RD
L_4	CS
L_5	RESET
L_6	V_{CC}
L_7	HLDA
L_8	DWR
L_9	DALE
L_{10}	A_{15}

INTERFACE SIGNAL DESCRIPTION

All inputs to the CEP are directly TTL-compatible.

V_{CC}: +5 Volts
V_{SS}: Ground

SYSTEM BUS SIGNALS

CLOCK (Clock, Input)

The Clock signal controls the CEP's internal operations and determines the rates of its data transfers. It is usually derived from a master system clock or the associated CPU clock. The Clock input accepts a TTL voltage level with a maximum undershoot of −0.5 V. The input signals $\overline{CS}$, HLDA, $\overline{RD}$, and $\overline{WR}$ can make transitions independent of the CEP clock. On the input signals READY and DREADY, transitions must meet set-up and hold requirements relative to the CEP clock, since these inputs do not contain internal synchronizers. Failure to meet these timing requirements may result in incorrect operation from the internal state machine with unpredictable consequences. See the timing diagrams for details.

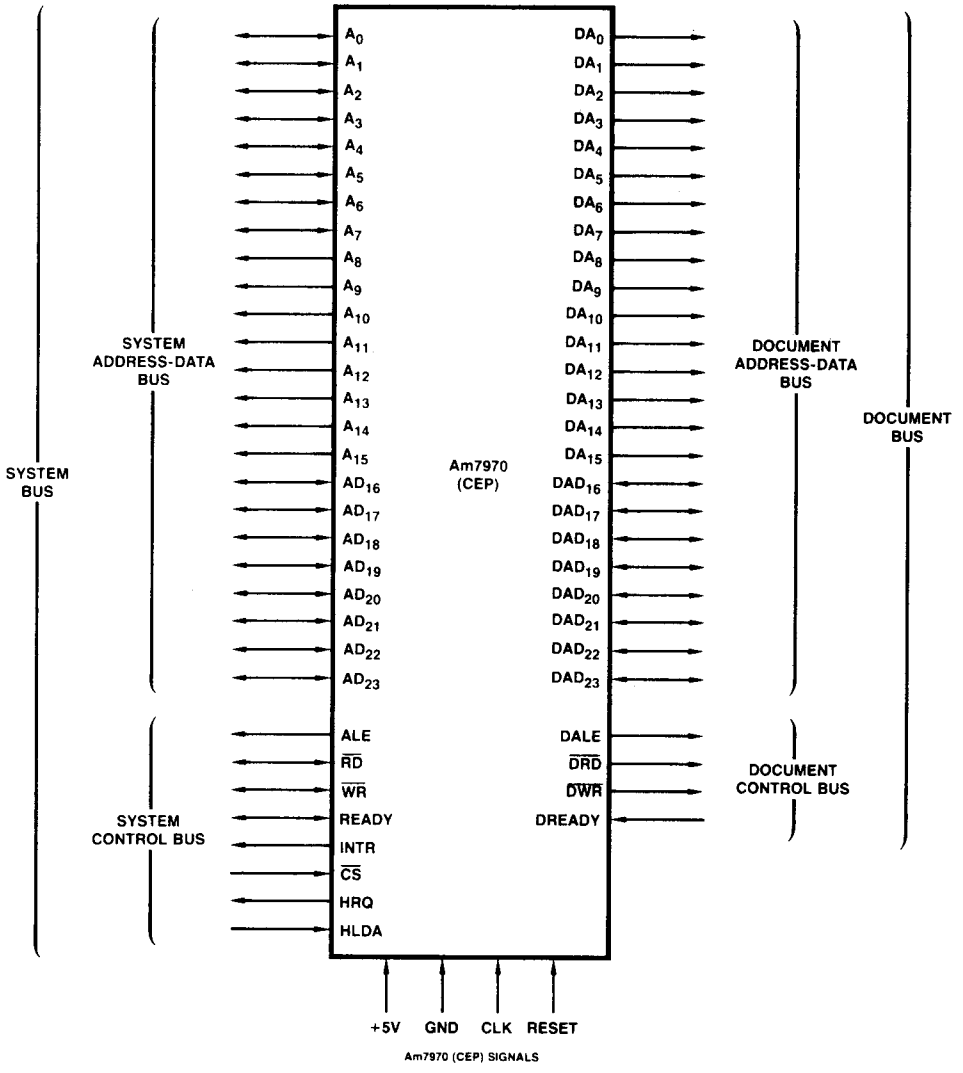


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Figure 2. Am7970 (CEP) Signals

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Refer to page 7-1 for Essential Information on Military Devices

$\overline{RD}$(Read, Input/Output, Three-state)
$\overline{RD}$ is a bidirectional, active-Low, three-state signal. A Low indicates that the AD_{16}–AD_{23} bus is being used for a Read Data Transfer. When the CEP is not in control of the system bus and the external system is transferring information from the CEP, $\overline{RD}$ is a timing input used by the CEP to move registered data onto the AD_{16}–AD_{23} bus. The $\overline{RD}$ cycle from the system should be completed only after the CEP's READY output has returned High. After $\overline{RD}$ returns to its High state, AD_{16}–AD_{23} will float. $\overline{RD}$ is an output when the CEP is Bus Master (HRQ and HLDA are both High). The CEP will assert $\overline{RD}$ Low when data from Main Memory is required. The CEP strobes this data into its internal buffers near the Low-to-High transition of $\overline{RD}$. During the first clock period of a $\overline{RD}$ cycle, AD_{16}–AD_{23} contain the upper eight bits of the Main Memory address. Address Lines A_0–A_{15} contain the lower 16 bits of the Main Memory address. These Lower Address Lines are non-multiplexed and remain active throughout the cycle. The Upper Address Lines are time-multiplexed with data. The address is defined as valid at the falling edge of ALE. Data must be valid with respect to $\overline{RD}$. See timing diagrams for details. $\overline{RD}$ and $\overline{WR}$ may both be Low when the CEP is a Bus Slave and $\overline{CS}$ is High. However, the CEP will never drive both $\overline{RD}$ and $\overline{WR}$ Low together.

$\overline{WR}$(Write, Input/Output, Three-state)
$\overline{WR}$ is a bidirectional, active-Low, three-state signal. A Low indicates that the AD_{16}–AD_{23} bus is being used for a Write Data Transfer. When the CEP is not in control of the system bus and the external system is transferring information to the CEP, $\overline{WR}$ is a timing input used by the CEP to move data from the AD_{16}–AD_{23} bus into its internal registers. The data will be loaded into the specified register before the CEP's READY output is driven High. This $\overline{WR}$ cycle from the system should be completed only after the CEP's READY output has returned High. After $\overline{WR}$ returns to its High state, AD_{16}–AD_{23} will float to three-state. $\overline{WR}$ is an output when the CEP is Bus Master (HRQ and HLDA are both High). The CEP will assert $\overline{WR}$ Low when data is to be written into Main Memory. The CEP drives this data onto its AD_{16}–AD_{23} lines near the High-to-Low transition of WR. During the first clock period of a $\overline{WR}$ cycle, AD_{16}–AD_{23} contain the upper eight bits of the Main Memory address. Address Lines A_0–A_{15} contain the lower 16 bits of the Main Memory address. These Lower Address Lines are non-multiplexed and remain active throughout the cycle. The Upper Address Lines are time-multiplexed with data. The address is defined as valid at the falling edge of ALE. The data is defined as valid with respect to $\overline{WR}$. See timing diagrams for details.

$\overline{CS}$(Chip Select, Input)
$\overline{CS}$ is an asynchronous, active-Low input. A CPU or other external device uses $\overline{CS}$ to activate the CEP for reading from or writing to its internal registers. Once asserted Low, this input can remain Low until all register accesses have been completed. Once $\overline{CS}$ is negated High, it may not be re-asserted Low again for at least 100 ns. There are no timing requirements between the $\overline{CS}$ input and the CEP clock; the $\overline{CS}$ input timing requirements are only defined relative to the $\overline{RD}$ and $\overline{WR}$ signals. $\overline{CS}$ is ignored when the CEP is in control of the system bus.

ALE(Address Latch Enable, Output)
This active-High signal is provided by the CEP to latch the address signals AD_{16}–AD_{23} into an address latch. This pin is never floated. ALE is asserted High during address time when the CEP is Bus Master; otherwise it is Low. Address is defined as valid prior to the High-to-Low transition of ALE.

HRQ(Hold Request, Output)
Hold Request is an active-High signal used by the CEP to obtain control of the bus from the system CPU or arbiter. Hold Request lines from multiple devices may be connected to a priority encoder. If the HLDA input is High after the HRQ output has been asserted High, HRQ will remain High until the CEP has completed a single transfer. After this High-to-Low Transition, the HRQ signal will remain Low for a minimum of 2 clocks.

HLDA(Hold Acknowledge, Input)
HLDA is an asynchronous, active-High input indicating that the CPU has relinquished the bus and that no higher priority device has assumed bus control. Since HLDA is internally synchronized by the CEP before being used, transitions on HLDA do not have to be synchronous with the CEP clock. The HLDA input can be connected to the HLDA output from the CPU (8086-type), to the output of a priority decoder, or to the output of some other arbitration device. The HLDA input normally remains High until the CEP drives the HRQ output Low.

READY(Ready, Input/Output, Three-state)
READY is a synchronous, active-High, three-state, bidirectional signal. READY is used as an input signal when the CEP is Bus Master. Slow memories may use READY to extend $\overline{RD}$ or $\overline{WR}$ cycles. This is accomplished by negating READY Low at the appropriate times and thus inserting Wait States until READY is returned High. READY must be High before Main Memory data can be accessed by the CEP. Care must be taken, however, to assure that this signal is synchronized to the CEP clock and thus meets its set-up and hold requirements. Failure to do so can result in unpredictable operation. READY is used as an output signal when the CEP is Bus Slave. After $\overline{CS}$ has been asserted Low by the CPU, READY will be driven Low by the CEP until it is able to provide or accept data for the current transaction. Once ready, the CEP will assert READY High at which time the CPU should complete the current read or write cycle by negating $\overline{RD}$ or $\overline{WR}$. See timing diagrams for details.

INTR(Interrupt Request, Output)
Interrupt Request is an active-High output used to interrupt the CPU. It is driven High whenever an exception or termination condition exists in either the Compressor (if the Compressor Interrupt Enable bit is set) or Expander (if the Expander Interrupt Enable bit is set). The INTR line will be reset to Low when the CPU reads the CEP Master Status Register or when the CEP is reset.

RESET(Reset, Input)
RESET is an asynchronous, active-High input which initializes the Am7970 to an idle state. This input must be driven High for at least four clock cycles.

A_0–A_7 /A_8–A_{15} (Lower Address Bus, A_0–A_7 are Input/Output, A_8–A_{15} are Three-State Outputs)
The Lower Address Bus is a non-multiplexed, bidirectional (on the least significant eight address lines, A_0–A_7 only), active-High, three-state bus used in addressing all system bus I/O and memory transactions. A_0 is the least significant bit position and A_{15} is the most significant bit position.

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When the CEP is not in control of the system bus (HLDA Low) and the $\overline{CS}$ input is asserted Low, A_0–A_7 are used as input address lines to access the CEP's internal registers. (The CEP's internal registers have been assigned even addresses.) During this time, the address lines A_8–A_{15} are ignored by the CEP. The input addresses on A_0–A_7 must be valid one set-up time before the $\overline{CS}$ input is driven Low and must remain valid throughout the register transaction. See timing diagrams for details.

When the CEP is in control of the main bus (HRQ and HLDA are High), DMA transactions with the Main Memory will occur. The presence of valid address on A_0–A_{15} is defined by the falling edge of ALE. During this Master Mode, A_0–A_{15} are used as non-multiplexed output address lines until HRQ is negated Low. After the High-to-Low transition of HRQ, the A_0–A_{15} lines will float to a three-state condition.

AD_{16}–AD_{23} (Address-Data Bus, Input/Output, Three-state)
The Address-Data Bus is a time-multiplexed (in Master Mode only), bidirectional, active-High, three-state bus used for all system bus I/O and memory transactions. When referring to the data cycle on this bus, AD_{16} is the least significant data bit position and AD_{23} is the most significant. The presence of a valid address during Bus Master operations is defined by the falling edge of ALE and the valid data is defined by the $\overline{WR}$ and $\overline{RD}$ signals; otherwise these lines are floating. The $\overline{RD}$ and $\overline{WR}$ outputs will return to their inactive-High levels only after the READY input has been sampled High. While the CEP $\overline{RD}$ output is Low and when the READY input is High, AD_{16}–AD_{23} must be provided with valid input data from the system. When the CEP $\overline{WR}$ output is asserted Low, AD_{16}–AD_{23} will be driven by the CEP with valid output data. The READY input must then return High to acknowledge receipt of the valid data and to allow the completion of the $\overline{WR}$ cycle. When the CEP is acting as a Bus Slave (HRQ and HLDA Low) and the $\overline{CS}$ input is driven Low, AD_{16}–AD_{23} are used strictly as data lines D_0–D_7. They behave as input data lines when $\overline{WR}$ is asserted Low and as output data lines when $\overline{RD}$ is asserted Low. At all other times they are floated to three-state. During Slave Mode operation, when $\overline{CS}$ is driven Low, the READY output will be asserted Low to signal that the CEP is not ready to complete the transaction. When the CEP is ready, the READY output will be driven High.

DOCUMENT STORE BUS SIGNALS

$\overline{DRD}$(Document Store Read, Output, Three-state)
$\overline{DRD}$ is an active-Low, three-state signal. A Low on this signal indicates that the DAD_{16}–DAD_{23} bus is being used for a Read Data Transfer. When the CEP does not have a Source or Destination Buffer located on the Document Store bus, this pin is floated to three-state. $\overline{DRD}$ is an output when the CEP is in control of the Document Bus. The CEP asserts $\overline{DRD}$ Low when data from Document Memory is required. The CEP strobes this data into its internal buffers near the Low-to-High transition of $\overline{DRD}$. During the first clock period of a $\overline{DRD}$ cycle, DAD_{16}–DAD_{23} contain the upper eight bits of the Document Memory address. Address Lines DA_0–DA_{15} contain the lower 16 bits of the Document Memory address. These Lower Address Lines are non-multiplexed and so remain active throughout the cycle. The Upper Address Lines are time-multiplexed between address and data. The address is defined as valid at the falling edge of DALE. The data is required to be valid with respect to $\overline{RD}$. See timing diagrams for details.

$\overline{DWR}$(Document Store Write, Output, Three-state)
$\overline{DWR}$ is an active-Low, three-state signal. A Low on this pin indicates that the DAD_{16}–DAD_{23} bus is being used for a Document Bus Write Data Transfer. When the CEP does not have a Source or Destination Buffer located on the Document Store bus, this pin is floated to three-state. $\overline{DWR}$ is an output when the CEP is Bus Master. The CEP will assert $\overline{DWR}$ Low when data is to be written into Document Memory. The CEP drives this data onto its DAD_{16}–DAD_{23} lines near the High-to-Low transition of $\overline{DWR}$. During the first clock period of a $\overline{DWR}$ cycle, DAD_{16}–DAD_{23} contain the upper eight bits of the Document Memory address. Document Address Lines DA_0–DA_{15} contain the lower 16 bits of the Document Memory address. These Lower Address Lines are non-multiplexed and remain active throughout the cycle. The upper eight Address Lines are time-multiplexed between address and data. The document address is defined as valid at the falling edge of DALE. The data is defined as valid with respect to $\overline{DWR}$. See timing diagrams for details.

DALE(Document Store Address Latch Enable, Output, Three-state)
This active-High signal is provided by the CEP to latch the Document Store address signals DAD_{16}–DAD_{23} into an address latch. When the CEP does not have a Source or Destination Buffer located on the Document Bus this pin is floated to three-state. DALE is asserted High during address time when the CEP is Bus Master; otherwise it is Low. Address is defined as valid prior to the transition of DALE.

DREADY(Ready, Input, Three-state)
DREADY is a synchronous, active-High, three-state signal. DREADY is used as an input signal when the CEP is Bus Master. Slow memories may use DREADY to extend $\overline{DRD}$ or $\overline{DWR}$ cycles. This is accomplished by negating DREADY Low at the appropriate times and thus inserting Wait States until DREADY is returned High. DREADY must be High before Document Memory data can be accessed by the CEP. Care must be taken, however, to ensure that this signal is synchronized to the CEP clock and thus meets its set-up and hold requirements. Failure to do so can result in unpredictable operation. DREADY may also be useful, in conjunction with transceiver and control logic, in hardware arbitration schemes on the Document Bus.

DA_0–DA_{15} (Document Store Lower Address Bus, Output, Three-state)
The Document Store Lower Address bus is a non-multiplexed, active-High, three-state bus used in addressing all local Document Memory transactions. DA_0 is the least significant bit position and DA_{15} is the most significant bit position.

When the CEP is in control of the Document Store Bus, the presence of valid address on DA_0–DA_{15} is defined by the falling edge of DALE. During this Master Mode, DA_0–DA_{15} will be used as non-multiplexed output address lines whenever the Compressor or the Expander is using the Document Store as a Source or Destination Buffer for the current transaction, otherwise this bus is floated to three-state.

DA_{16}–DA_{23} (Document Store Upper Address-Data Bus, Input/Output, Three-state)

The Document Store Upper Address-Data bus is a time-multiplexed, bidirectional, active-High, three-state bus used for all local Document Memory transactions. When referring to the data cycle on this bus, DAD_{16} is the least significant data bit position and DAD_{23} is the most significant. The presence of a valid address during Bus Master operations is defined by the falling edge of DALE and the valid data is defined by the $\overline{DWR}$ and $\overline{DRD}$ signals; otherwise these lines are floating. The $\overline{DRD}$ and $\overline{DWR}$ outputs will return to their inactive-High levels only after the DREADY input has been sampled High. While the CEP $\overline{DRD}$ output is Low and when the DREADY input is High, DAD_{16}–DAD_{23} must be provided with valid input data from the system. When the CEP $\overline{DWR}$ output is asserted Low, DAD_{16}–DAD_{23} will be driven by the CEP with valid output data. The DREADY input must then return High to acknowledge receipt of the valid data and to allow the completion of the $\overline{DWR}$ cycle.

REGISTER DESCRIPTION

The diagram shown in Figure 3 illustrates the Am7970 CEP's internal registers. Tables 1 and 2 list each register along with its size and access address. Table 3 cross-references these registers by address.

The state of the Status Register, Master Status Register, and GO bits after initialization by the RESET input are "0." The status of other bits after initialization by the RESET input is not specified.

MASTER CONTROL REGISTER (CMCR/EMCR)

The 8-bit Master Control Register, shown in Figure 4, is used to specify the desired mode of operation (One- or Two-Dimensional), the location of the Source and Destination Buffers (Main Memory or Document Store), the Interrupt Enable, the operation controls (Reset, Single-Line or Multi-Line), and the initiation of processing (Start or Stop Processing). The function of each of the Master Control bits is described in the following paragraphs.

The Least Significant Bit (Bit 0) is called the GO bit. The system program initiates compression or expansion operation by setting this bit to "1." Once set, the appropriate Status Register (Compressor Status Register or Expander Status Register) indicates that the selected processor is busy. Upon completion of the selected operation, this bit is reset to "0" automatically. Any attempt to load the Compressor Master Control Register when the Compressor is busy, or the Expander Master Control Register when the Expander is busy, terminates the selected processor with the appropriate error bits set in the Compressor Status Register or Expander Status Register respectively.

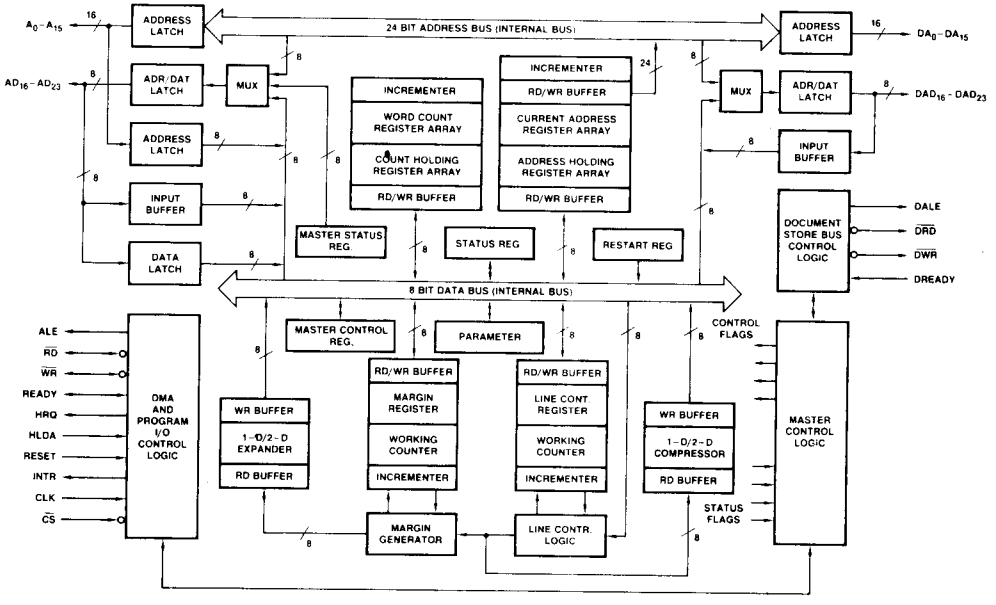

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Figure 3. Am7970 (CEP) Block Diagram

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Refer to page 7-1 for Essential Information on Military Devices

Table 1. Compressor Register Address Assignments

Name	Size (Bits)	Number of Bytes	Port Address(es)
Master Status Register (MSR)*	8	1	FE
Compressor Master Control Register (CMCR)	8	1	76
Compressor Parameter Register (CPR)	8	1	74
Compressor Status Register (CSR)	8	1	78
Compressor Express Register (CER)	8	1	68
Compressor Restart Control Register (CRCR)	8	1	48
Time Fill Register (TFLR)	8	1	44
Compressor Wraparound Register (CWR)	16	2	50 (LSB)/52 (MSB)
Left Margin Register (LMGR)	16	2	40 (LSB)/42 (MSB)
Right Margin Register (RMGR)	16	2	60 (LSB)/62 (MSB)
Top Margin Register (TMGR)	16	2	30 (LSB)/32 (MSB)
Compressor Page Width Register (CPWR)	16	2	70 (LSB)/72 (MSB)
Compressor Source Address Holding Register (CSAHR)	24	3	3A (LSB)/3C/3E (MSB)
Compressor Source Current Address Register (CSCAR)	24	3	0A (LSB)/0C/0E (MSB)
Compressor Destination Address Holding Register (CDAHR)	24	3	4A (LSB)/4C/4E (MSB)
Compressor Destination Current Address Register (CDCAR)	24	3	2A (LSB)/2C/2E (MSB)
Compressor Source Count Holding Register (CSCHR)	24	3	14 (LSB)/16/18 (MSB)
Compressor Source Working Count Register (CSWCR)	24	3	04 (LSB)/06/08 (MSB)
Compressor Destination Count Holding Register (CDCHR)	24	3	34 (LSB)/36/38 (MSB)
Compressor Destination Working Count Register (CDWCR)	24	3	24 (LSB)/26/28 (MSB)
Compressor Source Line Start Address Register (CSLSR)	24	3	5A (LSB)/5C/5E (MSB)
Compressor Destination Line Start Address Register (CDLSR)	24	3	6A (LSB)/6C/6E (MSB)

*This register is common to both the compressor and the expander.

Table 2. Expander Register Address Assignments

Name	Size (Bits)	Number of Bytes	Port Address(es)
Master Status Register (MSR)*	8	1	FE
Expander Master Control Register (EMCR)	8	1	F6
Expander Parameter Register (EPR)	8	1	F4
Expander Status Register (ESR)	8	1	F8
Expander Restart Control Register (ERCR)	8	1	C8
Expander Wraparound Register (EWR)	16	2	D0 (LSB)/D2 (MSB)
Expander Page Width Register (EPWR)	16	2	F0 (LSB)/F2 (MSB)
Expander Source Address Holding Register (ESAHR)	24	3	BA (LSB)/BC/BE (MSB)
Expander Source Current Address Register (ESCAR)	24	3	8A (LSB)/8C/8E (MSB)
Expander Destination Address Holding Register (EDAHR)	24	3	CA (LSB)/CC/CE (MSB)
Expander Destination Current Address Register (EDCAR)	24	3	AA (LSB)/AC/AE (MSB)
Expander Source Count Holding Register (ESCHR)	24	3	94 (LSB)/96/98 (MSB)
Expander Source Working Count Register (ESWCR)	24	3	84 (LSB)/86/88 (MSB)
Expander Destination Count Holding Register (EDCHR)	24	3	B4 (LSB)/B6/B8 (MSB)
Expander Destination Working Count Register (EDWCR)	24	3	A4 (LSB)/A6/A8 (MSB)
Expander Source Line Start Address Register (ESLSR)	24	3	DA (LSB)/DC/DE (MSB)
Expander Destination Line Start Address Register (EDLSR)	24	3	EA (LSB)/EC/EE (MSB)

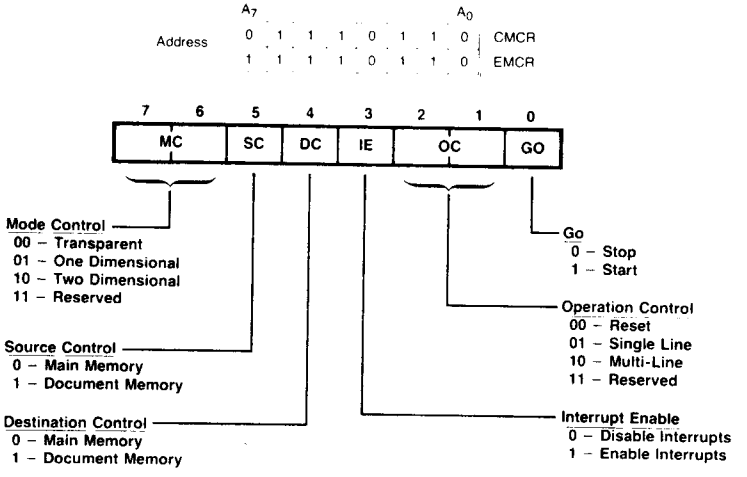
Note: All register addresses are even, the bytes in a register are, therefore, not addressed with contiguous addresses.

*This register is common to both the compressor and expander.

Table 3. Am7970 Internal Registers

	0	2	4	6	8	A	C	E
0			CSWCR (L)	CSWCR (M)	CSWCR (H)	CSCAR (L)	CSCAR (M)	CSCAR (H)
1			CSCHR (L)	CSCHR (M)	CSCHR (H)			
2			CDWCR (L)	CDWCR (M)	CDWCR (H)	CDCAR (L)	CDCAR (M)	CDCAR (H)
3	TMGR (L)	TMGR (H)	CDCHR (L)	CDCHR (M)	CDCHR (H)	CSAHR (L)	CSAHR (M)	CSAHR (H)
4	LMGR (L)	LMGR (H)	TFLR		CRCR	CDAHR (L)	CDAHR (M)	CDAHR (H)
5	CWR (L)	CWR (H)				CSLSR (L)	CSLSR (M)	CSLSR (H)
6	RMGR (L)	RMGR (H)			CER	CDLSR (L)	CDLSR (M)	CDLSR (H)
7	CPWR (L)	CPWR (H)	CPR	CCR	CSR			
8			ESWCR (L)	ESWCR (M)	ESWCR (H)	ESCAR (L)	ESCAR (M)	ESCAR (H)
9			ESCHR (L)	ESCHR (M)	ESCHR (H)			
A			EDWCR (L)	EDWCR (M)	EDWCR (H)	EDCAR (L)	EDCAR (M)	EDCAR (H)
B			EDCHR (L)	EDCHR (M)	EDCHR (H)	ESAHR (L)	ESAHR (M)	ESAHR (H)
C					ERCR	EDAHR (L)	EDAHR (M)	EDAHR (H)
D	EWR (L)	EWR (H)				ESLSR (L)	ESLSR (M)	ESLSR (H)
E						EDLSR (L)	EDLSR (M)	EDLSR (H)
F	EPWR (L)	EPWR (H)	EPR	ECR	ESR			MSR

(L): Low Byte
(M): Middle Byte
(H): High Byte



05777B-4

Figure 4. Compressor/Expander Master Control Register (CMCR/EMCR)

05777B

Refer to page 7-1 for Essential Information on Military Devices

Bits 1 and 2 of the Compressor Master Control Register or Expander Master Control Register are collectively referred to as the Operation Control (OC) bits. Three out of four possible operations are initiated in this field. The OC bits specify the desired operation according to the following table:

Bit 2 OC1	Bit 1 OC0	Operation
0	0	RESET
0	1	SINGLE-LINE
1	0	MULTI-LINE
1	1	RESERVED

RESET (00)

This operation selectively sets the Compressor or Expander to the same state generated by a hardware RESET. This flushes the input queue and clears the contents of the internal working registers, process control flags and appropriate status register. It does not clear the user-programmable control registers, the Compressor Master Control Register, Expander Master Control Register, Compressor Parameter Register, and Expander Parameter Register.

Following a Reset operation, the selected processor is in an idle state. If resumable operation of the current processing activity is necessary, the system should not issue a Reset operation since the clearing of the various registers invalidates any subsequent Restart operation. On the other hand, the system program *must* issue a Reset operation before starting a new sequence of events when no resumable operation from the previous processing is necessary; for example, when the CEP is going to process a new page. This software RESET between contexts is necessary to ensure that the input queue is properly flushed and that the upcoming sequence of operations is interpreted correctly.

SINGLE-LINE (01)

When Single-Line operation is initiated, one effective line of data from the Source Buffer is processed before the GO bit in the Master Control Register is cleared to "0." Such an event might be normal or in error. (See Status Register description for details of error status.) The next line or multiple lines of data can be restarted from where the preceding Single-Line operations ended if no errors have occurred.

The meaning of "effective line" depends on the mode that has been selected (One-Dimensional, Two-Dimensional, or Transparent) and thus, the contents of the appropriate Wraparound Register (One-Dimensional only) and Page Width Register. If the Wraparound Register is "0," the effective line is one scan line as defined in the Page Width Register. This "effective line" includes the reference line in Two-Dimensional Mode.

MULTI-LINE (10)

The Multi-Line operation processes data until either the appropriate Source Working Count Register (SWCR) or Destination Working Count Register (DWCR) reaches "0." At this time the selected processor terminates and the GO bit in the Master Control Register (MCR) is cleared to "0." Such an ending might be normal or in error. (See Status Register description for details of error status.)

RESERVED (11)

If the Reserved operation is initiated, the CEP terminates with an illegal operation error in the CSR or ESR, respectively (see Status Register section).

Bit 3 of the MCR is the Interrupt Enable (IE) bit. When the processor has terminated an operation, the CEP will interrupt the CPU if the IE bit is set to "1." However, if the IE bit is "0," interrupts are disabled and the Am7970 will not interrupt the CPU.

Bit 4 is the Destination Control (DC) bit and Bit 5 is the Source Control (SC) bit of the MCR register. This field specifies the residency of the Source and Destination Buffers. These control bits determine the buffer locations for the selected processor according to the following table:

Bit 5 SC	Bit 4 DC	Location
0	0	Source and Destination in Main Memory
0	1	Source in Main Memory, Destination in Document Store
1	0	Source in Document Store, Destination in Main Memory
1	1	Source and Destination in Document Store

Bits 6 and 7 of the MCR are collectively called the Mode Control Field: MC0 corresponds to Bit 6 and MC1 corresponds to Bit 7. The MC bits specify the desired mode for the selected processor according to the following table:

Bit 7 MC1	Bit 6 MC0	Mode
0	0	TRANSPARENT
0	1	ONE-DIMENSIONAL
1	0	TWO-DIMENSIONAL
1	1	RESERVED

TRANSPARENT (00)

Transparent Mode means that no data modification occurs in the selected processor; data merely passes through the processor via DMA. For example, consider the following: the Code Buffer is contained in the Document Store and all data transmissions take place from the Main Memory. Somehow, facilities must exist to transfer the required information from the Code Buffer in the Document Store to the Main Memory. By initiating Transparent Mode operation with the Document Store as the source and Main Memory as the destination, the processor can be made to perform the required information transfer in the same way as a conventional DMA controller. However, the effects of the Auto-End-of-Line (EOL) insertion feature, Margin Registers, Wraparound, Time Fill, and Express Registers must be fully considered before attempting such information moves. In Transparent Mode, the EOL code always consists of 16 bits on a byte boundary.

ONE-DIMENSIONAL (01)

One-Dimensional Mode specifies the standard Modified Huffman Code according to CCITT recommendation T.4. During this mode of operation, the processor takes into account the relevant Margin Registers, Wraparound Register, Express Register, Page Width, Auto-EOL, and Time Fill features. These registers are discussed individually under their respective headings.

TWO-DIMENSIONAL (10)

Two-Dimensional Mode specifies the standard Modified READ Code according to CCITT recommendations T.4 and T.6. During this mode of operation, the processor takes into account the Page Width, K-Parameter, Margins, Express Mode,

Auto-EOL, and Time Fill features. The Wraparound feature is not available with Two-Dimensional coding.

The Two-Dimensional Mode (MC1=1, MC0=0) utilizes both One-Dimensional and Two-Dimensional processes in conjunction with the K-Register and the K-Working-Register (not visible to the CPU). The K-Working-Register is decremented by one after each compressed line has been processed. If the K-Register contains "0" (K=infinity), the K-Working-Register continues to be decremented until the Source Buffer or the Destination Buffer overflows. Otherwise, the contents of the K-Register are used to update the K-Working-Register at "K" intervals.

The Am7970 Expander detects CCITT recommended extension codes (including exit codes). The CEP's response to detected extension codes are as follows:

1) If the three least significant bits of the detected extension code are **not** all "1s," the Extension Code Detected (ECD) bit in the Master Status Register is set to "1," the Extension (EXT) bits in the Master Status Register are loaded with the three least significant bits of the detected extension code and the Expander immediately terminates.
2) If the three least significant bits of the detected extension code are all "1s," all subsequent data is treated as uncompressed data until a CCITT recommended exit code is detected. After a CCITT recommended exit code has been detected, the CEP resumes its normal Two-Dimensional Expansion Mode of operations.

"Uncompressed data" is passed from the Source Buffer to the Destination Buffer without being expanded. "Uncompressed data" that has been written into the Destination Buffer differs from the Source Buffer data in two ways:

1) Extension code and Exit code will have been removed by the Expander.
2) Each time that the pattern 000001 occurs within the "uncompressed" data, it will be replaced by the pattern 00000.

When the EOL bit within the Expander Parameter Register has been set to "0," the uncompressed data will be checked for errors as it is written into the Destination Buffer.

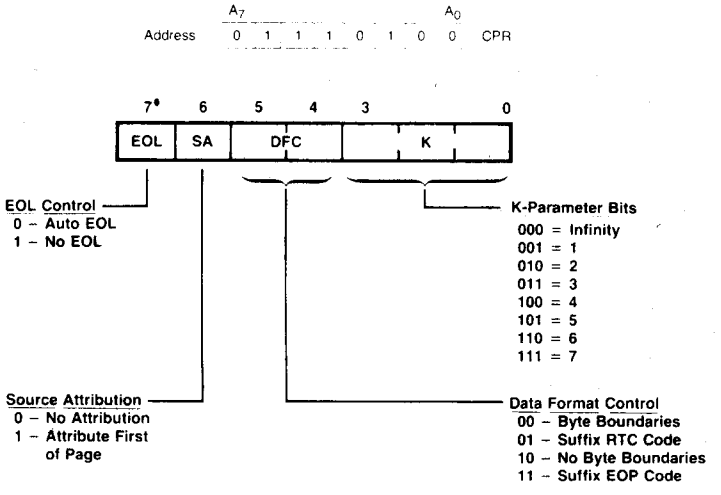
The Two-Dimensional Expander requires that each scan line be assigned a specific reference line. The Am7970 requires that each Two-Dimensional coded scan line use as its reference line the immediately preceding scan line.

RESERVED (11)

If the Reserved operation is initiated, the CEP terminates with an illegal operation error in the CSR or ESR, respectively (see Status Register section).

PARAMETER REGISTER (CPR/EPR)

This 8-bit register, shown in Figures 5 and 6, contains the Granularity factor (G-Parameter) for the Expander (used to repeat G scan lines) and specifies the data format for the Compressor and the beginning of the page attributes, as well as EOL control. The function of each of the Parameter bits is described in the following paragraphs.

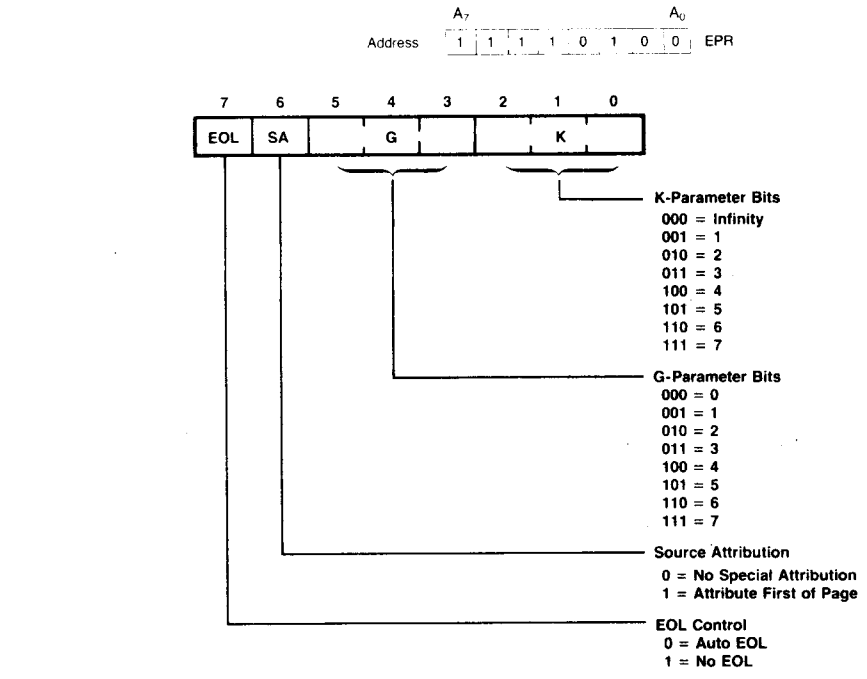


05777B-5

Figure 5. Compressor Parameter Register (CPR)

05777B

Refer to page 7-1 for Essential Information on Military Devices



05777B-6

Figure 6. Expander Parameter Register (EPR)

The Am7970 can be used to process (compress) single page documents that have been digitized as described below.

1) **A single page document is represented by an array of black and white pels.**
2) **Each row of pels is represented by a row of ones and zeros, i.e.:**
   each white pel = 0
   each black pel = 1
3) **A bit stream is formed from each row of pels by a scanner that moves from left to right.**
4) **The first bit each byte of the resulting bit stream is considered to be the least significant bit (bit 0).**

The first bit of each byte of compressed data that is provided by the Am7970 is considred to be the least significant bit (bit 0). The first bit of each byte of expanded data that is provided by the Am7970 compressed data is expanded by the Am7970 a scanner that moves from left to right is assumed.

Compressor Parameter Bits

Bits 0, 1, and 2 of the Compressor Parameter Register contain the K-Parameter. The K-Parameter specifies the number of two-dimensional lines to be encoded or decoded (K-1) with respect to each one-dimensional line. Values from one to seven and infinity (code 000) can be selected.

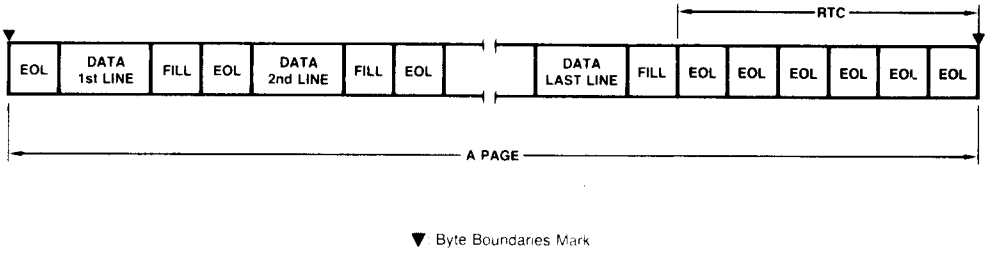
If One-Dimensional coding or Transparent Mode is specified in the Master Control Register, the selected processor logic ignores the K-Parameter.

The state of the K-Parameter bits after initialization by the RESET input is not specified.

Bit 3 in the compressor Parameter Register is reserved.

Bits 4 and 5 of the Compressor Parameter Register are collectively called the Compressed Data Format Control Field (CDF), CDF0 corresponds to Bit 4 and CDF1 corresponds to Bit 5. The CDF bits specify the desired compressed data format according to the following table:

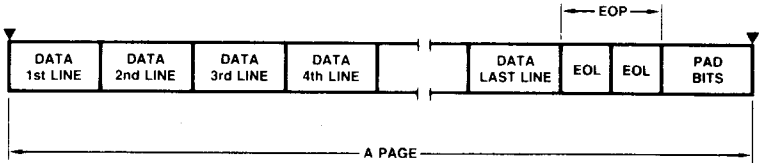
Bit 5 CDF1	Bit 4 CDF0	Compressed Data Format
0	0	Process on Byte Boundaries
0	1	Suffix Return-to-Control (RTC) Code
1	0	No Byte Boundaries
1	1	Suffix End-of-Page (EOP) Code



▼ Byte Boundaries Mark

05777B-7

Figure 7. G-3 Compressed Data Format

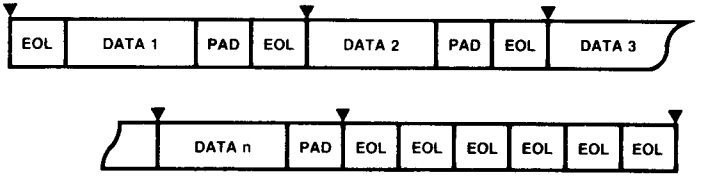


▼ Byte Boundaries Mark

05777B-8

Figure 8. G-4 Compressed Data Format

Compressed Data Format of the 1-DMode

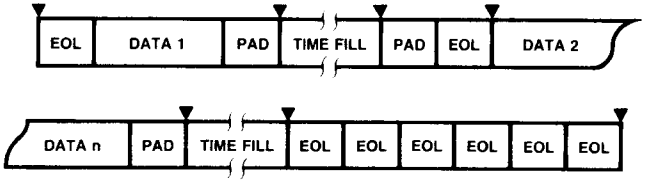


▼: Byte boundary mark

PAD: Consecutive any numbers of "0"s (if any)

05777B-9

Figure 9. Byte Boundary Conditioned with Auto EOL and No Time Fill



▼: Byte boundary mark

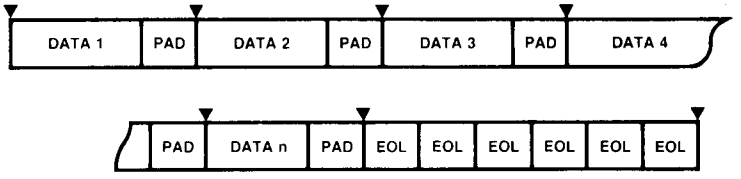
PAD: 1 to 7 "0"s (if any)

05777B-10

Figure 10. Byte Boundary Conditioned with Auto EOL and Time Fill

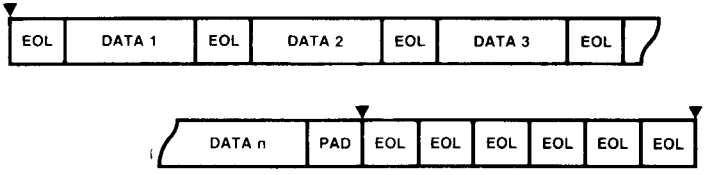
05777B

Refer to page 7-1 for Essential Information on Military Devices



05777B-11

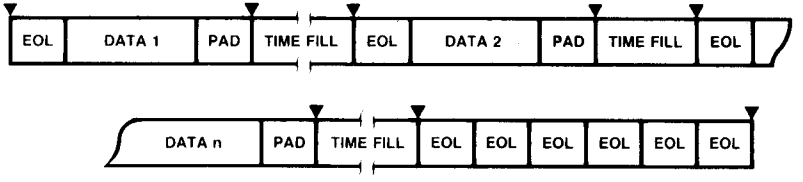
Figure 11. Byte Boundary Conditioned without EOL and Time Fill



▼: Byte boundary mark
PAD: 1 to 7 "0"s (if any)

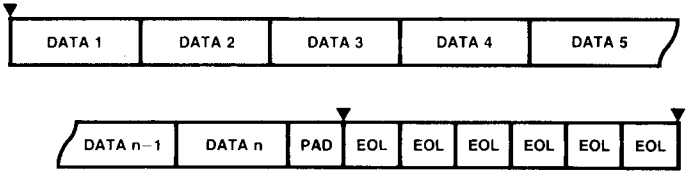
05777B-12

Figure 12. No Byte Boundary Conditioned with Auto EOL and No Time Fill



05777B-13

Figure 13. No Byte Boundary Conditioned with Auto EOL and Time Fill

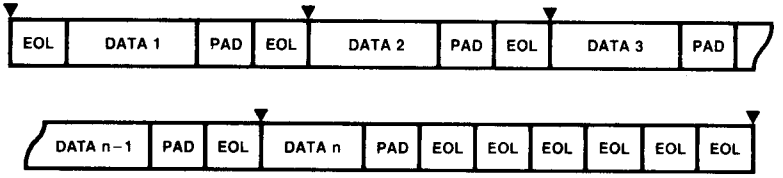


▼: Byte boundary mark
PAD: 1 to 7 "0"s (if any)

05777B-14

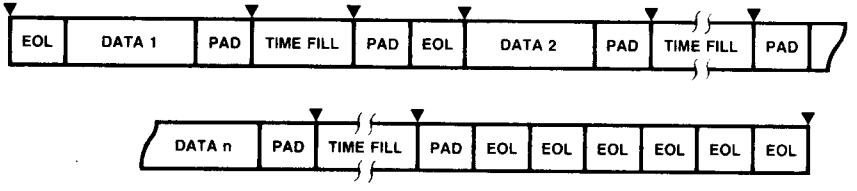
Figure 14. No Byte Boundary Conditioned without EOL and Time Fill

Compressed Data Format of the 2-D Mode



05777B-15

Figure 15. Byte Boundary Conditioned with Auto EOL and No Time Fill



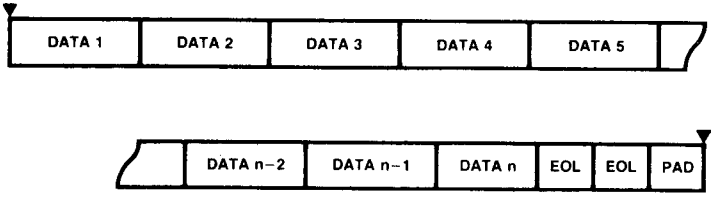
▼: Byte boundary mark

PAD: 1 to 7 0 s (if any)

1: Byte boundary conditioned with no EOL and no time fill is same as Figure.

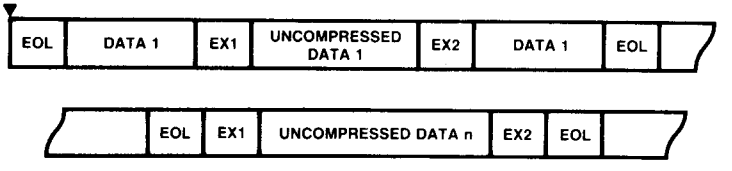
05777B-16

Figure 16. Boundary Conditioned with Auto EOL and Time Fill



05777B-17

Figure 17. No Byte Boundary Conditioned without EOL and Time Fill (G-4)



▼: Byte boundary mark

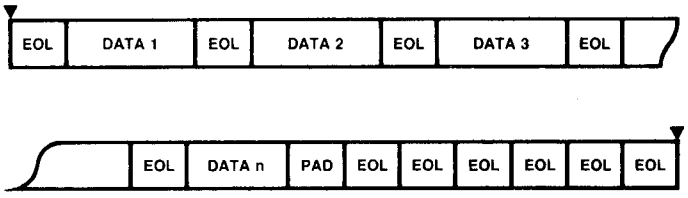
PAD: Consecutive any numbers of 0 s (if any)

EX1: Extention code (entry code)

EX2: Extension code (exit code)

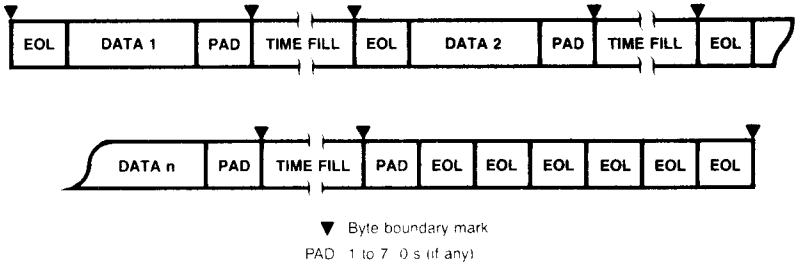
05777B-18

Figure 18. Uncompressed Data Format



05777B-19

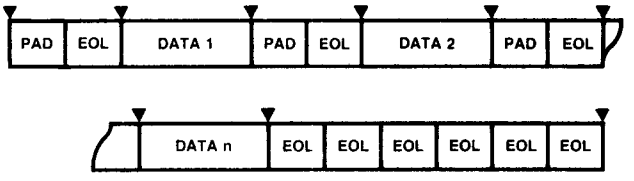
Figure 19. No Byte Boundary Conditioned with Auto EOL and No Time Fill



05777B-20

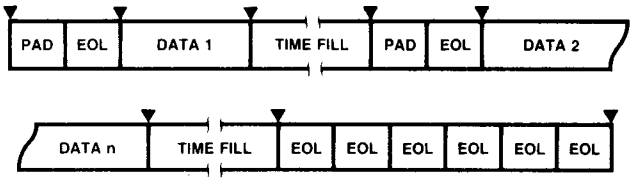
Figure 20. No Byte Boundary Conditioned with Auto and Time Fill

Compressed Data Format of the Transparent Mode



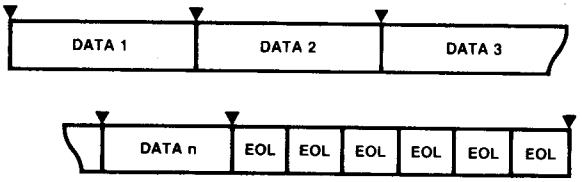
05777B-21

Figure 21. Byte Boundary Conditioned with Auto EOL and Not Time Fill



05777B-22

Figure 22. Byte Boundary Conditioned with Auto EOL and Time Fill



05777B-23

Figure 23. Byte Boundary Conditioned without EOL and Time Fill

Process on Byte Boundaries (00)
With this option, the Am7970 (CEP) is conditioned to end lines on byte boundaries. In conjunction with this option, if the Auto-EOL feature is suppressed (no EOL insertion), and if a coded line does not end on a byte boundary, the Am7970 adds enough Dummy Fill bits to end a line on a byte boundary. These Dummy Fill bits consist of one to seven consecutive "0s." If Auto-EOL is enabled, and a coded line including Time Fill (if any) plus the EOL code does not end on a byte boundary, the Am7970 adds enough Dummy Fill bits between the compressed DATA and EOL codes so that the line ends on a byte boundary. These Dummy Fill bits are also "0s" and are not distinguishable from Time Fill bits.

Caution: The Expander Byte Boundary Control Bit is located in the Restart Control Register.

Return-to-Control (RTC) Code (01)
The Suffix RTC Code specifies that the Return-to-Control code has six consecutive EOL codes as specified in the CCITT recommendation T.4. With this option, the Compressor will suffix an RTC code to the end of the terminal scan line. The Compressor is conditioned to end the RTC code on a byte boundary.

In normal Multi-Line operation, the RTC code will be suffixed following the end of the terminal line in which the Compressor Source Buffer overflow occurs, assuming line processing has been successfully completed. If a coded line including Time Fill (if any) plus the RTC code does not end on a byte boundary, the Compressor adds enough Dummy Fill bits between the compressed DATA and the RTC code to end the line on a byte boundary.

When error conditions arise during Multi-Line operation, the RTC code will not be suffixed. These error conditions are indicated by the Line Processing Incomplete (LPI) bit in the Compressor Status Register (CSR). These conditions are resumable because the rest of the coded line (including RTC code, if any) has been maintained by the Compressor internally and the suffix RTC command is suspended in the Compressor. If the GO command is issued after the Compressor Source Buffer or the Compressor Destination Buffer has been prepared, the Compressor resumes its previous process from where it left off.

For example, when a Compressor Source Buffer overflow occurs along with a Compressor Destination Buffer overflow, the processor terminates its operation promptly and the RTC code won't be suffixed. As another example, if the Compressor Source Buffer overflow has occurred with the Line Processing Incomplete and Wraparound Incomplete (if any), the Compressor terminates its operation promptly and the RTC code won't be suffixed.

In normal Single-Line operation, an RTC code will be suffixed following an end of line when that line's processing is completed. If a coded line including Time Fill (if any) and the RTC code does not end on a byte boundary, the Compressor adds enough Dummy Fill bits between the compressed DATA and the RTC code to end the line on a byte boundary. If the line processing has not been completed and the Compressor Destination Buffer overflow occurs, the Compressor terminates its operation promptly and the RTC code won't be suffixed.

As mentioned for Multi-Line operation, cases of error termination are indicated by the Line Processing Incomplete (LPI) bit in the Compressor Status Register (CSR). Although the Auto-EOL feature may be enabled, an EOL code won't be suffixed following an end of line when the suffix RTC code is defined.

No Byte Boundaries Control (10)
The No Byte Boundaries Control is the counterpart to the Process on Byte Boundaries (00) operation. The compressed data (including the Time Fill and EOL codes, if any) is not conditioned to end lines on a byte boundary.

For example, if the Auto-EOL feature is suppressed (no EOL insertion), and a coded line does not end on a byte boundary, the Compressor holds the excess compressed data beyond the last full byte boundary (one to seven bits) in an internal register. Then this remaining compressed data is combined with the next line of compressed data without Dummy Fill bits between the scan lines.

In Multi-Line operation on a Source Buffer overflow or in Single-Line operation, the Compressor processes the last full byte of source data but truncates any excess bits (one to seven) that do not comprise a byte at the end of the terminal line. In this case, the Compressor will indicate an error termination and the LPI bit will be set in the Compressor Status Register.

If a Compressor destination overflow has occurred, the Compressor terminates its operation promptly and the Compressor retains the remaining bits of the compressed data in an internal register. Under these circumstances, processing may be resumed by issuing the Compressor Go operation after preparing the Compressor Source Buffer or the Compressor Destination Buffer respectively. At this point, the Compressor combines the excess bits from the point of termination with the rest of the data to be compressed.

> As another example, if the Auto-EOL feature is enabled and a coded line (including the EOL and the Time Fill, if any) does not end on a byte boundary, the Compressor retains the excess bits of the EOL code (one to seven) in an internal register. Then the rest of the EOL code is combined with the next line of compressed data from where it left off (i.e., the EOL code won't be conditioned on a byte boundary).

Transparent Mode operation cannot be specified with the No Byte Boundaries Control. The Transparent Mode operation is always conditioned to end a line on a byte boundary, regardless of the Byte Boundary Control bit.

Bit 6 of the Compressor Parameter Register is called the Source Attribute (SA) bit. When the Source Attribute bit has been set to "1" with the K-Parameter at infinity, and the EOL bit is set to "1," the reference line for the beginning of a page will be an imaginary all-white line. In other words, all lines will be processed Two-Dimensionally according to the Group 4 recommendations. Also, for G4 compatibility, the first line of the Source Buffer must correspond to the first scan line of a page with no EOL set, No Byte Boundaries set, in Two-Dimensional Mode with "K" set to infinity, and with no Time Fill specified.

The SA bit will be sampled by the CEP as a Go operation is received. This Go operation must be specified only after the CEP is initialized by the RESET input or the Reset operation, or in other words, the CEP must be initialized at the beginning of a page. The SA bit in the Parameter Register will be cleared automatically after completing the first line of processing.

When the CEP is in a resumable condition in Two-Dimensional Mode without the K-Parameter set to infinity, and the EOL bit is set to "0," the processor will ignore the SA bit. If, however, the SA bit is set to "1" with the EOL bit set to "0," the processor will insert or detect a prefixed EOL code at the beginning of a page.

When the SA bit and EOL bit are both set to "0," the selected processor will operate without the prefixed EOL code. Thus, when the SA bit has been set to "1," the processor Source Buffer is attributed to the first portion of the page, but if the SA bit has been set to "0," the processor follows an ordinary operation procedure.

Bit 7 of the Compressor Parameter Register is called the EOL bit.

When the **Compressor** Parameter Register Bit 7 is set to "0," the Compressor will automatically suffix an EOL code to the end of a compressed line or to the end of a transparent line. With this option enabled, a compressed line or transparent line consists of data followed by Time Fill bits (if any) and an EOL code. This line will end on a byte boundary when the Byte Boundaries Control is specified; otherwise, it will not.

If this bit is set to "1," such automatic suffixing is suppressed. With this option enabled, a compressed line will consist of data only (no Time Fill bits or EOL codes).

When Auto-EOL is enabled with the Source Attribute bit in the Compressor Parameter Register set to "1," an EOL code will be prefixed to the first compressed line of the page. This prefixed EOL code always ends on an exact byte boundary when in the Transparent Mode because, in this case, it happens to be 16 bits.

Expander Parameter Bits

Bits 0, 1, and 2 of the Expander Parameter Register contain the K-Parameter. The K-Parameter specifies the number of two-dimensional lines to be encoded or decoded (K-1) with respect to each one-dimensional line. Values from one to seven and infinity (code 000) can be selected.

If One-Dimensional coding or Transparent Mode is specified in the Master Control Register, the selected processor logic ingores the K-Parameter.

The state of the K-Parameter bits after initialization by the RESET input is not specified.

Bits 3, 4, and 5 of the Expander Parameter Register are used to specify the G-Parameter granularity control. G0, G1, and G2 refer to **Bits 3, 4, and 5** of the Expander Parameter Register respectively. The following table lists the G-Parameters and the corresponding code:

Bit 5 G2	Bit 4 G1	Bit 3 G0	G-Parameter
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

The G-Parameter is used to specify the number of times that each scan line (a scan line has been specified by the value in the Expander Page Width Register) should be duplicated in the Destination Buffer. For instance, when G=3, each scan line that is accessed from the Source Buffer and then expanded is written into the Destination Buffer a total of four times. Note that an error condition will exist if the Expander Wraparound Register (EWR) is not "0" when the G-Parameter is non-zero. Such an error would be indicated by the EIC bit in the Expander Status Register. The Expander Wraparound Register, Expander Source Working Count Register, and Expander Destination Working Count Register are more fully described in their separate section of this document.

Bit 6 of the Expander Parameter Register is called the Source Attribute (SA) bit. When the Source Attribute bit has been set to "1" with the K-Parameter at infinity, and the EOL bit is set to "1," the reference line for the beginning of a page will be an imaginary all-white line. In other words, all lines will be processed Two-Dimensionally according to the Group 4 recommendations. Also, for G4 compatibility, the first line of the Source Buffer must correspond to the first scan line of a page with no EOL set, No Byte Boundaries set, in Two-Dimensional Mode with "K" set to infinity, and with no Time Fill specified.

The SA bit will be sampled by the CEP as a Go operation is received. This Go operation must be specified only after the CEP is initialized by the RESET input or the Reset operation, or in other words, the CEP must be initialized at the beginning of a page. The SA bit in the Parameter Register will be cleared automatically after completing the first line of processing.

When the CEP is in a resumable condition in Two-Dimensional Mode without the K-Parameter set to infinity, and the EOL bit is set to "0," the processor will ignore the SA bit. If, however, the SA bit is set to "1" with the EOL bit set to "0," the processor will insert or detect a prefixed EOL code at the beginning of a page.

When the SA bit and EOL bit are both set to "0," the Expander will operate without the prefixed EOL code. Thus, when the SA bit has been set to "1," the processor Source Buffer is attributed to the first portion of the page, but if the SA bit has been set to "0," the processor follows an ordinary operation procedure.

The state of the SA bit after initialization by the RESET input is not specified.

Bit 7 of the Expander Parameter Register is called the EOL bit.

When the **Expander** Parameter Register Bit 7 is set to "0," the Source Buffer data is assumed to contain EOL codes. This data will be checked for data errors. If the EOL bit is not set to "0," the data will not be checked for data errors; error-free data is assumed.

When the EOL bit is a "1" during the Transparent Mode or the One-Dimensional or the Two-Dimensional Modes, the Source Buffer data is assumed to contain no EOL codes and no Time Fill bits.

If the Expander GO bit is set to "1" with the EOL bit set to "1" and Expander SA bit set to "1," the Expansion Processor will start its operation when it has detected an EOL code from the previous line or prefixed from the beginning of a page, and it will continue its operation until it detects an EOL code on the current processing line. When this EOL has been detected, the Expansion Processor will check that the bit-length of the expanded current line is equal to

$$L = (EPWR * 8) * (EWR + 1)$$

Where: EPWR = The value of the Expander Page Width Register.
EWR = The value of the Expander Wraparound Register.

If the current line is not equal to this value, the Expansion Processor will terminate in an error-state with the DER bit in the Expander Status Register set to "1."

Caution: The Expander Byte Boundary Control bit is located in the Restart Control Register.

EXPRESS REGISTER (CER)

This 8-bit register specifies how many scan lines to skip before compressing the next line after the processing of the current line has been completed.

Figure 24 illustrates the Express Register. This register is used to specify (in binary) how many scan lines to skip after compressing the current line. If this register is loaded with a "0," every scan line will be compressed; this is the normal operating mode. The Compressor logic will not modify this register during its operation.

If the Express Mode is defined with Two-Dimensional Compression, the current compressed line will become the reference line for the next compressed line which is located "n" scan lines below it.

The Am7970 does not allow Wraparound and Express Modes to be specified simultaneously. If such a condition is specified, an error status will be indicated. The scan line length is obtained from the Compressor Page Width Register.

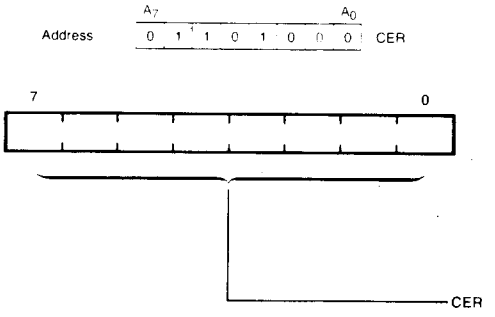


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Figure 24. Compressor Express Register (CER)

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WRAPAROUND REGISTER (CWR/EWR)

Figure 25 shows the Wraparound Register layout. This 16-bit register is used to specify the number of additional scan lines that will be grouped into one effective line. This effective line will be used for encoding and decoding. If the Wraparound Register is loaded with "0," then the effective line is identical to a scan line. This is the normal operating mode.

If this register is loaded with a "1," two scan lines will make up an effective line and so on. Wraparound Mode and Express Mode cannot be used simultaneously, and Wraparound Mode cannot be specified with Two-Dimensional Compression. Either of these conditions will result in an error. The Wraparound Register is not modified by the selected processor during its operation.

LEFT MARGIN REGISTER (LMGR)

Figure 26 shows the Left Margin Register layout. This 16-bit register is used to specify the width of the left-hand margin. If

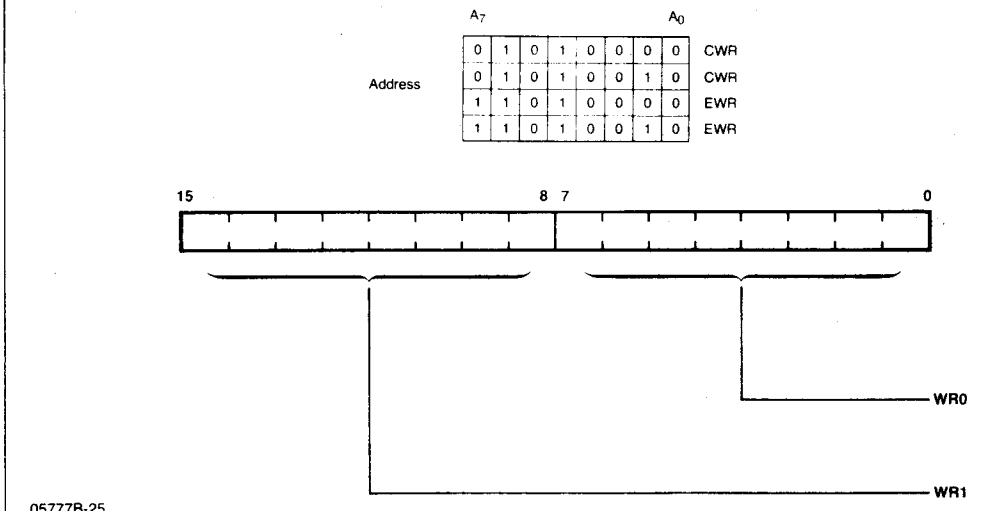

Figure 25. Compressor/Expander Wraparound Register (CWR/EWR)

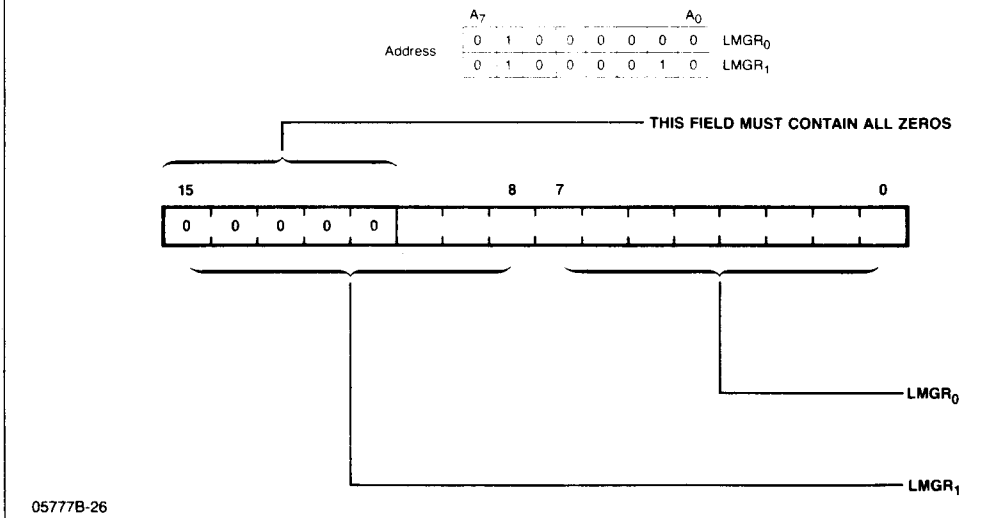

Figure 26. Left Margin Register (LMGR)

the value in the Left Margin Register is "0," then the original scan line will be used with no modification. When the Left Margin Register is non-zero, the number contained in this register specifies the left margin width in bytes.

For example, a "1" in the Left Margin Register means 8 pels of margin. When a compression operation is initiated with the left margin specified, then the Compressor obtains data from the Source Buffer via DMA as usual. However, the margin specification overrides the actual image data and forces the pels to be "white." Such overriding continues until the programmed margin requirements are satisfied.

Compression of the rest of the scan line proceeds as usual (see also Right Margin Register). The left margin is effective in Wraparound and Express Mode and will be included in One-Dimensional, Two-Dimensional, and Transparent Modes of operation.

Hence, if the left margin is specified while using Transparent Mode to accomplish a transfer of data from the Source Buffer to the Destination Buffer, the final data in the destination will differ from the data in the source because of the margin. The Compressor does not modify the Left Margin Register during its operation.

The sum of the left and right margin specifications must not be greater than the paper width specified. This would result in an error condition.

Bits 11 through 15 of the Left Margin Register must be set to "0."

RIGHT MARGIN REGISTER (RMGR)

Figure 27 shows the Right Margin Register layout. This 16-bit register is used to specify the width of the right hand margin. If the value in the Right Margin Register is "0," the original scan line will be used with no modification. When the Right Margin Register is non-zero, the number contained in this register specifies the right margin width in bytes.

For example, a "1" in the Right Margin Register means 8 pels of margin. When a compression operation is initiated with the right margin specified, then the Compressor obtains data from the Source Buffer via DMA as usual. However, the margin specification overrides the actual image data and forces the pels to be "white." Such overriding continues until the programmed margin requirements are satisfied.

Compression of the rest of the scan line proceeds as usual (see also Left Margin Register). The right margin is effective in Wraparound and Express Mode and is included in One-Dimensional, Two-Dimensional, and Transparent Modes of operation.

Hence, if the right margin is specified while using Transparent Mode to accomplish a transfer of data from the Source Buffer to the Destination Buffer, the final data in the destination will differ from the data in the source because of the margin. The Compressor does not modify the Right Margin Register during its operation.

The sum of the left and right margin specifications must not be greater than the paper width specified. This would result in an error condition.

Bits 11 through 15 of the Right Margin Register must be set to "0."

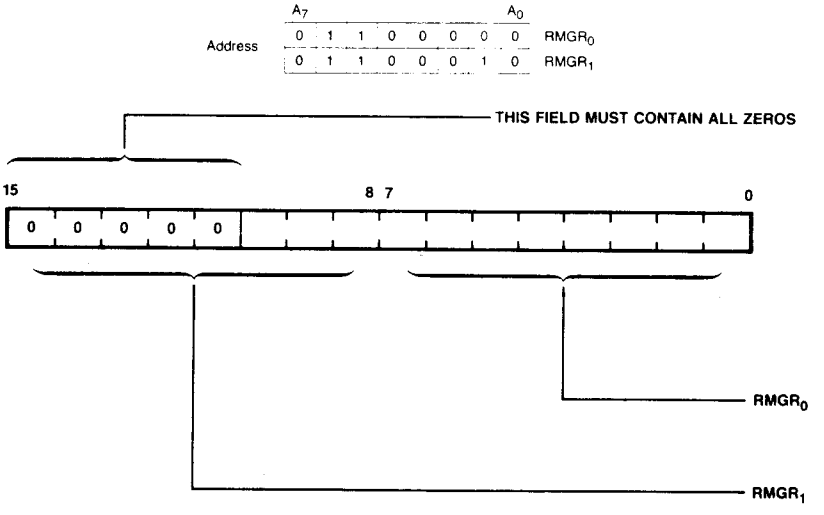

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Figure 27. Right Margin Register (RMGR)

TOP MARGIN REGISTER (TMGR)

Figure 28 shows the Top Margin Register layout. This register is used to specify the top margin width of a document. If the Top Margin Register is loaded with a "0," no top margin is specified.

If the Top Margin Register is non-zero, the number contained in this register specifies the desired top margin height in increments of one scan line. When a compression operation is initiated with the top margin specified, then the Compressor reads data from the Source Buffer via DMA as usual. However, the top margin specification overrides the data and forces "white" into the Compressor until the top margin requirements are satisfied. From then on, the usual compression operation takes place (also see Left and Right Margin Registers).

Since, by definition, the Top Margin white space is to occur only once per document, the Compressor logic decrements the Top Margin Register by one after processing each scan line until it reaches "0", at which time normal compression proceeds.

> The top margin is effective in both Wraparound and Express Modes. However, caution must be exercised when specifying Express Mode with a top margin since the Compressor logic of the Am7970 picks every "Nth" line ("N" being a function of the Express Register) to compress in Express Mode. For example, assume that Top Margin Register specifies "8" and the Express Register specifies "1." The Compressor then processes every other scan line (scan line 1, 3, etc.) in accordance with the Express Register specification, yet the Top Margin is affected by only those scan lines that were presented to the Compressor. Therefore, since the Top Margin is assigned to be "8," and every other scan line has been skipped, scan line "17" of the original picture will be the first coded line with real picture data on it in this example.

The top margin controls are effective in One-Dimensional, Two-Dimensional, and Transparent Modes. Hence, consideration must be given to the effects of Top Margin Register when using Transparent Mode to transfer data from the Source Buffer to the Destination Buffer.

TIME FILL REGISTER (TFLR)

Figure 29 shows the Time Fill Register layout. This 8-bit register is used to specify the minimum length of a coded line expressed in bytes. If the number of bytes in a compressed line is smaller than this number, Time Fill bits are required. Time Fill bits will be added to the compressed line such that the sum of the code bits and Time Fill bits is equal to or greater than the required line length. Time Fill bits are simply all "0s."

Specifying "0" in the Time Fill Register means that no time fill is desired, or in other words, zero minimum length is acceptable.

When the Auto-EOL feature is suppressed, the Am7970 will ignore the time fill requirement; no time fill is inserted. When the Auto-EOL is enabled and a coded line including Time Fill (if any) and EOL code does not end on a byte boundary, the Am7970 will add enough Dummy Fill bits between the compressed data and the EOL code to end the line on a byte boundary when the Byte Boundary Control has been specified. When the No Byte Boundaries Control is specified, the Am7970 Compressor will **not** condition the Time Fill bits to end lines on a byte boundary.

SOURCE ADDRESS HOLDING REGISTER (CSAHR/ESAHR)

Figure 30 shows the Source Address Holding Register layout. This 24-bit register contains the starting address of the Source Buffer for the selected processor. When a Restart process is initiated, the Source Address Holding Register provides the initial value to the working register. The contents of Source Address Holding Register are loaded automatically into the Source Current Address Register whenever the GO bit in the Master Control Register is set, in conjunction with the Source Address Control bit in the respective Restart Control Register being "0." The contents of the Source Address Holding Register are not modified by the processor during its operation.

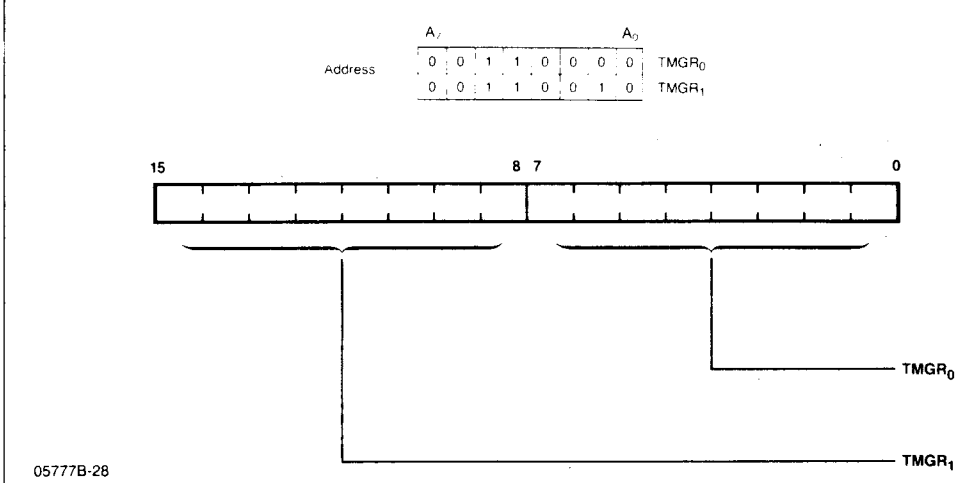

Figure 28. Top Margin Register (TMGR)

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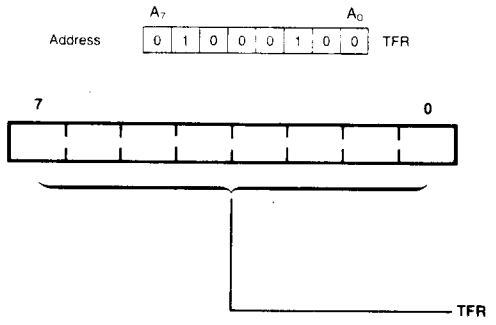

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Figure 29. Time Fill Register (TFR)

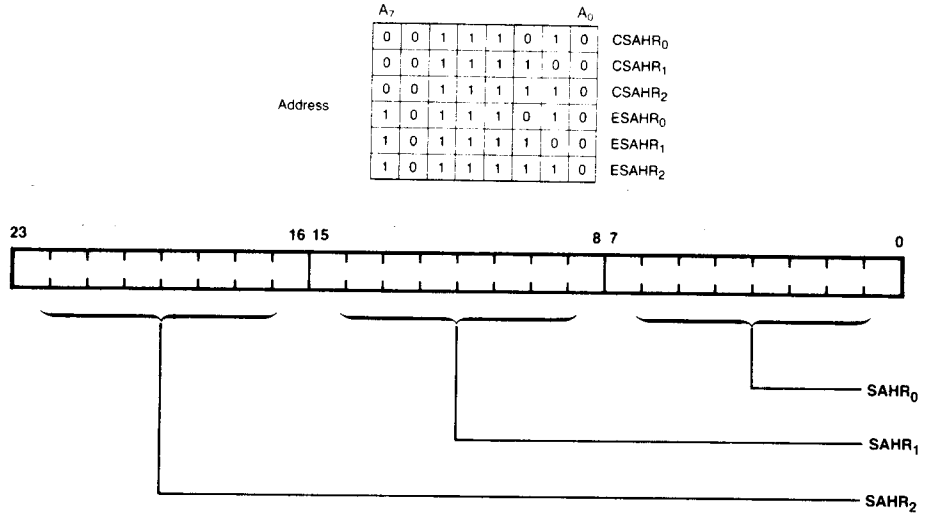

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Figure 30. Compressor/Expander Source Address Holding Register (CSAHR/ESAHR)

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SOURCE CURRENT ADDRESS REGISTER (CSCAR/ESCAR)

Figure 31 shows the Source Current Address Register layout. This 24-bit register provides the current address for all Compressor transactions with the Source Buffer. After each transaction this register is incremented by one and will wraparound through "0" after reaching a maximum value of all "1s." If the Source Address Control bit in the selected Restart Control Register is "0," the Source Current Address Register will be loaded from the Source Address Holding Register whenever a new Go operation is initiated. On the other hand, if the Source Address Control bit in the Restart Control Register is "1," the Source Current Address Register continues from its current value.

Two-Dimensional processing requires not only data for the current line but also corresponding data from the previous line. The Am7970 calculates the initial address of the reference line using the Source Line Start Address Register. From there on, the address of the reference line will be incremented appropriately.

DESTINATION ADDRESS HOLDING REGISTER (CDAHR/EDAHR)

Figure 32 shows the Destination Address Holding Register layout. This 24-bit register is the counterpart to the Source Address Holding Register. It specifies the starting address of the Destination Buffer during Restart operations. The contents of the Destination Address Holding Register will be automatically transferred into the Destination Current Address Register whenever the GO bit in the Master Control Register is set in conjunction with the Destination Address Control bit in the Restart Control Register being "0." The Destination Address Holding Register contents are not modified by the Compressor during its operation.

DESTINATION CURRENT ADDRESS REGISTER (CDCAR/EDCAR)

Figure 33 shows the Destination Current Address Register layout. This 24-bit register is used to obtain the current address for a transaction with the Destination Buffer. The Am7970 increments the Destination Current Address Register by one after each transaction and will wraparound through "0" after reaching a maximum value of all "1s."

When the Destination Address Control bit in the Restart Control Register is "0," the Destination Current Address Register will be loaded from the Destination Address Holding Register whenever the GO bit in the Master Control Register is set to "1." When the Destination Address Control bit is "1," the Destination Current Address Register will continue from the current value upon receipt of the Go operation.

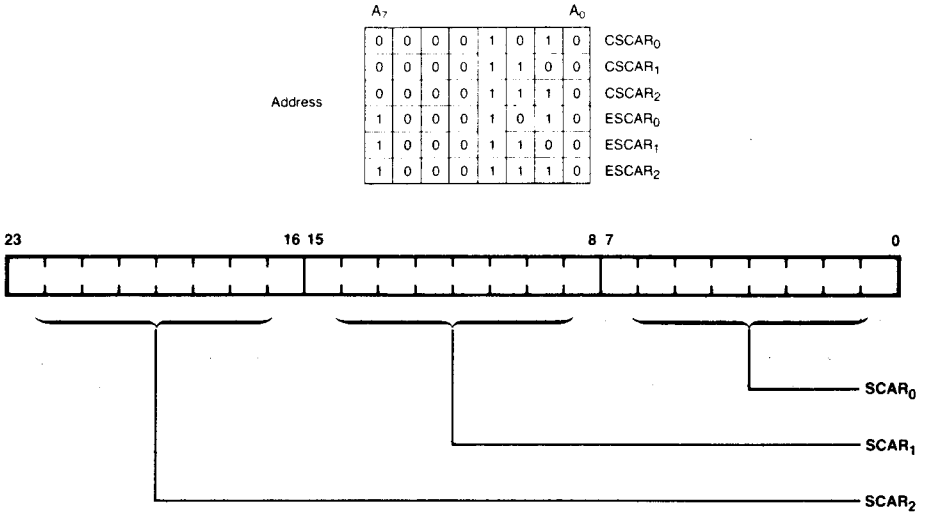

Figure 31. Compressor/Expander Source Current Address Register (CSCAR/ESCAR)

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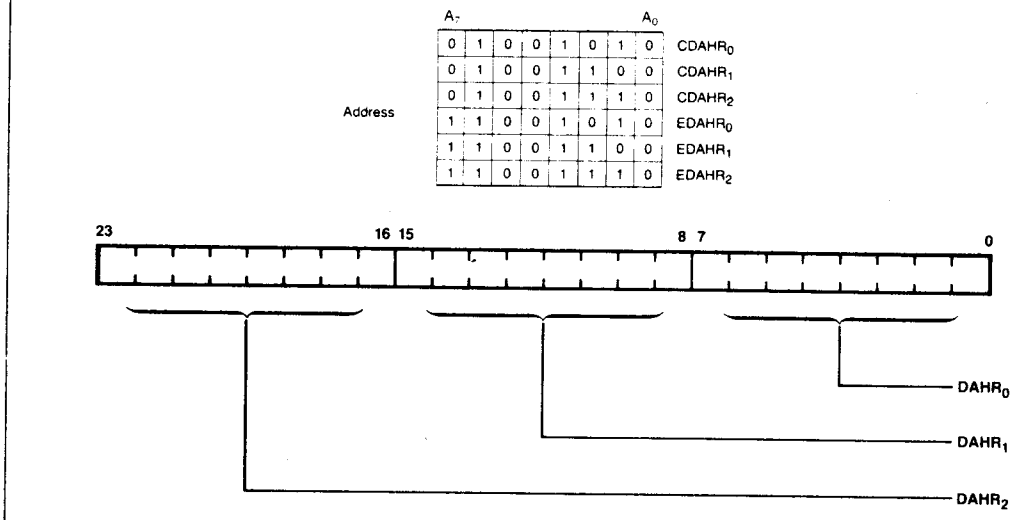

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Figure 32. Compressor/Expander Destination Address Holding Register (CDAHR/EDAHR)

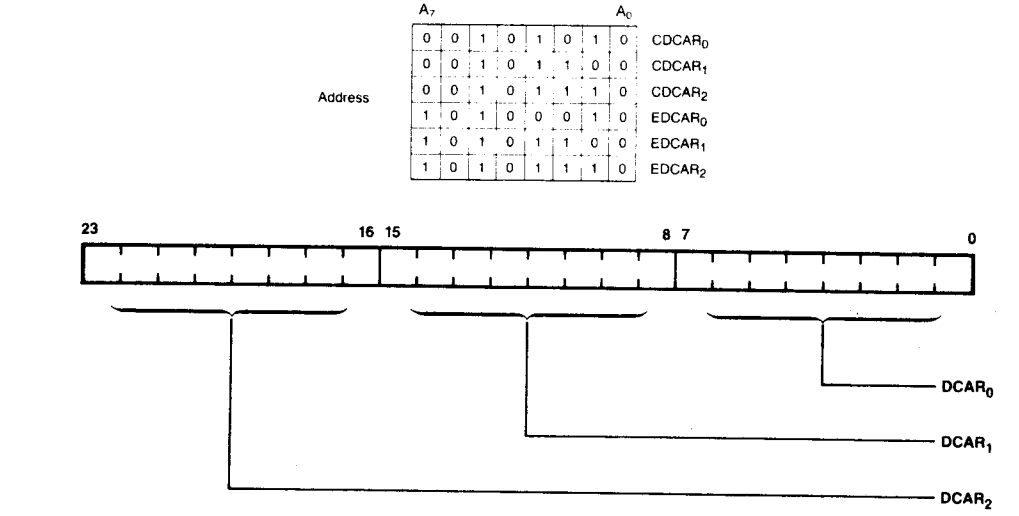

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Figure 33. Compressor/Expander Destination Current Address Register (CDCAR/EDCAR)

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SOURCE COUNT HOLDING REGISTER (CSCHR/ESCHR)

Figure 34 shows the Source Count Holding Register layout. This register is used to specify the Source Buffer length in bytes. The Am7970 requires that this buffer length be specified as a **negative number in two's complement form**.

The contents of the Source Count Holding Register are loaded automatically into the Source Working Count Register whenever a Go operation is initiated in conjunction with the Source Count Control bit in the Restart Control Register being "0."

Note: The CSCHR must be loaded with Source Buffer Length divided by contents of the (Express Register + "1").

SOURCE WORKING COUNT REGISTER (CSWCR/ESWCR)

Figure 35 shows the Source Working Count Register. This register is used to keep track of the number of Source Buffer accesses. Initially, the Source Working Count Register contains a 24-bit **negative number in two's complement form** specifying the number of bytes in the Source Buffer. The Am7970 increments the Source Working Count Register by one after completing each source transaction. The Source Overflow (SO) bit in the appropriate Status Register will be set to "1" immediately after the Source Working Count Register is exhausted.

It must be emphasized that a transaction does not necessarily mean one access. For example, for Two-Dimensional processing, the Am7970 will access the Source Buffer both for the current line and for the reference line. Thus, a transaction in Two-Dimensional will include twice as many Source Buffer accesses as a One-Dimensional transaction of the same type.

When the last byte of the Source Buffer corresponds to the end of an effective line, the Am7970 will process this byte and will attempt to store it in the destination and then terminate the processor. When the Am7970 terminates after storing a fully processed line successfully (that is, no premature destination overflow or error status), this is normal operation. Abnormal termination due to premature destination overflow or error status will be discussed in later sections of this document.

When the last byte obtained from the Source Buffer does not correspond to the end of an effective line, it means that the assigned Source Buffer length is less than what is needed by the Page Width Register and the Wraparound Register, if used. In this condition the Am7970 will process the byte and then terminate abnormally. The Wraparound Incomplete (WPI) bit and Line Processing Incomplete (LPI) bit in the Status Register will reflect the appropriate error termination.

When an operation is initiated with the Source Count Control bit in the Restart Control Register set to "0," the Source Working Count Register obtains its initial value from the Source Count Holding Register. When this control bit is a "1" and a Restart operation is initiated, the Source Working Count Register uses the existing value as the initial value.

DESTINATION COUNT HOLDING REGISTER (CDCHR/EDCHR)

Figure 36 shows the Destination Count Holding Register. This 24-bit register is used to specify the length (in bytes) of the Destination Buffer. The buffer length must be specified as a **negative number in two's complement form**. The contents of the Destination Count Holding Register are loaded automatically into the Destination Working Count Register whenever a Restart operation is initiated with the Destination Count Control bit in the Restart Control Register set to "0."

The Compressor logic does not modify this register during its operation.

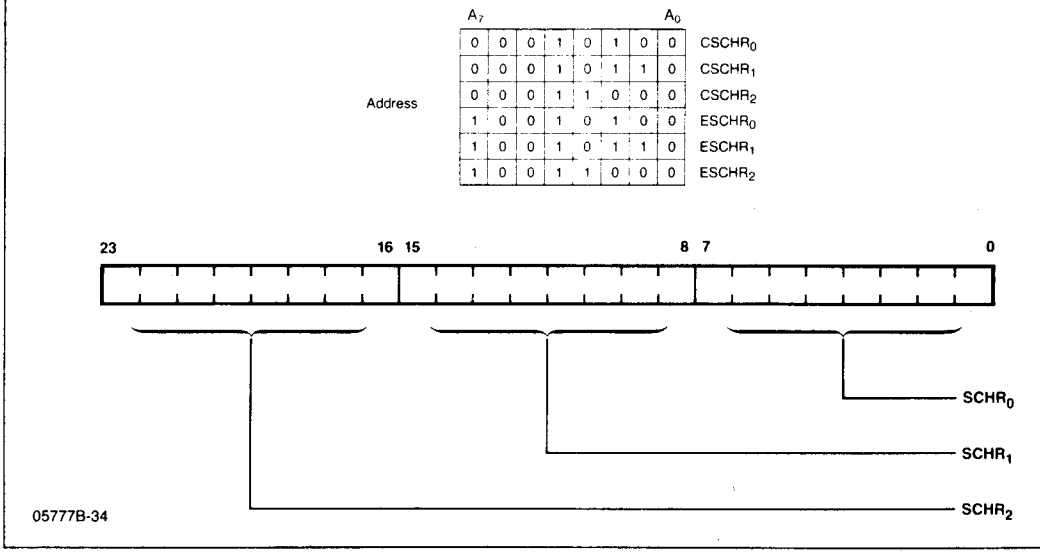

Figure 34. Compressor/Expander Source Count Holding Register (CSCHR/ESCHR)

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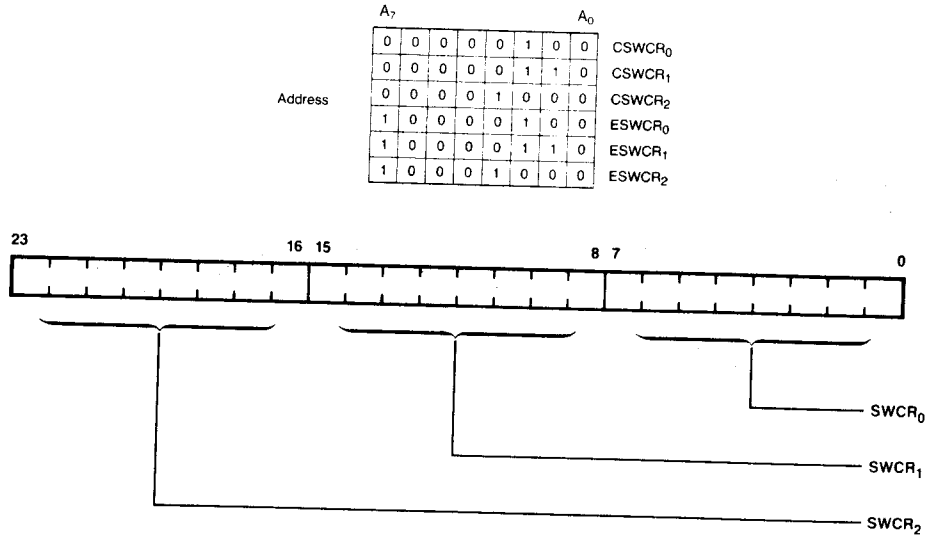

Figure 35. Compressor/Expander Source Working Count Register (CSWCR/ESWCR)

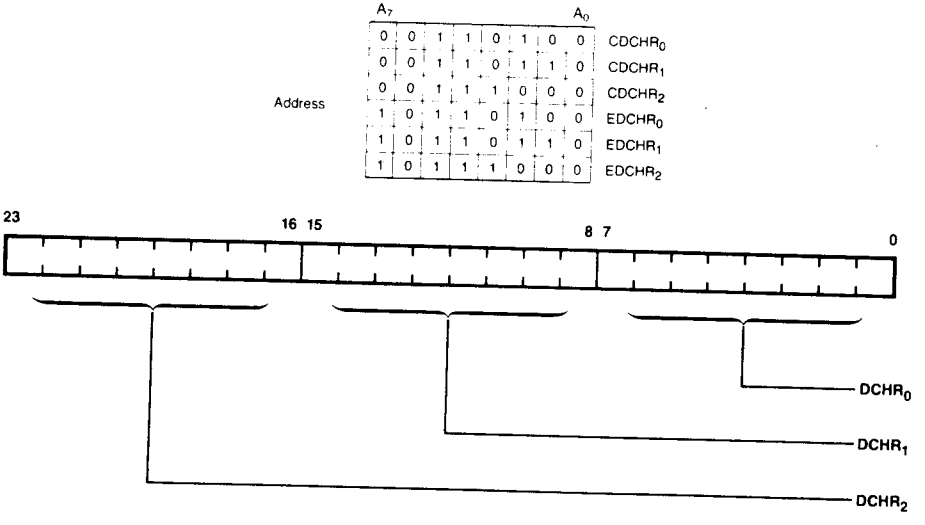

Figure 36. Compressor/Expander Destination Count Holding Register (CDCHR/EDCHR)

DESTINATION WORKING COUNT REGISTER (CDWCR/EDWCR)

Figure 37 shows the Destination Working Count Register. This 24-bit register is used to keep track of the number of Destination Buffer accesses. Initially, the Destination Working Count Register contains a 24-bit **negative two's complement number** specifying how many bytes long the Destination Buffer is.

The Am7970 increments the Destination Working Count Register by one after each destination transaction. As soon as the Destination Working Count Register reaches "0," the processor operation will terminate with processor Destination Overflow (DO) bit set in the appropriate Status Register. It should be noted that such a termination might be normal (error-free) or abnormal.

A normal termination occurs when the Am7970 is able to transfer a fully-processed line into the Destination Buffer without a premature destination overflow and the line did not result in an error such as negative compression. An abnormal termination due to premature destination overflow will result in an appropriate error status. In this condition the Am7970 will process the byte and then terminate abnormally. The Wraparound Incomplete (WPI) bit and Line Processing Incomplete (LPI) bit in the Status Register will reflect the appropriate error termination.

When a Restart operation is initiated with the Destination Count Control bit in the Restart Control Register set to "0," then the initial value loaded into the Destination Working Count Register is obtained from the Destination Count Holding Register. However, if this control bit is "1," the existing value in the Destination Working Count Register becomes the initial value.

STATUS REGISTER (CSR/ESR)

Figures 38 and 39 show the Status Register layout. This 8-bit register will indicate the outcome of the last operation initiated. The following paragraphs contain a detailed description of the Status Register bits for each processor.

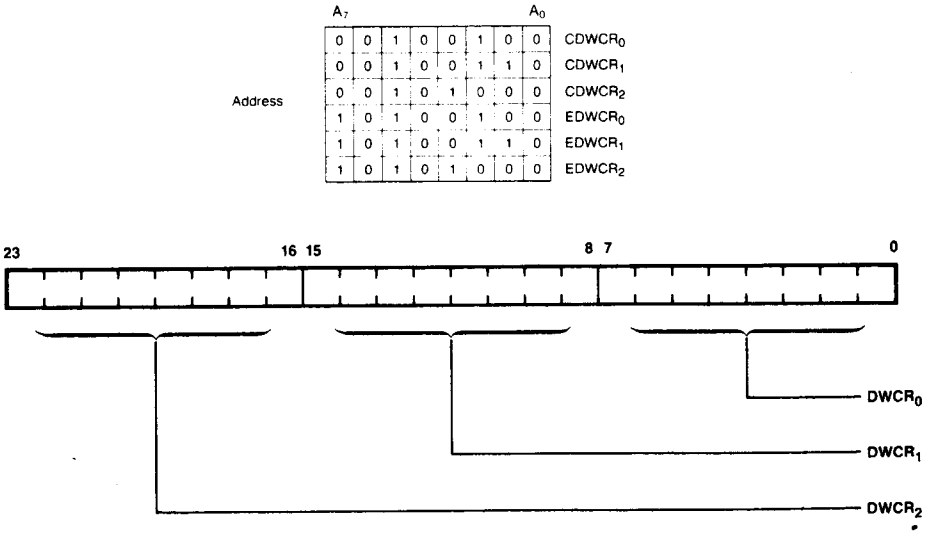

Figure 37. Compressor/Expander Destination Working Count Register (CDWCR/EDWCR)

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Refer to page 7-1 for Essential Information on Military Devices

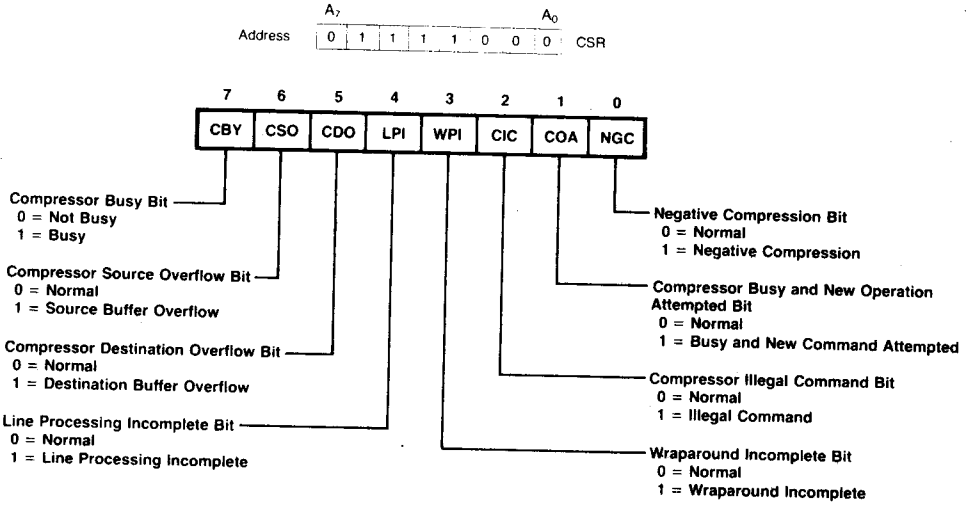

Figure 38. Compressor Status Register (CSR)

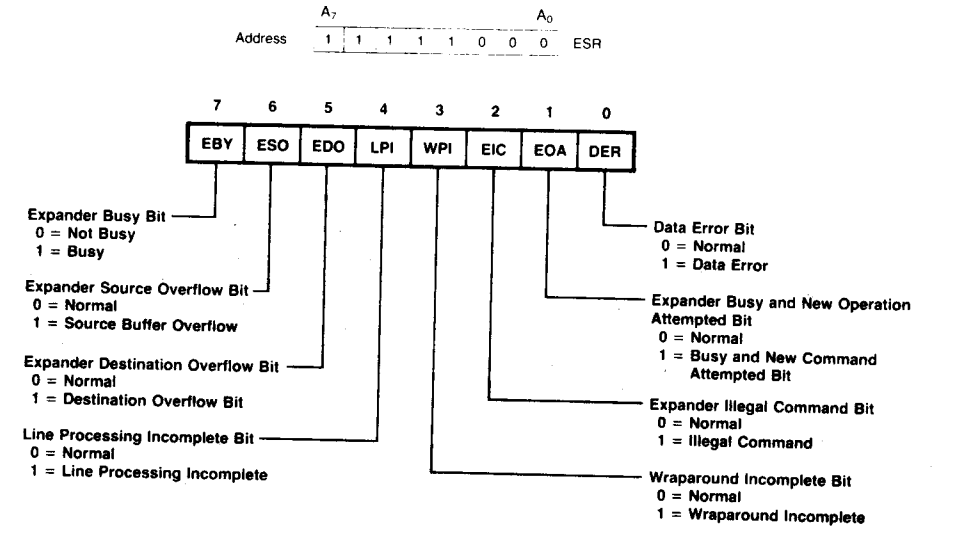

Figure 39. Expander Status Register (ESR)

Compressor Status Bits

Negative Compression (NGC) bit:

Bit 0 in the Compressor Status Register is set to "1" to indicate that the process of compressing the current line resulted in negative compression. This means that the total number of bytes in the compressed line is more than the number of bytes contained in the original effective line. The Am7970 checks for negative compression only after *completely processing* an effective line.

Prepositional EOL (if any) and Dummy Fill (if any) are included in determining the total number of bytes in a compressed line. Thus, the NGC indication reflects the effect of prepositional EOL and Dummy Fill bits in addition to the actual data. The Am7970 computes the number of bytes contained in the original effective line based on the contents of the Page Width Register and the Wraparound Register (when appropriate). Negative compression conditions are not checked during Transparent Mode of operation.

The Am7970 clears the NGC bit to "0" when a new operation is initiated from the Master Control Register.

Compressor Busy and New Operation Attempted (COA) bit:

Bit 1 in the Compressor Status Register is set to "1" to indicate that an attempt was made to write a new operation into the Master Control Register while the Compressor is still busy.

All registers which require user-specification in the Am7970 can be read as well as written by the host CPU. However, modifying the registers while the Compressor is operating is not allowed. Hence, the Am7970 will ignore any attempt to write into a register while the Compressor is busy. However, any erroneous attempt to write into the Master Control Register at such times sets the COA bit to "1" and marks the beginning of a Compressor termination. The actual termination will be indicated by the Compressor Busy (CBY) bit.

The COA bit will be cleared to "0" when a new operation is initiated.

Compressor Illegal Command (CIC) bit:

Bit 2 in the Compressor Status Register is set to "1" when the Compressor is directed to start operating with illegal conditions present. Any of the following will result in this status indication.

a) The Mode bits (CM0 and CM1) in the Master Control Register specify Two-Dimensional Compression and the Compressor Wraparound Register is non-zero. In other words, specifying Two-Dimensional Compression with Wraparound Mode is illegal.

b) The Compressor Express Register and Compressor Wraparound Register are both non-zero. In other words, specifying Express Mode and Wraparound Mode together is illegal.

c) The sum of the left and right margins represented by the Left Margin Register and Right Margin Register is greater than the page width specified in Compressor Page Width Register. In other words, specifying overlapping margins is illegal.

d) The Mode bits (CM0 and CM1) or the Control bits (CC0 and CC1) in the Master Control Register specify the reserved code.

e) The Compressor Page Width Register has been specified as "0."

From the above, it is apparent that the CIC bit is a check on the set-up conditions in the Compressor before it starts an operation. When the GO bit is set to "1" (that is, "start Compressor operation"), the Am7970 will clear the CIC bit to "0" and set the CBY bit to "1" to indicate busy status. The conditions for CIC status are then checked. If any illegal condition exists as stated above, the Am7970 will terminate the operation with the CIC bit set to "1" and CBY bit set to "0."

The state of this bit is "0" after a new operation is initiated.

Wraparound Incomplete (WPI) bit:

Bit 3 in the Compressor Status Register is set to "1" when the Compressor has terminated prior to successfully compressing an effective line. This status signifies that the Compressor has not satisfied the Compressor Wraparound Register requirements. The WPI bit being set in conjunction with the LPI bit gives a detailed indication of the status that exists when the Compressor is terminated. The setting of this bit marks the beginning of the Compressor termination. Actual termination will be indicated in the CBY bit of the Status Register. The WPI bit is cleared to "0" when a new operation is initiated.

Line Processing Incomplete (LPI) bit:

Bit 4 in the Compressor Status Register is set to "1" to indicate that the Compressor terminated without successfully processing a complete line; either a source or destination overflow occurred prematurely. There are three situations in which this occurs:

a) When the last byte obtained from the Source Buffer did not correspond to the last byte of the page and the Compressor Source Working Count Register overflowed.

b) When a Compressor Destination Working Count Register overflowed before the Compression operation reached the end of a scan line.

c) When a Compressor Destination Working Count Register overflowed before a fully compressed line could be stored in the destination. The term "fully compressed line" includes EOL (if any), data, Time Fill (if any), and Dummy Fill (if any).

The beginning of Compressor operation termination is marked by the LPI bit being set. Actual termination will be indicated by the CBY bit.

The LPI bit is cleared to "0" when a new operation is initiated.

Compressor Destination Overflow (CDO) bit:

Bit 5 of the Compressor Status Register is set to indicate that the Compressor Destination Working Count Register has reached "0." This register is initially loaded with a negative two's complement value and is incremented after each transaction with the Destination Buffer. When the Compressor Destination Working Count Register reaches "0" due to such incrementing, the CDO bit is set to "1," which marks the beginning of the Compressor termination process. The actual termination will be indicated by the CEP clearing the CBY bit to "0."

The CDO bit is cleared to "0" when a command is initiated.

Compressor Source Overflow (CSO) bit:

Bit 6 of the Compressor Status Register is set to "1" to indicate that the Compressor Source Working Count Register has reached "0." This register is initially loaded with a negative two's complement value and is incremented by one after each Source Buffer transaction. When the CSWCR reaches "0" due to such incrementing, source overflow has occurred and the CSO bit is set to "1." The Compressor will begin to terminate its operation after setting the CSO bit. Thus, there will be some elapsed time between setting the CSO bit and the actual termination as indicated by the CBY bit.

The CSO bit will be cleared to "0" when a command is initiated.

Compressor Busy (CBY) bit:

Bit 7 of the Compressor Status Register is set to "1" by the CEP to indicate that the Compressor is busy. Whenever a new operation is initiated (that is, the GO bit is set), the CBY will indicate busy status. The CBY bit will automatically become "0" when the Compressor terminates its operation. External access to any of the Am7970 registers is valid only when the CBY is "0," indicating "not busy." Otherwise the Am7970 might be modifying the registers as part of its normal operation.

If the CIE bit in the Master Control Register is "1," an interrupt to the CPU is asserted when the CBY becomes "not busy." The CSR bit can be polled by the host CPU for an indication of the completion of an operation.

Expander Status Register bits

Data Error (DER) bit:

Bit 0 in the Expander Status Register is called the Data Error (DER) bit. This bit indicates if a data error has been detected in the current effective line. If Bit 0 is set to "1," a premature termination of the Expander results. The address of the erroneous effective line will be recorded in the Expander Source Line Start Register. An error exists when the bit-length of an expanded effective line is not equal to

$$L = (EPWR * 8) * (EWR + 1)$$

Where: EPWR = The value of the Expander Page Width Register

EWR = The value of the Expander Wraparound Register.

An error might have resulted from a hardware failure or the inadvertent transformation of a valid Modified Huffman code word to another bit pattern due to noise. An unrecognizable code word would be ignored by the Expander. An effective line that contained an unrecognizable code word would be perceived by the Expander as too short and would cause the DER bit to be set to "1." **Note that the DER bit will only be set if the EOL bit in the Expander Parameter Register is set to Auto-EOL.**

The state of the DER bit, after a new command has been initiated by the the CPU, is "0."

Expander Busy and New Operation Attempted (EOA) bit:

Bit 1 is called the Expander Busy and New Operation Attempted (EOA) bit. This bit is set to "1" when an attempt is made to write a new command into the Expander Master Control Register while the Expander is still busy. Once the EOA bit is set to "1," the Expander will prematurely terminate and the Expander Busy (EBY) bit is cleared to "0."

After command has been initiated by the CPU, the state of the EOA bit is "0."

Expander Illegal Command (EIC) bit:

Bit 2 is set to "1" to indicate that the Expander was directed to start operating with any of the following illegal conditions present.

1) A Two-Dimensional Expansion Mode and a non-zero Wraparound Register have both been specified.
2) A non-zero Granularity Parameter and a non-zero Wraparound Register have both been specified.
3) EM0 and EM1 are both specified as "1."
4) EC0 and EC1 are both specified as "1."
5) The EPWR has been specified as "0."

If an Expander command is received when one or more of these conditions are present, the EIC bit will be set to "1" and the EBY bit will be cleared to "0."

After a new command has been initiated by the CPU, the state of the EIC bit is "0."

Wraparound Incomplete (WPI) bit:

Bit 3 is set to "1" to indicate that either the Source Buffer or the Destination Buffer overflowed after a complete scan line was expanded but before an entire effective line could be expanded.

After a new command has been initiated by the CPU, the state of the WPI bit is "0."

Line Processing Incomplete (LPI) bit:

Bit 4 is is set to "1" to indicate that either the Source Buffer or the Destination Buffer overflowed before an entire scan line could be expanded and written into the Destination Buffer.

The state of the LPI bit is "0" after a new command has been initiated by the CPU.

Expander Destination Overflow (EDO) bit:

Bit 5 is set to "1" to indicate that the Expander Destination Working Count Register has reached "0." This register is initially loaded with a negative two's complement value and is incremented after each transaction with the Destination Buffer. When the Expander Destination Working Count Register reaches "0" due to such incrementing, the EDO bit is set to "1." Setting of the EDO bit marks the beginning of the Expander termination process. The actual termination will be indicated by the CEP clearing the EBY bit to "0."

The state of the EDO bit is "0" after a new command has been initiated by the CPU.

Expander Source Overflow (ESO) bit:

Bit 6 is set to "1" to indicate that the Expander Source Working Count Register has reached "0." This register is initially loaded with a negative two's complement value and is incremented by one after each Source Buffer transaction. When the Expander Source Working Count Register reaches "0" due to such incrementing, overflow has occurred and the ESO bit will be set to "1." The Expander will begin to terminate its operation at this time. Thus there will be some elapsed time between setting the ESO bit to "1" and the actual Expander termination as indicated by the EBY bit.

The state of the ESO bit is "0" after a new command has been initiated by the CPU.

Expander Busy (EBY) bit:

Bit 7 is set to "1" to indicate that the Expander is busy. Whenever a new operation is initiated, the EBY bit is set to "1." When the Expander has completed its operation, the EBY bit is reset to "0."

PAGE WIDTH REGISTER (CPWR/EPWR)

Figure 40 shows the Page Width Register layout. This 16-bit register specifies the page width or length of a scan line in increments of 8 pels. The largest line the Am7970 can handle is 16K pels long because only 11 of these 16 bits are significant. **Bits 11 through 15** must be set to "0."

CCITT recommendation T.4 covers compression and expansion of scan lines no longer than 2560 bits. The Am7970 accommodates larger page widths up to 16K bits by allowing the use of multiple make-up codes.

Before starting a processor operation, the Am7970 checks the Page Width Register value against the Left Margin Register and the Right Margin Register values to ensure that the page width is greater than or equal to the sum of left and right margins. When the margin specifications are not consistent with the page width, the Am7970 will abort after setting the Illegal Command (IC) bit in the appropriate Status Register to "1."

The processor logic does not modify the Page Width Register during its operation.

RESTART CONTROL REGISTER (CRCR/ERCR)

Figure 41 shows the Restart Control Register layout. This 8-bit register contains control bits for specifying the initial values of the Source Current Address Register, Destination Current Address Register, Source Working Count Register, Destination Working Count Register, Source Line Start Address Register, and the Destination Line Start Address Register when a new processor operation is initiated. The following is a detailed description of the individual bits.

Source Count Control (SCC) bit:
When **Bit 0** in the Restart Control Register is "0," the contents of the Source Count Holding Register will be loaded into the Source Working Count Register when a new operation is initiated. When this bit is "1," such loading will not take place and the existing contents of the Source Working Count Register will be used for the new operation.

Source Address Control (SAC) bit:
When **Bit 1** in the Restart Control Register is "0," the contents of Source Address Holding Register will be loaded into the Source Current Address Register when a new operation is initiated. When this bit is "1," such loading will not take place and the existing contents of the Source Current Address Register will be used in the new operation.

Destination Count Control (DCC) bit:
When **Bit 2** of the Restart Control Register is "0," the contents of the Destination Count Holding Register will be loaded into the Destination Working Count Register when a new operation

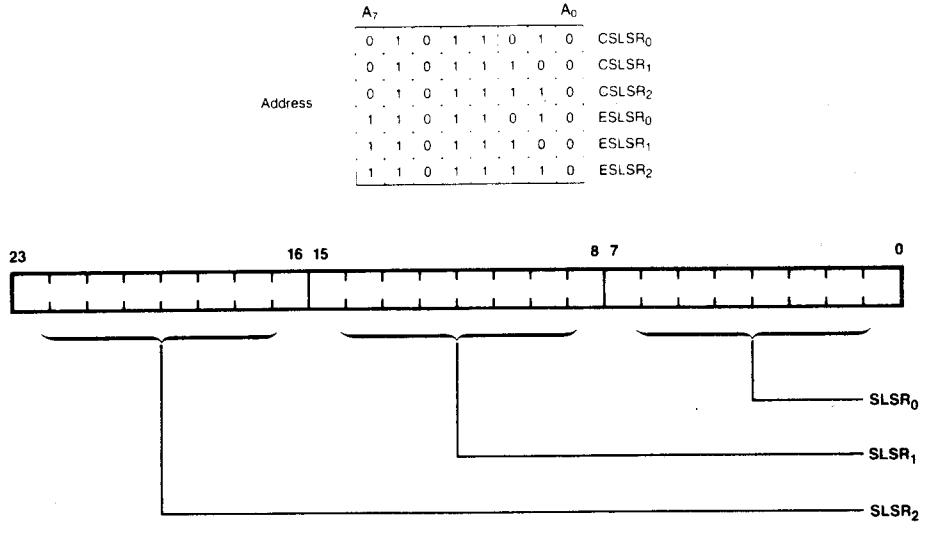

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Figure 40. Compressor/Expander Page Width Register (CPWR/EPWR)

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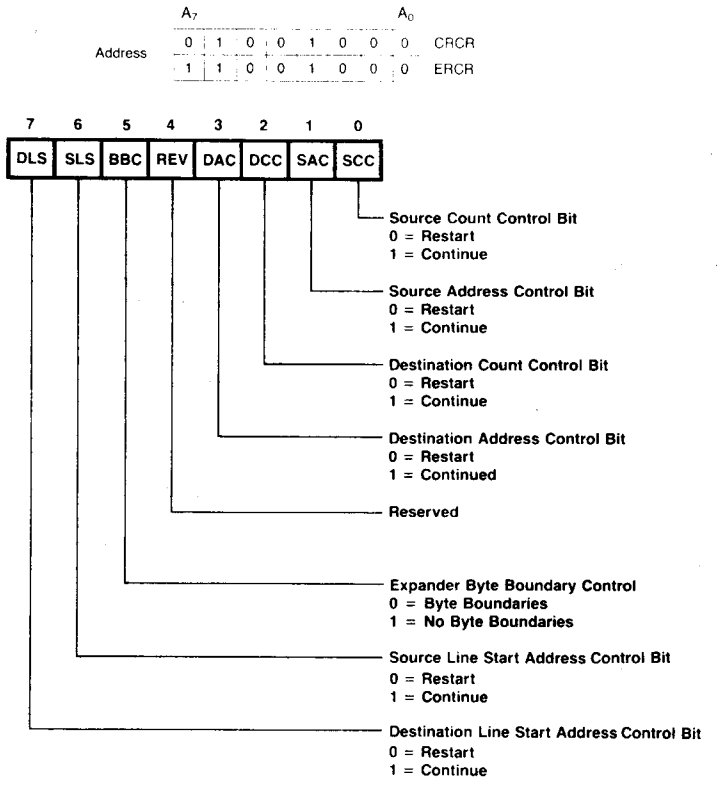

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Figure 41. Compressor/Expander Restart Control Register (CRCR/ERCR)

is initiated. When this bit is "1," such loading will not take place and the existing contents of the Destination Working Count Register will be used in the new operation.

Destination Address Control (DAC) bit:
When **Bit 3** of the Restart Control Register is "0," the contents of the Destination Address Holding Register will be loaded into the Destination Current Address Register when a new operation is initiated. When this bit is "1," such loading will not take place and the existing contents of the Destination Current Address Register will be used in the new operation.

Bit 4 is RESERVED

Expander Byte Boundary Control (BBC) bit:

Bit 5 in the Restart Control Register is the Expander Byte Boundary Control (BBC) bit. This bit is used to distinguish byte padding "0s" at the end of a coded line from the starting code of the next coded line, when the compressed data does not have EOL codes. If the compressed data was byte-adjusted without EOL codes, this bit should be set to "0."

When this bit is set to "1," the Expander will transfer the one to seven Dummy Fill bits, if incurred after an EOL, into the Destination Buffer, but will keep them in an internal register to be used in the beginning of the next line.

Source Line Start Address Control (SLC) bit:
When **Bit 6** of the Restart Control Register is "0," the Source Line Start Address Register will be loaded from either the Source Address Holding Register or the Source Current Address Register depending on whether the Source Address Control bit is "0" or "1" when a new operation is issued. When the Source Line Start Address Control bit is "1," the contents of the Source Line Start Address Register will not be modified when a new command is issued.

Destination Line Start Address Control (DLC) bit:
When **Bit 7** in the Restart Control Register is "0," the Destination Line Start Address Register will be loaded from the Destination Address Holding Register or the Destination Current Address Register, depending on whether the Destination Address Control bit is "0" or "1" when a new operation is issued. When the Destination Line Start Address Control bit is "1," the contents of the Destination Line Start Address Register will not be modified when a new command is issued.

SOURCE LINE START ADDRESS REGISTER (CSLSR/ESLSR)

Figure 42 shows the Source Line Start Address Register layout. This 24-bit register contains the address of the first byte of the current effective line in the Source Buffer. This register will be automatically updated when the Am7970 begins processing a new effective line. Thus, if the processor terminated after a successful completion of Single-Line operation, the Source Line Start Address Register will still contain the starting address of the line that was just completed.

During Multi-Line operations, the Am7970 will automatically begin processing the next line after successfully processing the previous line. In this case, the Compressor logic will always load the Source Current Address Register contents into the Source Line Start Register and then begin processing of the new line. This operation facilitates resetting the source back to the beginning of the line in case of a premature termination. The initial contents (not the updating process) of the Source Line Start Address Register are determined by the setting of certain bits in the Restart Control Register. For details of this operation see the description under the Restart Control Register section.

DESTINATION LINE START ADDRESS REGISTER (CDLSR/EDLSR)

Figure 43 shows the Destination Line Start Address Register layout. This 24-bit register contains the address of the first byte of the current line in the Destination Buffer. This register will be updated automatically when the processor starts a new line. Thus, if the processor terminates after the successful completion of a Single-Line operation, the Destination Line Start Address Register will still contain the starting address of the line that was just completed.

During Multi-Line operations, the processor will automatically begin processing the next line after successful completion of the previous line. In this case, the Am7970 logic will always load the Destination Line Start Address Register from the Destination Current Address Register before processing of the line begins. The Source Line Start Address Register is also loaded from the Source Current Address Register. Thus, before any access to the Destination Buffer for the new line, both the Source Line Start Address Register and the Destination Line Start Address Register will be updated. The operation will facilitate resetting the destination back to the beginning of a line in case of a premature termination.

The initial contents (not the updating process) of the Destination Line Start Address Register are determined by values loaded into the Restart Control Register. See the section on this register for further details.

MASTER STATUS REGISTER (MSR)

Figure 44 shows the Master Status Register layout. This 8-bit register provides both Expander and Compressor global status information to the CPU. The following is a detailed description of the various bits in this register.

Bits 0, 1, and 2 are the Extension (EXT) bits:
When **Bit 3** (ECD) is set to "1," the EXT bits will display the three least significant extension code bits which have been detected by the Expander. When the ECD bit is set to "0," the Extension bits are cleared to "0s." The EXT bits are also cleared when a new operation is initiated.

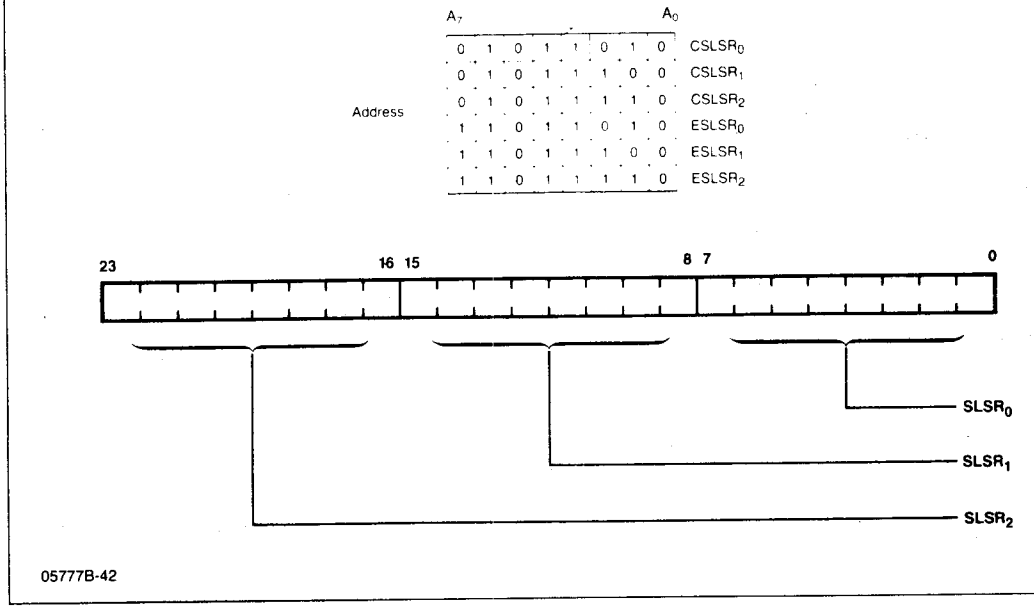

Figure 42. Compressor/Expander Source Line Start Address Register (CSLSR/ESLSR)

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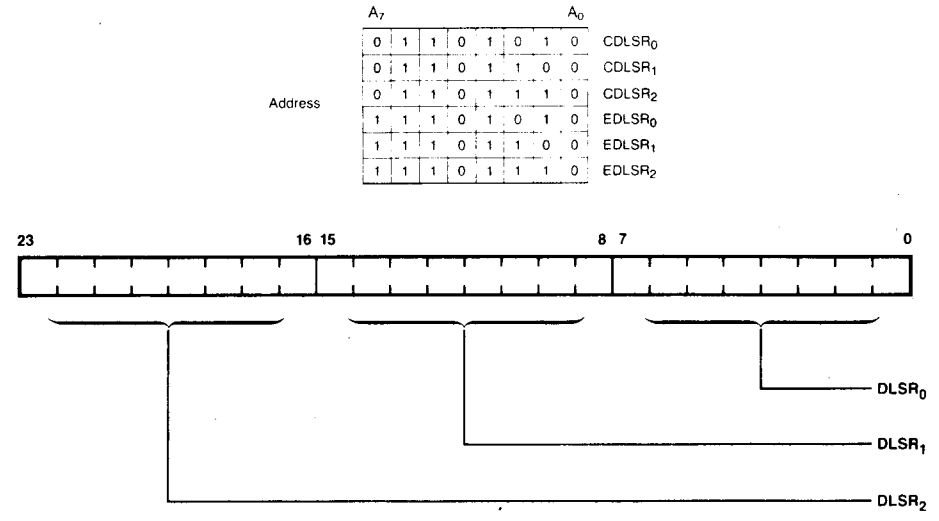

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Figure 43. Compressor/Expander Destination Line Start Address Register (CDLSR/EDLSR)

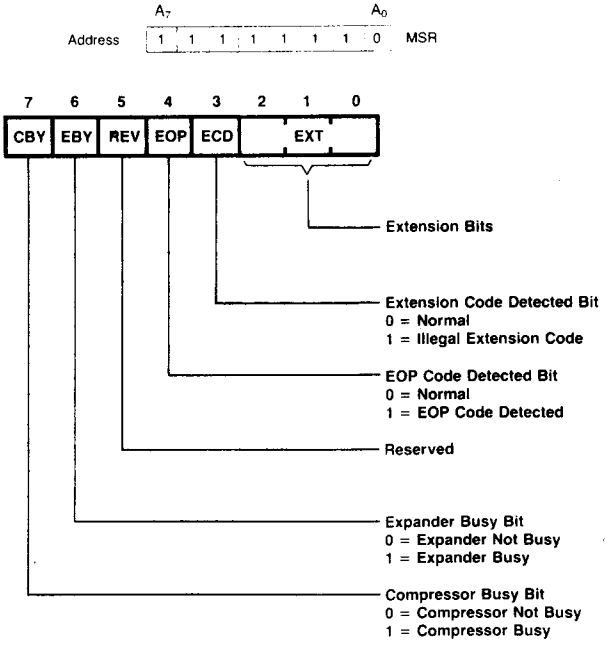

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Figure 44. Master Status Register (MSR)

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Bit 3 is the Extension Code Detected (ECD) bit: This bit is set by the Expander to indicate that an extension code, for which the least significant three bits are not all "1s," has been detected. The ECD bit is cleared to "0" after a new operation is initiated.

Bit 4 is the End-of-Page Detected (EOP) bit:
This bit is set by the Expander to indicate that an EOP code, made up of two contiguous EOL codes, has been detected in either One- or Two-Dimensional Expansion Mode. The Transparent Mode cannot detect an EOP code.

For example, two contiguous EOL code formats are:

000000000001000000000001	EOL codes for One-Dimensional or Group 4
000000000001100000000000011	EOL codes for Two-Dimensional or Group 3

The state of the EOP bit is "0" after a new operation is initiated.

Bit 5 of the Master Status Register is not used.

Bit 6 is the Expander Busy (EBY) bit:
This bit is equivalent to the EBY bit in the Expander Status Register.

Bit 7 is the Compressor Busy (CBY) bit:
This bit is equivalent to the CBY bit in the Compressor Status Register.

FUNCTIONAL DESCRIPTION

All CEP operations consist of at least three phases. In the first phase, the selected processor's registers are initialized to specify and control the desired operation. In the second phase, the processing operation itself is started and performed. The final phase involves terminating the selected processor and performing any actions that are appropriate to that termination. These different phases are described in detail in the following sections.

The Am7970 contains two separate buses—the System bus and Document Store bus. All control information exchanges between the Am7970 and the host processor take place only on the System bus. The Am7970 processes two types of data: uncompressed or image data and compressed or coded data. That portion of a memory where image data is held is called the Line Buffer. In a system using the Am7970, the Line Buffer can be located in the host CPU memory (called Main Memory) or in the Document Store. That portion of a memory where compressed data will reside is called Code Buffer. In an Am7970 system, the Code and Line Buffers can be located in the Main Memory or the Document Store. When the Am7970 needs data from the Line or Code Buffer located in the Main Memory, the transfer will take place on the System bus using the on-chip DMA facilities of the CEP. When the Am7970 needs data from the Line or Code Buffer located in the Document Store Memory, the transfer will take place on the Document Store bus.

The Am7970 is equipped with registers to specify the location of the Line Buffer, its starting address and assigned length, as well as the location of the Code Buffer, its starting address and assigned length.

The Am7970 Compressor is completely independent from the Expander. The Compressor has its own facilities to specify the Code Buffer and the Line Buffer. The Compressor will take image data from the Line Buffer and load the resulting compressed data into the Code Buffer. In an Am7970 system, the Compressor can be operating from its Line and Code Buffers while the Expander is using its own buffers. Such independent and simultaneous operation of the Compressor and Expander is called the full-duplex mode.

The Am7970 Expander will take compressed data from the Code Buffer for processing and the resulting image data will be loaded into the Line Buffer. The source for the expansion process is the Code Buffer and the destination is the Line Buffer.

For certain images (such as half-tones), the compressed data representing a line may be longer than the original line of the image. The Am7970 checks for this condition after compressing a line to alert the host processor of this situation via an Interrupt and Status Bit.

An End-of-Line (EOL) code may delimit each compressed line according to the CCITT recommendation for Group 3 facsimile apparatus. However, this automatic EOL insertion can be suppressed by appropriate bit settings of the Am7970 (Group 4).

The CCITT recommendation T.4 for Group 3 equipment requires that each coded line be a certain minimum length. Time Fill bits will be added by the CEP to a shorter line when necessary to meet this requirement. The Am7970 contains a Time Fill Register to specify the minimum line lengths (including zero).

Data is vulnerable to modification by transmission errors. When such data is expanded, the resulting image will be different from the original. The Am7970 checks whether the expanded line has the same number of picture elements as required by the specified paper width. If there is a discrepancy, the CPU will be alerted.

INITIALIZATION

The Am7970 has several initialization requirements. Those initialization requirements include:

- The Source Buffer definition,
- Attribute definition for the Source Buffers,
- The Destination Buffer definition,
- The restart conditions definition,
- The operating mode definition,
- The processing mode definition,
- Definition of the compressed data format,
- The minimum transmission time definition,
- The paper width definition,
- The optional function definitions.

The system program should specify certain initial conditions before starting the operation of the Am7970. The Source Buffer definition requires that the residency of the Source Buffer, the starting address of the Source Buffer and the capacity of the Source Buffer be specified. The system program should load "0" into the Compressor Source Control (CSC) bit/ Expander Source Control (ESC) bit in the Compressor Master Control Register (CMCR)/Expander Master Control Register (EMCR) when a Source Buffer that is located in the Main

Memory is required. If a Source Buffer that is located in the Document Store is required, then the system program should load a "1" into the CSC/ESC bit.

The system program should load a starting address into the Compressor Source Address Holding Register (CSAHR)/Expander Source Address Holding Register (ESAHR) and the Compressor Source Current Address Register (CSCAR)/Expander Source Current Address Register (ESCAR). Also, the system program should load the length (in bytes) of the Source Buffer into the Compressor Source Count Holding Register (CSCHR)/Expander Source Count Holding Register (ESCHR) and the Compressor Source Working Count Register (CSWCR)/Expander Source Working Count Register (ESWCR). The length of the Source Buffer has additional requirements that are discussed under the specific Source Register sections. The system program should adhere to these recommendations. The system program must set the Source Attribute (CSA/ESA) bit in the CPR/EPR Register when the CEP will process a new page. More detailed information is discussed in the sections on the CPR Register and the EPR Register.

The Destination Buffer definition requires that the residency of the Destination Buffer, the starting address of the Destination Buffer, and the capacity of the Destination Buffer be specified. The system program should load "0" into the Compressor Destination Control (CDC) bit/Expander Destination Control (EDC) bit in the CMCR/EMCR register when the Destination Buffer is located in the Main Memory. If the Destination Buffer is located in the Document Store, the system program should load "1" into the CDC/EDC bit. The system program should load the starting address into the Compressor Destination Address Holding Register (CDAHR)/Expander Destination Address Holding Register (EDAHR) and Compressor Destination Current Address Register (CDCAR)/Expander Destination Current Address Register (EDCAR). Also, the system program should load the negative two's complement of the length (in bytes) of the Destination Buffer into the Compressor Destination Count Holding Register (CDCHR)/Expander Destination Count Holding Register (EDCHR) and the Compressor Destination Working Count Register (CDWCR)/Expander Destination Working Count Register (EDWCR). The length of the Destination Buffer has some conditions that are are discussed in the specific sections which cover the Destination Registers and the system program should adhere to those recommendations.

The system program should load any Restart information into the Compressor Restart Control Register (CRCR)/Expander Restart Control Register (ERCR). The system program should follow the recommendations of the Restart Control Register section. The system program must specify a compressed data format by the Data Format Control (DFC) bits in the Compressor Parameter Register (CPR). This is discussed in more detail in the description of the CPR Register.

The system program should load the operating mode into the Compressor Master Control Register (CMCR)/Expander Master Control Register (EMCR). The system program should follow the recommendations of the Mode Control section under the Master Control Register description. Also the system program should load the operation control into the CMCR/EMCR, the minimum transmission condition into the Time Fill Register (TFLR) and the horizontal resolution into the Compressor Page Width Register (CPWR)/Expander Page Width Register (EPWR).

The definitions consist of eleven different functions. These functions are called:

- Optional Auto-EOL
- Optional byte boundary control
- Wraparound
- Express
- Top Margin
- Left Margin
- Right Margin
- Bottom Margin
- K-Parameter
- G-Parameter
- Interrupt Enable

The system program should load the Auto-EOL option into the AEOL bit in the Compressor Parameter Register (CPR). If the automatic insertion of an EOL code is required, the system program should load "0" into the AEOL bit. If this bit is "1," such automatic insertion of EOL is suppressed.

The system program should specify the Wraparound, Express, and the Top, Left, and Right Margin options by loading the corresponding registers. These optional functions are described in detail in their individual sections. The system program should adhere to those recommendations.

The system program should specify the K-Parameter in the K-Register when Two-Dimensional processing is required. If the granularity option is required, the system program should specify the G-Parameter in the Expander Parameter Register. The system program should load "1" into the Compressor Interrupt Enable (CIE) bit in the Compressor Master Control Register (CMCR)/Expander Interrupt Enable (EIE) bit in the Expander Master Control Register (EMCR) if an interrupt request is not required upon CEP termination. If an interrupt request is not required, the system program should load "0" into the CIE/EIE bit of the CMCR/EMCR register.

The system program should load "0" into the EOL bit in the Expander Parameter Register (EPR) when data with attached EOL is going to be received. If the data that is to be received contains no EOL codes, the system program should load "1" into the EOL bit in the EPR register.

START PROCESSING PROCEDURES

The Am7970 has two operating configurations. The Expander and the Compressor may be operated simultaneously in a full-duplex mode, or the Expander or the Compressor may be operated without the other processor (half-duplex). The system program can initiate the full-duplex mode by loading "1s" into the GO bits of the Compressor Master Control Register (CMCR) and the Expander Master Control Register (EMCR). If the half-duplex operation is required, the system program should load a "1" into the GO bit in the Compressor Master Control Register or the system program should load a "1" into the GO bit in the Expander Master Control Register. Further, the CEP has two different types of starting conditions: resumable operation and non-resumable operation. If resumable operation is required, the system program must not

issue a Reset operation via the appropriate Master Control Register or assert the RESET input. On the other hand, the system program must specify a Reset operation before starting its processing when no resumable operation is required; for example, the CEP is going to process a new page.

HOW TO USE THE STATUS REGISTERS

The CEP has three status registers: the Master Status Register (MSR), the Compressor Status Register (CSR), and the Expander Status Register (ESR). Bits 6 and 7 (EBY, CBY) in the MSR register provide both the Compressor and Expander general information to the CPU. These bits are known as the Expander Busy (EBY) bit and the Compressor Busy (CBY) bit. The system program should test Bits 6 and 7 if the MSR register general status information is required. If the system program requires detailed status information, then the system program should test the Compressor Status Register (CSR) or the Expander Status Register (ESR) directly. Bits 0 to 3 (EXT, ECD) in the Master Status Register (MSR) indicate the uncompressed mode status of the Expander. Bit 4 in the Master Status Register (MSR) indicates that the Expander detected an End-of-Page (EOP) code. If interrupts have not been enabled, the system program should periodically poll Bit 6 (EBY) and Bit 7 (CBY) in the MSR register. If the system program is enabled to respond to an interrupt, it should test the EBY bit and the CBY bit in the Master Status Register (MSR) when a CEP interrupt occurs.

INTERRUPT HANDLING

The Am7970 will drive its interrupt line (INTR) High when the Compressor Busy (CBY) bit in the Compressor Status Register (CSR) or the Expander Busy (EBY) bit in the Expander Status Register (ESR) changes from "1" to "0" while the Compressor Interrupt Enable (CIE) bit in the Compressor Master Control Register (CMCR) or the Expander Interrupt Enable (EIE) bit in the Expander Master Control Register (EMCR) has been set to "1." The INTR line will remain High until the Master Status Register (MSR) has been accessed by the system program. The system program may test the MSR register to distinguish Compressor interrupts from Expander interrupts. The system program should isolate the cause of the interrupt by reading the appropriate status register (CSR or ESR). The system program may then execute its interrupt service routine to respond to the interrupt.

STOPPING THE CEP

The CEP may be terminated by writing to the CEP's Master Control Register while the CEP is busy, or by issuing a hardware RESET. The soft abort will occur if the system program loads new information into the Master Control Register (Compressor or Expander) while the CEP is busy. If the system program is immediately required to stop, the system program should assert the RESET input of the Am7970. This is called a hardware stop. If the system program executes a hardware stop, the CEP will not save the current status. If the system program executes a software stop, the CEP will terminate its operation and keep the Compressor Busy and the New Operation Attempted (COA) bit or Expander Busy and New Operation Attempted (EOA) bit; however, this is not a resumable operation.

COMPRESSOR ERROR RECOVERY PROCEDURES

The Compressor will detect several error conditions: a premature source overflow, a premature destination overflow or an illegal command. An error condition will also be detected if a new command is attempted while the Compressor is busy or if negative compression occurs. A pre-mature source or destination overflow will be illuminated by the Wraparound Incomplete (WPI) bit or the Line Processing Incomplete (LPI) bit of the Compressor Status Register (CSR).

The error recovery procedure for an LPI error must include the redefinition of the Source Buffer or the Destination Buffer as follows:

1) Premature Source Overflow

   New CSCHR = N * Hr * Apw/8

   New CSWCR = 2's complement of new CSCHR − old CSCHR

   New CSCAR = CSLSR, new CDCAR = CDLSR

   CRCR = All one (X'FF')

   New CDWCR = old CDWCR = (CDCAR − CDLSR)

2) Premature Destination Overflow

   New CDCHR = N * Hr * Apw/8 (See Section 12)

   New CDWCR = 2's complement of new CDCHR − old CDCHR

   New CDCAR = CDLSR, new CSCAR = CSLSR

   CRCR = All one (X'FF')

   New CSWCR = old CSWCR − (CSCAR − CSLSR)

The error recovery procedure for a WPI error without an LPI error may include restarting the Source Buffer or the Destination Buffer. If an illegal command is detected, the system program should load Continue Operation into the CEP or reissue a new command to the CEP when the Compressor or Expander Busy and New Operation Attempted error (COA or EOA) is detected. If negative compression is detected, the system program should load a Continue Operation command into the CEP or the system program should replace the line of "negatively compressed" data with transparent data.

EXPANDER ERROR RECOVERY PROCEDURES

The Expander will detect several error conditions: a premature source overflow, a premature destination overflow, an illegal command, an Expander Busy and New Operation Attempted error, a data error or an undefined extension code. A premature source or destination overflow will be illuminated by the WPI bit and the LPI bit of the Expander Status Register (ESR). The error recovery procedure for a premature overflow requires that the Source Buffer and the Destination Buffer be redefined as follows:

1) Premature Source Overflow and LPI without WPI

   New ESCHR = N * Hr * Apw/8

   New ESWCR = 2's complement of new ESCHR − old ESCHR

   ERCR = All one (X'FF')

New EDWCR = old EDWCR − (EDCAR − EDLSR)

New ESCAR = ESLSR, new EDCAR = EDLSR

2) Premature Destination Overflow and LPI without WPI

New EDCHR = N * Hr * Apw/8

New EDWCR = 2's complement of new EDCHR − old EDCHR

New EDCAR = EDLSR, new ESCAR = ESLSR

ERCR = All one (X'FF')

New ESWCR = old ESWCR − (ESCAR − ESLSR)

If the system program detects a premature overflow and the WPI error bit is set without the LPI error bit being set, the system program should restart the Source or Destination Buffer. If an illegal command is detected, the system program should load Continue Operation into the CEP or reissue a new command to the CEP when the Expander Busy and New Operation Attempted (EOA) error is detected.

If a data error is detected, the system program should replace the error line with a copy of the previous line as follows:

New ESCAR = EDLSR N * Hr * Apw/8

N = EWR + 1

New ESWCR = 2's complement N * Hr * Apw/8

New EDCAR = EDLSR

New EDWCR = EDWCR − (EDCAR − EDLSR)

ERCR = All one (X'FF')

EM0 and EM1 = 0 (Transparent Mode)

CPU ACCESS OPERATIONS

The procedure by which a CEP register is accessed by the CPU is as follows:

Read Access Operation

1) The CPU places an address on the CPU address lines A_0–A_7 that specifies the intended register.
2) The CPU address decoder (external to the CEP) drives the $\overline{CS}$ input Low.
3) The CEP will drive the READY output Low.
4) The CPU will drive the $\overline{RD}$ input Low.
5) The CEP READY output will be driven High when the CEP register data is available.
6) AD_{16}–AD_{23} will be driven by the CEP with valid data.
7) The CPU will drive the CEP $\overline{RD}$ input High.
8) The $\overline{CS}$ input will be driven High. Further read accesses can be initiated by executing Step 1.

Note: If Step 7 precedes Step 5, the read access will be aborted by the CEP. If the read access is aborted, READY will be driven High and AD_{16}–AD_{23} will float. Further read accesses can be initiated by executing Step 1.

Write Access Operation

1) The CPU places an address on the CPU address lines A_0–A_7 that specifies the intended register.
2) The CPU address decoder (external to the CEP) drives the $\overline{CS}$ input Low.

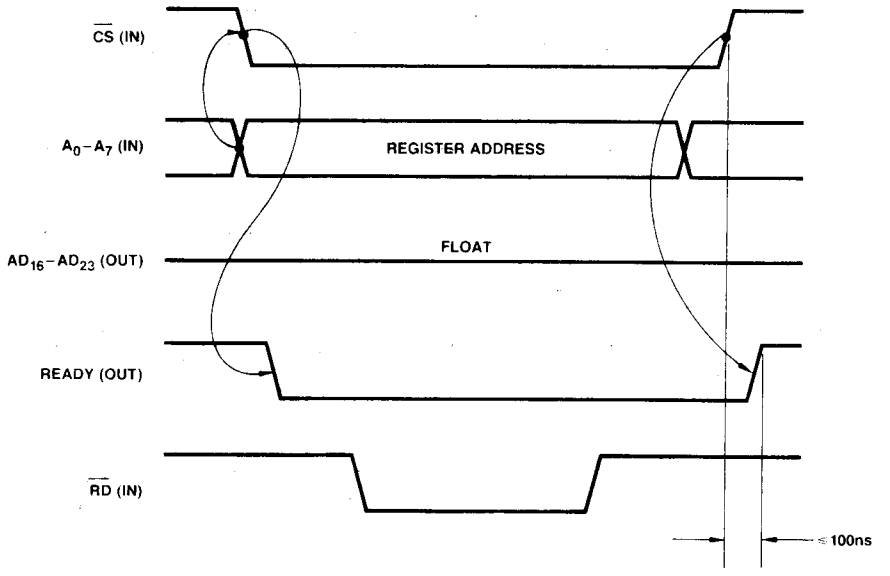

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Figure 45. CPU Program Read Access Abort Timing

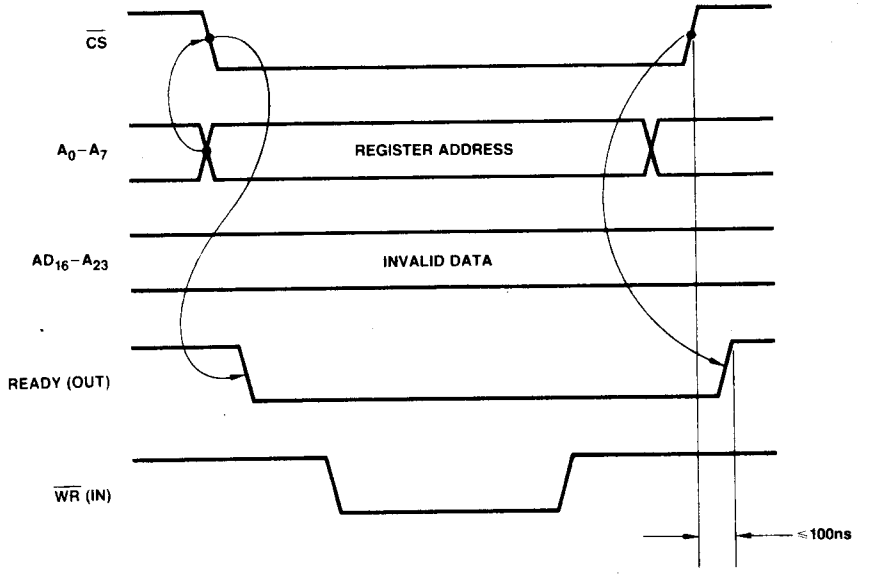

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Figure 46. CPU Program Write Access Abort Timing

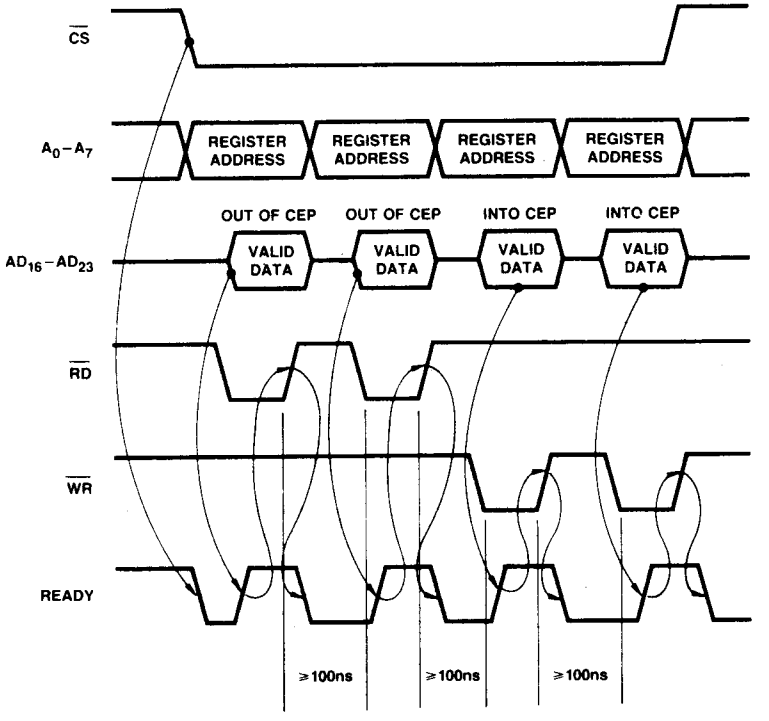

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Figure 47. CPU Block I/O Transaction Timing (CEP is slave)

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3) The CEP will drive the READY output Low.

4) The CPU will drive the $\overline{WR}$ input Low.

5) AD_{16}–AD_{23} will be driven by the CPU with valid data.

6) The CEP READY output will be driven High after data has been loaded into the appropriate register.

7) The CPU will drive the CEP $\overline{WR}$ input High.

8) The $\overline{CS}$ input will be driven High. Further write accesses can be initiated by executing Step 1.

Note: If Step 7 precedes Step 6, the write access will be aborted. If the write access is aborted, READY will be driven High. The contents of the specified register will not be altered. Further write accesses can be initiated by executing Step 1.

DMA OPERATION

The procedure by which the CEP executes a DMA operation is as follows:

Read Access Operation

1) The CEP drives the HRQ output High.

2) The CPU drives the HLDA input High.

3) The CEP drives the ALE output High and places a memory address (24 bits) on the CPU bus during CEP state T1. The address will be valid during the High to Low transition of the ALE output (CEP state T2, falling edge).

4) The CEP drives the $\overline{RD}$ output Low (CEP state T2, rising edge).

5) The state (High or Low) of the READY input is sampled by the rising edge of T2.

6) If the READY input is Low, a Wait State will be inserted. The READY input should become High when the memory location becomes available (CEP Wait State, rising edge).

7) If the READY input is High, then AD_{16}–AD_{23} must be driven with valid data (from the indicated memory location). The rising edge of T3 samples the data on AD_{16}–AD_{23}.

8) The CEP drives the $\overline{RD}$ output High (CEP state T3, rising edge).

9) The CEP drives the HRQ output Low.

10) The CPU drives the HLDA input Low.

Note: The CEP repeats Steps 1 through 8 until no further processing is required. The HRQ output will then be driven Low for at least two clock cycles. If additional bus transactions are required by the CEP, the CEP will drive the HRQ output High after a minimum of two clocks have elapsed (Step 1).

Write Access Operation

1) The CEP drives the HRQ output High.

2) The CPU drives the HLDA input High.

3) The CEP drives the ALE output High and places a memory address (24 bits) on the CPU bus (state T1, falling edge). The address will be valid during the High to Low transition of the ALE output.

4) AD_{16}–AD_{23} will be driven by the CEP with valid data (CEP state T2, falling edge).

5) The CEP drives the $\overline{WR}$ output Low (CEP state T2, rising edge).

6) The state (High or Low) of the READY input is sampled by the CEP at the state T2 rising edge.

7) If the READY input is Low, a Wait State will be inserted. The READY input should be driven High after data has been loaded into the appropriate memory location (CEP Wait State, rising edge).

8) The CEP drives the $\overline{WR}$ output High (CEP state T3, rising edge).

9) The CEP drives the HRQ output Low.

10) The CPU drives the HLDA input Low.

Note: The CEP repeats Steps 1 through 8 until no further processing is required. The HRQ output will then be driven Low for two clock cycles. If additional bus transactions are required by the CEP, the CEP will drive the HRQ output High (Step 1).

DOCUMENT STORE BUS OPERATION

The procedure by which the CEP executes a Document Store memory operation is as follows:

Read Access Operation

1) The CEP places a Document Store address (24 bits) on the Document Store bus (CEP state T1). The address will be valid during the High to Low transition of the DALE output (CEP state T2, falling edge).

2) The CEP drives the $\overline{DRD}$ output Low (CEP state DT2, rising edge).

3) The state (High or Low) of the READY input is sampled by DT2, rising edge.

4) If the DREADY input is Low, a Wait State will be inserted. The READY input should become High when the Document Store location becomes available (CEP Wait State, rising edge).

5) If the DREADY input is High, then DAD_{16}–DAD_{23} must be driven with valid data from the indicated Document Store location (CEP state DT3, falling edge).

6) The CEP drives the $\overline{DRD}$ output High (CEP state T3, rising edge).

Write Access Operation

1) The CEP places a Document Store address (24 bits) on the Document Store bus (CEP state T1, falling edge). The address will be valid during the High to Low transition of the DALE output (CEP state T2, falling edge).

2) DAD_{16}–DAD_{23} will be driven by the CEP with valid data (T2 falling edge).

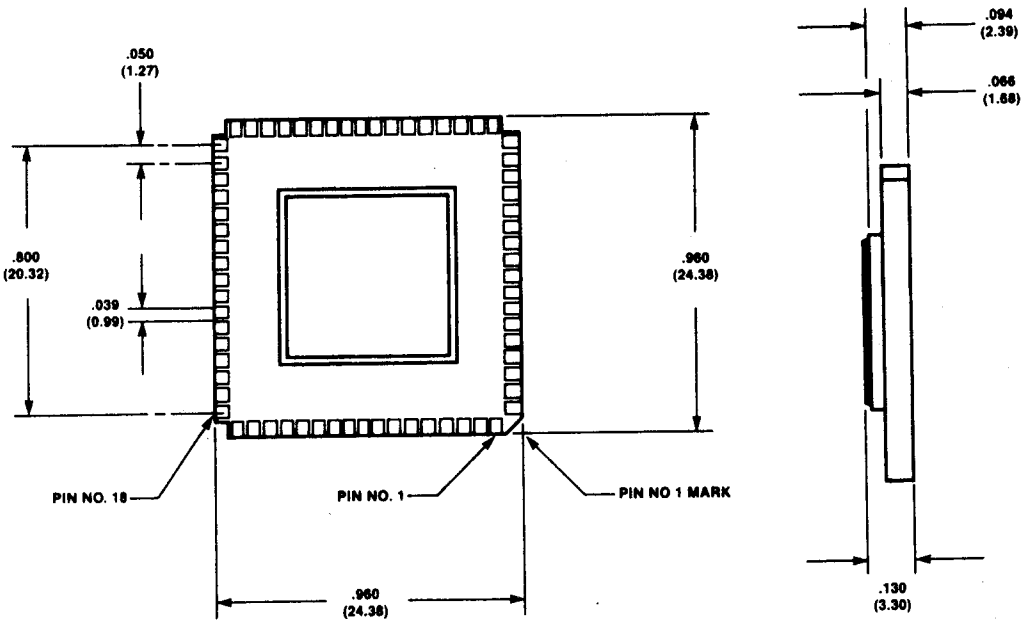
3) The CEP drives the $\overline{DWR}$ output Low (CEP state T2, rising edge).

4) The state (High or Low) of the DREADY input is sampled by the T2 rising edge.

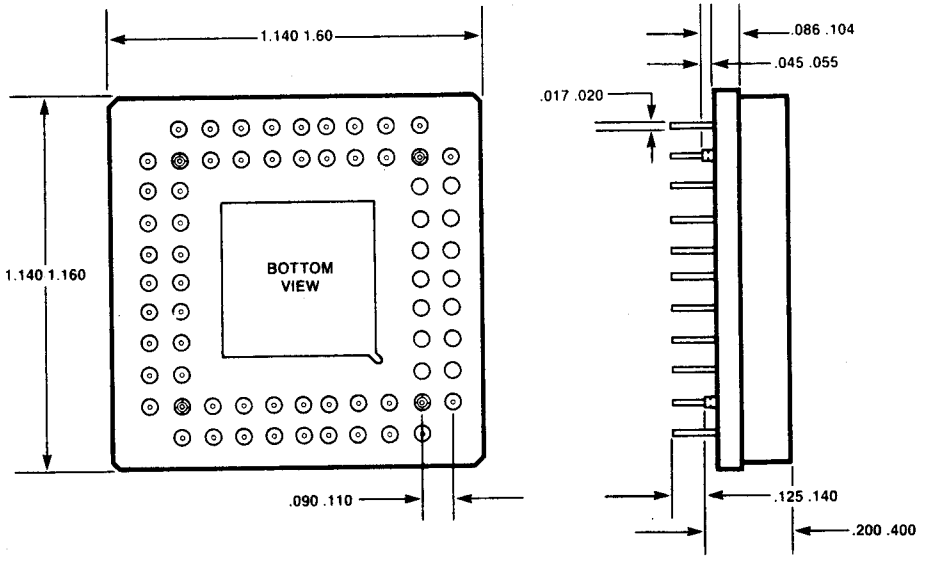
5) If the DREADY input is Low, a Wait State will be inserted. The DREADY input should be driven High after data has been loaded into the appropriate Document Store location (CEP Wait State, rising edge).

6) The CEP drives the $\overline{DWR}$ output High (CEP state DT3, rising edge).

PACKAGE SIZE



LCC PACKAGE



PGA PACKAGE

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Electrical Specifications
5 MHz Am7970 CEP

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	−65°C to +150°C
Voltage on Any Pin With Respect to Ground	−1.0V to +7.0V
Power Dissipation	

DC CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 5V±10%)

Symbol	Parameter	Test Conditions	Min	Max	Unit
VIL	Input Low Voltage		−0.5	0.8	V
VIH	Input High Voltage		2.0	V_{CC} + 0.5	V
VOL	Output Low Voltage	IOL = 3.2 mA		04	V
VOH	Output High Voltage	IOH = 400 µA	2.4		V
ICC	Power Supply Current	Ta = 25C			mA
ILL	Input Leakage Current	0V Vin V_{CC}		±10	µA
ILO	Output Leakage Current	0.45V V_{OUT} V_{CC}		±10	µA
VCL	Clock Input Low Voltage		−0.5	+0.8	V
VCH	Clock Input High Voltage		2.0	V_{CC}+0.5	V
CIN	Capacitance of Input Buffer (All input except A0–15, AD16–23, DA0–16, DAD16–23)	fc = 1 MHz		10.0	PF
CIO	Capacitance of I/O Buffer (A0–15, AD16–23, Da0–15, DAD16–23)	fc = 1 MHz		10.0	PF
CO	Capacitance of Output Buffers	fc = 1 MHz		10.0	PF

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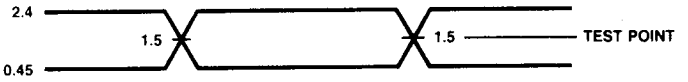
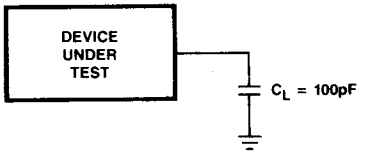
INPUT/OUTPUT AC Testing: Input. Output Waveform



AC Testing: Inputs are driven at 2.4V for logic "1" and 0.45V for a logic "0" timing measurements are made at 1.5V for both a logic "1" and "0"

AC Testing Load Circuit



C_L includes Jig Capacitance

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SWITCHING CHARACTERISTICS (TA = 0°C to 70°C, V_{CC} = 5V ±10%)
TIMING REQUIREMENTS

# Parameter	Description	Test Conditions	Min	Typ	Max	Unit
1 TCLCL	CLK Cycle Period	From 0.8V to 0.8V	200.0		2000.0	ns
2 TCHCL	CLK HIGH Time	From 2.0V to 2.0V	85.0			ns
3 TCLCH	CLK LOW Time	From 0.8V to 0.8V	85.0			ns
4 TCH1CH2	CLK Rise Time	From 0.8V to 2.0V			15.0	ns
5 TCL2CL1	CLK Fall Time	From 2.0V to 0.8V			15.0	ns
6 TRHVH	Power Supply HIGH to RESET LOW Time		4TCLCL			ns
7 TRHRL	RESET HIGH TIME		4TCLCL			ns
8 TRLSL	RESET LOW to First $\overline{CS}$		2TCLCL			ns
9 THAHCH	HLDA RE Set-up Time		30.0			ns
10 THALCH	HLDA FE Set-up Time		30.0			ns
11 TAVSL	Address Valid to $\overline{CS}$ LOW		20.0			ns
12 TSLRDL	$\overline{CS}$ LOW to $\overline{RD}$ FE Set-up Time		20.0			ns
13 TRDHSH	$\overline{RD}$ HIGH to Next Address Active		0.0			ns
14 TSLWRL	$\overline{CS}$ LOW to $\overline{WR}$ LOW		30.0			ns
15 TDVRYH	Data Valid to READY RE		30.0			ns
15a TDVWH	Data Valid to $\overline{WR}$ High		30.0			ns
16 TWRHDV	DATA Hold Time		20.0			ns
17 TWRHSH	$\overline{WR}$ to Address Active		0.0			ns
18 TRYLCH	READY FE Set-up Time		60.0			ns
19 TCHDXY	READY Hold Time		20.0			ns
20 TRYHCH	READY		20.0			ns
21 TDVCH	DATA IN Set-Up Time		30.0			ns
22 TCHDX	DATA IN Hold Time		10.0			ns

Note: Switching characteristics are targetted numbers and are subject to change without notice.

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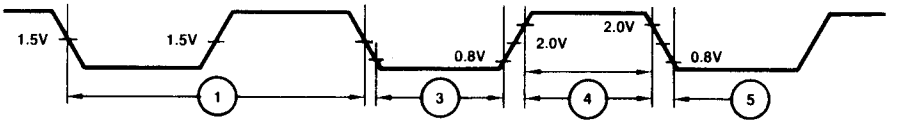
Refer to page 7-1 for Essential Information on Military Devices



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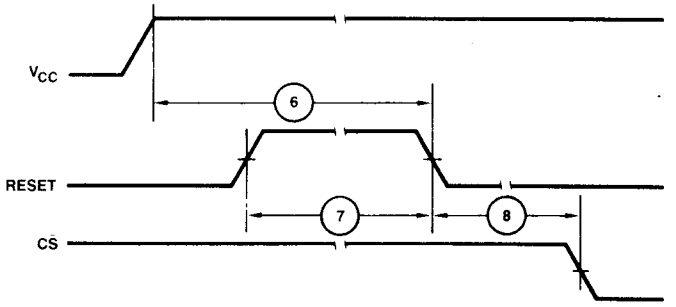
Timing Diagram 1. Clock Timing



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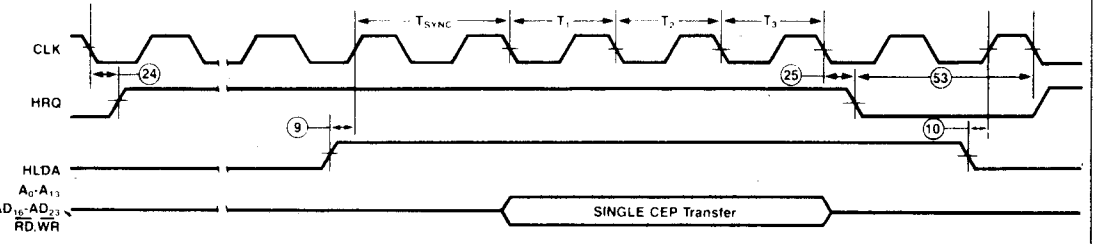
Timing Diagram 2. RESET Timing



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Timing Diagram 3. Bus Exchange Timing

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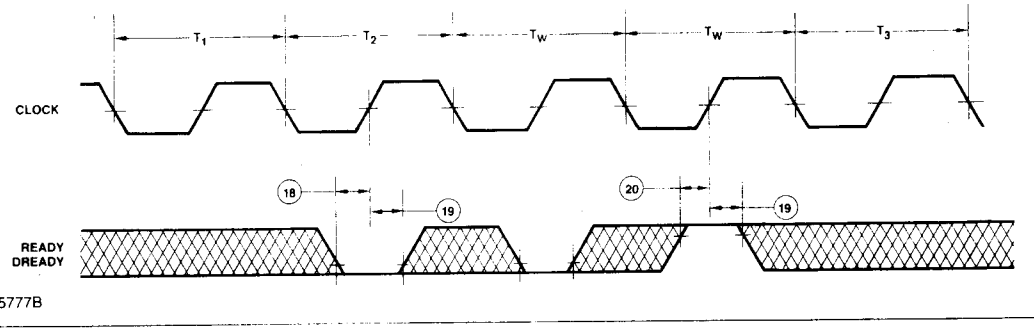
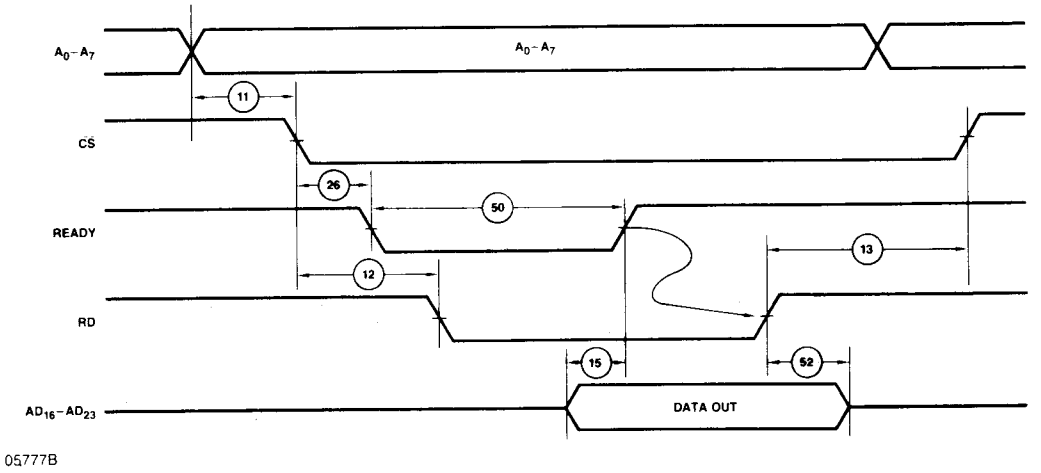
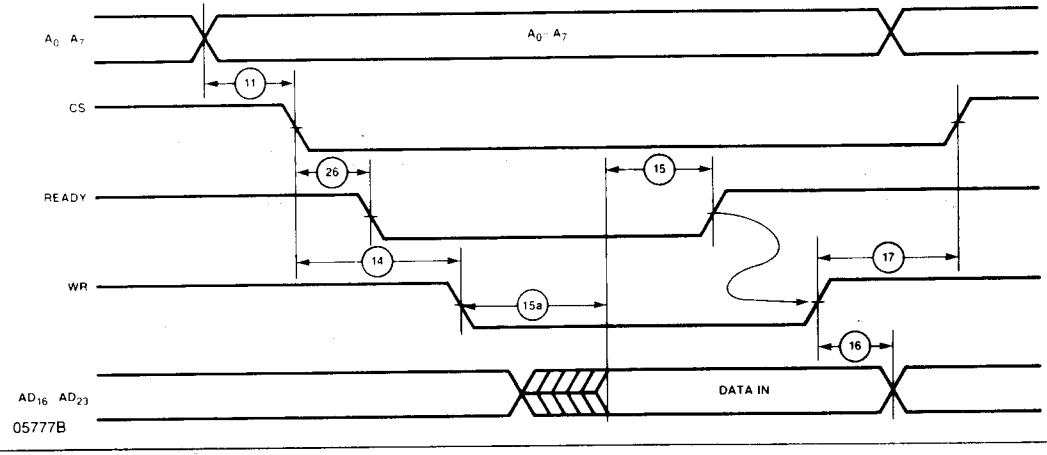


Timing Diagram 4. READY, DREADY Input Timing



Timing Diagram 5. CPU Program Read Timing



Timing Diagram 6. CPU Program Write Timing

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Refer to page 7-1 for Essential Information on Military Devices

SWITCHING CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 5V±10%)
Timing Responses

#	Parameter	Description	Test Conditions	Min	Typ	Max	Unit
24	TCLHRH	HRQ Active Delay	CL = 20–100PF for all 7970 Outputs (In addition to 7970 selfload)			80.0	ns
25	TCLHRL	HRQ Inactive Delay				85.0	ns
26	TSLRYL	READY Active Delay				80.0	ns
27	TCLAV	Address Valid Delay		10.0		80.0	ns
28	TCLLH	ALE Active Delay				65.0	ns
29	TLHLL	ALE Width		70.0			ns
30	TAVAL	Address Valid to ALE LOW		55.0			ns
31	TCHLL	ALE Inactive Delay				65.0	ns
32	TLLAX	Address Hold Time to ALE Inactive (A16–A23)		50.0			ns
33	TCLAZ	Address Float Delay From Clock FE				50.0	ns
34	TCLAX	Address Hold Time (A0–A15)		15.0			ns
35	TAZRL	Address Float to $\overline{RD}$ Active		0.0			ns
36	TCHRL	$\overline{RD}$ Active Delay		10.0		50.0	ns
37	TRLRH	$\overline{RD}$ Width		TCLCL-40			ns
38	TCHRH	$\overline{RD}$ Inactive Delay		10.0		50.0	ns
39	TRHAV	$\overline{RD}$ Inactive to Next Address Active		TCLCL			ns
40	TCLDX	DATA Hold Time		10.0			ns
41	TCHCTV	Control Active Delay 2		10.0		110.0	ns
42	TCLDV	DATA Valid Delay From Clock FE				110.0	ns
43	TCHWL	$\overline{WR}$ Active Delay		10.0		50.0	ns
44	TWLWH	$\overline{WR}$ Width		TCLCL-40			ns
45	TCHWH	$\overline{WR}$ Inactive Delay		0.0		50.0	ns
46	TWHDX	DATA Hold Time After $\overline{WR}$		60.0			ns
47	TCHDX	DATA Hold Time		10.0			ns
48	TOLOH	Output Rise Time	From 0.8V to 2.0V			15.0	ns
49	TOHOL	Output Fall Time	From 2.0V to 0.8V			10.0	ns
50	TRYW	READY Width		2TCLCL-75			ns
51	TDVRYH	DATA Valid to READY HIGH		30.0		90.0	ns
52	TRDHDV	DATA OUT Not Valid Delay		0.0		50.0	ns
53	THRLHR	HRQ Low To HRQ High		2TCLCL			ns

Note: Switching characteristics are targetted numbers and are subject to change without notice.

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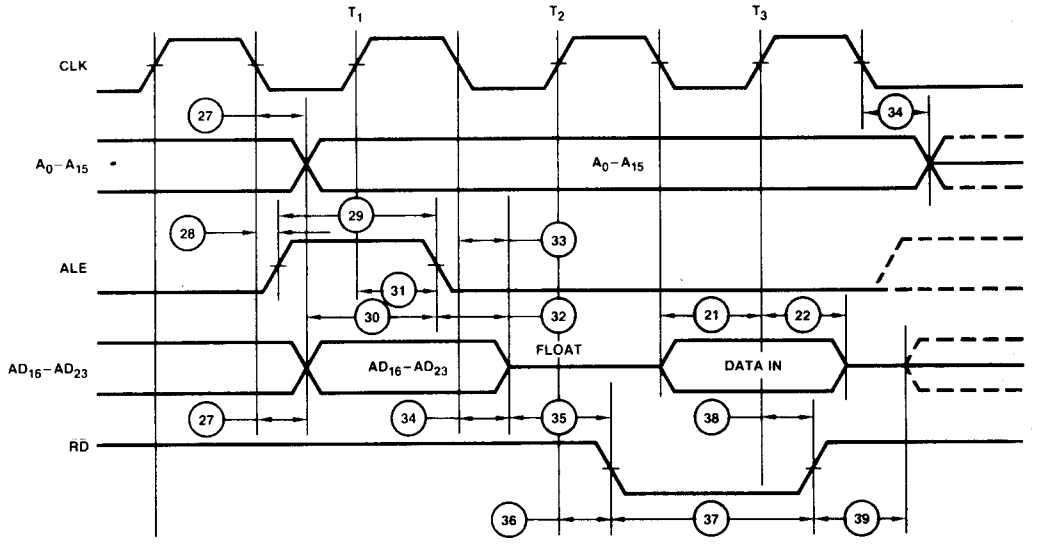
Refer to page 7-1 for Essential Information on Military Devices



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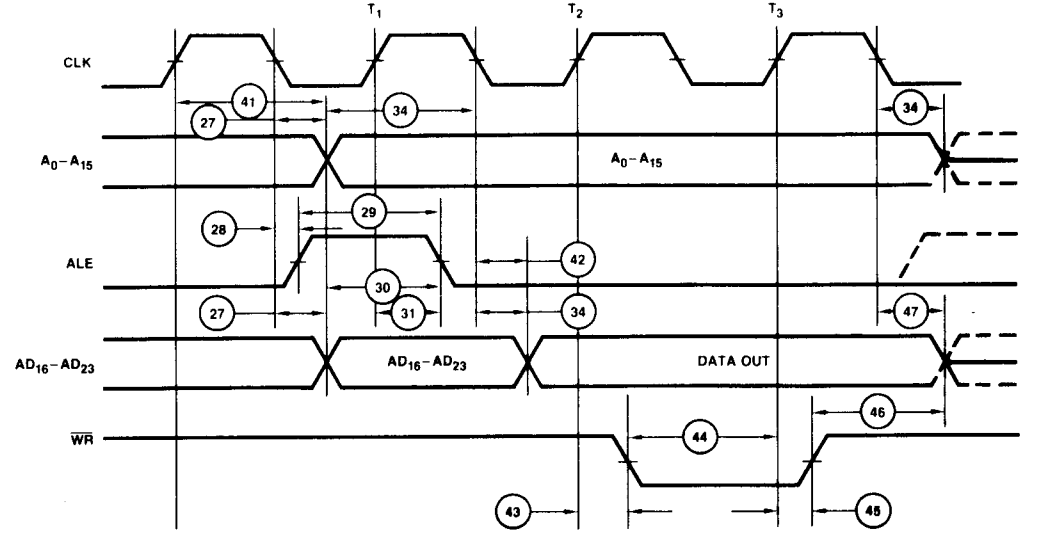
Timing Diagram 7. DMA Read Operation



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Timing Diagram 8. DMA Write Operation

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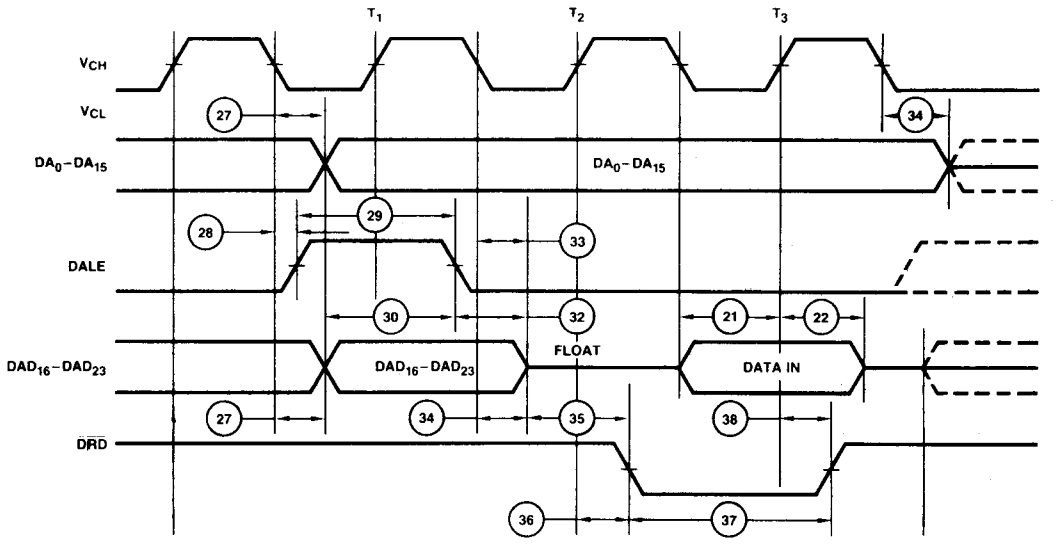

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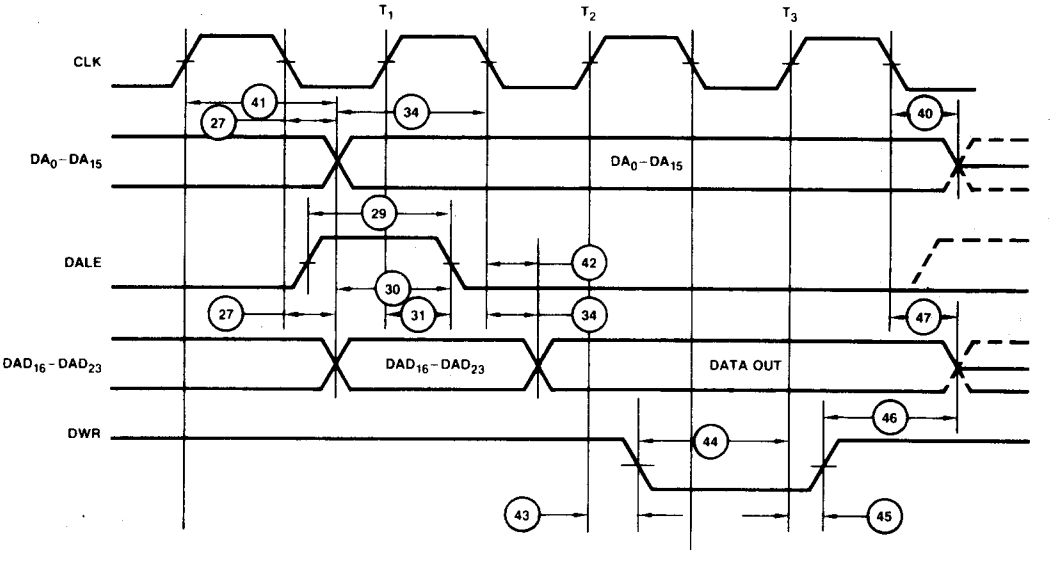
Timing Diagram 9. Document Store Bus Read Operation



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Timing Diagram 10. Document Store Bus Write Operation

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Refer to page 7-1 for Essential Information on Military Devices