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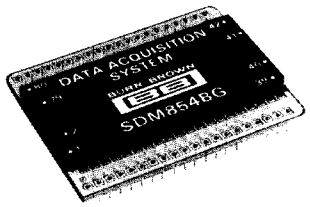


SDM854

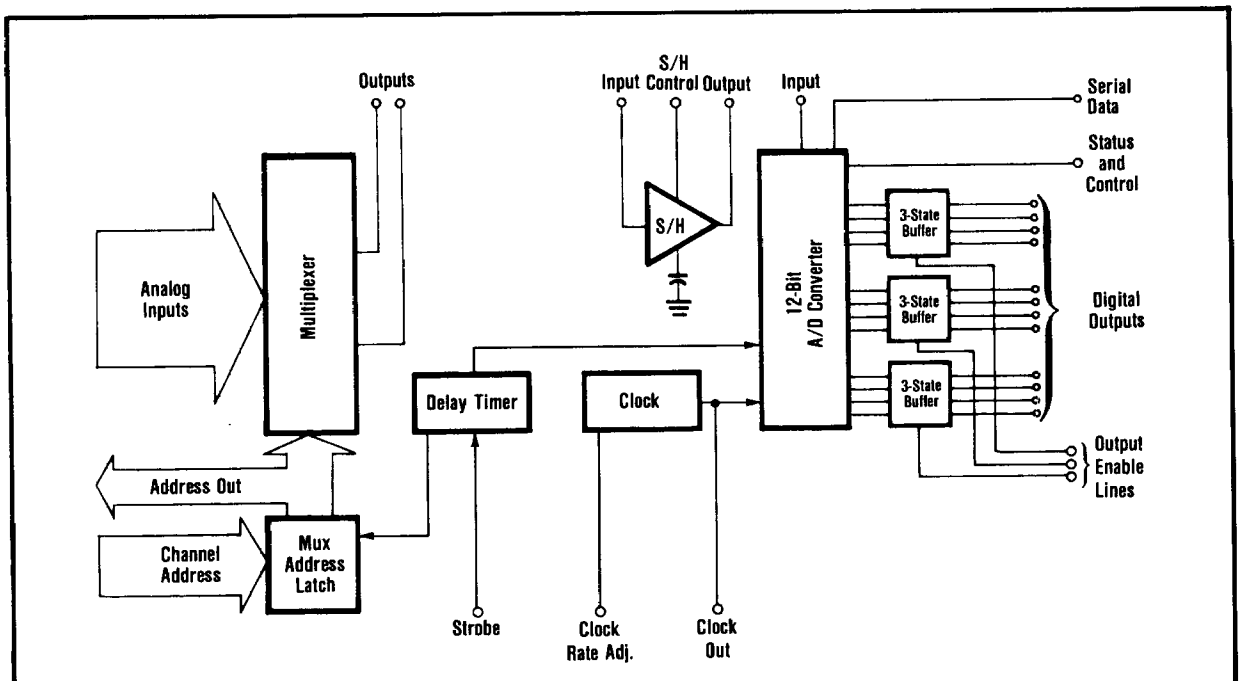
HYBRID DATA ACQUISITION SYSTEM

FEATURES

- MINIATURE SIZE
- LOW COST
- 12-BIT, ±0.012% LINEARITY ERROR
- INPUTS UP TO ±10 VOLTS
- WIDE TEMPERATURE RANGE
- SELECTABLE 16 SINGLE, 8 DIFFERENTIAL INPUTS
- THREE-STATE OUTPUT BUFFERS

DESCRIPTION

The SDM854 is a complete data acquisition system contained in a miniature 2.2" x 1.7" x 0.22" (55.9mm x 43.2mm x 5.6mm) ceramic package. This system offers all the functions available in large modular data acquisition systems. Inputs up to ±10V can be accepted and low-level inputs can be accommodated by connecting an external instrumentation amplifier to the output of the multiplexer and to the input of the sample/hold amplifier. Digital resolution is 12 bits with accuracy of ±0.024% at a throughput rate of 27kHz.



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SYSTEM DESCRIPTION

The SDM854 contains all components necessary to multiplex and convert analog signals up to ±10V into equivalent digital outputs. Throughput sampling rates are from 27kHz (12-bit resolution) to 70kHz (8-bit resolution) in the overlap mode of operation. The SDM854 can be configured to accept either 8-channel differential or 16-channel single-ended signals and can be expanded almost without limit with external multiplexers. Three-state outputs are provided for easy interface to microprocessor and other bus-structure systems. The system components are illustrated in Figure 1 and described in the following paragraphs.

ANALOG MULTIPLEXER

The analog multiplexer consists of two CMOS integrated circuits. Pin interconnects are used to select 16-channel single-ended or 8-channel differential operation. In single-ended operation the multiplexer can be used in a pseudo-differential mode by connecting an external amplifier's inverting input to common remote signal ground. Channel selection is made by an internally latched 3- or 4-bit binary word, for differential or single-ended operation respectively.

SAMPLE/HOLD

A complete stand-alone circuit, the sample/hold amplifier features buffered output, 10μsec acquisition time, and 100nsec aperture time.

Input, output, and mode control lines are brought out to separate pins. This allows maximum system flexibility for performing functions, such as automatic gain ranging, with no loss of aperture time.

ANALOG-TO-DIGITAL CONVERTER

The ADC is a 12-bit, 25μsec converter with 0.01% linearity error. Its features include positive and negative reference voltage outputs, external gain and offset adjustments, straight binary or two's complement output, serial data and clock outputs, status output, a short cycle feature, and a clock rate control for higher throughput rates at lower resolution or accuracy.

THREE-STATE OUTPUT BUFFERS

Digital outputs of the ADC are internally buffered by LSTTL three-state buffers. Three separate enable lines are brought out for easy interfacing to 4-, 8- or 16-bit data buses. $\overline{\text{MSB}}$ and BUSY are also buffered by separate three-state devices, each with its own enable line.

ADDRESS LATCH

Outputs of the 4-bit LSTTL register latch are connected to the address inputs of the multiplexer. This latch serves as an address storage register for the selected analog input. It may be loaded through 4 address inputs. Other inputs are LOAD and CLEAR. The 3 least significant bits are used for 8-channel differential mode addressing.

DELAY TIMER

A delay timer allows settling time for the multiplexer and sample/hold circuits before conversion begins. The delay is adjustable over a wide range by use of an external resistor or capacitor. This allows for longer settling time if an external instrumentation amplifier is used and is operating at high gains, or shorter settling time for lower resolution operation.

CHANNEL EXPANSION

The number of analog input channels of the SDM854 can be easily increased by using Burr-Brown's MPC8D (8-channel differential) and MPC16S (16-channel single-ended) multiplexers. These are latch-free devices which contain internal binary decoding at TTL or MOS levels and may be integrated into a system with minimal external logic.

SYSTEM PERFORMANCE

The SDM854 is configured for random channel selection. With the addition of an external counter they can be

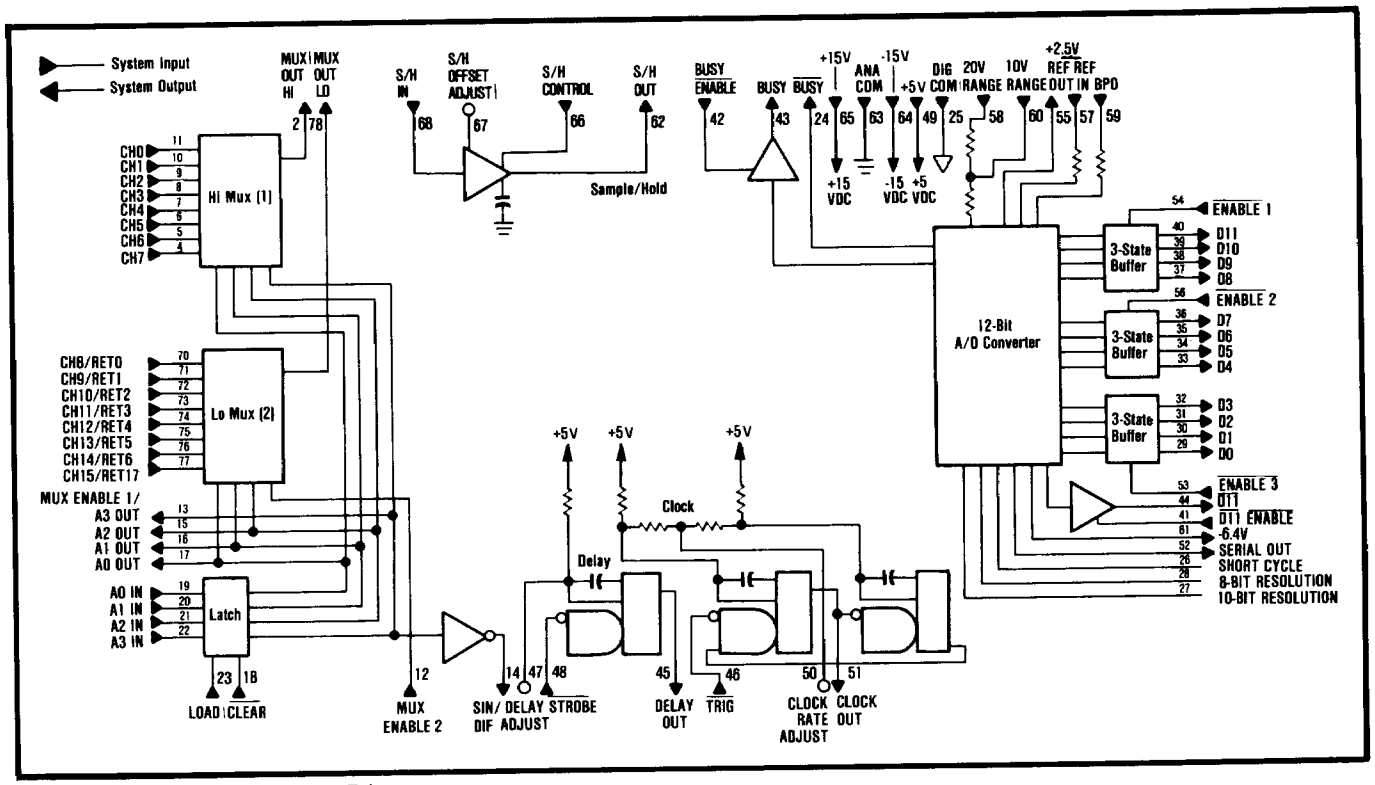


FIGURE 1. SDM854 Block Diagram.

configured to continuously sequence through all analog channels or sequence through all analog channels on command from an external trigger.

With the appropriate 4-bit (single-ended) or 3-bit (differential) channel address on the latch inputs, and DELAY OUT (pin 45) tied to the LOAD input (pin 23), a negative going edge is applied to the $\overline{\text{STROBE}}$ input (pin 48). This starts the delay timer, latches the multiplexer address, and allows the input signal to pass through the multiplexer, and sample/hold before starting the A/D conversion. The DELAY OUT signal (pin 45) is also connected to the $\overline{\text{TRIG}}$ input (pin 46) and the A/D conversion is initiated on the negative-going edge. The S/H CONTROL input (pin 66) is connected to $\overline{\text{BUSY}}$ (pin 24) so that the sample/hold is in the HOLD mode during the A/D conversion.

By using overlap programming the settling time effects of the analog multiplexer and external instrumentation amplifier (if used) can be reduced, extending throughput sampling rates up to 27kHz for 12-bit and 70kHz for 8-bit resolution (ADC short-cycled). This mode of operation is most useful when converting low-level inputs to accommodate the increased settling time of the external instrumentation amplifier. Overlap programming is accomplished by connecting $\overline{\text{BUSY}}$ to $\overline{\text{STROBE}}$ and S/H CONTROL; DELAY OUT to LOAD and $\overline{\text{TRIG}}$. In this mode of operation the address of the next channel to be converted is latched and the output of the external instrumentation amplifier allowed to settle to a new value during the present conversion.

DIGITAL INPUT SPECIFICATIONS

Address Inputs (A0 - A3)	One standard LSTTL load, positive true
Address Coding	4-bit binary
LOAD	One standard LSTTL load, positive true, address loaded on positive edge.
$\overline{\text{CLEAR}}$	One standard LSTTL load, negative true, low level clears address latch.
$\overline{\text{STROBE}}$	One standard TTL load, high-to-low transition triggers the delay timer.
$\overline{\text{TRIG}}$	One standard TTL load, a negative going edge initiates the A/D conversion.
SHORT CYCLE	One standard LSTTL load, logic 1 for 12-bit resolution. Connect to "8-bit" or "10-bit" for 8- or 10-bit resolution.
$\overline{\text{ENABLE 1}}$, $\overline{\text{ENABLE 2}}$, $\overline{\text{ENABLE 3}}$, $\overline{\text{D11 ENABLE}}$, $\overline{\text{BUSY ENABLE}}$	One standard LSTTL load, a low level enables the 3-state output.
S/H CONTROL	TTL compatible, 10μA maximum input current. Logic 0 = Hold mode, Logic 1 = Sample (track) mode.
MUX ENABLE 2	TTL compatible, 2μA input current, logic 0 enables multiplexer 2 (channels 8-15).

DIGITAL OUTPUT SPECIFICATIONS

Parallel Data Outputs	5 standard TTL loads, positive true 3-state.
Serial Output	2 standard TTL loads, positive true, NRZ, time serial data output beginning with D11 (see Timing Diagram).
$\overline{\text{D11}}$	5 standard TTL loads, positive true, 3-state.
$\overline{\text{BUSY}}$	5 standard TTL loads, low during A/D conversion.
BUSY	5 standard TTL loads, high during A/D conversion, 3-state
CLOCK OUT	5 standard TTL loads, for synchronizing serial out data (see Timing Diagram).
Address Outputs (A0 - A3)	5 LSTTL or 2 standard TTL loads, positive true
DELAY OUT	5 standard TTL loads, high during delay period, triggered by Strobe input.
SIN DIF	5 LSTTL or 2 standard TTL loads, high while addressing channels 0-7, low while addressing channels 8-15.

SPECIFICATIONS

ELECTRICAL

Typical at T_A = +25°C and rated power supplies unless otherwise noted.

PARAMETER	MIN	TYP	MAX	UNITS
TRANSFER CHARACTERISTICS				
Resolution	12			Bits
Number of Analog Channels		16SIN/8DIF		
Throughput Rate (Normal mode)				
SDM854AG	33	35		kHz
SDM854BG	25	27		kHz
Throughput Rate (Overlap mode)				
SDM854AG	38	40		kHz
SDM854BG	27	29		kHz
ANALOG INPUTS				
ADC Input Voltage Ranges		0 to +10, ±5, ±10		V
Mux Input Voltage Range				
Absolute max without damage			±35	V
For linear operation			±15	V
Mux Input Impedance, OFF Channel			10^{11}	Ω
Mux Input Impedance, ON Channel		1.5	1.8	kΩ
Input Leakage, OFF Channel		0.02		nA
Output Leakage, All Channels Disabled		0.2		nA
Output Leakage with Input Overvoltage of				
+35V		1		nA
-35V		1		μA
TEMPERATURE STABILITY				
System Accuracy				
Unipolar		±15	±25	ppm/°C
Bipolar		±10	±20	ppm/°C
Linearity Drift			±2	ppm/°C of FSR
REFERENCE VOLTAGES				
Positive Output	+2.490	+2.500	+2.510	V
Positive Output Drift		±5	±10	ppm/°C
Negative Output	-6.0	-6.4	-6.8	V
Negative Output Drift		±15	±10	ppm/°C
ACCURACY				
Throughput Accuracy				
0 to +10V, ±5V, ±10V, AG			±0.048	% of FSR(1)
0 to +10V, ±5V, ±10V, BG			±0.024	% of FSR
Linearity				
AG			±0.024	% of FSR
BG			±0.012	% of FSR
Differential Linearity				
AG		±0.024	±0.048	% of FSR
BG		±0.012	±0.024	% of FSR
Quantizing Error			±0.012	% of FSR
System Gain Error(2)		±0.1	±0.3	%
System Offset Error(2)		±0.1	±0.3	% of FSR
Power Supply Sensitivity +15V		±0.0007		%/%ΔV
Power Supply Sensitivity -15V		±0.0007		%/%ΔV
Power Supply Sensitivity +5V		±0.001		%/%ΔV
DYNAMIC ACCURACY				
Sample/Hold Characteristics				
Aperture Time		100		nsec
Acquisition Time		10		μsec
Feedthrough (10V step)		±1.4		mV
OUTPUTS				
Digital Output Coding		Binary, Offset Binary, Two's Complement		
Serial Output Coding		Nonreturn to zero (NRZ)		
ADC Conversion Time(3)		25	30	μsec
Clock Frequency(3)		520		kHz
Delay(4)		15		μsec

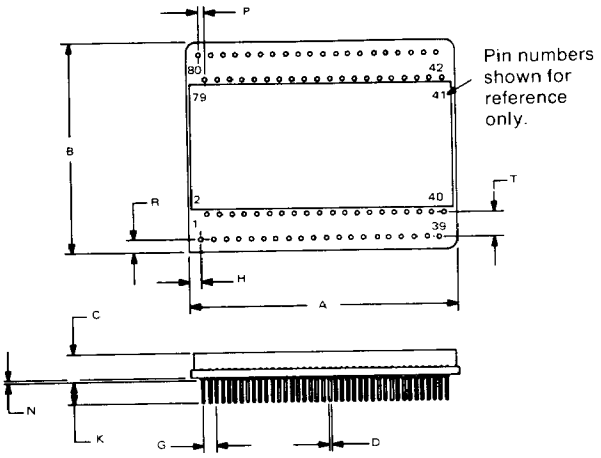
PARAMETER	MIN	TYP	MAX	UNITS
POWER REQUIREMENTS				
Rated Voltage for Specified Accuracy	±14.5	±15	±15.5	V
	+4.75	+5	+5.25	V
Quiescent Current				
+15VDC		+10	+20	mA
-15VDC		-35	-50	mA
+5VDC		+170	+220	mA
Power Dissipation		1300	1750	mW
ENVIRONMENTAL				
Specification Temperature Range	-25		+85	°C
Operating Temperature Range	-40		+85	°C
Storage Temperature Range	-55		+125	°C

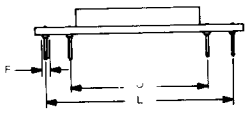
NOTES:
1. FSR means Full Scale Range (FSR is 20V for ±10V range).
2. Adjustable to zero.
3. Conversion time and clock frequency can be externally adjusted from 13μsec (f_{clock} = 1.0MHz) to 110μsec (f_{clock} = 118kHz). (Conv. times are for 12-bit resolution.) (See Figure 9.)
4. Can be externally adjusted from 3μsec to 300μsec.

PIN DESIGNATIONS

NC	1	80	NC
MUX OUT HI	2	79	NC
NC	3	78	MUX OUT LO
CH7	4	77	CH15/RET7
CH6	5	76	CH14/RET6
CH5	6	75	CH13/RET5
CH4	7	74	CH12/RET4
CH3	8	73	CH11/RET3
CH2	9	72	CH10/RET2
CH1	10	71	CH9/RET1
CH0	11	70	CH8/RET0
MUX ENABLE 2	12	69	NC
MUX ENABLE 1/A3 OUT	13	68	S/H IN
SIN/DIF	14	67	S/H OFFSET ADJUST
A2 OUT	15	66	S/H CONTROL
A1 OUT	16	65	+15VDC
A0 OUT	17	64	-15VDC
$\overline{\text{CLEAR}}$	18	63	ANA COM
A0 IN	19	62	S/H OUT
A1 IN	20	61	-6.4V REF OUT
A2 IN	21	60	10V RANGE
A3 IN	22	59	BIPOLAR OFFSET
$\overline{\text{LOAD}}$	23	58	20V RANGE
$\overline{\text{BUSY}}$	24	57	+2.5V REF IN
DIG COM	25	56	$\overline{\text{ENABLE 2}}$
SHORT CYCLE	26	55	+2.5V REF OUT
10-BIT RESOLUTION	27	54	$\overline{\text{ENABLE 1}}$
8-BIT RESOLUTION	28	53	$\overline{\text{ENABLE 3}}$
D0 · LSB	29	52	SERIAL OUT
D1	30	51	CLOCK OUT
D2	31	50	CLOCK RATE ADJUST
D3	32	49	+5VDC
D4	33	48	$\overline{\text{STROBE}}$
D5	34	47	DELAY ADJUST
D6	35	46	$\overline{\text{TRIG}}$
D7	36	45	DELAY OUT
D8	37	44	$\overline{\text{D11}}$
D9	38	43	BUSY
D10	39	42	BUSY $\overline{\text{ENABLE}}$
D11 · MSB ·	40	41	$\overline{\text{D11}}$ $\overline{\text{ENABLE}}$

MECHANICAL





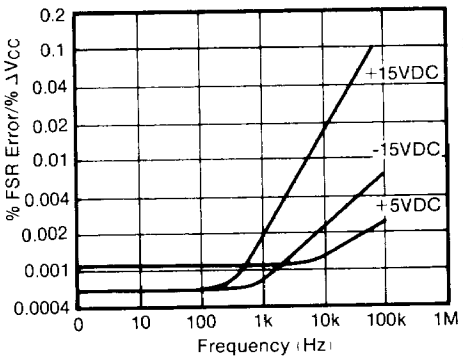
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	2.120	2.180	53.85	55.37
B	1.670	1.720	42.42	43.69
C	.170	.230	4.32	5.84
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.100 BASIC		2.54 BASIC	
K	.150	.250	3.81	6.35
L	1.500 BASIC		38.1 BASIC	
N	.002	.010	0.05	0.25
P	.050 BASIC		1.27 BASIC	
R	.100 BASIC		2.54 BASIC	
T	.200 BASIC		5.08 BASIC	
U	1.100 BASIC		27.94 BASIC	

NOTE:
Leads in true position within 0.015" (0.38mm) R at MMC at seating plane.

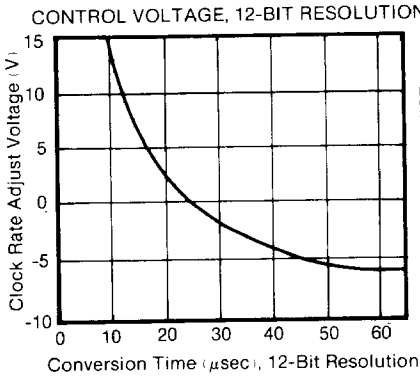
MATERIAL: Ceramic
WEIGHT: 32 grams (1.2 oz)
MATING CONNECTOR:
2350MC (set of four 20-pin strips) or
0422MC (assembled unit)

TYPICAL PERFORMANCE CURVES

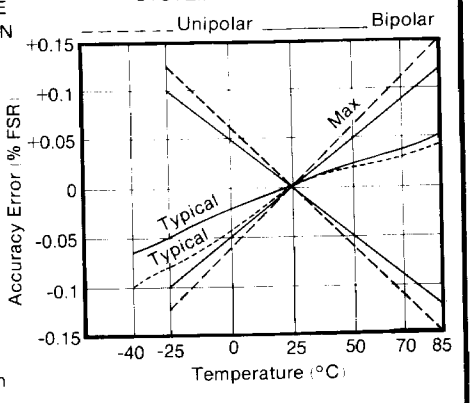
POWER SUPPLY REJECTION VS POWER SUPPLY RIPPLE FREQUENCY



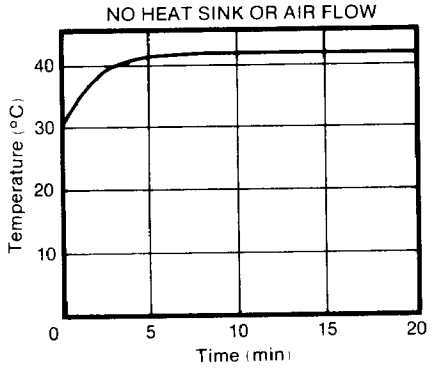
A/D CONVERSION TIME VS CLOCK RATE CONTROL VOLTAGE, 12-BIT RESOLUTION



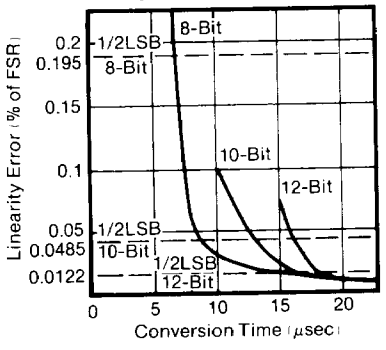
SYSTEM ACCURACY DRIFT



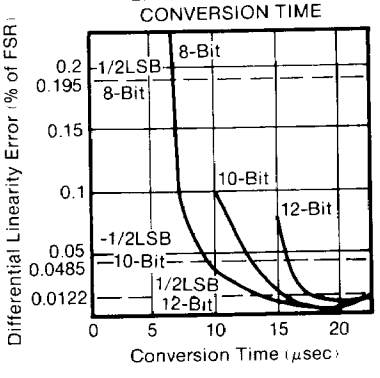
CASE TEMPERATURE VS TIME WITH NO HEAT SINK OR AIR FLOW



A/D CONVERTER LINEARITY ERROR VS CONVERSION TIME



A/D CONVERTER DIFFERENTIAL LINEARITY ERROR VS CONVERSION TIME



DESCRIPTION OF PIN FUNCTIONS

NUMBER	DESIGNATION	DESCRIPTION
Pin 1	NC	No connection.
Pin 2	MUX OUT HI	High output of the analog input multiplexer. Connect to pin 78 (MUX OUT LO) and pin 68 (S H IN) for single-ended input operation.
Pin 3	NC	No connection.
Pins 4 thru 11	CH7-CH0	The first 8 (of 16) analog inputs for single-ended operation or for 8-channel differential input operation.
Pin 12	MUX ENABLE 2	Connect to pin 14 (SIN DIF) for single-ended input operation. Connect to pin 13 (MUX ENABLE 1) for differential input operation.
Pin 13	MUX ENABLE 1 A3 OUT	Leave open for single-ended input operation. Connect to pin 12 (MUX ENABLE 2) for differential input operation. Also, A3 output line.
Pin 14	SIN DIF	Single Differential input operation. Connect to pin 12 (MUX ENABLE 2) for single-ended operation. Leave open for differential input operation.
Pins 15, 16, 17	A0 OUT - A2 OUT	Output lines from input channel address latch (A3 OUT is on pin 13).
Pin 18	$\overline{\text{CLEAR}}$	A low on this line clears the address latch causing the SDM854 to address channel 0 regardless of the information present on AO IN - A3 IN. Connect to +5VDC or to user logic circuitry.
Pins 19, 20, 21, 22	AO IN - A3 IN	Address lines that select one of 16 analog input signals (CH0-CH15). 0000 selects channel 0 and 1111 selects channel 15. Connect A3 to ground for 8-channel differential operation. The address is latched with a positive TTL edge on the LOAD (pin 23).
Pin 23	LOAD	A positive TTL edge on this pin latches the input channel address present on AO IN - A3 IN (pins 19, 20, 21, 22).
Pin 24	$\overline{\text{BUSY}}$	This signal will be low during the A D conversion (≈25μsec). Output data is not valid while this signal is low. Connect to S H CONTROL (pin 66).
Pin 25	DIG COM	Digital common. Connect to ANA COM (pin 63) as close to the SDM854 as possible.
Pin 26	SHORT CYCLE	This pin allows short cycling the A D converter for lower resolutions thereby obtaining faster conversion times. Connect to +5VDC (pin 49) for 12-bit resolution, (pin 27) for 10-bit resolution, or (pin 28) for 8-bit resolution.
Pin 27	10-BIT RESOLUTION	To short cycle to 10-bit resolution connect to pin 26. Otherwise, make no connection.
Pin 28	8-BIT RESOLUTION	To short cycle to 8-bit resolution, connect to pin 26. Otherwise, make no connection.
Pins 29 thru 40	D0-D11	12-bit data bus, 3-state low power Schottky TTL-compatible.
Pin 41	$\overline{\text{D11 ENABLE}}$	$\overline{\text{D11}}$ (pin 44) is enabled when $\overline{\text{D11 ENABLE}}$ is low.
Pin 42	BUSY $\overline{\text{ENABLE}}$	BUSY (pin 43) is enabled when BUSY $\overline{\text{ENABLE}}$ is low.
Pin 43	BUSY	3-state output that will be high only while an A D conversion is in process. Output data is not valid while this signal is high.
Pin 44	$\overline{\text{D11}}$	$\overline{\text{MSB}}$. Use instead of D11 when two's complement output is required.
Pin 45	DELAY OUT	This pulse is used to delay the beginning of the A D conversion to allow for the settling of the multiplexer and sample hold.
Pin 46	$\overline{\text{TRIG}}$	A negative TTL edge on this pin initiates the A D conversion. Connect to DELAY OUT (pin 45).
Pin 47	DELAY ADJUST	When the SDM854 is addressed, an internal delay of approximately 15μsec is initiated to allow for multiplexer and sample hold settling time. The delay can be shortened for faster lower-resolution operation.
Pin 48	$\overline{\text{STROBE}}$	A negative TTL edge on this pin initiates the DELAY OUT pulse.
Pin 49	+5VDC	+5VDC at 200mA maximum, 170mA typical.
Pin 50	CLOCK RATE ADJUST	Varying the voltage at this pin changes the clock frequency and thereby changes the conversion speed of the A D converter. Connect to DIG COM (pin 25) for 12-bit operation (25μsec A D conversion time). Connect to +5VDC for 10-bit operation and connect to +15VDC for 8-bit operation (see page 11).
Pin 51	CLOCK OUT	A D converter clock output. Output is present only during A D conversion. N + 1 TTL pulses are output at a 520kHz rate where N is the resolution.
Pin 52	SERIAL OUT	Serial output data in NRZ format is synchronous with CLOCK OUT (pin 51) signal. Use negative edge of CLOCK OUT to strobe each bit.
Pins 53, 54, 56	$\overline{\text{ENABLE 3}}$ $\overline{\text{ENABLE 1}}$ $\overline{\text{ENABLE 2}}$	3-state enable lines for data bus D11 - D0 (MSB = D11). $\overline{\text{ENABLE 1}}$ (pin 54) enables D11 - D8; $\overline{\text{ENABLE 2}}$ (pin 56) enables D7 - D4; $\overline{\text{ENABLE 3}}$ (pin 53) enables D3 - D0. A low on the enable line enables data outputs.
Pin 55	+2.5V REF OUT	Positive voltage reference output. Connect to REF IN (pin 57) (through 50Ω) for unipolar or bipolar operation (unless an external reference is used). Also connect to BPO (pin 59) (through 25Ω) for bipolar operation.
Pin 57	+2.5V REF IN	Reference voltage input. Connect to +2.5V REF OUT (pin 55) (through 50Ω resistor or 100Ω pot) or use external +2.5V reference (+2.5V ±10mV at 0.5mA required).
Pin 58	20V RANGE	**A/D converter input resistor. Leave open unless an external IA with a gain greater than 2 is used. (Input multiplexers are limited to ±10V maximum input voltage.)**
Pin 59	BIPOLAR OFFSET	A D converter bipolar offset. Connect to REF OUT (pin 55) through a 25Ω resistor or a 50Ω pot for bipolar operation. Leave open for unipolar operation.
Pin 60	10V RANGE	A D converter input resistor. Using without IA: connect to S H OUT (pin 62) for ±5V max input operation.
Pin 61	-6.4V REF OUT	Negative voltage reference output. Maximum current drain from this point without degradation of specifications is 200μA.
Pin 62	S H OUT	Sample hold output. Connect to 10V RANGE (pin 60) or 20V RANGE (pin 58) for normal operations.

DESCRIPTION OF PIN FUNCTIONS [CONT]

NUMBER	DESIGNATION	DESCRIPTION
Pin 63	ANA COM	Analog common. Connect to DIG COM (pin 25) as close to the SDM854 as possible.
Pin 64	-15VDC	-15VDC at 30mA typical.
Pin 65	+15VDC	+15VDC at 30mA typical.
Pin 66	S/H CONTROL	A low signal on this line causes the sample/hold to enter the hold mode. Connect to $\overline{\text{BUSY}}$ (pin 24).
Pin 67	S/H OFFSET ADJUST	Offset adjust for sample/hold (see Figure 8).
Pin 68	S/H IN	Input to sample/hold amplifier. Connect to MUX OUT HI (pin 2) and MUX OUT LO (pin 78).
Pin 69	NC	No connection.
Pins 70 thru 77	CH8-CH15 RET0 - RET7	Analog inputs 8 through 15 for single-ended operation or analog returns 0 through 7 for differential input operation.
Pin 78	MUX OUT LO	Multiplexer output for CH8-CH15 (single-ended) or RET0-RET7 (differential). Connect to MUX OUT HI (pin 2) and S/H IN (pin 68) for single-ended operation.
Pin 79	NC	No connection.
Pin 80	NC	No connection.

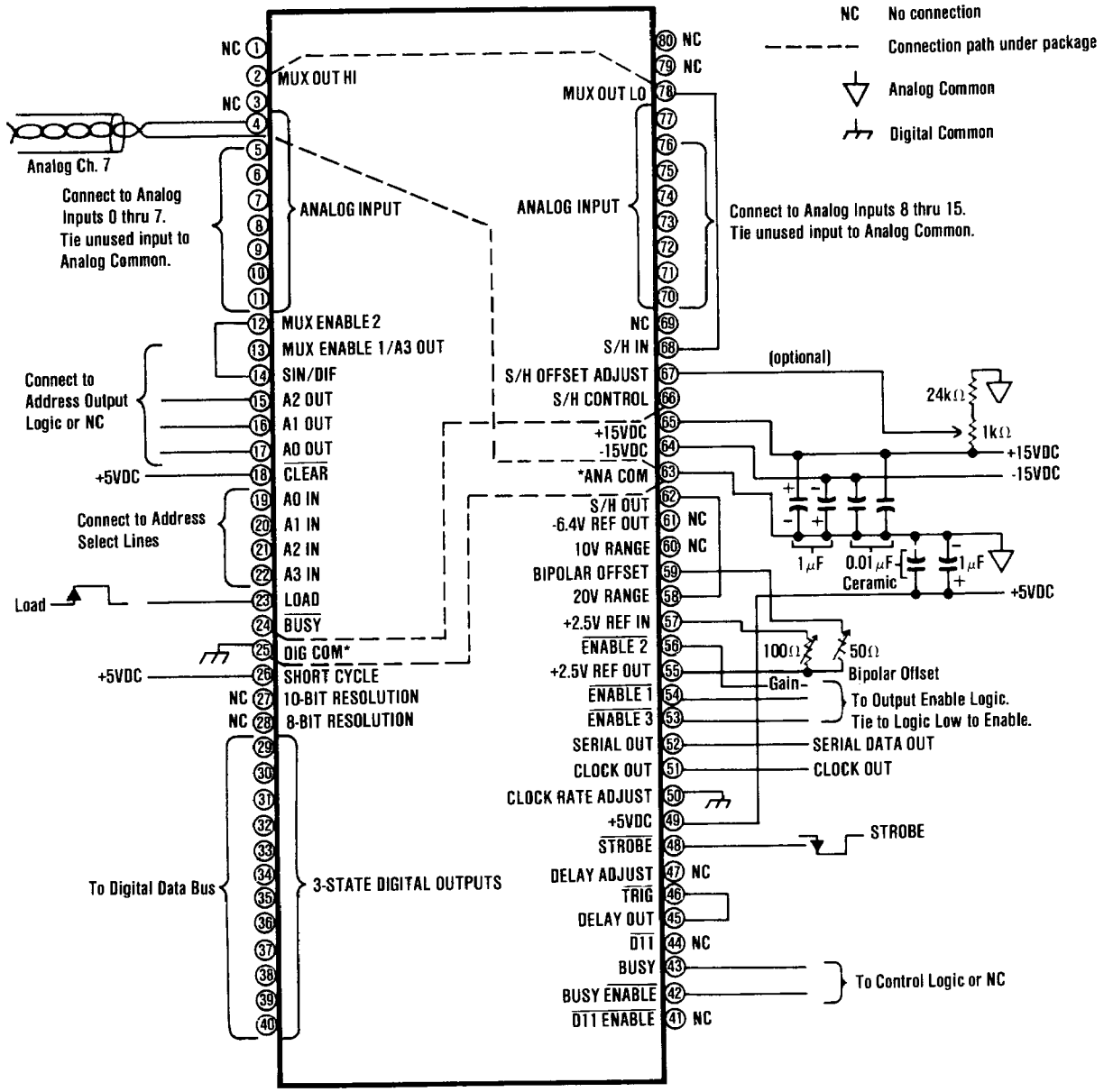


FIGURE 2. Connection Diagram for SDM854 Operating Under These Conditions:
Analog Input: Bipolar, single-ended; Reference Voltage: Internal; Resolution: 12-bits; Mode: Normal; Digital Output: Binary.

SETUP PROCEDURE

INPUT CONNECTIONS

Unused analog inputs must be connected to ANA COM, pin 63. When long leads are connected to the inputs, care must be taken that leads do not pick up excessive noise from external equipment and wiring. When low-level applications are undertaken, it is usually advisable to operate the system as an 8-channel, differential input system. This will require an external differential amplifier to be wired in between the output of the multiplexer and the sample/hold amplifier. In this way any noise will be common to both input wires, and will be rejected by the instrumentation amplifier. For best noise rejection use twisted shielded pair cable. The inputs of the SDM854 are protected from damage by voltage as high as ±35 volts and from short spikes well in excess of this for a few microseconds; however, careful wiring and cable routing practices are recommended.

Single-Ended Inputs

For single-ended inputs connect pin 2 and pin 78 (MUX OUT HI and MUX OUT LO) to pin 68 (SAMPLE/HOLD amplifier input), all unused inputs to the multiplexer and all signal returns to pin 63 (ANA COM).

Differential Inputs With External Instrumentation Amplifier

Connect the signal inputs to pins 4 through 11, and their returns to 77 through 70. Connect pin 12 to 13. Connect pins 2 and 78 to the noninverting and inverting input of the amplifier respectively. The output of the amplifier is connected to pin 68.

SAMPLE/HOLD

Connect S/H CONTROL, pin 66, to the ADC $\overline{\text{BUSY}}$ output, pin 24.

ANALOG-TO-DIGITAL CONVERTER INPUT VOLTAGE RANGE

The analog-to-digital converter is essentially a current input device having a current input range of 0 to 2mA The input may be considered a virtual ground summing point. To convert voltage to current, a center tapped 10kΩ resistor is internally connected to this summing point. This is illustrated in Figure 3.

The interconnection of the ADC pins and the S/H OUT, pin 62, are shown in Table I.

TABLE I. ADC Range Jumpers.

Input Range (V)	Jumper
0 to +10	59 Open, 60 to 62, 58 Open
-5 to +5	59 to 55, 60 to 62, 58 Open
-10 to +10	59 to 55, 58 to 62, 60 Open

NOTE: Input ranges in Table I apply to ADC only.

OUTPUT CODE

For unipolar binary and offset binary use D11 (pin 40) for the most significant bit. Two's complement binary is obtained by using pin 44, $\overline{\text{D11}}$, as the most significant bit. One's complement code may be obtained by a different offset adjustment in the calibration procedure. Two's complement and one's complement codes are usually used only for bipolar signal ranges. For 12-bit resolution, SHORT CYCLE (pin 26) is left open or taken to +5VDC. Connect pin 26 to pin 27 (10-bit) or pin 28 (8-bit) to obtain lower resolution. The conversion time will be shortened by the following formula:

(Conversion Time) = (25μsec) x [1 - (12-R/13)]
where R is the resolution desired.

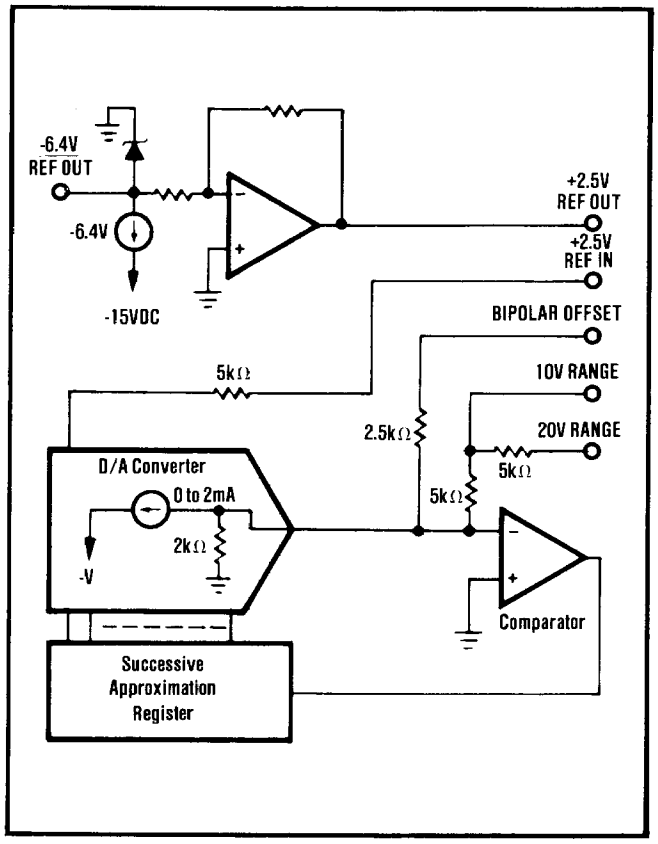


FIGURE 3. Analog-to-Digital Converter.

NORMAL AND OVERLAP MODE

The two basic modes of system operation are normal and overlap. In normal operation the channel address, N, is loaded or clocked into the address latch. The addressed channel will remain selected during its analog-to-digital conversion. In overlap mode channel N + 1 is selected while channel N is being converted. This can be used to increase the system throughput rate by allowing the multiplexer and external instrumentation amplifier to settle while a conversion is being made. In this way the throughput rate is limited by the sample/hold acquisition time and the analog-to-digital converter conversion time. For this reason, the overlap mode is more desirable for low-level signals. Table II and Figures 4 and 5 provide additional timing details. At high signal levels a high source resistance may increase the multiplexer settling time to an extent which makes the overlap mode desirable.

Normal Mode Connections

Connect DELAY OUT, pin 45 to $\overline{\text{TRIG}}$, pin 46.

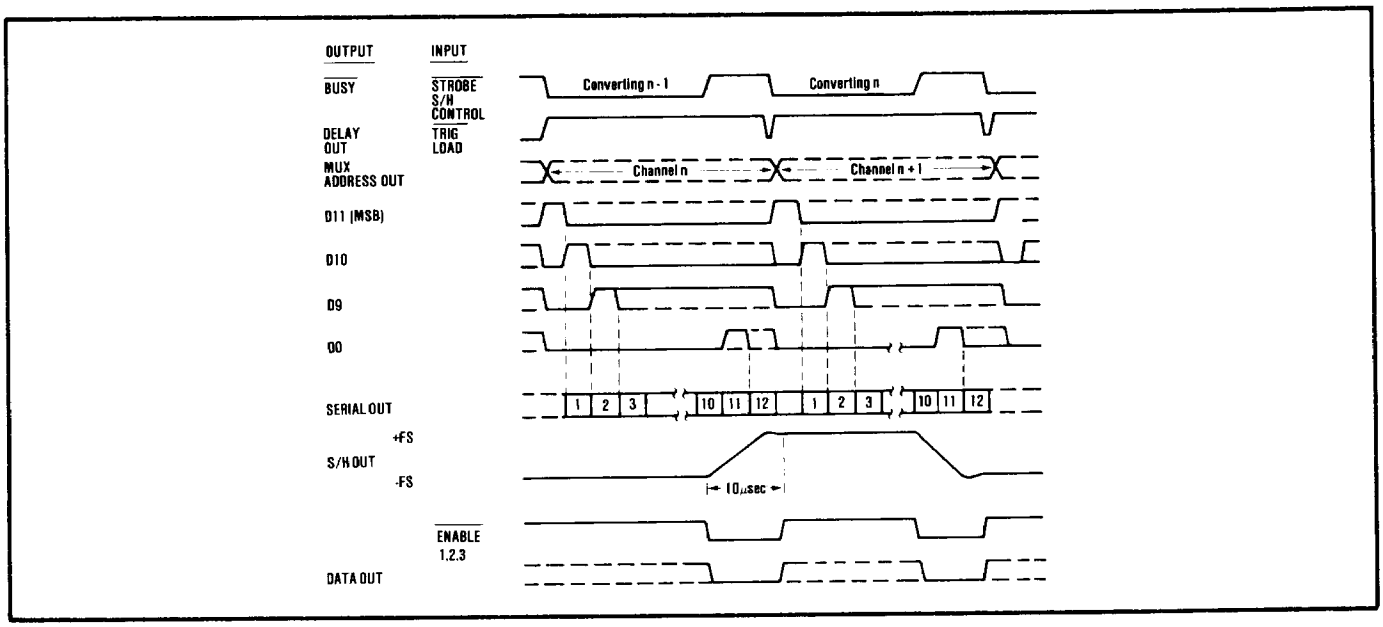


FIGURE 4. System Timing for Overlap Operation.

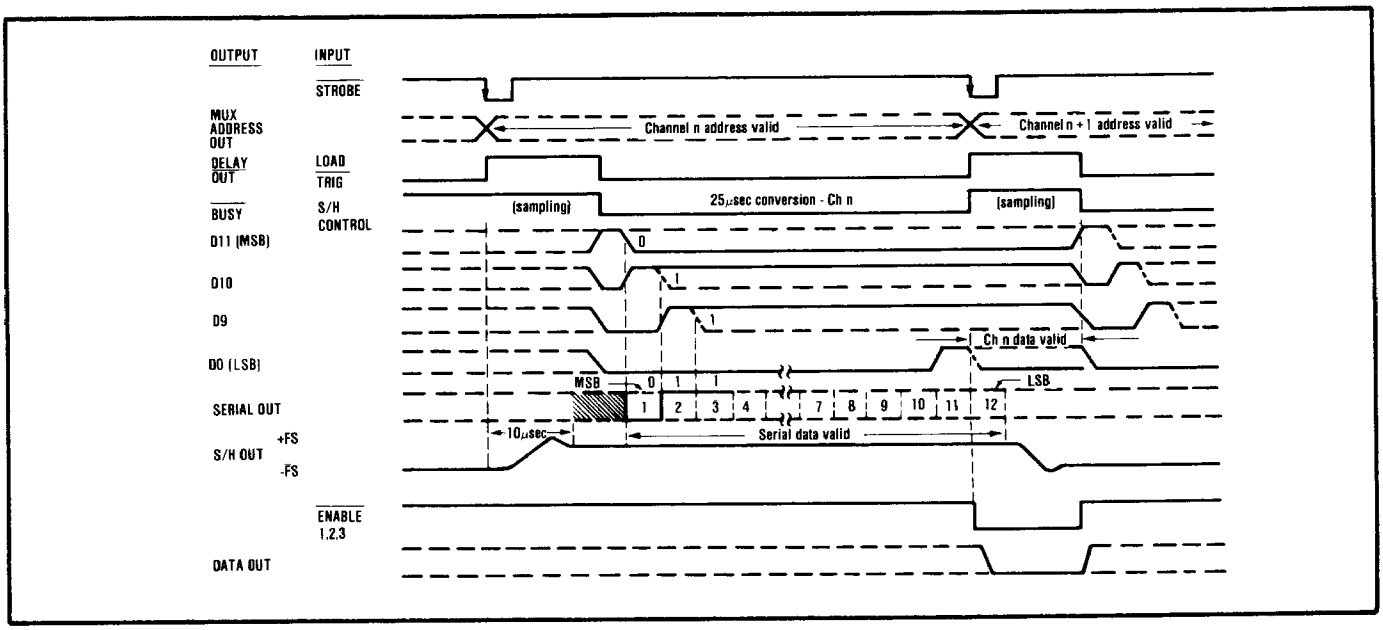


FIGURE 5. System Timing for Normal Operation.

Overlap Mode Connections

Connect $\overline{\text{BUSY}}$, pin 24 to $\overline{\text{STROBE}}$, pin 48, and DELAY OUT, pin 45 to TRIG, pin 46. Adjust the delay as described in the following paragraph.

DELAY ADJUSTMENT

The delay timer may be adjusted with an external capacitor or resistor from DELAY ADJUST (pin 47) to +5VDC. A capacitor will increase the delay to allow for increased settling time while a resistor will decrease the delay to allow for increased throughput rate with an external high speed instrumentation amplifier or lower resolution operation.

The values of R and C versus delay are shown in Figures 6 and 7.

GROUNDING CONSIDERATIONS

The circuit configuration of a high speed successive approximation A/D converter is such that low-level analog and digital signals are in close proximity. In fact the two circuits are actually interconnected; for this reason no AC noise voltage should be allowed to exist between digital and analog ground. Digital and analog ground should be connected as close to the unit as possible. In a typical application an SDM module will be used near a computer. For best results the SDM digital ground should be connected to the computer's +5VDC supply ground at the supply terminal. The ±15VDC supply ground should be connected to the +5VDC supply ground at the SDM only. The Burr-Brown Model 546 +5VDC to ±15VDC DC/DC converter is a convenient way to do this. For single-ended systems, signal returns are connected to analog ground.

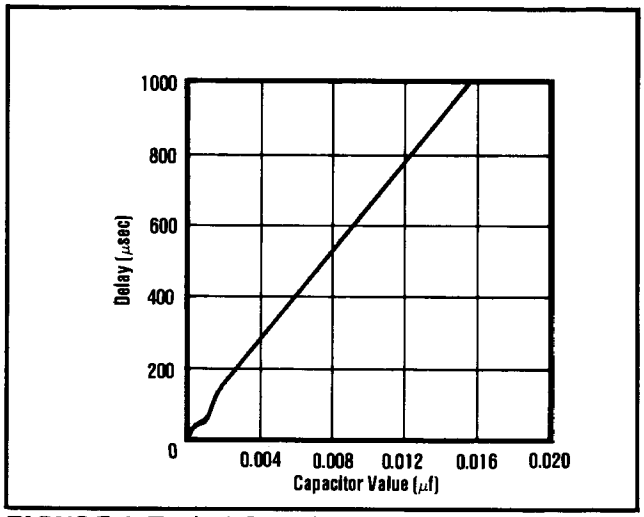


FIGURE 6. Typical Capacitor Value to Increase Delay Time*.

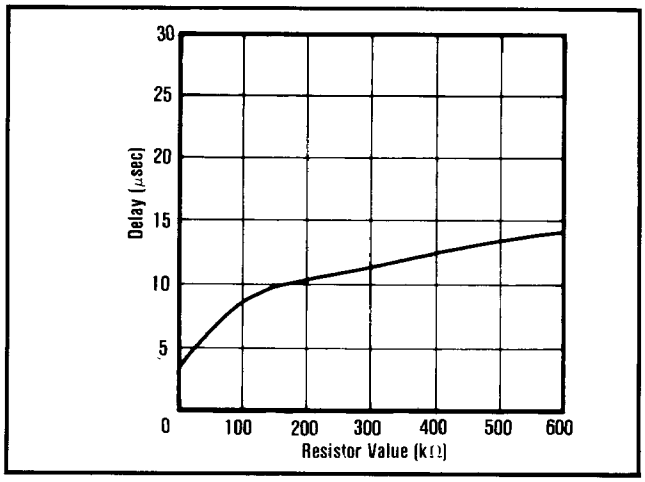


FIGURE 7. Typical Resistor Value to Decrease Delay Time.*

*Capacitor or resistor is connected from pin 47 to +5V supply.

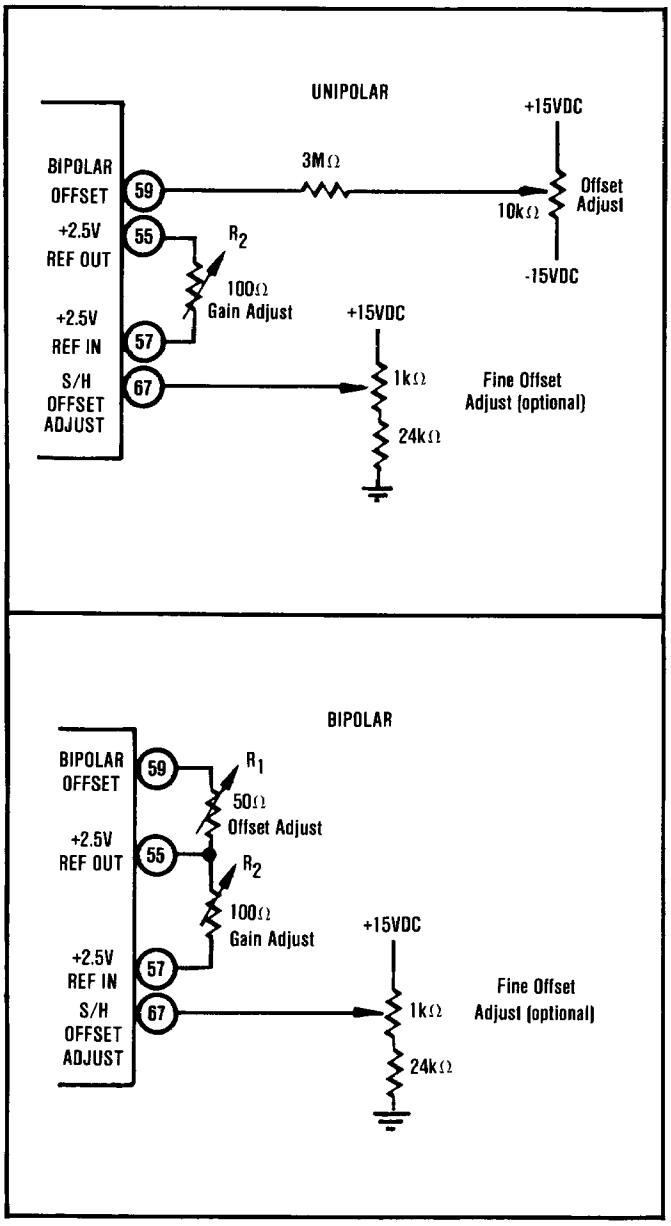


FIGURE 8. External Gain and Offset Adjustment.

CALIBRATION PROCEDURE

GAIN AND OFFSET ADJUSTMENT

External gain and offset adjustment potentiometers are shown in Figure 8. Cermet pots with a T.C.R. of ±100ppm/°C or less should be used. The adjustments shown each have a range of ±0.3% of the Full Scale Range.

If adjustment of gain and offset is not required R1 and R2 should be replaced with 25Ω and 50Ω resistors respectively. These resistors should be low T.C. (<±100ppm/°C) metal film or equivalent.

The S/H OFFSET ADJUST (pin 67) may be used as a fine offset adjustment.

The easiest way to calibrate the device is to connect a voltage source to multiplexer input CH0 (either differential or single-ended input operation may be used). Channel zero will be addressed by simply connecting $\overline{\text{CLEAR}}$ to DIG COM.

After the CH0 voltage source has been addressed, set it to the most negative value of the input range being used plus 1/2LSB. Twelve-bit LSB voltage values are given in Table III. Connect a triggering source to $\overline{\text{STROBE}}$ and adjust the offset potentiometer until all output bits are logic 0 with bit DØ dithering between logic 0 and 1. Change the source voltage to the most positive value of the input range minus 3/2LSB. Adjust the gain potentiometer until all output bits are logic 1 with bit D0 dithering between logic 1 and 0. When a resolution less than 12 bits is used, the LSB voltage is given by the formula in Table II where N is the number of output bits. One's complement coding is obtained by shifting the previous adjustments up by 1/2LSB using the offset potentiometer.

TABLE II. LSB Values for 12-Bit Resolution.

LSB (Volts) = (Range)/(2^N)

Range	LSB Voltage (12-Bits)
5V	1.22mV
10V	2.44mV

CLOCK RATE ADJUSTMENT

To obtain higher throughput rates at lower accuracy the A/D clock rate can be adjusted by varying the voltage on the clock rate adjust pin. This point should be connected to digital common for 12-bit accuracy, +5VDC for 10-bit accuracy, or +15VDC for 8-bit accuracy giving conversion times of 25μsec, 15μsec and 10μsec respectively. The conversion speed can also be continuously varied from about 13μsec to 110μsec (12-bit resolution) with a potentiometer as shown in Figure 9.

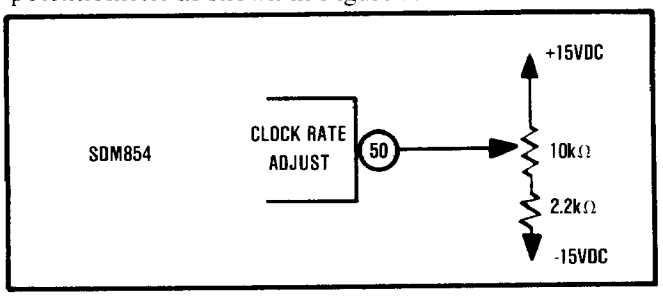


FIGURE 9. Clock Rate Adjustment.

CHECKOUT PROCEDURE

Checkout is essentially accomplished by the calibration procedure. Before the unit is plugged into a new installation, it is well to go over the pin connection list to be sure that all 80 pins have been properly connected in the setup. Linearity and monotonicity may be verified by varying the input voltage over the complete range during the calibration procedure.

LATCH

Latch operation can be verified by connecting a pulse generator to the LOAD input. The address inputs (A0 IN - A3 IN) should appear at the address outputs (A0 OUT -A3 OUT).

MULTIPLEXER

To check the multiplexer connect a voltmeter to the multiplexer output (pin 2 and pin 78) and observe that the output changed when the address was changed.

SAMPLE/HOLD

The sample hold circuit can be checked during the calibration procedure by observing the output of the S/H OUT (pin 62) with an oscilloscope. The waveform should be approximately as in Figure 10.

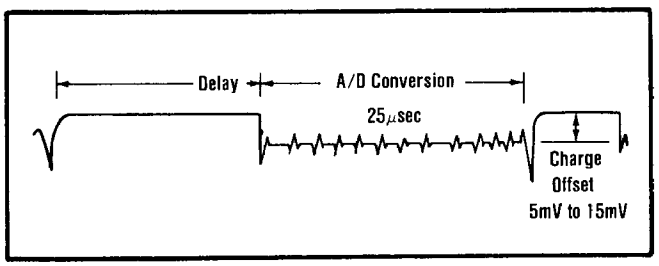


FIGURE 10. Sample/Hold Output Waveform.

The charge offset will vary in a linear manner from about 5mV for -10V to 15mV for +10V. This is compensated for by the offset and gain adjustments of the A/D converter. The spikes during conversion are normal noise caused by the converter operation.

ANALOG-TO-DIGITAL CONVERTER

The ADC can be checked out as an individual circuit element. Connect a fixed voltage to either 20V RANGE (pin 58) or 10V RANGE (pin 60). After adjusting the gain and offset errors as described on page 10, the digital output should represent the analog input as shown in Table III. To enable the three-state buffers, pins 53, 54 and 56 should be connected to logic 0.

TABLE III. Delay Timer Settings for Specified Settling Time Accuracies Using an External Burr-Brown 3630 Instrumentation Amplifier.

Full Scale Input Range	ADC Range	Amplifier Gain	Resolution	Delay Timer Setting (μsec)		
				To ±0.2%	To ±0.05%	To ±0.01%
20V (±10V)	-10 to +10	1	4.88mV	60	75	100
1V	0 to +10	10	244μV	50	60	75
0.1V	0 to +10	100	24.4μV	100	115	150
10mV	0 to +10	1000	2.44μV	500	700	1000

In overlap, when the external amplifier multiplexer settling time is less than the ADC conversion time, set the delay timer for the ADC conversion time plus the sample hold acquisition time (30μsec plus 10μsec). When the external amplifier multiplexer settling time exceeds the ADC conversion time plus the S/H acquisition time, set the delay timer for the external amplifier multiplexer time.

APPLICATION NOTES

CHANNEL CAPACITY EXPANSION

The SDM854 may be easily expanded to any number of channels by using Burr-Brown Models MPC8D and MPC16S. The MPC8D is an 8-channel double-ended multiplexer, and the MPC16S is a 16-channel single-ended multiplexer. The devices are CMOS FET units which can operate from supply voltages up to ±20VDC. They feature latch-free operation with full input protection. Binary decoding and level shifting circuits are included. Logic levels are jumper selectable for TTL or CMOS. Packaging is a 28-pin DIP.

There are two methods for using these devices for channel capacity expansion. The SDM854 multiplexer may be expanded by shunt or series connected multiplexers. Shunt connection refers to connecting the output of several multiplexers together and enabling each in sequence. The disabled devices present a very high resistance to the common output line. The disadvantages to this scheme are increased leakage current and output capacitance. For these reasons shunt connections are usually used only when it is desired to expand the capacity by a factor of two or three. A shunt connected system logic diagram is shown in Figure 11. Forty-eight single-ended

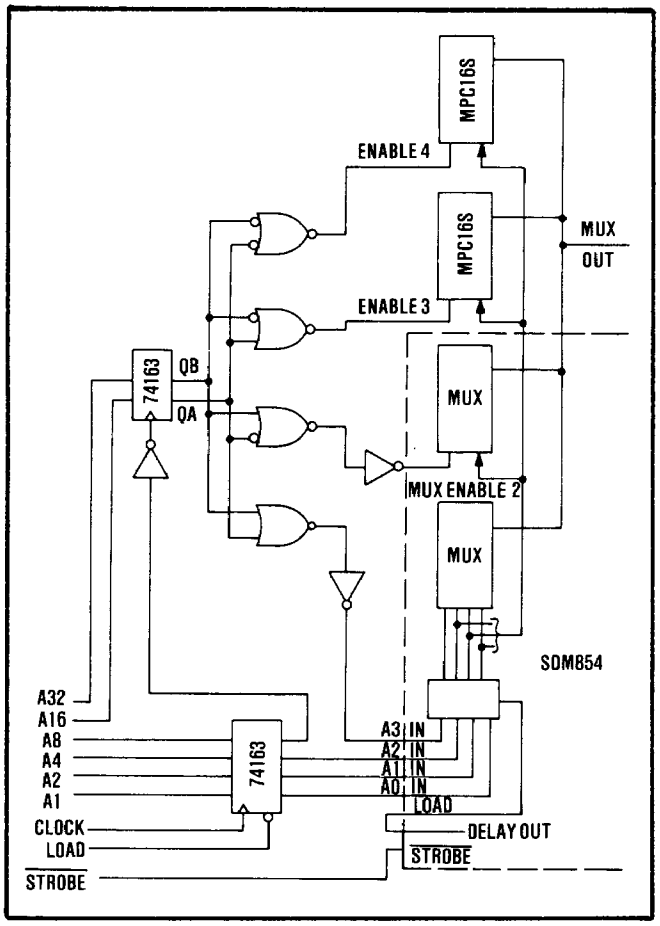


FIGURE 11. Shunt Connected Multiplexer System, 32 Single-Ended Channels.

channels are indicated; however, 24 double-ended channels could easily be realized by using two MPC8D's and connecting the two-sided outputs appropriately. For large systems series connected expansion is usually used. In this method the outputs of a second tier of multiplexers are connected to the inputs of the SDM854 multiplexer. This allows up to 256 single-ended or 128 double-ended channels to be addressed. A third tier can be used for 4096 single or 2048 double-ended channels. A logic diagram of a series system is shown in Figure 12. Double-ended operation can be obtained by using the MPC8D instead of the MPC16S and connecting the SDM854 for double-ended operation.

SEQUENTIAL ADDRESSING

Simply adding an external counter will allow sequential addressing of all 16 input channels (see Figure 13).

MULTIPLEXER CIRCUIT OPERATION

At the address and enable inputs a voltage is interpreted as a logic "1" if it is greater than 2.4 volts; and "0" if less than 0.8 volts.

When an input channel has been selected the "on resistance" from input to output is 3kΩ. The input capacitance for each channel is approximately 7pF, while the output capacitance is approximately 25pF for each 8-channel multiplexer. A circuit model of an ON channel is shown in Figure 14.

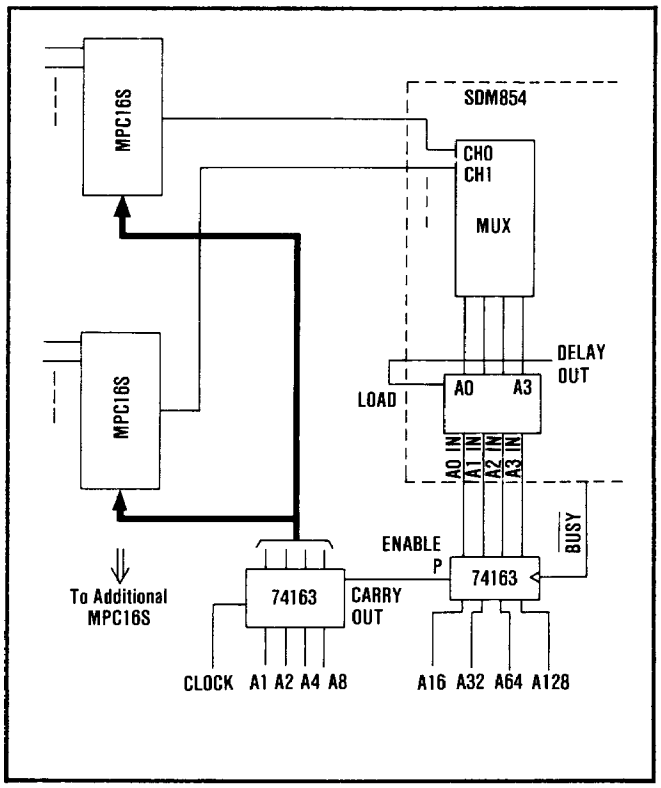


FIGURE 12. Series Connected Multiplexers, 256 Single-Ended Channels (Sequential Addressing).

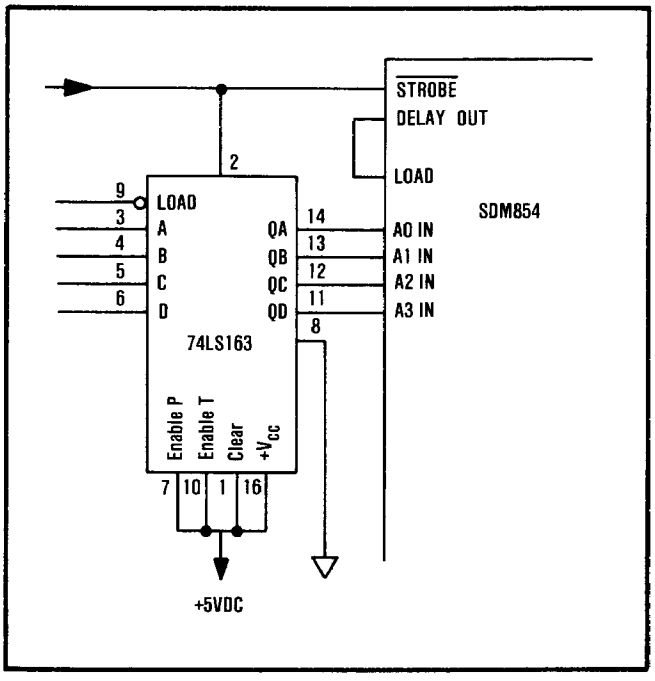


FIGURE 13. Sequential Addressing.

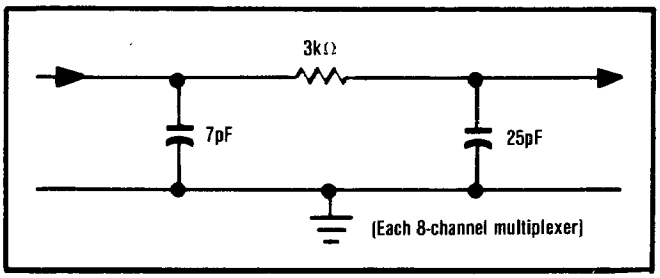


FIGURE 14. ON Channel Circuit Model.

This model is very important when high speed switching of high output impedance sources is required. For example, if the full accuracy and resolution of the system is required, the signal at the output of the multiplexer must be allowed to settle to about 0.01%. If the source impedance is 1kΩ, the 7pF can be neglected and the multiplexer has a time constant of 2.8kΩ x 50pF = 140nsec. It requires approximately 9 time constants to settle to 0.01%; 1.26μsec is well within the 15μsec of the SDM854 delay timer. However, if the source impedance had been 10kΩ, the 0.01% settling time would have approached 6μsec. For high speed multiplexing of higher impedance sources, it will usually be desirable to parallel the 7pF input capacitor with a large capacitor; however, this could limit the source bandwidth. In any case there is no point in making it any larger than 10^4 times the output capacitance, or 0.5μF. When this size storage capacitor is used, the output time constant is 1.8kΩ x 50pF = 90nsec. This means that the system settling time is essentially determined by the settling time of a differential amplifier and sample/hold circuit. For switching of large signals it must be remembered that the ON resistance is the channel resistance of a FET, and, as such, it is a nonlinear function of the applied voltages. Any FET will current limit at its I_{DSS} value. As a result, the previous calculations are only an approximation derived from a linearized model. The settling time to 0.01% for a 20V step is approximately 4.0μsec for source impedance less than 1kΩ.

The analog and digital inputs have reverse biased diode circuits which prevent damage from discharge of static electricity. However, it is still wise to take reasonable precaution against static discharge.

BINARY SCALING

Binary scaling of the A/D converter provides LSB voltages of 2.5mV, 2.5mV, and 5.0mV for voltage ranges of 0 to 10.24V, -5.12V to +5.12V, and -10.24V to ±10.24 respectively. These may be obtained by adding external resistors in series with input resistors of the A/D converter. Metal film resistors with temperature coefficients of less than 100ppm/°C are recommended. This is shown in Figure 15.

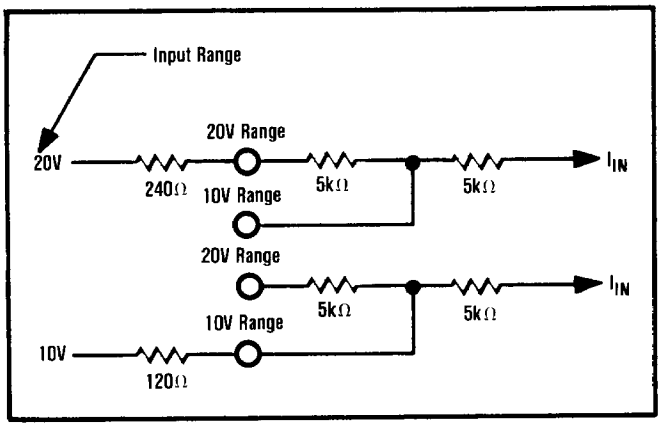


FIGURE 15. Binary Scaling.

USING AN INSTRUMENTATION AMPLIFIER WITH THE SDM854

When low-level signals are being converted, such as with thermocouples, strain gauges, etc., it will be necessary to use an instrumentation amplifier (IA) with the SDM854 to utilize the full dynamic range of a 12-bit system. This can be done by connecting the IA between the multiplexer and sample/hold amplifier because the output of the multiplexer and the input of the sample/hold amplifier are both brought out separately on the SDM854.

There are two ways an external IA can be connected to increase the versatility of the system. The most accurate way is to use the amplifier in a true differential mode as shown in Figure 16, where a Burr-Brown 3630 is connected

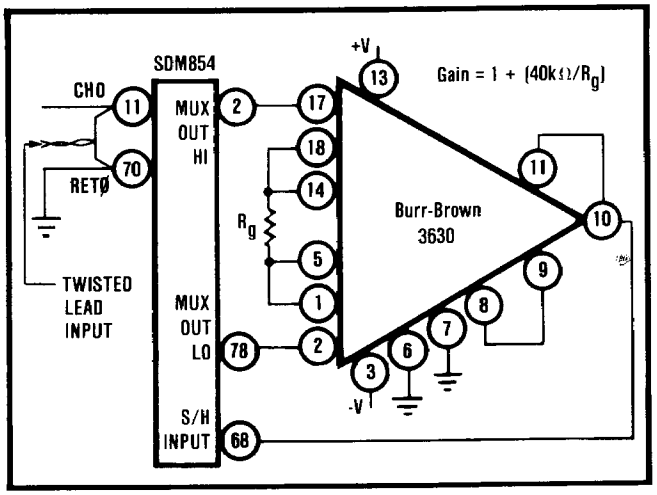


FIGURE 16. Instrumentation Amplifier Connection for True Differential Input.

to the SDM854 for differential operation. This configuration is ideal where the input lines run over a long distance or through noisy environments. For best results the input links should be in twisted shielded pairs with the shield grounded at one end to prevent ground loop currents from forming.

A second way to use an IA is in the pseudo-differential mode as shown in Figure 17. This method is ideal if all of

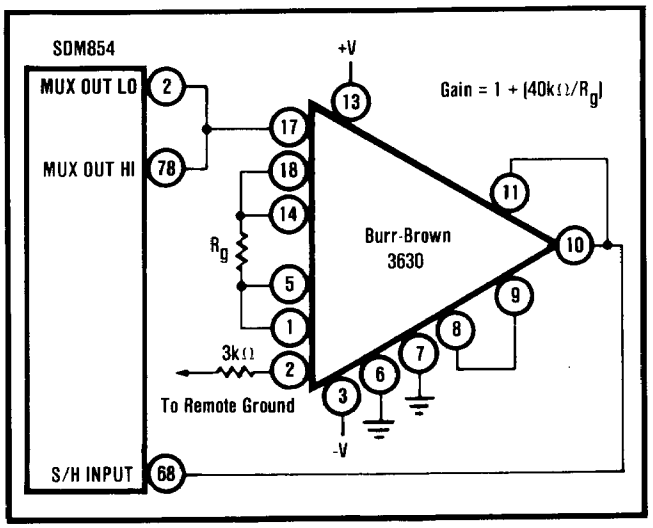


FIGURE 17. Instrumentation Amplifier Connection for Pseudo-Differential Input.

the input signals come from the same general area and at the same ground potential. In this application the inverted input of the IA can be used as a ground sense line. The IA will then reject the difference in ground potential and any common noise pick up from the ground sense line and the signal path. Care should be taken to match the impedance to ground from both inputs of the IA. This will insure the rejection of bias current effects from the IA. For better noise rejection the input lines should be grouped and shielded with the shield grounded at one end as in the true differential connection. One advantage of the pseudo-differential connection is that the multiplexers are operated in the single-ended mode allowing for 16 different input signals versus only 8 inputs in the true differential operation.

In both the true differential and pseudo-differential operation care should be taken in choosing the correct IA to maintain the high accuracy and linearity of the system.

Some of the important characteristics are:

1. Linearity error $\leqslant 0.012\%$ at all gains
2. Offset current drift $\leqslant 1/2LSB/(Gain)(R_{source})\Delta T$
3. CMRR $> CM_{signal}/1/2LSB$
4. Offset voltage drift $< 1/2LSB/(GAIN)\ \Delta T$
5. High input impedance $> R_{source} \times 10^4$

The importance of initial offsets are somewhat minimized by the capability to cancel out offset at several points in the system. The Burr-Brown 3630 was chosen for this application because of its high linearity, good drift spec and CMRR characteristics. Some of the accuracy calculations for the Burr-Brown 3630 are as follows:

Nonlinearity = $\pm 0.002 + 10^{-5}$ (Gain) % FS at G $\leqslant$ 100
nonlinearity is $\leqslant 0.003\%$FS

Input impedance = $10^9\Omega$ so source impedance up to 100kΩ can be used.

Voltage offset drift at Gain = 100
$0.25\mu V/°C \leqslant 1.22mV/100\Delta T$ so $\Delta T \leqslant 49°C$
for errors $\leqslant 1/2LSB$.

CMRR at Gain = 100 is 110dB

CM range = 10V/1.22mV = 78dB.

THERMOCOUPLE TEMPERATURE ACQUISITION

Thermocouples are often used as temperature sensors for process control systems. Thermocouples are characterized by temperature coefficients of $10\mu V/°C$ to $70\mu V/°C$ and operating ranges of minus hundreds to plus thousands of degrees centigrade. When the SDM854 is operated with an external instrumentation amplifier gain of 100 to 1000, it may be connected directly to these devices. However, electronic instrumentation is usually mounted in a temperature controlled environment with long runs of thermocouple wire to the actual point of temperature measurement. These long wire runs often pick up large common-mode noise signals of 60Hz or higher frequencies. When the SDM854 is used as an 8-channel differential input system, the high common-mode rejection of the external instrumentation amplifier will reject common-mode noise. To minimize differential mode noise, signal wires should be twisted and possibly shielded. As a rule, an open twisted pair is better than a coax, and a shielded, twisted pair better still. In applications where these wiring practices cannot always be observed, a differential RC filter may be used (see Figure 18).

The 10kΩ resistors and a $10\mu F$ capacitor provide low-pass filtering ($f_c = 0.8Hz$) while the 1MΩ resistors supply bias current to the instrumentation amplifier. The remote sensor should be earth grounded to prevent common-mode voltages from exceeding the ±15V range of the multiplexer. This will usually supply bias current; however, the resistors provide a back up. It is not obvious what resistance the bias currents of the amplifiers will see. The 1MΩ resistors do not enter into an error calculation for input drift because the low resistance of the sensor shorts any differential current of the amplifier. Offset or difference current is merely the difference between the bias currents of each input. See page 15 for a worst-case error analysis of the input filter for multiplexed data acquisition systems. The 1MΩ resistors could have been put on the output side of the multiplexer eliminating the

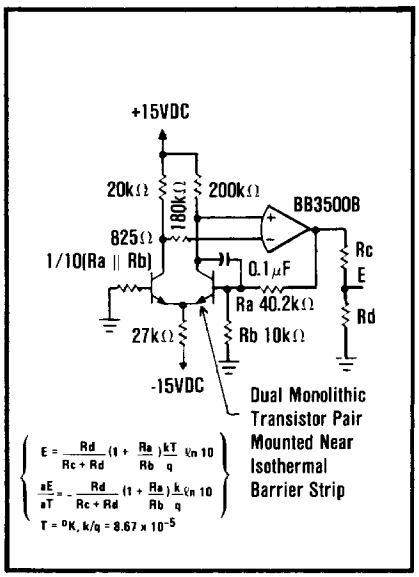


FIGURE 18. Ambient Temperature Sensor

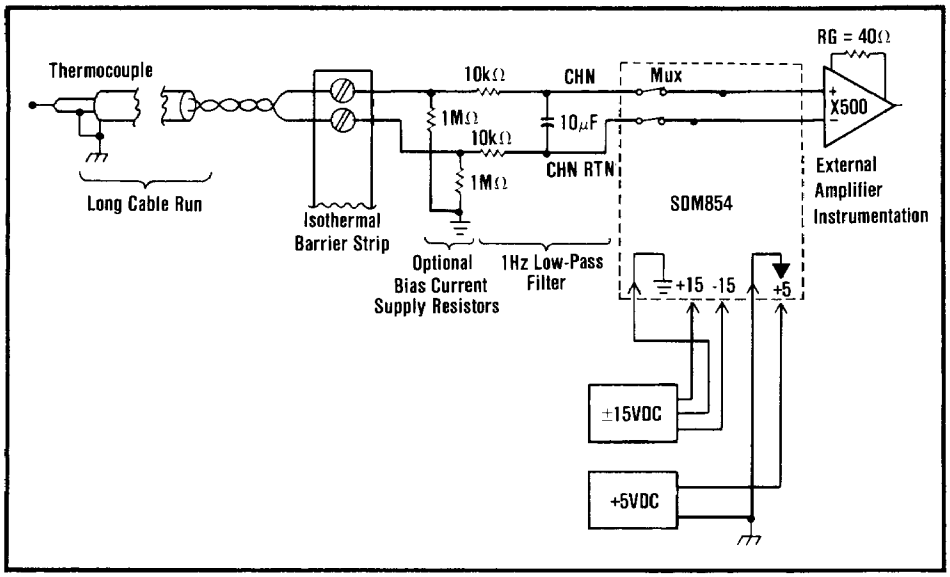


FIGURE 19. Thermocouple Inputs

need for repeating them for each input; however, this would have loaded the 10kΩ resistors of the filter causing a possible 1% error for static conditions.

To complete a thermocouple system it is necessary to terminate all thermocouple wire pairs at an isothermal box or connector strip of some type. An ordinary barrier strip in an enclosed cabinet with even air circulation is usually adequate. The temperature of this barrier strip must be monitored to allow the observed thermocouple emf to be cold junction compensated. Figure 19 shows an excellent circuit for this purpose. Its output is connected to one of the input channels to supply ambient temperature data to the system computer.

INPUT FILTER DESIGN FOR LOW-LEVEL SYSTEMS

When the SDM854 is used to acquire low-level sensor data, it is often desired to place a low-pass, passive filter on each input. This is usually done to reduce any differential mode, power line frequency pickup. Figure 20 shows such a circuit.

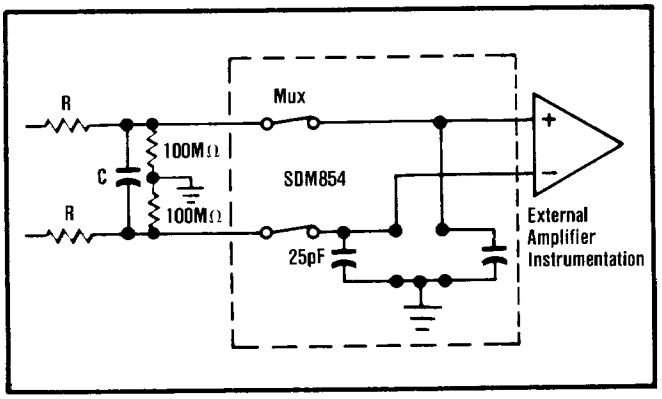


FIGURE 20. Input Filter Design for Low-Level System.

This circuit is deceptive in its simplicity. Actually four errors sources should be considered in its design. They are loading, offset current, charge transfer, and pump out current.

The static loading error is simply the resistive divider created by the filter resistors and the 100MΩ input resistance. For low-level sensors, 0.1% system accuracy is usually adequate. Thus R should be less than 10^{-3} x (100MΩ) = 100kΩ. However, if the inputs are scanned at a high speed, and between scans the multiplexer can be addressed to a unique channel having a lower resistance, higher filter resistance can be tolerated because the large filter capacitor will act as a voltage source during the 30μsec to 100μsec period required to read each channel. The filter capacitors will then recharge between scans.

The input offset current caused by the bias currents of the external instrumentation amplifier as well as any leakage current of the multiplexer will cause an error voltage proportional to the size of the filter resistors ($E = I_{os} \times 2R$). Of course, this is a static error and as for loading error, may not be important for some operating conditions. If all channels have the same resistance most of this error may be corrected by the offset adjustment of the analog-to-digital converter. If the offset current drift is 0.1nA/°C the error is 2R x 0.1nV/°C. For 10kΩ resistors this would be 2μV/°C.

When the multiplexer scans, charge will be transferred from the filter capacitor to the 25pF output capacitance of the multiplexer. For less than 0.1% of full scale error, the filter capacitor must be large than 25000pF. This assumes that adjacent channels may differ by the full scale voltage.

Pumpout current refers to charge being transferred from the filter capacitor to the multiplexer capacitance at time intervals short enough that the filter capacitor does not have time to recharge between scans. At high scan rates this may be considered a DC current which may add to the offset current. Assume a 10μF capacitor sampled once per millisecond. For a 20mV full scale range, the maximum effective current is (20mV x 25pF) / 1msec = 0.5nA. If the filter resistors are 10kΩ, a 0.5nA x 20kΩ = 10μV error is created.

When no input filter is used, the signal source must be able to charge the multiplexers and any cable capacitance during the channel acquisition time of the multiplexer and external amplifier. This is discussed on page 13. When all of these errors as well as the basic 2.0μV/°C input offset voltage drift of the external amplifier are considered, the overall system accuracy may be estimated.

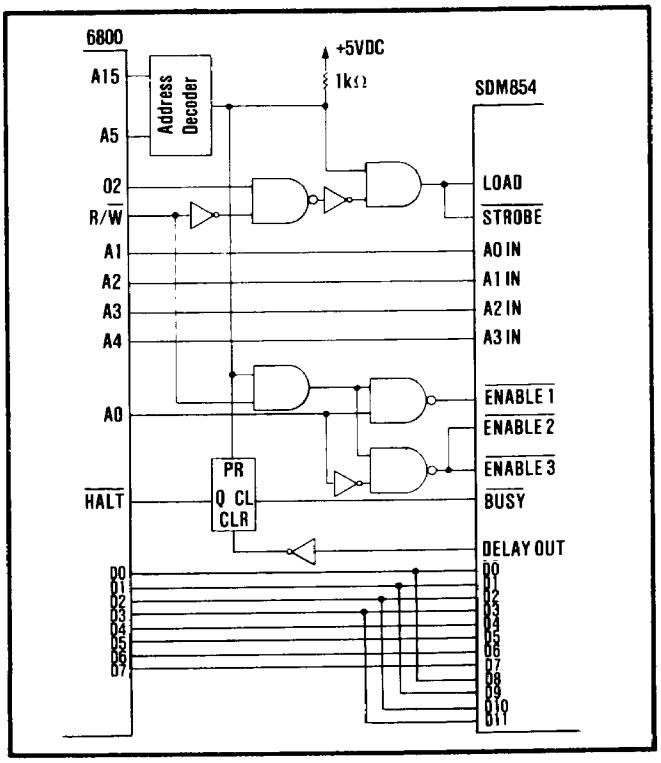


FIGURE 21. SDM854 Interfaced to 6800 Microprocessor.

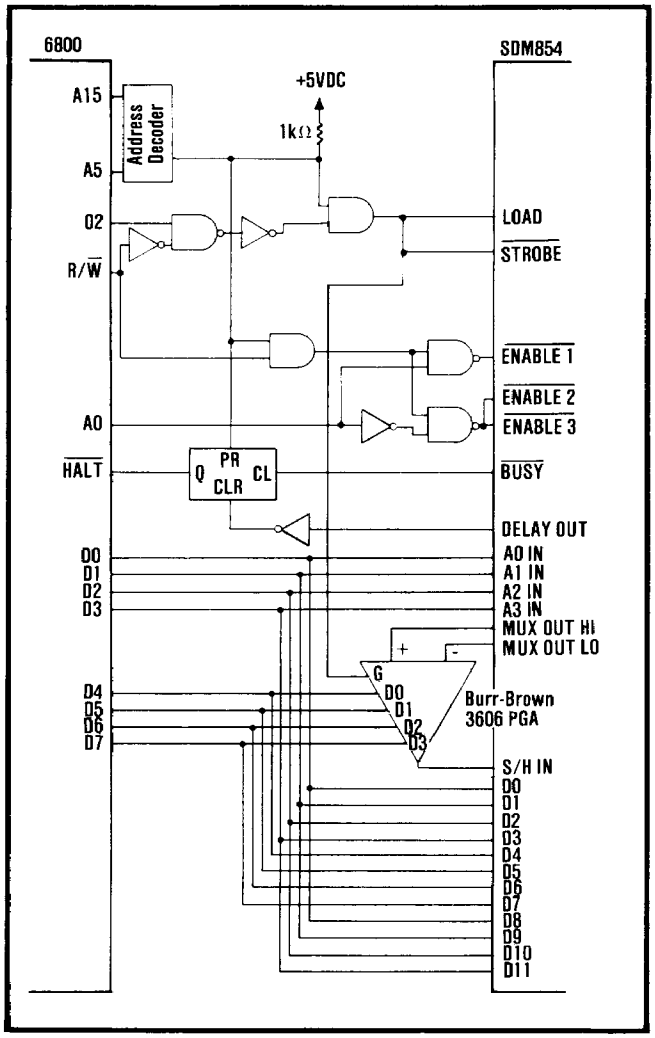


FIGURE 22. SDM854 and 3606 PGA Interfaced to 6800.

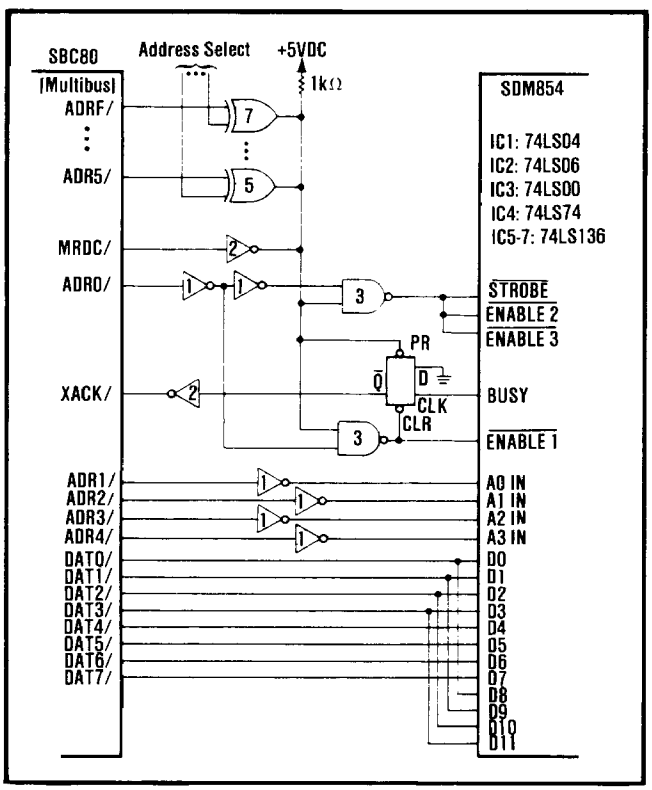


FIGURE 23. SDM854 Interfaced to SBC80 Multibus.

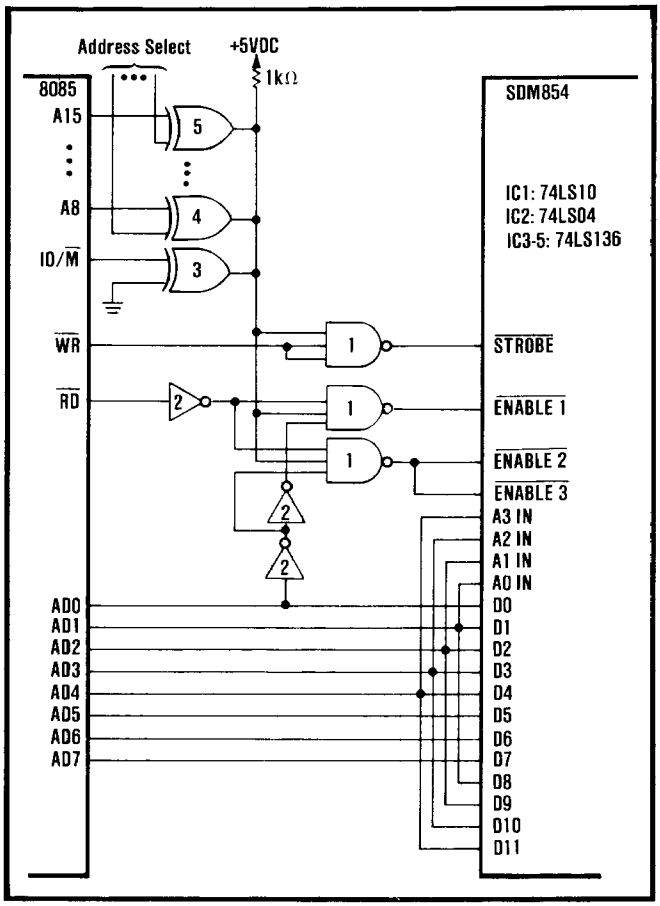


FIGURE 24. SDM854 Interfaced to 8085.

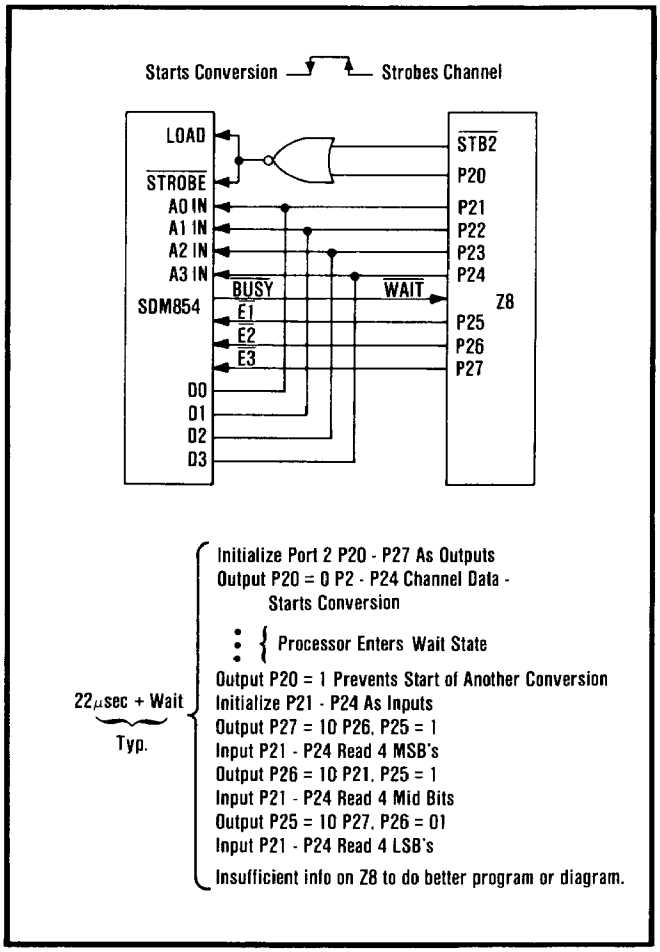


FIGURE 25. SDM854 Interfaced to Z8.