

41JP Dual 128-Bit Static Shift Register

Features

- Two 128-bit static shift registers
- TTL-compatible inputs and outputs
- Separate single-phase clock, negative-edge triggered for each register
- DC to 2.048 MHz operation
- Single 5 V supply (330 mW max)

Description

The 41JP Dual 128-Bit Static Shift Register is an NPN silicon, bipolar, monolithic, sealed junction, beam-lead chip encapsulated in a 16-pin plastic dual in-line package (DIP).

User Information

Pin Descriptions

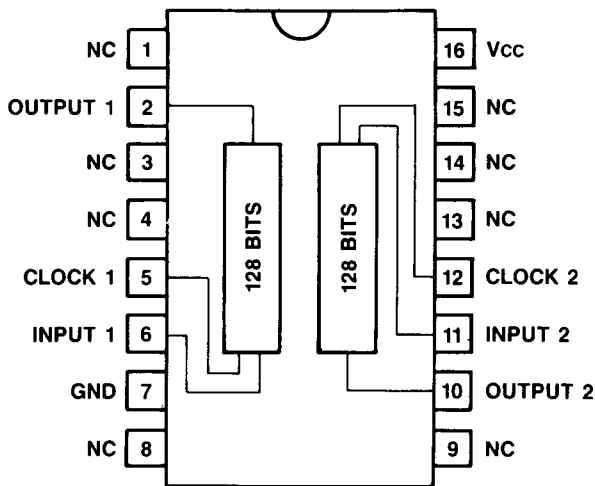


Figure 1. Pin Function Diagram

Table 1. Pin Descriptions

Pin	Symbol	Type	Name/Function
1	NC	—	No connection.
2	OUTPUT 1	O	Serial data output.
3,4	NC	—	No connection.
5	CLOCK 1	I	Clock.
6	INPUT 1	I	Serial data input.
7	GND	—	Ground.
8,9	NC	—	No connection.
10	OUTPUT 2	O	Serial data output.
11	INPUT 2	I	Serial data input.
12	CLOCK 2	I	Clock.
13—15	NC	—	No connection.
16	Vcc	—	+5 V supply.

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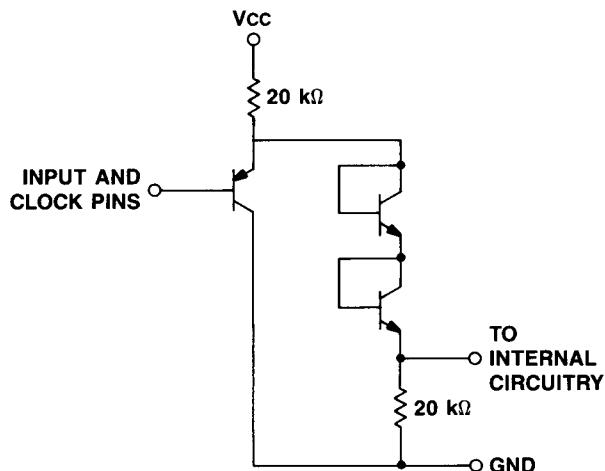


Figure 2. Basic Input Schematic

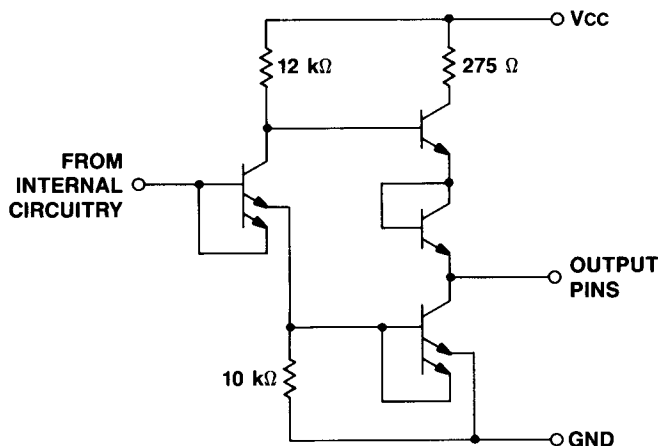


Figure 3. Basic Output Schematic

Characteristics

Electrical Characteristics

$T_A = 0 \text{ to } 85^\circ\text{C}$, $V_{CC} = 5.0 \pm 0.5 \text{ V}$

Parameter	Symbol	Min	Max	Unit
Input Voltage (Leads 5, 6, 11, 12)				
Low Level	V_{IL}	0	0.8	V
High Level	V_{IH}	1.8	5.5	V
Input Forward Current ($V_{IN} = 0.4 \text{ V}$)				
Low Level (Leads 5, 12)	$I_{IL5,12}$	—	35	μA
High Level (Leads 6, 11)	$I_{IH6,11}$	—	60	μA
Input Reverse Current ($V_{IN} = 2.4 \text{ V}$)	I_{IH}	—	10	μA
Output Voltage				
Low Level ($I_L = 5.0 \text{ mA}$)	V_{OL}	0	0.4	V
High Level ($I_L = -1 \text{ mA}$)	V_{OH}	2.4	—	V
Short Circuit Output Current	I_{OS}	-5.0	-25	mA
Power Supply Current Drain	I_{CC}	40 typ	65	mA

Maximum Ratings

Power supply voltage (V_{CC})	7.0 V
Input voltage (V_I)	5.5 V
Operating temperature range (T_A)	-40 to +125°C
Storage temperature range (T_{STG})	-40 to +125°C

Maximum ratings are defined as the limiting conditions that the user can apply to the device under all variations of circuit and environmental conditions. If any rating is exceeded, permanent damage to the device may result.

Bonding or soldering of the external leads of these devices can be performed safely at temperatures up to 300°C.

Timing Characteristics

$T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{ V}$

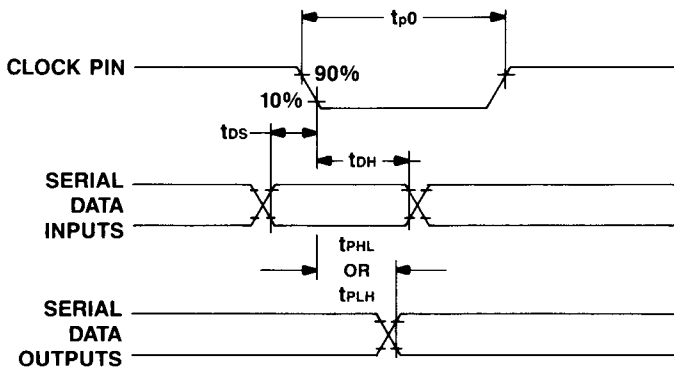
Symbol	Description	Min	Typ	Max	Unit
f _{max}	Maximum Clock Frequency	2.048	2.7	—	MHz
t _{p0} t _{p1}	Clock Pulse Width	220 220	180 140	— —	ns ns
t _{DS}	Data Setup Time	25	-50	—	ns
t _{DH}	Data Hold Time	75	50	—	ns
t _{PLH} t _{PLH}	Output Delay Low-to-High	— 24	180 80	220 —	ns ns
t _{PHL}	Output Delay High-to-Low	—	130	220	ns

$T_A = 70^\circ\text{C}$, $V_{CC} = 5\text{ V}$

Symbol	Description	Min	Typ	Max	Unit
f _{max}	Maximum Clock Frequency	2.048	2.5	—	MHz
t _{p0} t _{p1}	Clock Pulse Width	220 220	200 150	— —	ns ns
t _{DS}	Data Setup Time	25	-40	—	ns
t _{DH}	Data Hold Time	75	40	—	ns
t _{PLH} t _{PLH}	Output Delay Low-to-High*	— 24	200 60	220 —	ns ns
t _{PHL}	Output Delay High-to-Low	—	140	220	ns

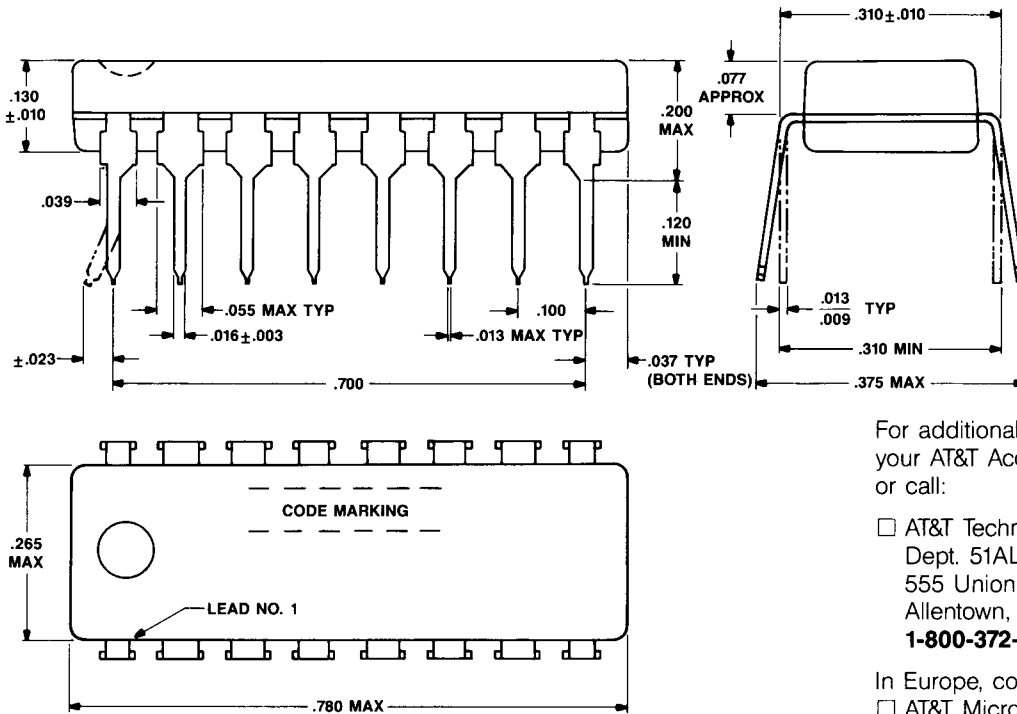
* At a frequency of 2.048 MHz, data appears at the output 24 ns prior to the next positive edge of the clock, t_{p0} = 250 ns.

Timing Diagram



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Outline Diagram (Dimensions in Inches)



Notes:
 Lead may be solder coated.
 Measured with leads constrained to insertion center dimension.
 Lead No. 1 can be identified by a circular depression.

Ordering Information

Device Code	Package	Temperature	Comcode
41JP	16-Pin Plastic DIP	0 to 85°C	103196291

008184 ✓ - X

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