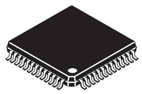
Product Preview

3.3V Differential ECL/PECL PLL Clock Generator

MPC9991

3.3V DIFFERENTIAL ECL/PECL PLL CLOCK GENERATOR



FA SUFFIX
52 LEAD LQFP PACKAGE
CASE 848D

The MPC9991 is a 3.3 V compatible, PLL based ECL/PECL clock driver. Using SiGe technology and a fully differential design ensures optimum skew and PLL jitter performance. The performance of the MPC9991 makes the device ideal for workstation, mainframe computer and telecommunication applications. With output frequencies up to 400 MHz and output skews less than 150 ps[1] the device meets the needs of the most demanding clock applications. The MPC9991 offers a differential ECL/PECL input for applications which need to lock to an existing clock signal. It also offers a secondary single–ended ECL/PECL clock for system test capabilities.

Features

- 13 differential outputs, PLL based clock generator
- SiGe technology supports minimum output skew (max. 150 ps[1])
- Supports up to three individual generated output clock frequencies with a maximum clock frequency up to 400 MHz
- External PLL feedback supports zero-delay capability
- Selectable SYNC pulse generation
- ECL/PECL compatible differential clock inputs and outputs
- Single 3.3V (PECL) or -3.3V (ECL) supply
- Ambient temperature range 0°C to +70°C
- Standard 52 lead LQFP package
- Pin and function compatible to the MPC991

Functional Description

The MPC9991 utilizes PLL technology to frequency lock its outputs onto an input reference clock. Normal operation of the MPC9991 requires the connection of the differential PLL feedback output QFB to the differential feedback input FB_IN to close the PLL feedback path. The reference clock frequency and the divider for the feedback path determine the VCO frequency. Both must be selected to match the VCO frequency range. The MPC9991 features frequency programmability between the three output banks outputs as well as the output to input relationships. Output frequency ratios of 1:1, 2:1, 3:1, 3:2, 4:1, 4:3, 4:3:1 and 4:3:2 can be realized. The three banks of outputs can each be programmed by the FSEL[3:0] pins of the device. There are 16 different output frequency configurations available in the device. Additionally, the device supports a separate configurable feedback output. This allows for the feedback frequency to be programmed independently of the other outputs, providing six input to output frequency ratios that can be configured by the FSEL_FB[2:0] inputs. The external feedback feature enables the use of the MPC9991 as a zero-delay buffer. The VCO_SEL pin provides an extended PLL input reference frequency range.

The SYNC pulse generator monitors the phase relationship between the QA[3:] and QC[2:0] output banks. The SYNC generator output signals the coincident edges of the two output banks. This feature is useful for non binary relationships between output frequencies (i.e., 3:2 or 4:3 relationships). The SYNC_SEL input switches the QD[1:0] outputs between the SYNC signals and an extensions to the QC bank of outputs. The REF_SEL pin selects the differential ECL/PECL compatible input pair or a single-ended ECL/PECL compatible input as the reference clock signal. The $\overline{\text{PLL\_EN}}$ control selects the PLL bypass configuration for test and diagnosis. In this configuration, the selected input reference clock is routed directly to the output dividers bypassing the PLL. The PLL bypass is fully static and the minimum clock frequency specification and all other PLL characteristics do not apply. The MPC9991 requires an external reset signal for start-up and for PLL recovery in the case the external feedback is interrupted. The MPC9991 is fully 3.3V (PECL) or -3.3V (ECL) compatible and requires no external loop filter components. All inputs accept PECL/ECL compatible differential signals while the outputs provide PECL/ECL compatible levels with the capability to drive terminated 50 Ω transmission lines. The device is pin and function compatible to the MPC991 and is packaged in a 52-lead LQFP package.

1. Final specification of this parameter is pending characterization.

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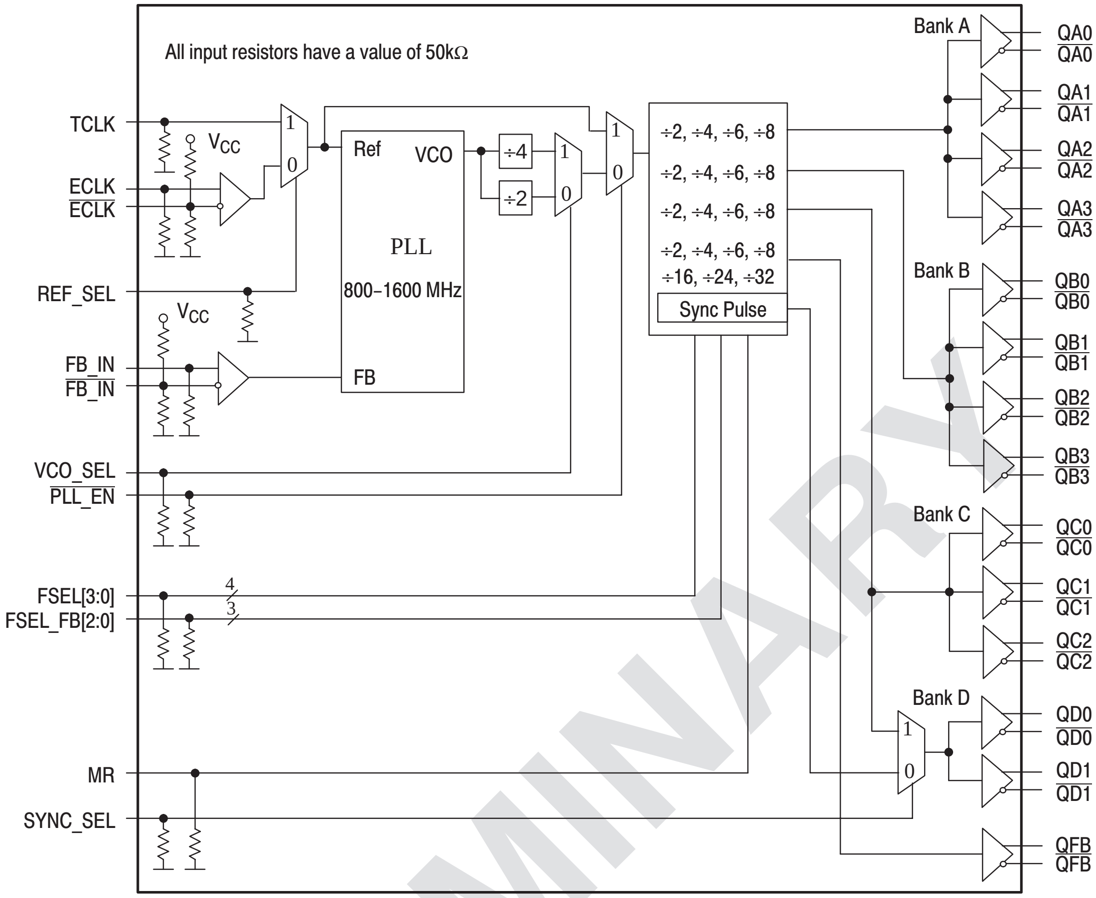

Figure 1. MPC9991 Logic Diagram

FUNCTION TABLE

Control	Default	0	1
REF_SEL	0	Selects ECLK, $\overline{\text{ECLK}}$ as PLL refererence signal input	Selects TCKL as PLL reference signal input
VCO_SEL	0	Selects VCO÷2. (high input frequency range)	Selects VCO÷4. The VCO frequency is scaled by a factor of 4 (low input frequency range).
$\overline{\text{PLL\_EN}}$	0	Normal operation mode with PLL enabled.	Test mode with the PLL bypassed. The reference clock is substituted for the internal VCO output. MPC9991 is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable.
MR	0	Normal operation	Reset of the device. During reset the PLL feedback loop is open and the internal VCO is tied to its lowest frequency. The MPC9991 requires reset at power-up and after any loss of PLL lock. Loss of PLL lock may occur when the external feedback path is interrupted. The length of the reset pulse should be greater than one reference clock cycle (CCLKx)
SYNC_SEL	0	QD[1:0] outputs generate a SYNC signal	QD[1:0] outputs generate clock signals that match the QC[2:0] outputs
VCO_SEL, FSEL[3:0] and FSEL_FB[2:0] control the operating PLL frequency range and input/output frequency ratios. See Table 2 and Table 3 for the device frequency configuration.			

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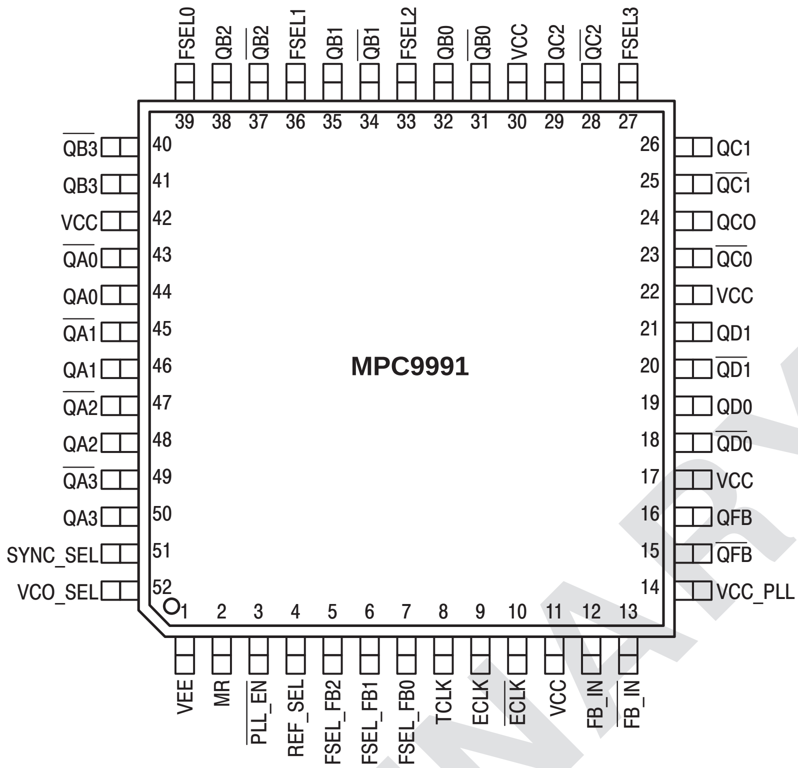


Figure 2. MPC9991 52–Lead Package Pinout (Top View)

Table 1: PIN CONFIGURATION

Pin	I/O	Type	Function
ECLK, $\overline{ECLK}$	Input	PECL/ECL	Differential reference clock signal input
TCLK	Input	PECL/ECL	Single-ended test clock input
FB_IN, $\overline{FB\_IN}$	Input	PECL/ECL	Differential PLL feedback clock signal input, connect to QFB, $\overline{QFB}$
VCO_SEL	Input	PECL/ECL	VCO operating frequency select
$\overline{PLL\_EN}$	Input	PECL/ECL	PLL Enable/Bypass mode select
REF_SEL	Input	PECL/ECL	PLL reference signal input select
MR	Input	PECL/ECL	Device reset
FSEL[3:0]	Input	PECL/ECL	Output frequency divider select
FSEL_FB[2:0]	Input	PECL/ECL	Frequency divider select for the QFB output
SYNC_SEL	Input	PECL/ECL	QD output mode select
QA[0-3], $\overline{QA[0\text{-}3]}$	Output	PECL/ECL	Differential clock outputs (bank A)
QB[0-3], $\overline{QB[0\text{-}3]}$	Output	PECL/ECL	Differential clock outputs (bank B)
QC[0-2], $\overline{QC[0\text{-}2]}$	Output	PECL/ECL	Differential clock outputs (bank C)
QD[0-1], $\overline{QD[0\text{-}1]}$	Output	PECL/ECL	Differential clock/SYNC signal outputs (bank D)
QFB, $\overline{QFB}$	Output	PECL/ECL	Differential PLL feedback clock output (connect to FB_IN, $\overline{FB\_IN}$)
VEE[a]	Supply	VEE	Negative power supply
V_{CC}	Supply	VCC	Positive power supply. All V_{CC} pins must be connected to the positive power supply for correct DC and AC operation
VCC_PLL	Supply	VCC	PLL positive power supply (analog power supply). It is recommended to use an external RC filter for the analog power supply pin VCC_PLL. Please see applications section for details

a. In ECL mode (negative power supply mode), VEE is -3.3V and VCC is connected to GND (0V).
In PECL mode (positive power supply mode), VEE is connected to GND (0V) and VCC is +3.3V.
In both modes, the input and output levels are referenced to the most positive supply (VCC).

Table 2: Output Divider PLL Feedback M (QFB)

VCO_SEL	FSEL_B2	FSEL_FB1	FSEL_FB0	QFB
0	0	0	0	VCO÷4
0	0	0	1	VCO÷8
0	0	1	0	VCO÷12
0	0	1	1	VCO÷16
0	1	0	0	VCO÷16
0	1	0	1	VCO÷32
0	1	1	0	VCO÷48
0	1	1	1	VCO÷64
1	0	0	0	VCO÷8
1	0	0	1	VCO÷16
1	0	1	0	VCO÷24
1	0	1	1	VCO÷32
1	1	0	0	VCO÷32
1	1	0	1	VCO÷64
1	1	1	0	VCO÷96
1	1	1	1	VCO÷128

Table 3: Output Divider N (Bank A to Bank C)

VCO_SEL	FSEL3	FSEL2	FSEL1	FSEL0	QA[3:0]	QB[3:0]	QC[2:0]
0	0	0	0	0	VCO÷4	VCO÷4	VCO÷4
0	0	0	0	1	VCO÷4	VCO÷4	VCO÷8
0	0	0	1	0	VCO÷4	VCO÷8	VCO÷8
0	0	0	1	1	VCO÷4	VCO÷4	VCO÷12
0	0	1	0	0	VCO÷4	VCO÷12	VCO÷12
0	0	1	0	1	VCO÷4	VCO÷8	VCO÷12
0	0	1	1	0	VCO÷4	VCO÷8	VCO÷16
0	0	1	1	1	VCO÷4	VCO÷12	VCO÷16
0	1	0	0	0	VCO÷4	VCO÷4	VCO÷16
0	1	0	0	1	VCO÷4	VCO÷16	VCO÷16
0	1	0	1	0	VCO÷8	VCO÷8	VCO÷12
0	1	0	1	1	VCO÷8	VCO÷12	VCO÷12
0	1	1	0	0	VCO÷8	VCO÷12	VCO÷16
0	1	1	0	1	VCO÷12	VCO÷12	VCO÷16
0	1	1	1	0	VCO÷12	VCO÷16	VCO÷16
0	1	1	1	1	VCO÷16	VCO÷16	VCO÷16
1	0	0	0	0	VCO÷8	VCO÷8	VCO÷8
1	0	0	0	1	VCO÷8	VCO÷8	VCO÷16
1	0	0	1	0	VCO÷8	VCO÷16	VCO÷16
1	0	0	1	1	VCO÷8	VCO÷8	VCO÷24
1	0	1	0	0	VCO÷8	VCO÷24	VCO÷24
1	0	1	0	1	VCO÷8	VCO÷16	VCO÷24
1	0	1	1	0	VCO÷8	VCO÷16	VCO÷32
1	0	1	1	1	VCO÷8	VCO÷24	VCO÷32
1	1	0	0	0	VCO÷8	VCO÷8	VCO÷32
1	1	0	0	1	VCO÷32	VCO÷32	VCO÷32
1	1	0	1	0	VCO÷16	VCO÷16	VCO÷24
1	1	0	1	1	VCO÷16	VCO÷24	VCO÷24
1	1	1	0	0	VCO÷16	VCO÷24	VCO÷32
1	1	1	0	1	VCO÷24	VCO÷24	VCO÷32

Table 4: ABSOLUTE MAXIMUM RATINGS[a]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	-0.3	3.6	V	
V_{IN}	DC Input Voltage	-0.3	V_{CC}+0.3	V	
V_{OUT}	DC Output Voltage	-0.3	V_{CC}+0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	-65	125	°C	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 5: GENERAL SPECIFICATIONS

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		V_{CC} – 2		V	
MM	ESD Protection (Machine Model)	TBD			V	
HBM	ESD Protection (Human Body Model)	TBD			V	
CDM	ESD Protection (Charged Device Model)	TBD			V	
LU	Latch–Up Immunity	200			mA	
C_{IN}	Input Capacitance		4.0		pF	Inputs
θ_{JC}	Thermal resistance (junction-to-ambient, junction-to-board, junction-to-case)		TBD		°C/W	
T_J	Operating junction temperature[a] (continuous operation) MTBF = 9.1 years	0		110	°C	

a. Operating junction temperature impacts device life time. Maximum continuous operating junction temperature should be selected according to the application life time requirements (See application note AN1545 for more information). The device AC and DC parameters are specified up to 110°C junction temperature allowing the MPC9991 to be used in applications requiring industrial temperature range. It is recommended that users of the MPC9991 employ thermal modeling analysis to assist in applying the junction temperature specifications to their particular application.

Table 6: PECL DC CHARACTERISTICS (V_{CC} = 3.3V ± 5%, V_{EE} = GND, T_A = 0°C to 70°C)[a]

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Differential PECL clock inputs (ECLK, $\overline{ECLK}$ and FB_IN, $\overline{FB\_IN}$)[b]						
V_{PP}	AC differential input voltage[c]	0.1		1.3	V	Differential operation
V_{CMR}	Differential cross point voltage[d]	1.0		V_{CC}-0.3	V	Differential operation
Single-ended PECL clock inputs (TCLK, VCO_SEL, $\overline{PLL\_EN}$, MR, REF_SEL, SYNC_SEL, FSEL_FB[2:0], FSEL[3:0])						
V_{IH}	Input High Voltage	TBD		TBD		
V_{IL}	Input Low Voltage	TBD		TBD		
I_{IN}	Input Current			±TBD	µA	V_{IN} = TBD or V_{IN} = TBD
PECL clock outputs (QA[3:0], $\overline{QA[3:0]}$, QB[3:0], $\overline{QB[3:0]}$, QC[2:0], $\overline{QC[2:0]}$, QD[1:0], $\overline{QD[1:0]}$)						
V_{OH}	Output High Voltage	TBD	V_{CC}-1.005	TBD	V	Termination 50Ω to V_{TT}
V_{OL}	Output Low Voltage	TDB	V_{CC}-1.705	TBD	V	Termination 50Ω to V_{TT}
Supply Current						
I_{EE}	Maximum Quiescent Supply Current without output termination current		TBD	TBD	mA	V_{EE} pin
I_{CCe}	Maximum Quiescent Supply Current, outputs terminated 50Ω to V_{TT}		TBD	TBD	mA	V_{CC} pins

a. AC characteristics are design targets and pending characterization.
b. Clock inputs driven by PECL compatible signals.
c. V_{PP} is the minimum differential input voltage swing required to maintain AC characteristics.
d. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.
e. I_{CC} includes current through the output resistors (all outputs terminated to V_{TT}).

Table 7: ECL DC CHARACTERISTICS (V_{EE} = –3.3V ± 5%, V_{CC} = GND, T_A = 0°C to 70°C)[a]

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Differential ECL clock inputs (ECLK, $\overline{ECLK}$ and FB_IN, $\overline{FB\_IN}$)[b]						
V_{PP}	Differential input voltage[c]	0.1		1.3	V	Differential operation
V_{CMR}	Differential cross point voltage[d]	V_{EE}+1.0		-0.3	V	Differential operation
I_{IN}	Input Current[a]			±150	µA	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$
Single-ended ECL clock inputs (TCLK, VCO_SEL, $\overline{PLL\_EN}$, MR, REF_SEL, SYNC_SEL, FSEL_FB[2:0], FSEL[3:0])						
V_{IL}	Input Voltage Low			-1.46	V	
V_{IH}	Input Voltage High	-1.14			V	
I_{IN}	Input Current[e]			±150	µA	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$
ECL clock outputs (QA[3:0], $\overline{QA[3:0]}$, QB[3:0], $\overline{QB[3:0]}$, QC[2:0], $\overline{QC[2:0]}$, QD[1:0], $\overline{QD[1:0]}$)						
V_{OH}	Output High Voltage	TBD	-1.005	TBD	V	Termination 50Ω to V_{TT}
V_{OL}	Output Low Voltage	TBD	-1.705	TBD	V	Termination 50Ω to V_{TT}
Supply current and V						
I_{EE}	Maximum Quiescent Supply Current without output termination current		TBD	TBD	mA	V_{EE} pin
I_{CCf}	Maximum Quiescent Supply Current, outputs terminated 50Ω to V_{TT}		TBD	TBD	mA	V_{CC} pins

a. DC characteristics are design targets and pending characterization.
b. Clock inputs driven by PECL compatible signals.
c. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.
d. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.
e. Input have internal pullup/pulldown resistors which affect the input current.
f. I_{CC} includes current through the output resistors (all outputs terminated to V_{TT}).

Table 8: AC CHARACTERISTICS (ECL: V_{EE} = –3.3V ± 5%, V_{CC} = GND, or PECL: V_{CC} = 3.3V ± 5%, V_{EE} = GND, T_A = 0°C to 70°C)[a b]

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{ref}	Input reference frequency ÷4 feedback ÷8 feedback ÷12 feedback ÷16 feedback ÷24 feedback ÷32 feedback ÷48 feedback ÷64 feedback ÷96 feedback ÷128 feedback Input reference frequency in PLL bypass mode[c]	200.0 100.0 66.6 50.0 33.3 25.0 16.6 12.5 8.3 6.25		400.0 200.0 133.3 100.0 66.6 50.0 33.3 25.0 16.6 12.5 TBD	MHz MHz MHz MHz MHz MHz MHz MHz MHz MHz MHz	PLL locked PLL bypass
f_{VCO}	VCO frequency range[d]	800		1600	MHz	
f_{MAX}	Output Frequency ÷4 output ÷8 output ÷12 output ÷16 output ÷24 output ÷32 output	200.0 100.0 66.6 50.0 33.3 25.0		400.0 200.0 133.3 100.0 66.6 50.0	MHz MHz MHz MHz MHz MHz	PLL locked
V_{PP}	Differential input voltage[e] (peak-to-peak)		0.3	1.3	V	
V_{CMR}	Differential input crosspoint voltage[f] PECL ECL			V_{CC}-0.3 -0.3	V	
$V_{O(P-P)}$	Differential output voltage (peak-to-peak)		0.8	TBD	V	
f_{refDC}	Reference Input Duty Cycle	40		60	%	
$t_{(\varnothing)}$	Propagation Delay (static phase offset) ECLK, $\overline{ECLK}$ to FB_IN, $\overline{FB\_IN}$ TCLK to FB_IN, $\overline{FB\_IN}$		 ±150 ±150		 ps ps	PLL locked
$t_{sk(O)}$	Output-to-output Skew[g]			150	ps	
DC	Output duty cycle	45	50	55	%	
$t_{JIT(CC)}$	Cycle-to-cycle jitter RMS (1 σ)[h]		TBD		ps	
$t_{JIT(PER)}$	Period Jitter RMS (1 σ)		TBD		ps	
$t_{JIT(\varnothing)}$	I/O Phase Jitter RMS (1 σ)		TBD		ps	
BW	PLL closed loop bandwidth[i]				kHz	
t_{LOCK}	Maximum PLL Lock Time		10		ms	
t_r, t_f	Output Rise/Fall Time	0.05		TBD	ns	20% to 80%

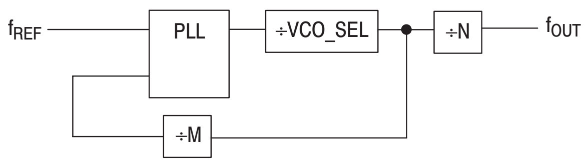
a. AC characteristics are design targets and pending characterization.
b. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
c. In bypass mode, the MPC9991 divides the input reference clock.
d. The input reference frequency must match the VCO lock range divided by the total feedback divider ratio: $f_{ref} = f_{VCO} \div (M \cdot VCO\_SEL)$.
e. V_{PP} is the minimum differential input voltage swing required to maintain AC characteristics including tpd and device-to-device skew.
f. V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} (AC) range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} (AC) or V_{PP} (AC) impacts the device propagation delay, device and part-to-part skew.
g. See application section for part-to-part skew calculation.
h. See application section for a jitter calculation for other confidence factors than 1 σ.
i. -3 dB point of PLL transfer characteristics.

APPLICATIONS INFORMATION

MPC9991 Configurations

Configuring the MPC9991 amounts to properly configuring the internal dividers to produce the desired output frequencies. The output frequency can be represented by this formula:

$$f_{OUT} = f_{REF} \cdot M \div N$$



where f_{REF} is the reference frequency of the selected input clock source (ECLK or TCLK), M is the PLL feedback divider and N is a output divider. M is configured by the FSEL_FB[2:0] and N is configured for all output banks by the FSEL[3:0] inputs.

The reference frequency f_{REF} and the selection of the feedback-divider M is limited by the specified VCO frequency range. f_{REF} and M must be configured to match the VCO frequency range of 800 to 1600 MHz in order to achieve stable PLL operation:

$$f_{VCO,MIN} \le (f_{REF} \cdot VCO\_SEL \cdot M) \le f_{VCO,MAX}$$

The PLL post-divider VCO_SEL is either a divide-by-two or a divide-by-four and can be used to situate the VCO into the specified frequency range. This divider is controlled by the VCO_SEL pin. VCO_SEL effectively extends the usable input frequency range while it has no effect on the output to reference frequency ratio.

The output frequency for each bank can be derived from the VCO frequency and output divider:

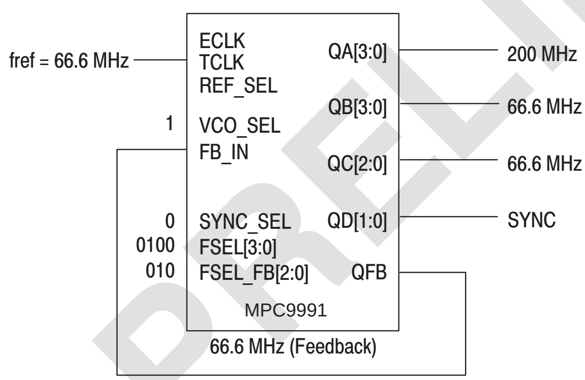
$$f_{QA[4:0]} = f_{VCO} \div (VCO\_SEL \cdot N_A)$$
$$f_{QB[4:0]} = f_{VCO} \div (VCO\_SEL \cdot N_B)$$
$$f_{QC[3:0]} = f_{VCO} \div (VCO\_SEL \cdot N_C)$$

Table 9: MPC9991 Divider

Divider	Function	VCO_SEL	Values
M	PLL feedback FSEL_FB[2:0]	÷2	4, 8, 12, 16, 32, 48, 64
		÷4	8, 16, 24, 32, 64, 96, 128
N_A	Bank A Output Divider FSEL_A	÷2	4, 8, 12, 16
		÷4	8, 16, 24, 32
N_B	Bank B Output Divider FSEL_B	÷2	4, 8, 12, 16
		÷4	8, 16, 24, 32
N_C	Bank C Output Divider FSEL_C	÷2	4, 8, 12, 16
		÷4	8, 16, 24, 32

Table 9 shows the various PLL feedback and output dividers. The output dividers for the three output banks allow the user to configure the outputs into 1:1, 2:1, 3:1, 3:2, 4:1, 4:3, 4:3:1 and 4:3:2 frequency ratios. Figure 3 and Figure 4 display example configurations for the MPC9991:

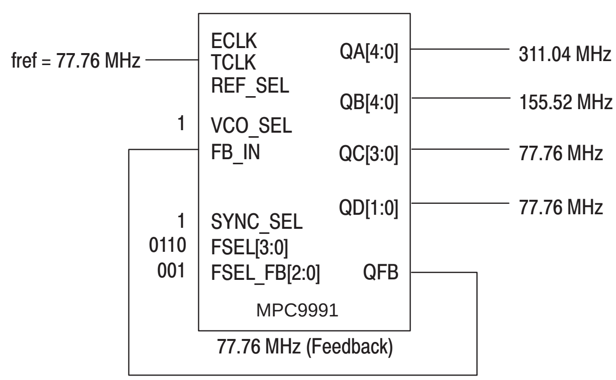
Figure 3. Example Configuration



MPC9991 example configuration (feedback of QFB = 66.6 MHz, VCO_SEL=÷4, M=6, N_A=2, N_B=6, N_C=6, f_{VCO}=1600 MHz).

Frequency range	Min	Max
Input	33.3 MHz	66.6 MHz
QA outputs	100 MHz	200 MHz
QB outputs	33.3 MHz	66.6 MHz
QC outputs	33.3 MHz	66.6 MHz

Figure 4. Example Configuration



MPC9991 example configuration (feedback of QFB = 77.76 MHz, VCO_SEL=÷2, M=8, N_A=2, N_B=4, N_C=8, f_{VCO}=1244.16 MHz).

Frequency range	Min	Max
Input	50 MHz	100 MHz
QA outputs	200 MHz	400 MHz
QB outputs	100 MHz	200 MHz
QC outputs	50 MHz	100 MHz
QD outputs	50 MHz	100 MHz

SYNC Output Description

The MPC9991 has a system synchronization pulse generator. In configurations with the output frequency relationships are not integer multiples of each other SYNC provides a signal for system synchronization purposes. The MPC9991 monitors the relationship between the A bank and the C bank of outputs. The SYNC output is asserted (logic high) depending on the placement of the clock edges of the QA and QC outputs. The QSYNC pulse width is equal to the period of the higher of the QA and QC output frequencies. Figure 5 shows various waveforms for the SYNC pulse. The SYNC signal is defined for all possible combinations of the bank A and bank C outputs. The SYNC signal is routed to the QD bank of outputs if the SYNC_SEL input is set to logic 0, otherwise the SYNC signal generation is disabled and the QD outputs match the QC output bank signals.

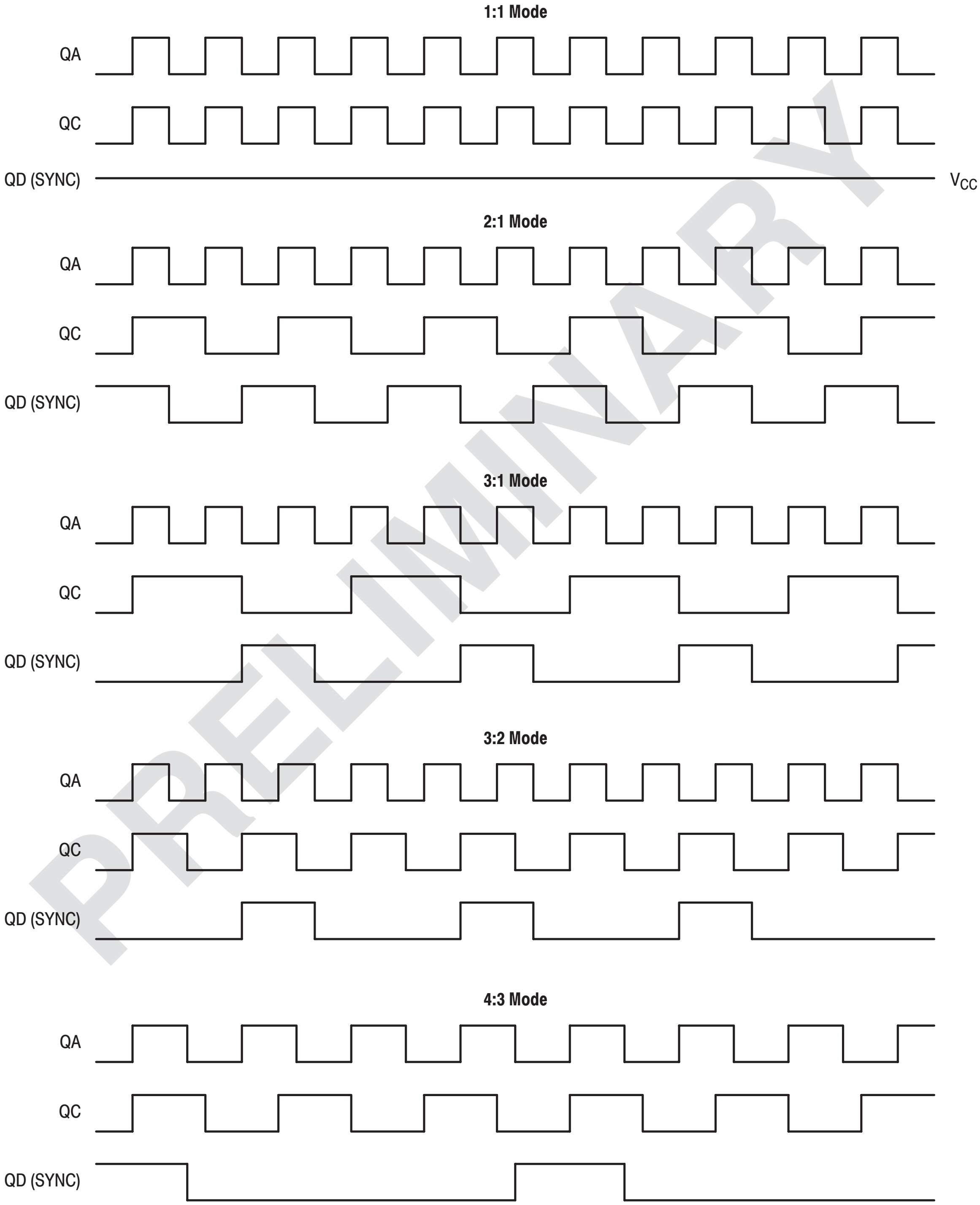


Figure 5. QSYNC Timing Diagram

Power Supply Filtering

The MPC9991 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the V_{CC_PLL} power supply impacts the device characteristics, for instance I/O jitter. The MPC9991 provides separate power supplies for the output buffers (V_{CC}) and the phase-locked loop (V_{CC_PLL}) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the V_{CCA_PLL} pin for the MPC9991. Figure 6 illustrates a typical power supply filter scheme. The MPC9991 frequency and phase stability is most susceptible to noise with spectral content in the 100kHz to 20MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor R_F. From the data sheet the I_{CC_PLL} current (the current sourced through the V_{CC_PLL} pin) is typically 3 mA (5 mA maximum), assuming that a minimum of 2.325V (V_{CC}=3.3V or V_{CC}=2.5V) must be maintained on the V_{CC_PLL} pin. The resistor R_F shown in Figure 6 "V_{CC_PLL} Power Supply Filter" must have a resistance of 9-10Ω (V_{CC}=2.5V) to meet the voltage drop criteria.

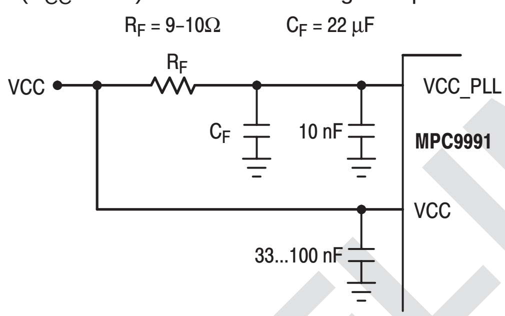


Figure 6. V_{CC_PLL} Power Supply Filter

The minimum values for R_F and the filter capacitor C_F are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 6 "V_{CC_PLL} Power Supply Filter", the filter cut-off frequency is around 3-5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9991 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Using the MPC9991 in zero–delay applications

Nested clock trees are typical applications for the MPC9991. Designs using the MPC9991 as LVCMOS PLL fanout buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fanout buffers. The external feedback option of the MPC9991 clock driver allows for its use as a zero delay buffer. One example configuration is to use a ÷4 output as a feedback to the PLL and configuring all other outputs to a divide-by-4 mode. The propagation delay through the device is virtually eliminated. The PLL aligns the feedback clock output edge with the clock input reference edge resulting a near zero delay through the device. The maximum insertion delay of the device in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset, I/O jitter (phase or long-term jitter), feedback path delay and the output-to-output skew error relative to the feedback output.

Calculation of part-to-part skew

The MPC9991 zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs of two or more MPC9991 are connected together, the maximum overall timing uncertainty from the common CCLKx input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD,\ LINE(FB)} + t_{JIT(\varnothing)} \cdot CF$$

This maximum timing uncertainty consist of 4 components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:

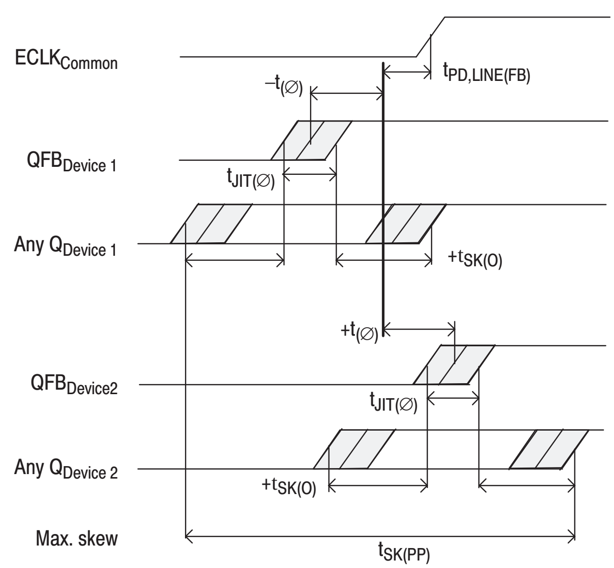


Figure 7. MPC9991 max. device-to-device skew

Due to the statistical nature of I/O jitter a RMS value (1 σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 10.

Table 10: Confidence Facter CF

CF	Probability of clock edge within the distribution
$\pm 1\sigma$	0.68268948
$\pm 2\sigma$	0.95449988
$\pm 3\sigma$	0.99730007
$\pm 4\sigma$	0.99993663
$\pm 5\sigma$	0.99999943
$\pm 6\sigma$	0.99999999

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device. In the following example calculation a I/O jitter confidence factor of 99.7% ($\pm 3\sigma$) is assumed, resulting in a worst case timing uncertainty from input to any output of -345 ps to 345 ps[1] relative to CCLK:

$$t_{SK(PP)} = [-150ps...150ps] + [-150ps...150ps] + [(15ps \cdot -3)...(15ps \cdot 3)] + t_{PD,\ LINE(FB)}$$

$$t_{SK(PP)} = [-345ps...345ps] + t_{PD,\ LINE(FB)}$$

Due to the frequency dependence of the I/O jitter, Figure 8 “Max. I/O Jitter versus frequency” can be used for a more precise timing performance analysis.

TBD
See MPC961C application section for
an example I/O jitter characteristics

Figure 8. Max. I/O Jitter versus frequency

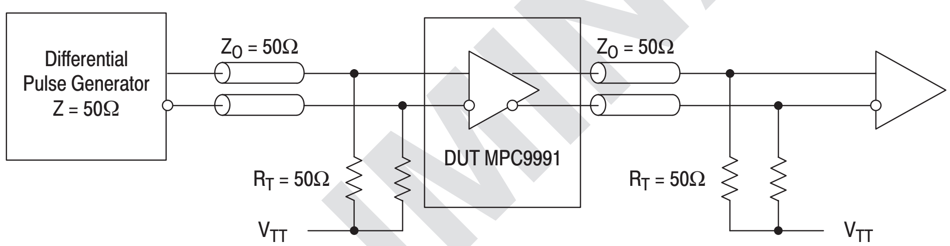


Figure 9. MPC9991 AC test reference