

### DESCRIPTION

This family is a 16M bit dynamic RAM organized 4,194,304 x 4-bit configuration with Extended Data Out mode CMOS DRAMs. Extended Data Out mode offers high speed random access of memory cells within the same row. The circuit and process design allow this device to achieve high performance and low power dissipation. Optional features are access time(60,70 or 80ns) and refresh cycle(2K Ref. or 4K Ref.) and package type(SOJ or TSOP-II) and power consumption(Normal or Low power with self refresh). Hyundai's advanced circuit design and process technology allow this device to achieve high bandwidth, low power consumption and high reliability.

### ORDERING INFORMATION

Part Number	Ref.	Power	Pkg.
HY51V17404AJ	2K		SOJ
HY51V17404ASLJ	2K	SL-part	SOJ
HY51V17404AT	2K		TSOP-II
HY51V17404ASLT	2K	SL-part	TSOP-II
HY51V16404AJ	4K		SOJ
HY51V16404ASLJ	4K	SL-part	SOJ
HY51V16404AT	4K		TSOP-II
HY51V16404ASLT	4K	SL-part	TSOP-II

\* Reverse TSOP-II packages are also available

### FEATURES

- Part Number Information

- HY51V17404A: 2K Ref.
- HY51V16404A: 4K Ref.

- Max. Active Power Dissipation

Speed	2K	4K
60	432 mW	324 mW
70	360 mW	288 mW
80	324 mW	252 mW

- Fast access time and cycle time

Speed	tRAC	tCAC	tHPC
60ns	60ns	15ns	25ns
70ns	70ns	18ns	30ns
80ns	80ns	20ns	35ns

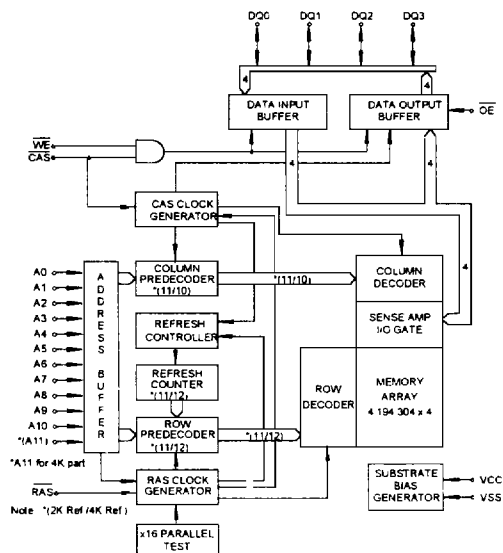
- Extended Data Out Operation
- Single power supply of 3.3V ± 0.3V
- Read-Modify-Write Capability
- Early Write or Output Enable controlled write
- LVTTTL compatible inputs and outputs
- /CAS-before-/RAS, /RAS-only, Hidden and Self Refresh Capability
- Refresh cycles

Part No.	Ref.	Normal	SL-part
HY51V17404A	2K	32ms	256ms
HY51V16404A	4K	64ms	

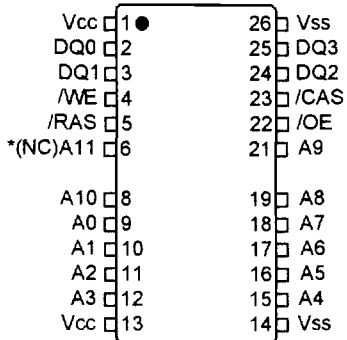
- JEDEC standard pinout

- 24/26-pin Plastic SOJ (300 mil)
- 24/26-pin Plastic TSOP-II (300mil)

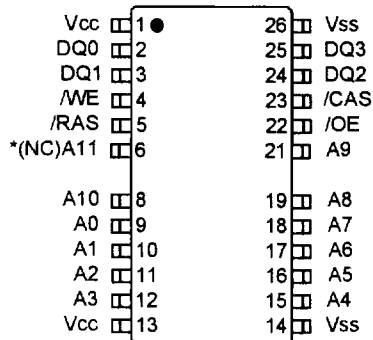
### BLOCK DIAGRAM



**PIN CONFIGURATION (Marking Side)**



24/26-pin Plastic SOJ (300mil)



24/26-pin Plastic TSOP-II (300mil)

\*(N.C) : For 2K Refresh product

**PIN DESCRIPTION**

/RAS	Row Address Strobe
/CAS	Column Address Strobe
/WE	Write Enable
/OE	Output Enable
A0-A11	Address Inputs (4K Product)
A0-A10	Address Inputs (2K Product)
DQ0-DQ3	Data Input/Output
Vcc	Power (+3.3V)
Vss	Ground
NC	No Connection

**ABSOLUTE MAXIMUM RATINGS**

SYMBOL	PARAMETER	RATING	UNIT
T <sub>A</sub>	Ambient Temperature	0 to 70	°C
T <sub>STG</sub>	Storage Temperature	-55 to 150	°C
V <sub>IN</sub> , V <sub>OUT</sub>	Voltage on Any Pin relative to V <sub>SS</sub>	-0.5 to 4.6	V
V <sub>CC</sub>	Voltage on V <sub>CC</sub> relative to V <sub>SS</sub>	-0.5 to 4.6	V
I <sub>OS</sub>	Short Circuit Output Current	50	mA
P <sub>D</sub>	Power Dissipation	1.0	W
T <sub>SOLDER</sub>	Soldering Temperature · Time	260 · 10	°C · sec

Note: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

**RECOMMENDED DC OPERATING CONDITIONS**

(T<sub>A</sub>=0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>CC</sub>	Power Supply Voltage	3.0	3.3	3.6	V
V <sub>IH</sub>	Input High Voltage	2.0	-	V <sub>CC</sub> +0.3	V
V <sub>IL</sub>	Input Low Voltage	-0.3	-	0.8	V

Note: All voltages are referenced to V<sub>SS</sub>.

**DC CHARACTERISTICS**

(T<sub>A</sub>=0°C to 70°C, V<sub>CC</sub>=3.3V ± 0.3V and V<sub>SS</sub>=0V, unless otherwise noted.)

Symbol	Parameter	Test Condition	Speed/ Power	Max. Current		UNIT
				2K Ref	4K Ref	
icc1	Operating Current	/RAS and /CAS cycling t <sub>RC</sub> =t <sub>RC</sub> (min.)	60	120	90	mA
			70	100	80	
			80	90	70	
icc2	LVTTL Standby Current	/RAS=/CAS ≥ V <sub>IH</sub> other inputs ≥ V <sub>SS</sub>	SL-part	1 1	1 1	mA
icc3	/RAS-only Refresh Current	/CAS=V <sub>IH</sub> , /RAS cycling t <sub>RC</sub> =t <sub>RC</sub> (min.)	60	120	90	mA
			70	100	80	
			80	90	70	
icc4	EDO Mode Current	/RAS=V <sub>IL</sub> , /CAS, Address cycling t <sub>HPC</sub> =t <sub>HPC</sub> (min.)	60	110	80	mA
			70	90	70	
			80	80	60	
icc5	CMOS Standby Current	/RAS = /CAS ≥ V <sub>CC</sub> -0.2V	SL-part	500	500	μA
				200	200	
icc6	/CAS-before- /RAS Refresh Current	/RAS and /CAS cycling t <sub>RC</sub> =t <sub>RC</sub> (min.)	60	120	90	mA
			70	100	80	
			80	90	70	
icc7	Battery Back-up Current (SL-part)	t <sub>RC</sub> =125 μs(2K Ref), 62.5 μs(4K Ref) /CAS = CBR cycling or 0.2V /OE & /WE=V <sub>CC</sub> - 0.2V Address =V <sub>CC</sub> -0.2V or 0.2V DQ0-DQ3 =V <sub>CC</sub> -0.2V, 0.2V or open	t <sub>RAS</sub> ≤ 300ns	300	350	μA
			t <sub>RAS</sub> ≤ 1 μs	500	600	μA
icc8	Self Refresh Current (SL-part)	/RAS & /CAS = 0.2V Other pins are same as Icc7		300	300	μA

Symbol	Parameter	Test condition	Min.	Max.	UNIT
I <sub>LI</sub>	Input Leakage current (Any Input)	V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub> + 0.3 All other pins not under test=V <sub>SS</sub>	-10	10	μA
I <sub>LO</sub>	Output Leakage current (Any Input)	V <sub>SS</sub> ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> /RAS & /CAS at V <sub>IH</sub>	-10	10	μA
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2.0mA	-	0.4	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -2.0mA	2.4	-	V

**NOTE**

1. Icc1, Icc3, Icc4 and Icc6 depend on output loading and cycle rates(t<sub>RC</sub> and t<sub>HPC</sub>).
2. Specified values are obtained with outputs unloaded.
3. Icc is specified as an average current. In Icc1, Icc3, Icc6, address can be changed only once while /RAS=V<sub>IL</sub>. In Icc4, address can be changed maximum once while /CAS=V<sub>IH</sub> within one EDO mode cycle time t<sub>HPC</sub>.
4. Only /RAS(max.) = 1 μs is applied to refresh of battery backup but t<sub>RAS</sub>(max.) = 10 μs is to applied to normal functional operation.
5. Icc5(max.) = 200 μA, Icc7 and Icc8 are applied to SL-part only.

**AC CHARACTERISTICS**

(T<sub>A</sub>=0°C to 70°C, V<sub>cc</sub>=3.3V ± 0.3V and V<sub>ss</sub>=0V, unless otherwise noted.)

#	SYMBOL	PARAMETER	HY51V17404A / HY51V16404A						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t <sub>RC</sub>	Random Read or Write Cycle Time	110	-	130	-	150	-	ns	
2	t <sub>RWC</sub>	Read-Modify-Write Cycle Time	155	-	180	-	200	-	ns	
3	t <sub>HPC</sub>	EDO Mode Cycle Time	25	-	30	-	35	-	ns	2
4	t <sub>HPRWC</sub>	EDO Mode Read-Modify-Write Cycle Time	75	-	85	-	95	-	ns	2
5	t <sub>RAC</sub>	Access Time from /RAS	-	60	-	70	-	80	ns	5,6,7
6	t <sub>CAC</sub>	Access Time from /CAS	-	15	-	18	-	20	ns	5,6
7	t <sub>AA</sub>	Access Time from Column Address	-	30	-	35	-	40	ns	5,7
8	t <sub>CPA</sub>	Access Time from Column Precharge	-	35	-	40	-	45	ns	5
9	t <sub>CLZ</sub>	/CAS to Output Low Impedance	3	-	3	-	3	-	ns	5
10	t <sub>CEZ</sub>	Out Buffer Turn-Off Delay Time from /CAS	3	15	3	18	3	20	ns	8
11	t <sub>T</sub>	Transition Time (Rise and Fall)	2	50	2	50	2	50	ns	3
12	t <sub>RP</sub>	/RAS Precharge Time	40	-	50	-	60	-	ns	
13	t <sub>RAS</sub>	/RAS Pulse Width	60	10K	70	10K	80	10K	ns	
14	t <sub>RASP</sub>	/RAS Pulse Width (EDO Mode)	60	200K	70	200K	80	200K	ns	
15	t <sub>RSH</sub>	/RAS Hold Time	15	-	18	-	20	-	ns	
16	t <sub>CSH</sub>	/CAS Hold Time	45	-	50	-	55	-	ns	
17	t <sub>CAS</sub>	/CAS Pulse Width	11	10K	14	10K	17	10K	ns	
18	t <sub>RCD</sub>	/RAS to /CAS Delay Time	20	45	20	52	20	60	ns	6
19	t <sub>RAD</sub>	/RAS to Column Address Delay Time	15	30	15	35	17	40	ns	7
20	t <sub>CRP</sub>	/CAS to /RAS Precharge Time	5	-	5	-	5	-	ns	11
21	t <sub>CP</sub>	/CAS Precharge Time	10	-	12	-	14	-	ns	
22	t <sub>ASR</sub>	Row Address Set-up Time	0	-	0	-	0	-	ns	
23	t <sub>RAH</sub>	Row Address Hold Time	10	-	10	-	12	-	ns	
24	t <sub>ASC</sub>	Column Address Set-up Time	0	-	0	-	0	-	ns	
25	t <sub>CAH</sub>	Column Address Hold Time	10	-	10	-	15	-	ns	
26	t <sub>RAL</sub>	Column Address to /RAS Lead Time	30	-	35	-	40	-	ns	
27	t <sub>RCS</sub>	Read Command Set-up Time	0	-	0	-	0	-	ns	
28	t <sub>RCH</sub>	Read Command Hold Time Referenced to /CAS	0	-	0	-	0	-	ns	9
29	t <sub>RRH</sub>	Read Command Hold Time Referenced to /RAS	0	-	0	-	0	-	ns	9
30	t <sub>WCH</sub>	Write Command Hold Time	10	-	10	-	15	-	ns	
31	t <sub>WP</sub>	Write Command Pulse Width	10	-	10	-	15	-	ns	
32	t <sub>RWL</sub>	Write Command to /RAS Lead Time	12	-	12	-	17	-	ns	
33	t <sub>CWL</sub>	Write Command to /CAS Lead Time	12	-	12	-	17	-	ns	
34	t <sub>DS</sub>	Data-In Set-up Time	0	-	0	-	0	-	ns	10
35	t <sub>DH</sub>	Data-In Hold Time	10	-	10	-	10	-	ns	10

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**AC CHARACTERISTICS**

(Continued)

#	SYMBOL	PARAMETER	HY51V17404A / HY51V16404A						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
36	tREF	Refresh Period (2048 cycles)	32	-	32	-	32	-	ms	
		Refresh Period (4096 cycles)	64	-	64	-	64	-	ms	
		Refresh Period (SL-part)	256	-	256	-	256	-	ms	
37	tWCS	Write Command Set-up Time	0	-	0	-	0	-	ns	11
38	tCWD	/CAS to /WE Delay Time	34	-	40	-	44	-	ns	11
39	tRWD	/RAS to /WE Delay Time	79	-	92	-	104	-	ns	11
40	tAWD	Column Address to /WE Delay Time	49	-	57	-	64	-	ns	11
41	tCSR	/CAS Set-up Time (CBR Cycle)	5	-	5	-	5	-	ns	
42	tCHR	/CAS Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	
43	tRPC	/RAS to /CAS Precharge Time	5	-	5	-	5	-	ns	
44	tCPT	/CAS Precharge Time (CBR Counter Test)	20	-	25	-	25	-	ns	
45	tROH	/RAS Hold Time Reference to /OE	10	-	10	-	10	-	ns	
46	tOEA	/OE Access Time	-	15	-	18	-	20	ns	
47	tOED	/OE to Data Delay Time	15	-	18	-	20	-	ns	
48	tOEZ	Output Buffer Turn Off Delay Time from /OE	3	15	3	18	3	20	ns	8
49	tOEH	/OE Command Hold Time	15	-	18	-	20	-	ns	
50	tCPWD	/WE Delay Time from /CAS Precharge	54	-	62	-	69	-	ns	11
51	tRHCP	/RAS Hold Time from /CAS Precharge	35	-	40	-	45	-	ns	
52	tWRP	/WE to /RAS Precharge Time (CBR cycle)	10	-	10	-	10	-	ns	
53	tWRH	/WE to /RAS Hold Time (CBR cycle)	10	-	10	-	10	-	ns	
54	tRASS	/RAS Pulse Width (Self Refresh)	100	-	100	-	100	-	µs	
55	tRPS	/RAS Precharge Time (Self Refresh)	110	-	130	-	150	-	ns	
56	tCHS	/CAS Hold Time (Self Refresh)	-50	-	-50	-	-50	-	ns	
57	tDOH	Output Data Hold Time	5	-	5	-	5	-	ns	
58	tREZ	Output Buffer Turn Off Delay from /RAS	3	15	3	18	3	20	ns	
59	tWEZ	Output Buffer Turn Off Delay from /WE	3	15	3	18	3	20	ns	
60	tWED	/WE to Data Delay Time	15	-	18	-	20	-	ns	
61	tOEP	/OE Precharge Time	5	-	5	-	5	-	ns	
62	tWPE	/WE Pulse Width (EDO cycle)	5	-	5	-	5	-	ns	
63	tOCH	/OE to /CAS Hold Time	5	-	5	-	5	-	ns	
64	tCHO	/CAS Hold Time to /OE	5	-	5	-	5	-	ns	

**TEST MODE**

#	SYMBOL	PARAMETER	HY51V17404A / HY51V16404A						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	:RC	Random Read or Write Cycle Time	109	-	129	-	149	-	ns	
2	:RWC	Read-Modify-Write Cycle Time	142	-	165	-	192	-	ns	
3	:HPC	EDO Mode Cycle Time	30	-	35	-	40	-	ns	2
4	:HPRWC	EDO Mode Read-Modify-Write Cycle Time	75	-	83	-	95	-	ns	2
5	:RAC	Access Time from /RAS	-	65	-	75	-	85	ns	5,6,7
6	:CAC	Access Time from /CAS	-	20	-	23	-	25	ns	5,6
7	:AA	Access Time from Column Address	-	35	-	40	-	45	ns	5,7
8	:CPA	Access Time from Column Precharge	-	40	-	45	-	50	ns	5
13	:RAS	/RAS Pulse Width	65	10K	75	10K	85	10K	ns	
14	:RASP	/RAS Pulse Width ( EDO Mode)	65	200K	75	200K	85	200K	ns	
15	:RSH	/RAS Hold Time	20	-	23	-	25	-	ns	
16	:CSH	/CAS Hold Time	50	-	55	-	60	-	ns	
17	:CAS	/CAS Pulse Width	16	10K	19	10K	22	10K	ns	
26	:RAL	Column Address to /RAS Lead Time	35	-	40	-	45	-	ns	
38	:CWD	/CAS to /WE Delay Time	39	-	45	-	49	-	ns	11
39	:RWD	/RAS to /WE Delay Time	84	-	97	-	109	-	ns	11
40	:AWD	Column Address to /WE Delay Time	54	-	62	-	69	-	ns	11
46	:OEA	/OE Access Time	-	20	-	23	-	25	ns	
47	:OED	/OE to Data Delay Time	20	-	23	-	25	-	ns	
49	:OEH	/OE Command Hold Time	20	-	23	-	25	-	ns	
50	:CPWD	/WE Delay Time from /CAS Precharge	59	-	67	-	74	-	ns	11

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In Test Mode, data are written into 16 sectors (Each is composed of 1M bits) in parallel and retrieved the same way. Column address A0 and A1 are not used. If, upon reading, 4-bit data from 4 sectors connected to one DQ pin are equal (all '1's or '0's), the DQ pin indicates a '1'. If they are not equal, the DQ pin indicates a '0'. The 4M x 4 DRAM can be tested in the same way as a 1M x 4 DRAM is tested.

/WE ( when in /CAS-before-/RAS cycle ) puts the 4Mx4 DRAM into Test Mode and a /CAS-before-/RAS or a /RAS-only refresh cycle put it back into Normal Mode. /WE (when in /CAS-before-/RAS cycle) shall be used for the refresh operation in the test mode. The Test Mode function reduces test time(1/4 in case of N test pattern).

**NOTE**

1. An initial pause of 200 μs is required after power-up followed by 8 /RAS only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CBR refresh cycles instead of 8 /RAS only refresh cycles are required.
2.  $t_{ASC} \geq t_{CP}(\text{min.})$ , assume  $t_T = 2\text{ns}$
3.  $V_{IH}(\text{min.})$  and  $V_{IL}(\text{max.})$  are reference levels for measuring timing of input signals. Transition times are measured between  $V_{IH}(\text{min.})$  and  $V_{IL}(\text{max.})$
4. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ( $T_A = 0$  to  $70^\circ\text{C}$ ) is assured.
5. Measured at  $V_{OH} = 2.0\text{V}$  and  $V_{OL} = 0.8\text{V}$  with a load equivalent to 1 TTL loads and 100pF.
6. Operation within the  $t_{RCD}(\text{max.})$  limit insures that  $t_{RAC}(\text{max.})$  can be met.  $t_{RCD}(\text{max.})$  is specified as a reference point only. If  $t_{RCD}$  is greater than the specified  $t_{RCD}(\text{max.})$  limit, then access time is controlled by  $t_{CAC}$
7. Operation within the  $t_{RCD}(\text{max.})$  limit insures that  $t_{RAC}(\text{max.})$  can be met.  $t_{RAD}(\text{max.})$  is specified as a reference point only. If  $t_{RAD}$  is greater than the specified  $t_{RAD}(\text{max.})$  limit, then access time is controlled by  $t_{AA}$
8.  $t_{CEZ}(\text{max.})$ ,  $t_{OEZ}(\text{max.})$ ,  $t_{REZ}(\text{max.})$  and  $t_{WEZ}(\text{max.})$  define the time at which the output achieves the open circuit condition and is not referred to output voltage levels.
9. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle..
10. These parameters are referred to /CAS leading edge in early write cycles and to /WE leading edge in Read-Modify-Write cycles.
11.  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$ ,  $t_{AWD}$  and  $t_{CPWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{WCS} \geq t_{WCS}(\text{min.})$ , the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle. If  $t_{CWD} \geq t_{CWD}(\text{min.})$ ,  $t_{RWD} \geq t_{RWD}(\text{min.})$  and  $t_{CPWD} \geq t_{CPWD}(\text{min.})$ , then the cycle is a Read-Modify-Write cycle and data out will contain data read from the selected cell. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
12. If /RAS goes to high before /CAS high going, the open circuit condition of the output is achieved by /CAS high going. If /CAS goes to high before /RAS high going, the open circuit condition of the output is achieved by /RAS high going.

**CAPACITANCE**

( $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$ ,  $V_{SS} = 0\text{V}$  and  $f = 1\text{MHz}$ , unless otherwise noted.)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
CIN1	Input Capacitance (A0 - A11)	-	5	pF
CIN2	Input Capacitance (/RAS, /CAS, /WE, /OE)	-	7	pF
CDQ	Data Input /Output Capacitance (DQ0 - DQ3)	-	7	pF