Advance Product Information

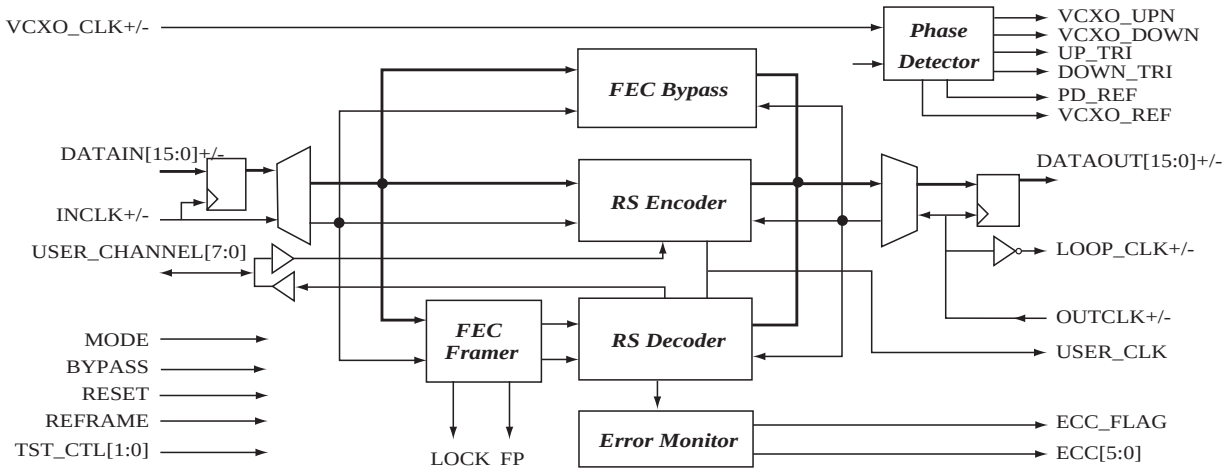
VSC9210

2.488 Gbits/sec SONET/SDH
FEC Encoder and Decoder (CODEC) Chipset

Features

- Out of Band Reed-Solomon Encoding and Decoding using a (255,241) Code
- Realizes a Decoder Output BER of 10^{-20} for Input BER of 10^{-5}
- Processes Data Rates up to 2.654Gb/s and Information Rates to 2.488Gb/s
- Device Pin Configurable as Stand-alone Encoder, Decoder, or Transparent Bypass
- Provides a Dedicated Uuser Defined Data Channel for Transparent out of Band Communications.
- Bit Rate and Protocol Independent
- Interfaces Directly with Vitesse OC-48 Rate Components
- PECL and TTL I/O
- Telecom Temperature Range: 0 - 85C
- +3.3V Power Supply
- Thermally Enhanced 208 PQFP Package
- Evaluation Platform with Dual Rate 2.488G/ 2.66G Components Available

VSC9210 Block Diagram



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Functional Overview

The device utilizes two 16 bit differential PECL I/O ports to interface with a high speed multiplexer and a demultiplexer. For the encoder, the 1:16 demultiplexer (VSC8164) is used to convert the incoming 2.5 Gbps STS-48 information to a 16 bit parallel data at 155 MHz to interface with the VSC9210. After the encoding process, the 16 bit parallel output data from the VSC9210 is obtained at 165 MHz and is converted to a 2.65 Gbps data stream using the 16:1 multiplexer (VSC8169). In the case of the decoder configuration, the demultiplexer operates on a 2.65 Gbps data stream while the multiplexer provides the 2.5 Gbps STS-48 information stream. Clock dividers are incorporated within the VSC9210 to provide control of an external PLL circuit for synthesizing the necessary reference clock for the multiplexer. In the case of the bypass mode, the input and output rates are identical and both the multiplexer and demultiplexer operate at 2.5 Gbps.

The VSC9210 can be operated at or below unencoded and encoded data rates of 155Mbs and 165Mbs respectively. The ratio of the two input clocks (INCLK and OUTCLK) must be 15/16 for encoder operation, and 16/15 for decoder operation. Management of the clocking interface allows the FEC device to operate at multiple clock rates.

An architecture that includes SONET/SDH performance monitoring is also available. The VSC8151 SONET/SDH Section Terminator device has a built in 16 bit PECL interface that allows the encoder VSC8164 demultiplexer and decoder VSC8169 multiplexer to be replaced. This enables the construction of a system that is protocol and bit rate transparent but has optional performance monitoring features for SONET/SDH data.

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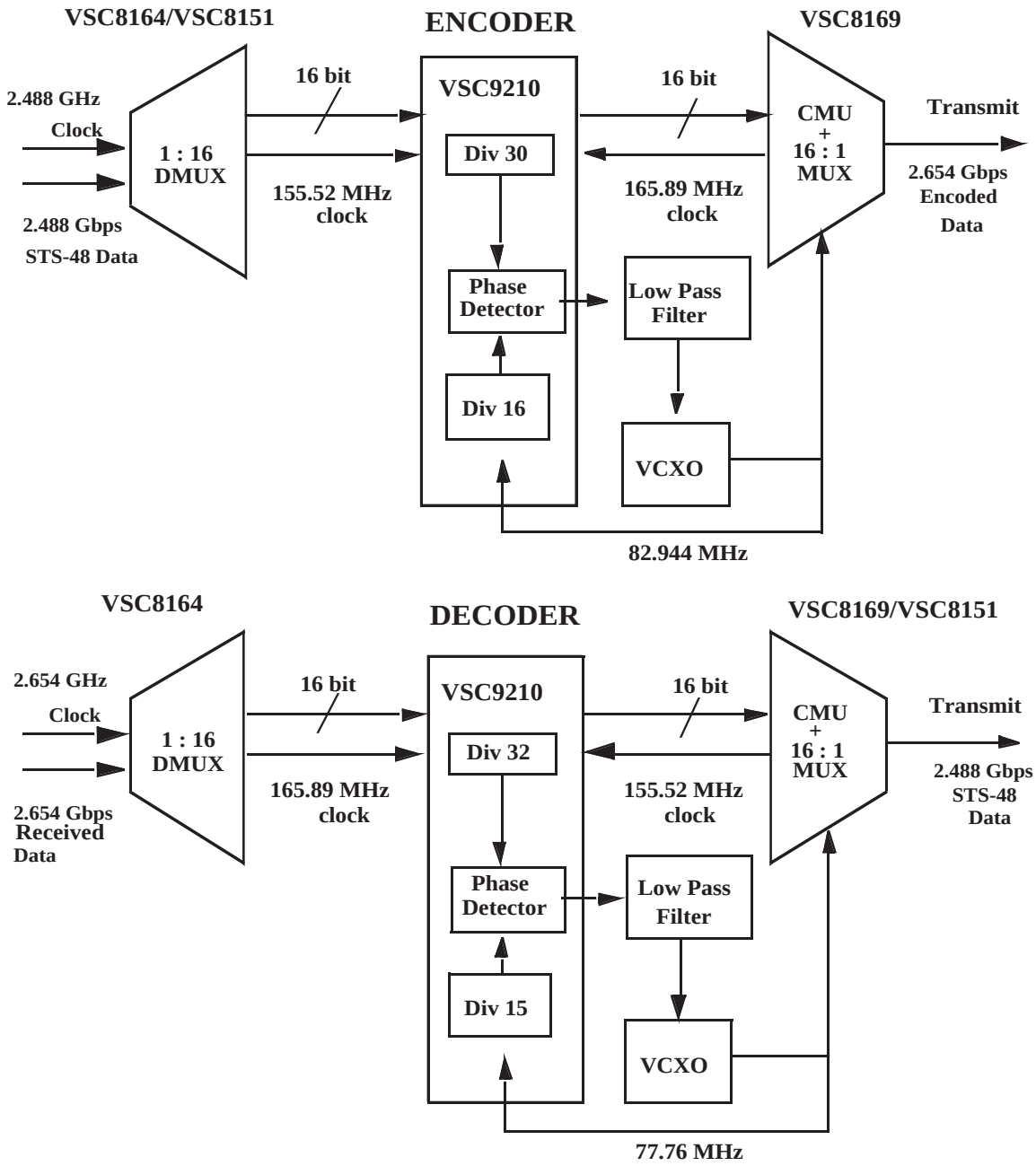
Figure 1: FEC System Diagram



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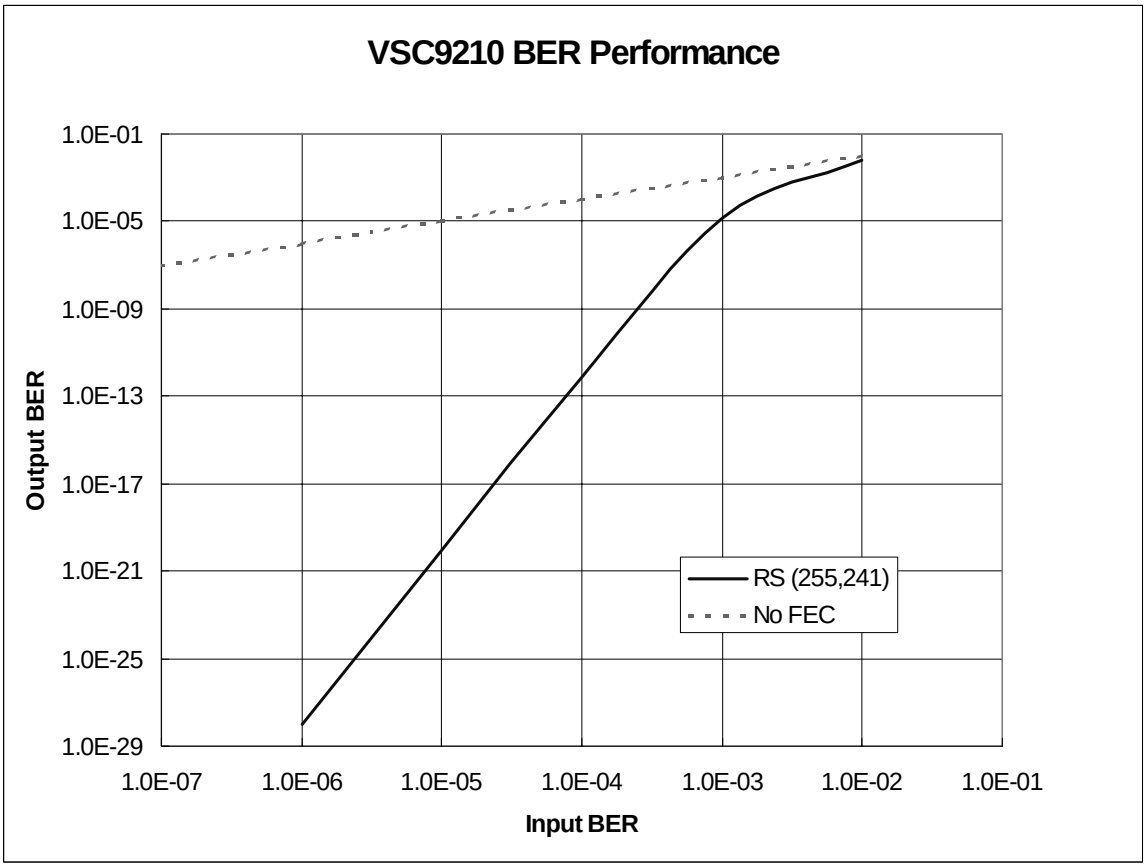
Overview of Reed-Solomon Codes

The VSC9210 CODEC device performs error correction and detection using Reed-Solomon (RS) codes. The codeword comprises *n* symbols each being *m* bits long with $n = 2^m - 1$. An (*n*,*k*) code is guaranteed to correct '*t*' symbol errors occurring anywhere in the codeword, with $2t = n-k$. RS codes can also correct burst errors. An (*n*,*k*) RS code can correct a minimum of $m(t-1) + 1$ bits of burst error within every codeword up to a maximum of *mt* bits depending on the occurrence of the burst error across the symbol boundaries. During encoding for non-systematic RS codes, a *k* symbol information vector is converted to an *n* symbol codeword by multiplying with a generator polynomial. The decoding process involves computing the error locations and the magnitude of the errors, and performing the error correction. Decreasing the ratio *k/n* improves the error correction performance of the code, but requires an increased encoded data output rate.

A symbol length of 8 (*m* = 8) results in a 255 symbol codeword that offers efficient error correction performance. The (255,241) code can correct 7 symbol errors and can handle a maximum burst error of 49 - 56 bits within each codeword as detailed above. For an input BER of 10^{-5} the output BER is 10^{-20}.

Figure 2: Theoretical Output BER versus Input BER for the VSC9210



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Signal Definitions

Signal	*Name*	*I/O*	*Freq/ Type*	*Description*
DATAIN[15:0] +/-	Parallel Receive Data.	I	155/166Mbs PECL	This parallel data bus receives the incoming STS-48 at 155MHz (or Encoded data at 166 MHz). DATAIN[15] is the most significant bit and DATAIN[0] is the least significat bit. DATAIN[15] corresponds to the first arriving bit on the serial data stream. DATAIN[15:0] is sampled on the rising edge of INCLK.
INCLK +/-	Parallel Receive Data Clock.	I	155/166MHz PECL	This clock reference is used to capture the Parallel Receive Data on the rising edge. The clock frequency is 155.52MHz relating to STS-48 for Encoder operation; 165.888MHz for Decoder operation (16/15 ratio).
DATAOUT[15:0] +/-	Parallel Transmit Data	O	166/155 Mbs PECL	This parallel data bus outputs the Encoded Data at 166MHz (or Decoded STS-48 data at 155MHz). DATAOUT[15] is the most significant bit and DATAOUT[0] is the least significat bit. DATAOUT[15] corresponds to the first transmitted bit on the serial data stream.
OUTCLK +/-	Parallel Transmit Data Clock.	I	166/155MHz PECL	This clock reference is used to output the Parallel Transmit Data on the falling edge after Encode or Decode operation is complete. The clock frequency is 166.888MHz for Encoder operation; 155.52MHz relating to STS-48 for Decoder operation (15/16 ratio).
LOOP_CLK +/-	Parallel Transmit Data Loopback Clock.	O	166/155MHz PECL	This clock is used by the receiving device to capture DATAOUT[15:0] on the rising edge. It is an inverted version of the received OUTCLK input signal.
MODE	Mode Control	I	STATIC TTL	Static control pin to set device to Encoder or Decoder operation (when not in Bypass mode; BYPASS = 0). MODE = 0 for Encoder, MODE = 1 for Decoder. Signal has internal pulldown.
BYPASS	FEC Bypass Control	I	STATIC TTL	Active high signal to disable FEC Encode/Decode operation. INCLK and OUTCLK ***must*** be same rate (155.52 MHz). Signal has internal pulldown.

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Signal	*Name*	*I/O*	*Freq/ Type*	*Description*
RESET	Reset	I	TTL	Active high asynchronous reset signal used during manufacturing. Not required for system use. Schmidt trigger input with internal pulldown.
REFRAME	FEC Re-Frame Control	I	TTL	Active high asynchronous control to force a new FEC Frame search. Intended for testing only, not required for system operation. Schmidt trigger input with internal pulldown.
SYNC_INHIBIT	FIFO Self-Synchronize Inhibit	I	STATIC TTL	Not required for STS-48 system use. Signal has internal pulldown.
TEST_CTL[1:0]	Manufacturing Test Control	I	STATIC TTL	Allows USER_CHANNEL[7:0] to be used as a test port for manufacturing tests. For user operation these ***must*** be set to" 00". Signals have internal pulldown.
USER_CHANNEL[7:0]	User Data Channel	I/O	2mA TTL	Bidirectional User Data Channel: input for Encoder, output for Decoder. Input is captured relative to rising edge of USER_CLK in Encoder mode. Output should be captured on rising edge of USER_CLK when in Decoder mode; data is valid when ECC_FLAG is low. Signals are open drain output and require external pullup resistors of approximately 10K to V_{DD}.
ECC[5:0]	Error Correction Count	O	2mA TTL	Provides count of corrected errors in previous FEC Codeword (2048 bits). Data is to be captured with USER_CLK. Data is valid only when ECC_FLAG is low, otherwise data output is $3F_H$.
ECC_FLAG	Error Correction Count Flag	O	2mA TTL	Active high signal indicating that the previous Codeword had an uncorrectable quantity of errors; greater than 7 symbol errors. When high, ECC[5:0] and USER_CHANNEL[7:0] will be invalid.
FP	FEC Frame Pulse	O	4mA TTL	Active high frame signal that occurs every Codeword (1.296 MHz) when FEC Framer is in lock. When Framer is in lock but verifying LOCK status is correct, FP signals are not presented. Pulse width is approximately eight INCLK cycles.
LOCK	FEC Framer Lock Status	O	2mA TTL	Active high signal indicating FEC Framing is in lock.

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Signal	*Name*	*I/O*	*Freq/ Type*	*Description*
USER_CLK	User Data Channel Clock	O	4mA TTL	Clock used for USER_CHANNEL, ECC[5:0], ECC_FLAG, FP, and LOCK access.
VCXO_UPN/_DOWNN	Phase Detector Error	O	8mA	Active low error signals from the internal Phase Detector to be used by an external summing and integrating loop filter to drive a VCXO in the PLL circuit. Signals are open-drain and require external pullup resistors.
UP_TRI/DOWN_TRI	Tri-state Phase Detector Error	O	4mA TTL	Error signals from internal Phase Detector that are to be tied together to create a single error signal for an external integrating loop filter to drive a VCXO in the PLL circuit. Signals are Tri-state when no phase error is present.
PD_REF/PD_VCXO	External Phase Detector Scaled Clocks	O	5.184MHz 2mA TTL	PD_REF is the scaled input clock (INCLK) and PD_VCXO is the scaled vcxo clock (VCXO_CLK) that can be used by an external phase detector circuit if desired.
VCXO_CLK +/-	VCXO Input Clock	I	78/83MHz PECL	Input clock from external VCXO in PLL circuit. Signal is scaled to 5.184 MHz to drive internal phase detectors and PD_VCXO.

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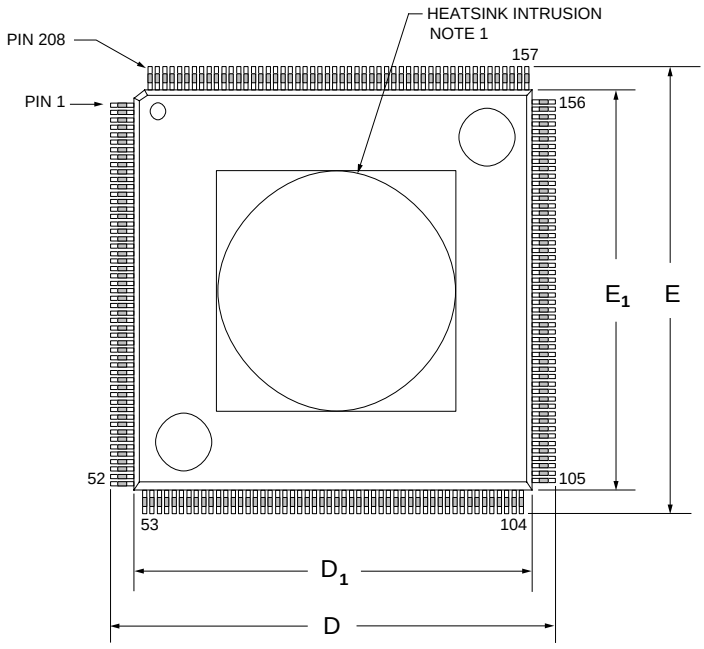
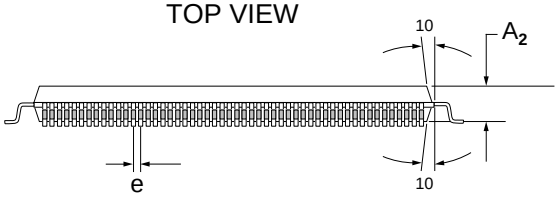
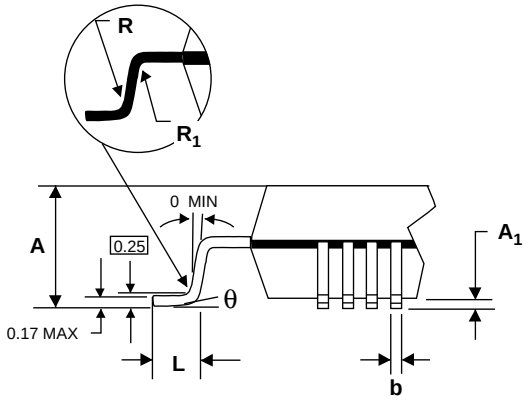
Package Information



TOP VIEW





Key	*mm*	*Tolerance*
A	4.10	MAX
A1	0.50	MAX
A2	3.49	±.10
D	30.60	±.20
D1	28.00	±.10
E	30.60	±.20
E1	28.00	±.10
L	.88	+.15/-.10
e	.50	BASIC
b	.22	±.05
q	0°-7°	
R	.15	TYP
R1	.25	MAX

NOTES:
1) 0.0127 Maximum
20.32 +/- 0.50 DIA.
Package #: 101-228-6
Issue #:

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