LM5111 Dual 5A Compound Gate Driver

Check for Samples: LM5111

FEATURES

- **Independently Drives Two N-Channel MOSFETs**
- **Compound CMOS and Bipolar Outputs Reduce Output Current Variation**
- **5A Sink/3A Source Current Capability**
- **Two Channels can be Connected in Parallel to Double the Drive Current**
- **Independent Inputs (TTL Compatible)**
- **Fast Propagation Times (25 ns Typical)**
- **Fast Rise and Fall Times (14 ns/12 ns Rise/Fall with 2 nF Load)**
- **Available in Dual Non-Inverting, Dual Inverting and Combination Configurations**
- **Supply Rail Under-Voltage Lockout Protection (UVLO)**
- **LM5111-4 UVLO Configured to Drive PFET through OUT_A and NFET through OUT_B**
- **Pin Compatible with Industry Standard Gate Drivers**

DESCRIPTION

The LM5111 Dual Gate Driver replaces industry standard gate drivers with improved peak output current and efficiency. Each “compound” output driver stage includes MOS and bipolar transistors operating in parallel that together sink more than 5A peak from capacitive loads. Combining the unique characteristics of MOS and bipolar devices reduces drive current variation with voltage and temperature. Under-voltage lockout protection is also provided. The drivers can be operated in parallel with inputs and outputs connected to double the drive current capability. This device is available in the SOIC package or the thermally enhanced VSSOP package.

TYPICAL APPLICATIONS

- **Synchronous Rectifier Gate Drivers**
- **Switch-mode Power Supply Gate Driver**
- **Solenoid and Motor Drivers**

PACKAGES

- **SOIC-8**
- **Thermally Enhanced VSSOP**

Block Diagram

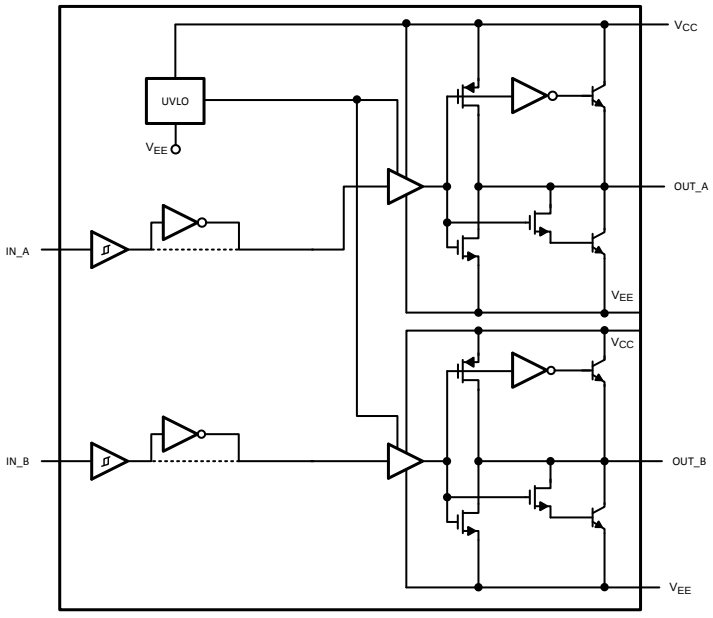


Figure 1. Block Diagram of LM5111

Connection Diagram

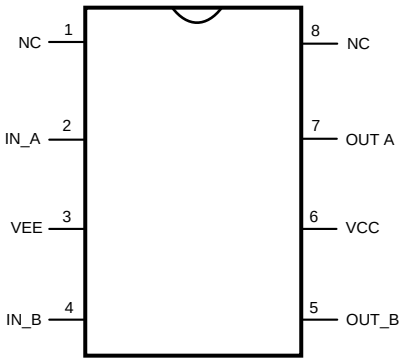


Figure 2. 8-Lead SOIC or VSSOP

PIN DESCRIPTIONS

Pin	Name	Description	Application Information
1	NC	No Connect	
2	IN_A	'A' side control input	TTL compatible thresholds.
3	VEE	Ground reference for both inputs and outputs	Connect to power ground.
4	IN_B	'B' side control input	TTL compatible thresholds.
5	OUT_B	Output for the 'B' side driver.	Voltage swing of this output is from VCC to VEE. The output stage is capable of sourcing 3A and sinking 5A.
6	VCC	Positive output supply	Locally decouple to VEE.
7	OUT_A.	Output for the 'A' side driver.	Voltage swing of this output is from VCC to VEE. The output stage is capable of sourcing 3A and sinking 5A.
8	NC	No Connect	
	EP (VSSOP Package)		It is recommended that the exposed pad on the bottom of the package be soldered to ground plane on the PC board to aid thermal dissipation.

Configuration Table

Part Number	"A" Output Configuration	"B" Output Configuration	Package
LM5111-1M/-1MX/-1MY/-1MYX	Non-Inverting (Low in UVLO)	Non-Inverting (Low in UVLO)	SOIC, VSSOP
LM5111-2M/-2MX/-2MY/-2MYX	Inverting (Low in UVLO)	Inverting (Low in UVLO)	SOIC, VSSOP
LM5111-3M/-3MX/-3MY/-3MYX	Inverting (Low in UVLO)	Non-Inverting (Low in UVLO)	SOIC, VSSOP
LM5111-4M/-4MX/-4MY/-4MYX	Inverting (High in UVLO)	Non-Inverting (Low in UVLO)	SOIC, VSSOP

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

V_{CC} to V_{EE}	−0.3V to 15V
IN to V_{EE}	−0.3V to 15V
Storage Temperature Range, (T_{STG})	−55°C to +150°C
Maximum Junction Temperature, (T_J(max))	+150°C
Operating Junction Temperature	+125°C
ESD Rating	2kV

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For guaranteed specifications and test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

Electrical Characteristics

T_J = −40°C to +125°C, V_{CC} = 12V, V_{EE} = 0V, No Load on OUT_A or OUT_B, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	V_{CC} Operating Range	V_{CC}−V_{EE}	3.5		14	V
V_{CCR}	V_{CC} Under Voltage Lockout (rising)	V_{CC}−V_{EE}	2.3	2.9	3.5	V
V_{CCH}	V_{CC} Under Voltage Lockout Hysteresis			230		mV
I_{CC}	V_{CC} Supply Current (I_{CC})	IN_A = IN_B = 0V (5111-1)		1	2	mA
		IN_A = IN_B = V_{CC} (5111-2)		1	2	
		IN_A = V_{CC}, IN_B = 0V (5111-3)		1	2	
CONTROL INPUTS						
V_{IH}	Logic High		2.2			V
V_{IL}	Logic Low				0.8	V
V_{thH}	High Threshold		1.3	1.75	2.2	V
V_{thL}	Low Threshold		0.8	1.35	2.0	V
HYS	Input Hysteresis			400		mV
I_{IL}	Input Current Low	IN_A=IN_B=V_{CC} (5111-1-2-3)	−1	0.1	1	µA
I_{IH}	Input Current High	IN_B=V_{CC} (5111-3)	10	18	25	
		IN_A=IN_B=V_{CC} (5111-2)	−1	0.1	1	
		IN_A=IN_B=V_{CC} (5111-1)	10	18	25	
		IN_A=V_{CC} (5111-3)	-1	0.1	1	
OUTPUT DRIVERS						
R_{OH}	Output Resistance High	I_{OUT} = −10 mA(1)		30	50	Ω
R_{OL}	Output Resistance Low	I_{OUT} = + 10 mA(1)		1.4	2.5	Ω
I_{Source}	Peak Source Current	OUTA/OUTB = V_{CC}/2, 200 ns Pulsed Current		3		A
I_{Sink}	Peak Sink Current	OUTA/OUTB = V_{CC}/2, 200 ns Pulsed Current		5		A
SWITCHING CHARACTERISTICS						
td1	Propagation Delay Time Low to High, IN rising (IN to OUT)	C_{LOAD} = 2 nF See Figure 3 and Figure 4		25	40	ns
td2	Propagation Delay Time High to Low, IN falling (IN to OUT)	C_{LOAD} = 2 nF See Figure 3 and Figure 4		25	40	ns
t_r	Rise Time	C_{LOAD} = 2 nF See Figure 3 and Figure 4		14	25	ns
t_f	Fall Time	C_{LOAD} = 2 nF See Figure 3 and Figure 4		12	25	ns
LATCHUP PROTECTION						
	AEC - Q100, Method 004	T_J = 150°C		500		mA
THERMAL RESISTANCE						
θ_{JA}	Junction to Ambient, 0 LFPM Air Flow	SOIC Package VSSOP Package		170 60		°C/W
θ_{JC}	Junction to Case	SOIC Package VSSOP Package		70 4.7		°C/W

(1) The output resistance specification applies to the MOS device only. The total output current capability is the sum of the MOS and Bipolar devices.

Timing Waveforms

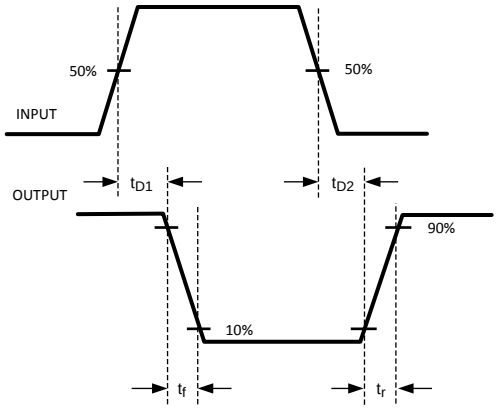


Figure 3. Inverting

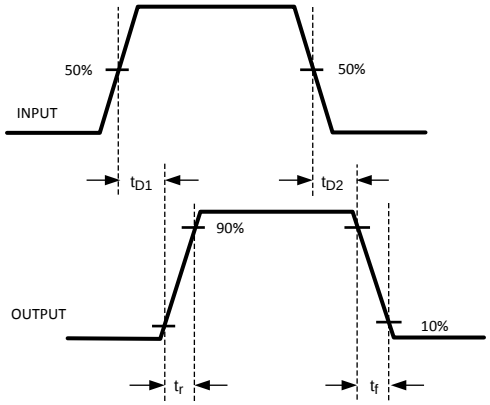


Figure 4. Non-Inverting

Typical Performance Characteristics

Supply Current vs Frequency

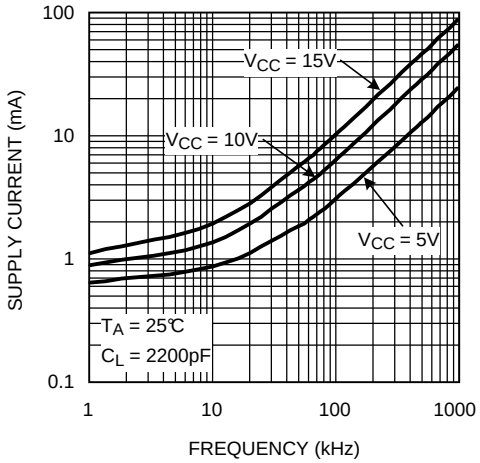


Figure 5.

Supply Current vs Capacitive Load

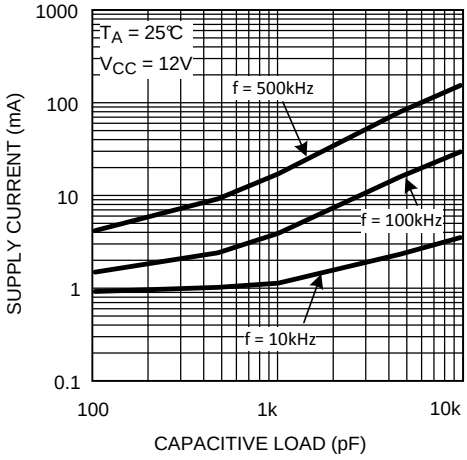


Figure 6.

Rise and Fall Time vs Supply Voltage

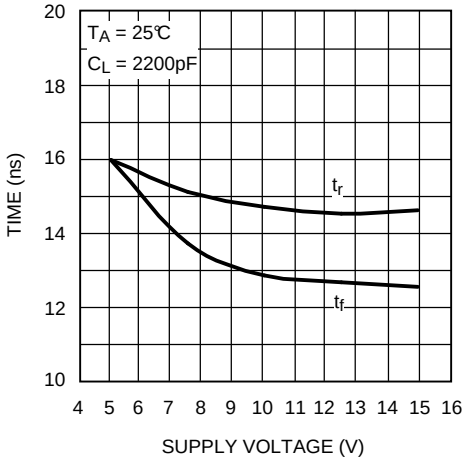


Figure 7.

Rise and Fall Time vs Temperature

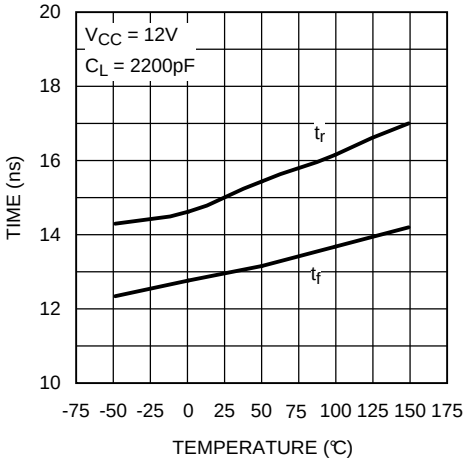


Figure 8.

Rise and Fall Time vs Capacitive Load

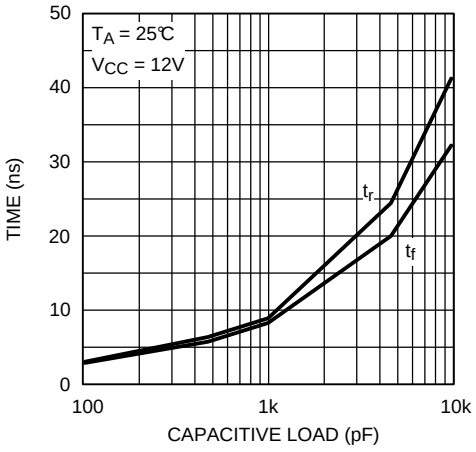


Figure 9.

Delay Time vs Supply Voltage

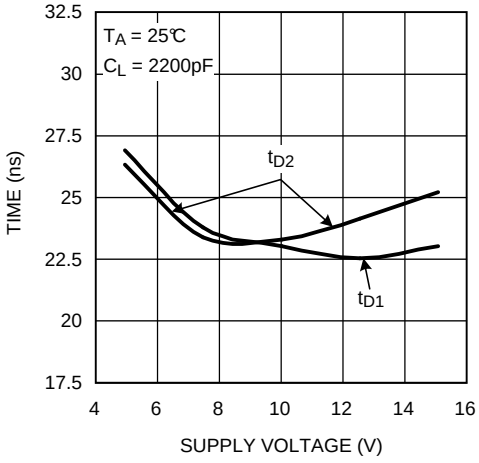


Figure 10.

Typical Performance Characteristics (continued)

Delay Time vs Temperature

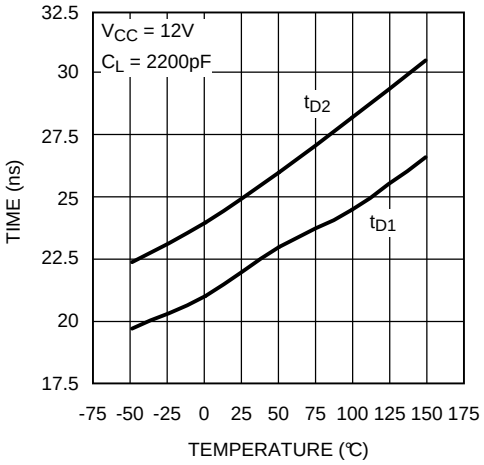


Figure 11.

RDSON vs Supply Voltage

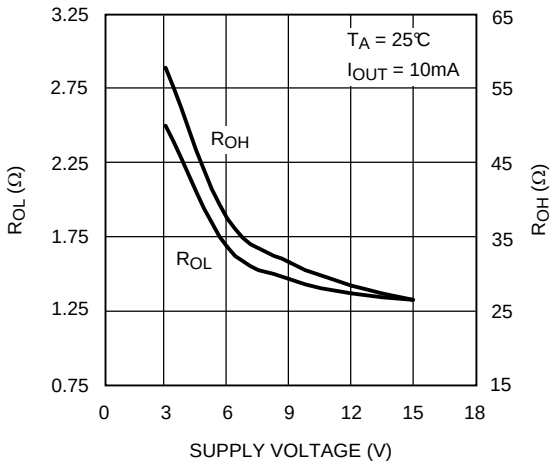


Figure 12.

UVLO Thresholds and Hysteresis vs Temperature

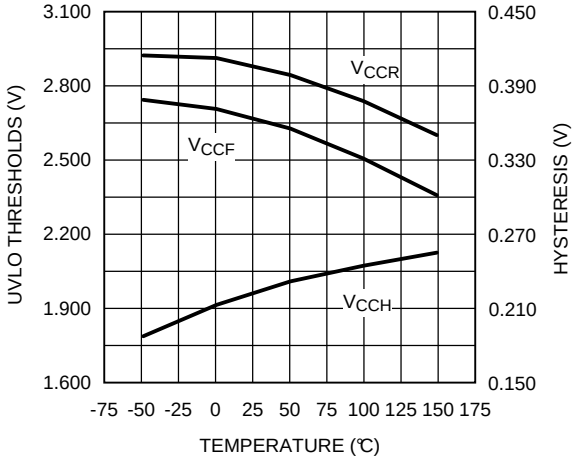


Figure 13.

Detailed Operating Description

LM5111 dual gate driver consists of two independent and identical driver channels with TTL compatible logic inputs and high current totem-pole outputs that source or sink current to drive MOSFET gates. The driver output consist of a compound structure with MOS and bipolar transistor operating in parallel to optimize current capability over a wide output voltage and operating temperature range. The bipolar device provides high peak current at the critical threshold region of the MOSFET VGS while the MOS devices provide rail-to-rail output swing. The totem pole output drives the MOSFET gate between the gate drive supply voltage V_{CC} and the power ground potential at the V_{EE} pin.

The control inputs of the drivers are high impedance CMOS buffers with TTL compatible threshold voltages. The LM5111 pinout was designed for compatibility with industry standard gate drivers in single supply gate driver applications.

The input stage of each driver should be driven by a signal with a short rise and fall time. Slow rising and falling input signals, although not harmful to the driver, may result in the output switching repeatedly at a high frequency.

The two driver channels of the LM5111 are designed as identical cells. Transistor matching inherent to integrated circuit manufacturing ensures that the AC and DC peformance of the channels are nearly identical. Closely matched propagation delays allow the dual driver to be operated as a single with inputs and output pins connected. The drive current capability in parallel operation is precisely 2X the drive of an individual channel. Small differences in switching speed between the driver channels will produce a transient current (shoot-through) in the output stage when two output pins are connected to drive a single load. Differences in input thresholds between the driver channels will also produce a transient current (shoot-through) in the output stage. Fast transition input signals are especially important while operating in a parallel configuration. The efficiency loss for parallel operation has been characterized at various loads, supply voltages and operating frequencies. The power dissipation in the LM5111 increases be less than 1% relative to the dual driver configuration when operated as a single driver with inputs/ outputs connected.

An Under Voltage Lock Out (UVLO) circuit is included in the LM5111, which senses the voltage difference between V_{CC} and the chip ground pin, V_{EE}. When the V_{CC} to V_{EE} voltage difference falls below 2.8V both driver channels are disabled. The UVLO hysteresis prevents chattering during brown-out conditions and the driver will resume normal operation when the V_{CC} to V_{EE} differential voltage exceeds approximately 3.0V.

The LM5111-1, -2 and -3 devices hold both outputs in the low state in the under-voltage lockout (UVLO) condition. The LM5111-4 is distinguished from the LM5111-3 by the active high output state of OUT_A during UVLO. When VCC is less than the UVLO threshold voltage, OUT_A of the LM5111-4 will be locked in the high state while OUT_B will be disabled in the low state. This configuration allows the LM5111-4 to drive a PFET through OUT_A and an NFET through OUT_B with both FETs safely turned off during UVLO.

The LM5111 is available in dual non-inverting (-1), dual Inverting (-2) and the combination inverting plus non-inverting (-3, -4) configurations. All configurations are offered in the SOIC and VSSOP plastic packages.

Layout Considerations

Attention must be given to board layout when using LM5111. Some important considerations include:

1. A Low ESR/ESL capacitor must be connected close to the IC and between the V_{CC} and V_{EE} pins to support high peak currents being drawn from V_{CC} during turn-on of the MOSFET.
2. Proper grounding is crucial. The drivers need a very low impedance path for current return to ground avoiding inductive loops. The two paths for returning current to ground are a) between LM5111 V_{EE} pin and the ground of the circuit that controls the driver inputs, b) between LM5111 V_{EE} pin and the source of the power MOSFET being driven. All these paths should be as short as possible to reduce inductance and be as wide as possible to reduce resistance. All these ground paths should be kept distinctly separate to avoid coupling between the high current output paths and the logic signals that drive the LM5111. A good method is to dedicate one copper plane in a multi-layered PCB to provide a common ground surface.
3. With the rise and fall times in the range of 10 ns to 30 ns, care is required to minimize the lengths of current carrying conductors to reduce their inductance and EMI from the high di/dt transients generated by the LM5111.
4. The LM5111 footprint is compatible with other industry standard drivers including the TC4426/27/28 and UCC27323/4/5.
5. If either channel is not being used, the respective input pin (IN_A or IN_B) should be connected to either V_{EE} or V_{CC} to avoid spurious output signals.

Thermal Performance

INTRODUCTION

The primary goal of thermal management is to maintain the integrated circuit (IC) junction temperature (T_J) below a specified maximum operating temperature to ensure reliability. It is essential to estimate the maximum T_J of IC components in worst case operating conditions. The junction temperature is estimated based on the power dissipated in the IC and the junction to ambient thermal resistance θ_{JA} for the IC package in the application board and environment. The θ_{JA} is not a given constant for the package and depends on the printed circuit board design and the operating environment.

DRIVE POWER REQUIREMENT CALCULATIONS IN LM5111

The LM5111 dual low side MOSFET driver is capable of sourcing/sinking 3A/5A peak currents for short intervals to drive a MOSFET without exceeding package power dissipation limits. High peak currents are required to switch the MOSFET gate very quickly for operation at high frequencies.

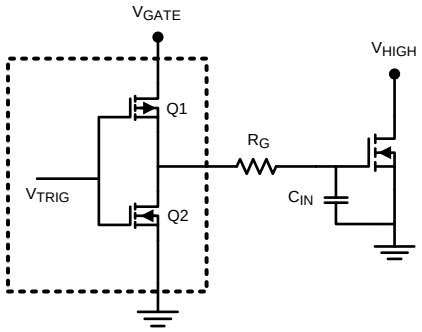


Figure 14.

The schematic above shows a conceptual diagram of the LM5111 output and MOSFET load. Q1 and Q2 are the switches within the gate driver. R_G is the gate resistance of the external MOSFET, and C_{IN} is the equivalent gate capacitance of the MOSFET. The gate resistance Rg is usually very small and losses in it can be neglected. The equivalent gate capacitance is a difficult parameter to measure since it is the combination of C_{GS} (gate to source capacitance) and C_{GD} (gate to drain capacitance). Both of these MOSFET capacitances are not constants and vary with the gate and drain voltage. The better way of quantifying gate capacitance is the total gate charge Q_G in coloumbs. Q_G combines the charge required by C_{GS} and C_{GD} for a given gate drive voltage V_{GATE}.

Assuming negligible gate resistance, the total power dissipated in the MOSFET driver due to gate charge is approximated by

$$P_{DRIVER} = V_{GATE} \times Q_G \times F_{SW}$$

where

- F_{SW} = switching frequency of the MOSFET (1)

For example, consider the MOSFET MTD6N15 whose gate charge specified as 30 nC for V_{GATE} = 12V.

The power dissipation in the driver due to charging and discharging of MOSFET gate capacitances at switching frequency of 300 kHz and V_{GATE} of 12V is equal to

$$P_{DRIVER} = 12V \times 30\ nC \times 300\ kHz = 0.108W. \quad (2)$$

If both channels of the LM5111 are operating at equal frequency with equivalent loads, the total losses will be twice as this value which is 0.216W.

In addition to the above gate charge power dissipation, - transient power is dissipated in the driver during output transitions. When either output of the LM5111 changes state, current will flow from V_{CC} to V_{EE} for a very brief interval of time through the output totem-pole N and P channel MOSFETs. The final component of power dissipation in the driver is the power associated with the quiescent bias current consumed by the driver input stage and Under-voltage lockout sections.

Characterization of the LM5111 provides accurate estimates of the transient and quiescent power dissipation components. At 300 kHz switching frequency and 30 nC load used in the example, the transient power will be 8 mW. The 1 mA nominal quiescent current and 12V V_{GATE} supply produce a 12 mW typical quiescent power.

Therefore the total power dissipation

$$P_D = 0.216 + 0.008 + 0.012 = 0.236W. \quad (3)$$

We know that the junction temperature is given by

$$T_J = P_D \times \theta_{JA} + T_A \quad (4)$$

Or the rise in temperature is given by

$$T_{RISE} = T_J - T_A = P_D \times \theta_{JA} \quad (5)$$

For SOIC package, θ_{JA} is estimated as 170°C/W for the conditions of natural convection. For VSSOP, θ_{JA} is typically 60°C/W.

Therefore for SOIC T_{RISE} is equal to

$$T_{RISE} = 0.236 \times 170 = 40.1°C \quad (6)$$

CONTINUOUS CURRENT RATING OF LM5111

The LM5111 can deliver pulsed source/sink currents of 3A and 5A to capacitive loads. In applications requiring continuous load current (resistive or inductive loads), package power dissipation, limits the LM5111 current capability far below the 5A sink/3A source capability. Rated continuous current can be estimated both when sourcing current to or sinking current from the load. For example when sinking, the maximum sink current can be calculated as:

$$I_{SINK}(MAX) := \sqrt{\frac{T_J(MAX) - T_A}{\theta_{JA} \cdot R_{DS}(ON)}}$$

where

- R_{DS}(on) is the on resistance of lower MOSFET in the output stage of LM5111 (7)

Consider T_J(max) of 125°C and θ_{JA} of 170°C/W for an SO-8 package under the condition of natural convection and no air flow. If the ambient temperature (T_A) is 60°C, and the R_{DS}(on) of the LM5111 output at T_J(max) is 2.5Ω, this equation yields I_{SINK}(max) of 391mA which is much smaller than 5A peak pulsed currents.

Similarly, the maximum continuous source current can be calculated as

$$I_{SOURCE}(MAX) := \frac{T_J(MAX) - T_A}{\theta_{JA} \cdot V_{DIODE}}$$

where

- V_{DIODE} is the voltage drop across hybrid output stage which varies over temperature and can be assumed to be about 1.1V at T_J(max) of 125°C (8)

Assuming the same parameters as above, this equation yields I_{SOURCE}(max) of 347mA.

REVISION HISTORY

Changes from Revision F (March 2013) to Revision G	Page
• Changed layout of National Data Sheet to TI format	10

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5111-1M/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	5111 -1M	Samples
LM5111-1MX	NRND	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 125	5111 -1M	
LM5111-1MX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	5111 -1M	Samples
LM5111-1MY/NOPB	ACTIVE	MSOP-PowerPAD	DGN	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		SJKB	Samples
LM5111-1MYX/NOPB	ACTIVE	MSOP-PowerPAD	DGN	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		SJKB	Samples
LM5111-2M/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	5111 -2M	Samples
LM5111-2MX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	5111 -2M	Samples
LM5111-2MY/NOPB	ACTIVE	MSOP-PowerPAD	DGN	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		SJLB	Samples
LM5111-2MYX/NOPB	ACTIVE	MSOP-PowerPAD	DGN	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		SJLB	Samples
LM5111-3M	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 125	5111 -3M	
LM5111-3M/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	5111 -3M	Samples
LM5111-3MX	NRND	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 125	5111 -3M	
LM5111-3MX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	5111 -3M	Samples
LM5111-3MY/NOPB	ACTIVE	MSOP-PowerPAD	DGN	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		SJNB	Samples
LM5111-4M/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	SN | CU SN	Level-1-260C-UNLIM		5111 -4M	Samples
LM5111-4MX/NOPB	ACTIVE	SOIC	D	8		TBD	Call TI	Call TI		5111 -4M	Samples
LM5111-4MY/NOPB	ACTIVE	MSOP-PowerPAD	DGN	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		SSYB	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5111-4MYX/NOPB	ACTIVE	MSOP-PowerPAD	DGN	8		TBD	Call TI	Call TI		SSYB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

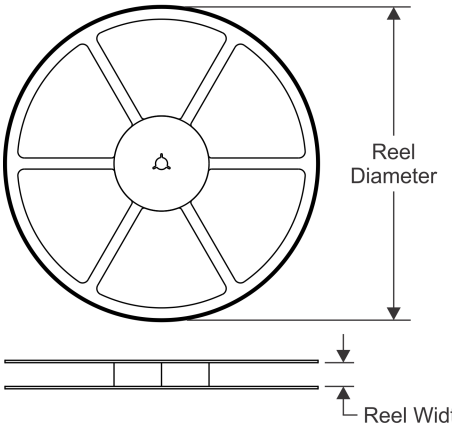
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

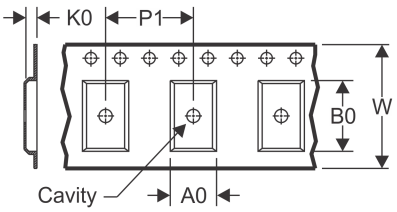
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

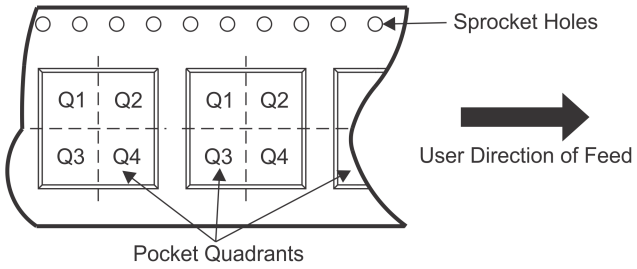


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

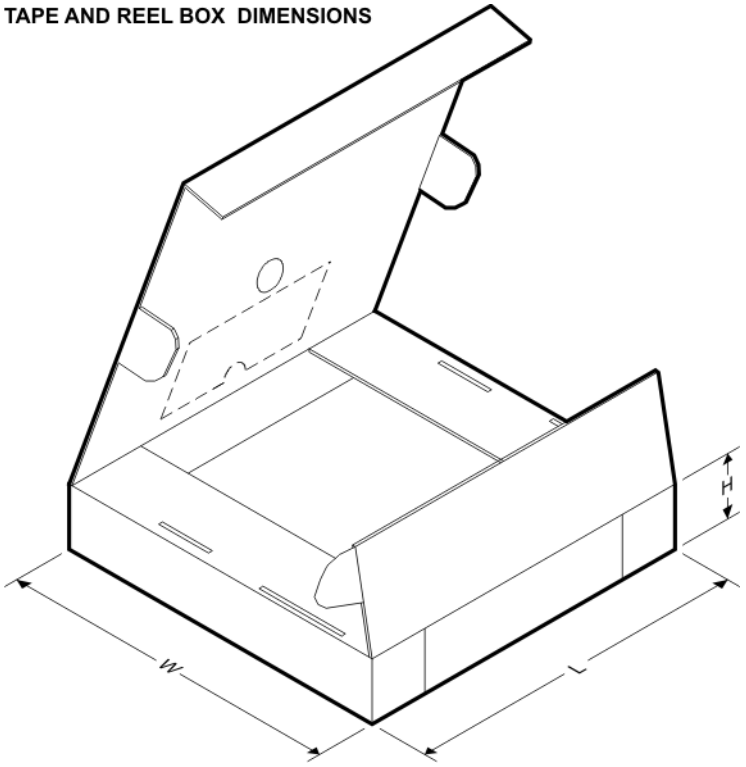


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5111-1MX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5111-1MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5111-1MY/NOPB	MSOP-Power PAD	DGN	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5111-1MYX/NOPB	MSOP-Power PAD	DGN	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5111-2MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5111-2MY/NOPB	MSOP-Power PAD	DGN	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5111-2MYX/NOPB	MSOP-Power PAD	DGN	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5111-3MX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5111-3MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5111-3MY/NOPB	MSOP-Power PAD	DGN	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5111-4MY/NOPB	MSOP-	DGN	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
	Power PAD											

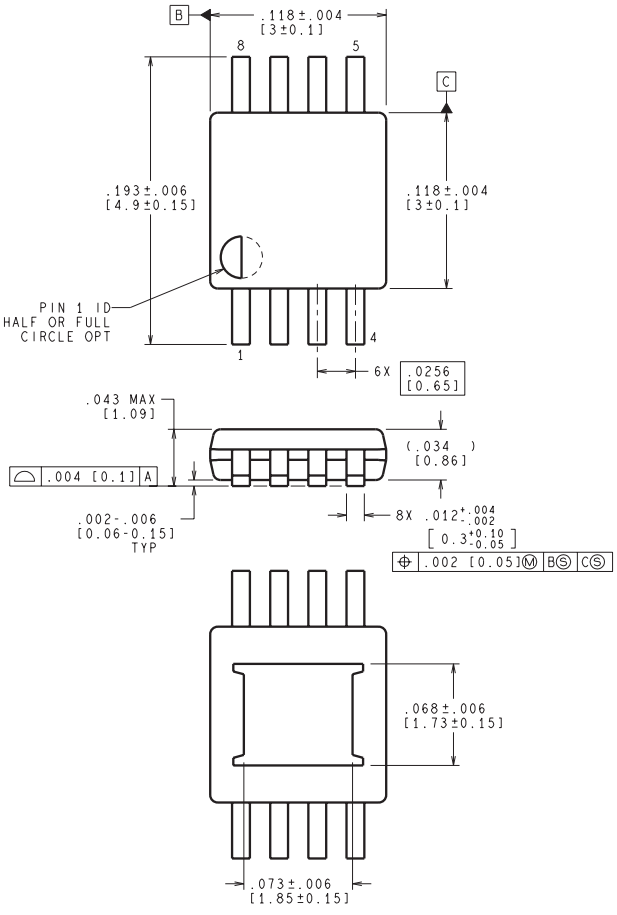
TAPE AND REEL BOX DIMENSIONS



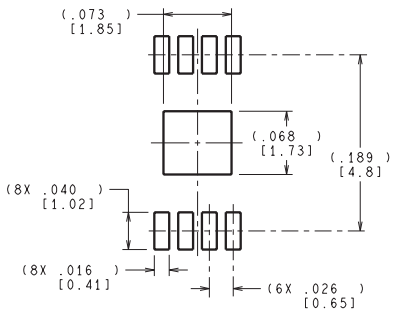
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5111-1MX	SOIC	D	8	2500	367.0	367.0	35.0
LM5111-1MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM5111-1MY/NOPB	MSOP-PowerPAD	DGN	8	1000	210.0	185.0	35.0
LM5111-1MYX/NOPB	MSOP-PowerPAD	DGN	8	3500	367.0	367.0	35.0
LM5111-2MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM5111-2MY/NOPB	MSOP-PowerPAD	DGN	8	1000	210.0	185.0	35.0
LM5111-2MYX/NOPB	MSOP-PowerPAD	DGN	8	3500	367.0	367.0	35.0
LM5111-3MX	SOIC	D	8	2500	367.0	367.0	35.0
LM5111-3MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM5111-3MY/NOPB	MSOP-PowerPAD	DGN	8	1000	210.0	185.0	35.0
LM5111-4MY/NOPB	MSOP-PowerPAD	DGN	8	1000	210.0	185.0	35.0

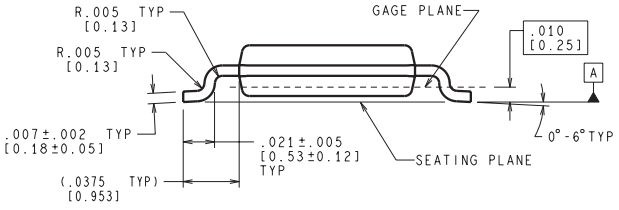
DGN0008A



BOTTOM VIEW



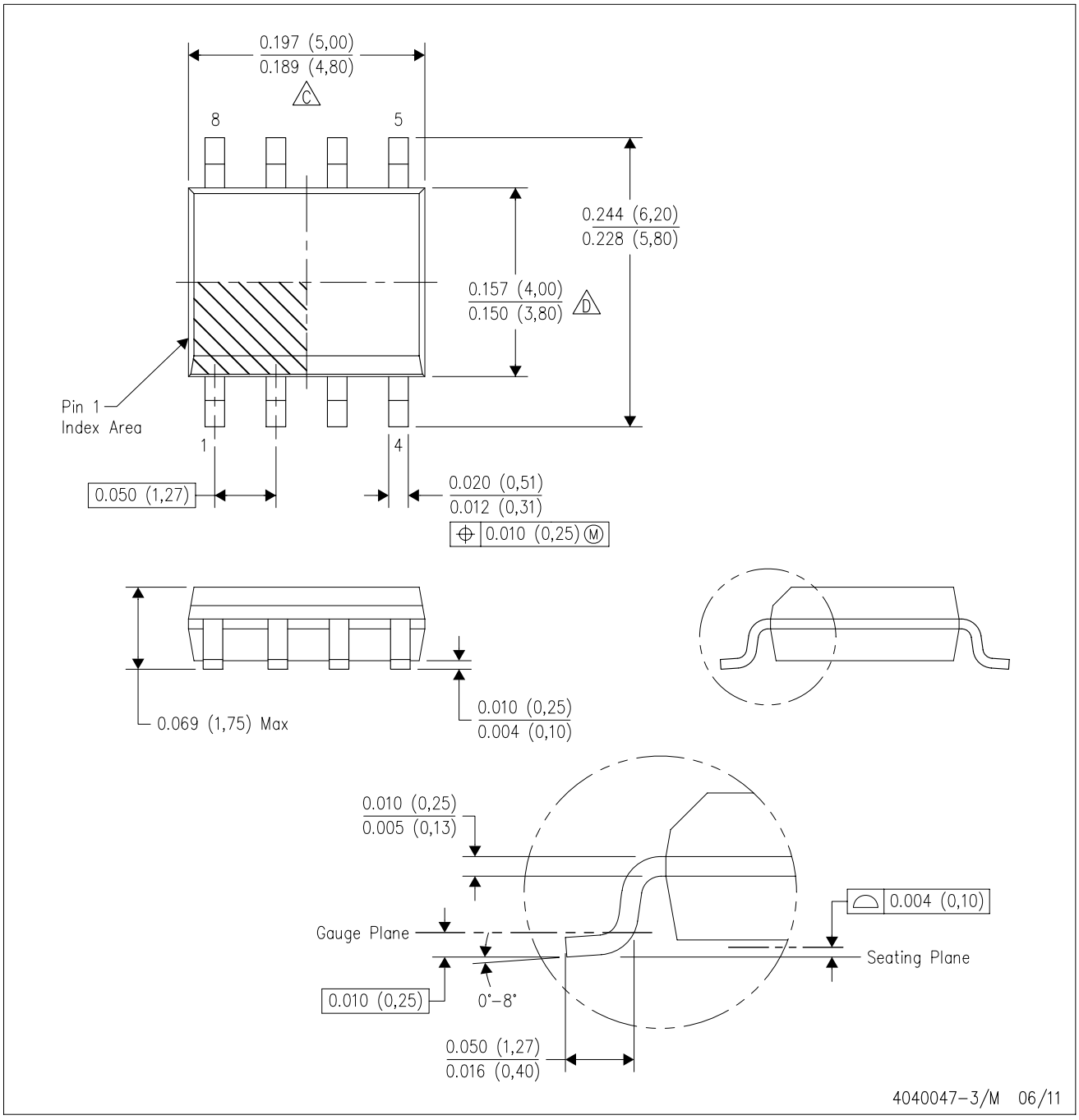
RECOMMENDED LAND PATTERN



CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

MUY08A (Rev A)

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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