
Space FPGA Configuration Memory

DATASHEET

[See Applicable Errata in Section 13.](#)

Features

- 4 Mbits On-Chip Flash Array
- Memory Designed to Store Configuration Programs for Field Programmable Gate Arrays (FPGAs)
- In-System Programming (ISP) via Two-Wire Bus
- Simple Interface to SRAM FPGAs
- Compatible with AT40K devices
- Cascadable Read-Back to Support Additional Configurations or Higher-Density Arrays
- Memory Write Protection
- Programmable Reset Polarity
- Low-power Rad-Hard non volatile 0.18µm CMOS process
- Operating range:
 - Voltage : 3V to 3.6V
 - Temperature : -55 to +125°C
- Operating power consumption : 72 mW max
- High-Reliability
 - Endurance: 50,000 write cycles (in page mode)
 - Data retention: 10 Years @ 125°C
- Radiation Tolerance
 - Tested up to a Total Dose of 60 krad (Si)
 - RHA capability of 30 krad (Si) according to MIL STD 883 Method 1019
- Quality Grades :
 - QML-V or Q
- Package : 305 Mils FP18
- Mass : 1 g

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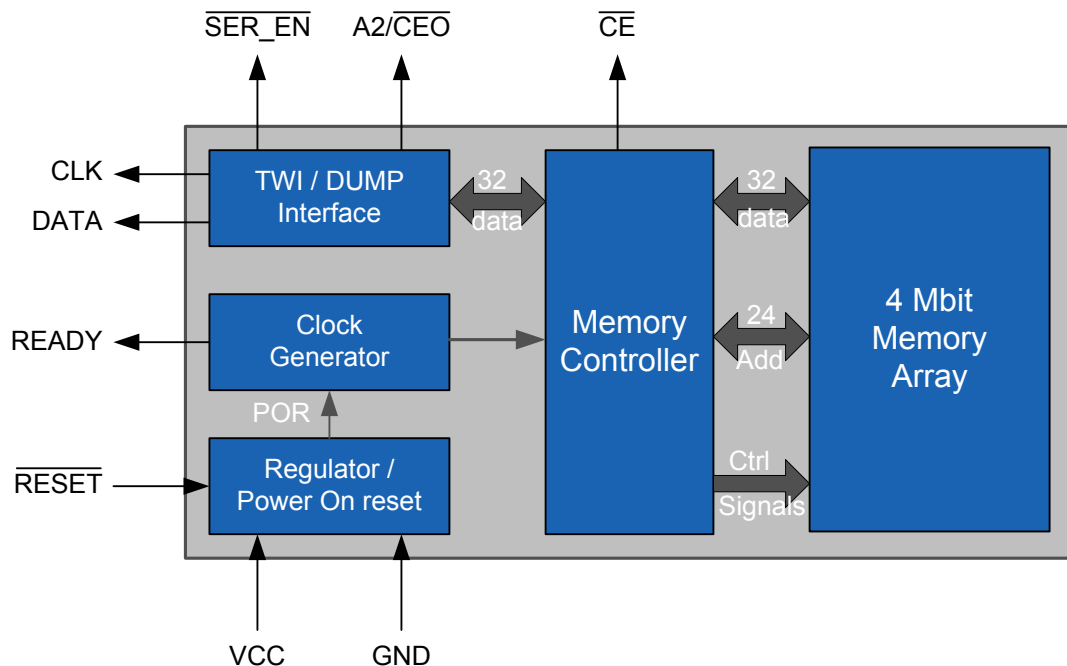
1. Description

The AT69170E FPGA configuration memory (configurator) is an electrically erasable and re-programmable RadHard memory organized as 4Mx1bit. It is an easy-to-use and cost-effective configuration memory for space Field Programmable Grid Array (FPGA). It is manufactured with ATMEL low power non volatile CMOS RadHard process.

It is packaged in the 18-pin 305 Mills wide Flat Pack package. AT69170E uses a simple serial-access procedure to configure one or more FPGA devices. A two wire interface (TWI) is available for memory programming.

The user can select the polarity of the reset function by programming a dedicated sequence. These devices also support a write-protection mechanism within its programming mode.

2. Block Diagram

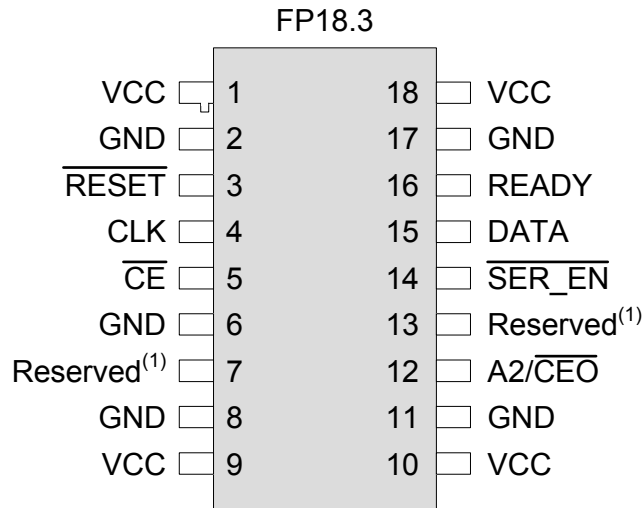


3. Pin Configuration

3.1 Package Description

The AT69170E is packaged in a 18-pins flat pack package.

Figure 3-1. Pin assignment



- Note:
1. “Reserved” pins are bonded internally. **DO NOT CONNECT.**
 2. The package lid is connected to GND

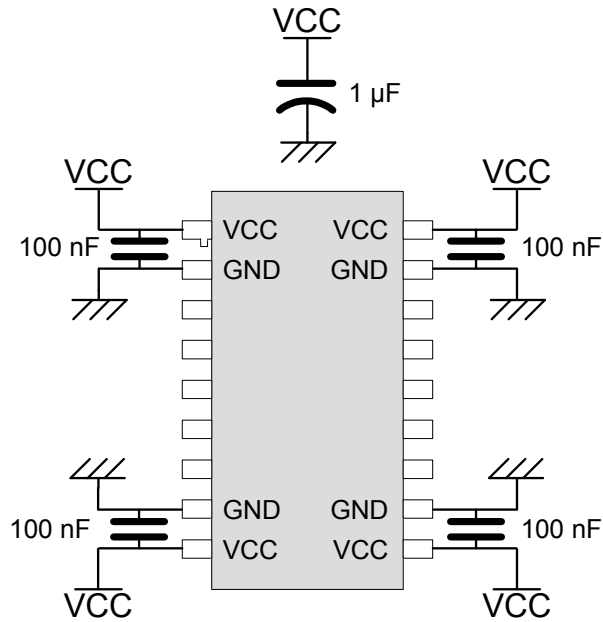
3.2 Pin Description

| Symbol | Name and Function | Type |
|---------------------------|--|-------|
| VCC | <p>Power Supply input</p> <p>The VCC pin is used to supply the source voltage to the device. Operations at invalid VCC voltages may produce spurious results and should not be attempted.</p> <p>It is recommended to implement two decoupling capacitors between VCC and GND. Each capacitor must have a minimum of 100 nF capacitance.</p> | Power |
| GND | <p>Ground pin</p> <p>The ground reference for the power supply. GND should be connected to the system ground.</p> | Power |
| $\overline{\text{RESET}}$ | <p>Reset input (operates only in Dump Mode)</p> <p>The polarity of this input is programmable. For Atmel FPGA's, the $\overline{\text{RESET}}$ pin should be programmed active low and connected to the FPGA's INIT pin (see Figure 9-3 on page 24).</p> <p>When the $\overline{\text{RESET}}$ pin is active, both address and bit counters are reset. This pin does not reset the device in the Two-Wire serial programming mode ($\overline{\text{SER_EN}}$ low).</p> | Input |

| Symbol | Name and Function | Type |
|-----------------------------|--|----------------|
| CLK | <p>Clock input</p> <p>The clock input is used to increment the internal address and bit counters for reading and programming.</p> <p>In Two-Wire serial programming mode ($\overline{\text{SER_EN}}$ Low), the CLK pin must be compliant with the TWI frame description provided in Section 8. "TWI mode" on page 8.</p> <p>In Dump Mode, the serial data will be provided on the CLK's falling edge (see Figure 10-5 on page 31).</p> | Input |
| $\overline{\text{CE}}$ | <p>Chip Enable input (active low, operates only in Dump Mode)</p> <p>Low : address counter is incremented by CLK.</p> <p>High : address and bit counters are disabled.</p> <p>This pin has no effect on the device in the Two-Wire serial programming mode ($\overline{\text{SER_EN}}$ Low).</p> | Input |
| A2/ $\overline{\text{CEO}}$ | <p>A2 : device selection input (operates only in TWI mode)</p> <p>Device selection input is used to configure the device address for multiple device configuration. A2 enables to attach two AT69170E devices on the same bus ($\overline{\text{SER_EN}}$ low). A2 pin configured to a logic "0" or "1" level. It is recommended to connect it to GND or VCC through a 10 kΩ pull-up resistor.</p> <p>CEO : Chip Enable Output (operates only in DUMP mode)</p> <p>$\overline{\text{CEO}}$ is an active low output which goes low when the address counter of the memory has reached the end of the memory plan. In a daisy chain mode including multiple AT69170E devices, the $\overline{\text{CEO}}$ pin of a device is connected to the $\overline{\text{CE}}$ input of the following device in the chain. (see Figure 10. on page 28).</p> | Input / Output |
| $\overline{\text{SER_EN}}$ | <p>Serial Mode Enable input (active low)</p> <p>Low : Two-Wire serial programming mode</p> <p>High : Dump Mode.</p> <p>For applications not using the TWI serial mode, $\overline{\text{SER_EN}}$ should be tied to VCC.</p> | Input |
| DATA | <p>DATA I/O</p> <p>It is an open-drain bi-directional pin in TWI mode ($\overline{\text{SER_EN}}$ Low).</p> <p>It is an output in Dump Mode ($\overline{\text{SER_EN}}$ high)</p> | |
| READY | <p>Open-drain reset state output</p> <p>It is an open-drain output. The READY is driven low during Power-On Reset. It is recommended to use a 4.7 kΩ pull-up resistor.</p> <p>The device does not operate while this signal remains low.</p> | |

3.3 Power supply decoupling

It is recommended to add decoupling capacitors as close as possible to the power supply pins of the device.



4. Device Modes Summary

| INPUT | | | | I/O | | OUTPUT | DEVICE MODES |
|-----------------------------|---------------------------|------------------------|---------|------|----------------------------|--------|---|
| $\overline{\text{SER_EN}}$ | $\overline{\text{RESET}}$ | $\overline{\text{CE}}$ | CLK | DATA | $\overline{\text{A2/CEO}}$ | READY | |
| X | X | X | X | X | X | L | Power-on initialisation |
| H | A | X | X | HZ | X | H | Device Reset |
| H | I | H | X | HZ | X | H | Standby Mode |
| H | I | L | Running | OUT | OUT (H) | H | FPGA Dump Mode (Single Device Configuration) |
| H | I | L | Running | OUT | OUT (L) | H | FPGA Dump Mode (Daisy Chain Configuration) |
| L | X | X | Running | I/O | IN | H | TWI Mode (Device Programming) |

X: means don't care between H or L

A : means Active State

I : means Inactive State

HZ : means High Impedance

The active level of the $\overline{\text{RESET}}$ pin depends on the reset polarity configuration.

5. Factory Settings

The following table lists the parameters that can be changed by the user and their respective factory settings. Those parameters can be changed by means of special functions described in [Section 8.5.3 on page 21](#).

| Parameter | Factory Setting | Comments |
|-------------------------------|-----------------|---|
| Data Protection | Disabled | The changing procedure is described in Section 8.5.3.1 on page 21 |
| $\overline{\text{RESET}}$ pin | Active low | The changing procedure is described in Section 8.5.3.2 on page 22 |

6. Power-On initialisation

The AT69170E provides a READY output pin to indicate that the memory power-on sequence is completed and ready for use.

7. Standby Mode

The AT69170E enters in a standby mode whenever $\overline{\text{CE}}$ input pin is asserted high in FPGA loading mode. In standby mode, the data output pin remains in high impedance.

8. TWI mode

8.1 Definitions

MASTER : any TWI device controlling the transfer of data, such as a microprocessor.

SLAVE : device being controlled. EEPROMs are always considered as slaves

TRANSMITTER : device currently sending data on the bus. May be either a master or a slave.

RECEIVER : device currently receiving data on the bus. May be either a master or a slave.

WORD : 32 bit of data, formatted as a 4-byte packet.

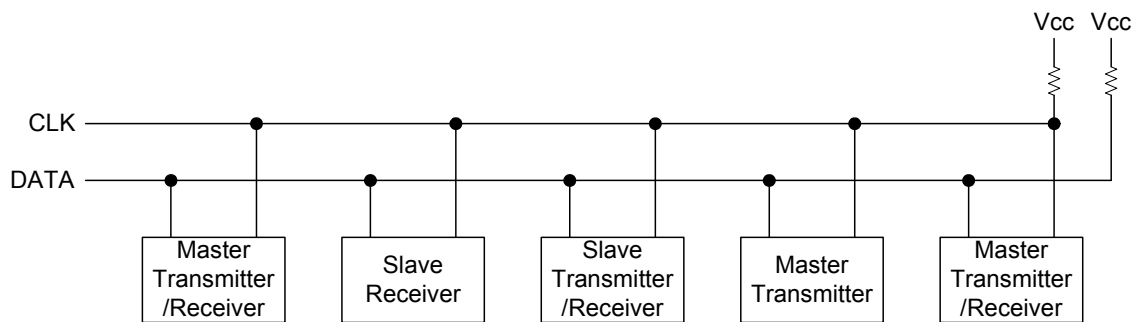
PAGE : 128 sequential word locations starting at 3-byte address boundary, that may be programmed during a “page write” programming cycle.

8.2 TWI Bus Description

The internal memory of the AT69170E is accessed through a TWI bus which is enabled when $\overline{\text{SER_EN}}$ pin is driven Low.

The TWI is a bi-directional 2-wire bus which supports a serial synchronous data transmission protocol. A device that sends data onto the bus (DATA wire) is defined as transmitter and a device receiving data as receiver. The bus works in Master/Slave mode. Several slave and master devices can be attached to the bus but only one master and one slave can communicate at a time. The bus is always controlled by the master device which generates the serial clock (CLK wire), controls the bus access and generates the START and STOP conditions. Both master and slaves can operate as transmitter and receiver but the master determines which mode is activated. The slave devices are identified by a unique address on the bus and only one slave can be selected at a time by the master. The data sent onto the bus by the transmitter are acknowledged by the receiver.

Figure 8-1. Typical System Configuration



The AT69170E is a Slave Transmitter / Receiver.

8.3 TWI Bus Characteristics

The following bus conditions have been defined.

8.3.1 Bus Ready

The bus is ready when both data and clock lines remain high. A data transfer may be initiated only when the bus is ready.

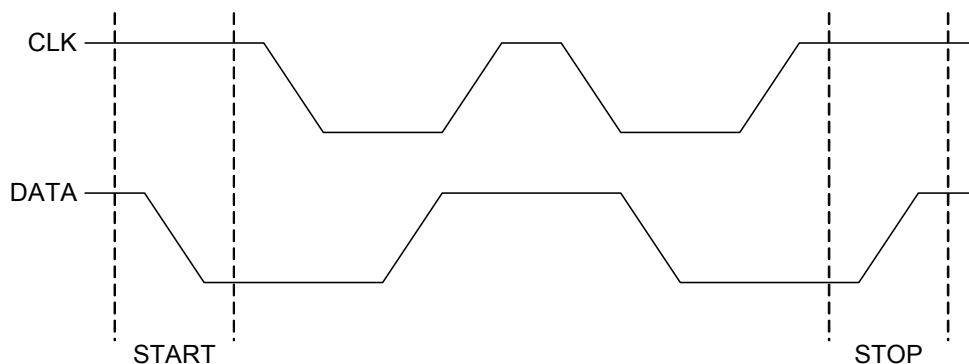
8.3.2 Start and Stop Conditions

A high to low transition of the DATA line while the clock (CLK) is high determines a START condition.

A low to high transition of the DATA line while the clock (CLK) is high determines a STOP condition.

All data transfers must be preceded by a START condition and terminated by a STOP condition

Figure 8-2. Definition of START and STOP Conditions



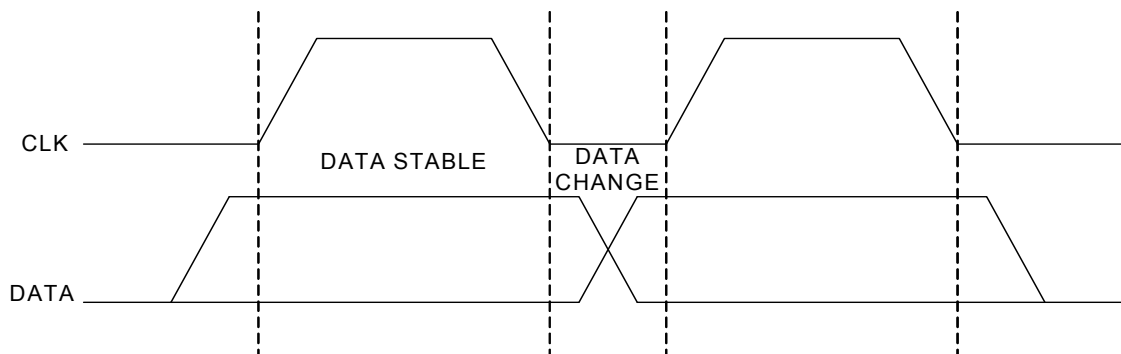
8.3.3 Clock and Data Transitions

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the high period of the clock signal. The data on the line must be changed during the low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and the STOP conditions is determined by the maximum page size (see [Section 8.4](#)).

Changes in the data line while the clock line is high will be interpreted as a START or STOP condition.

Figure 8-3. Data Validity



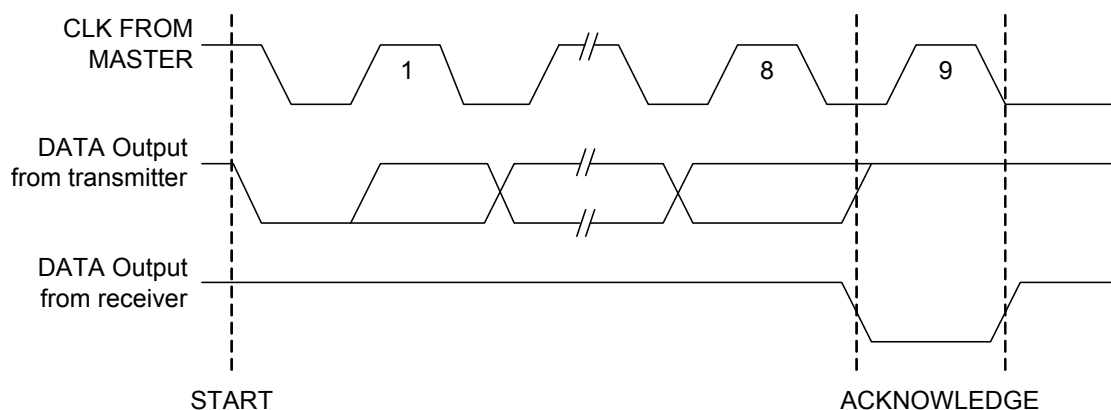
8.3.4 Acknowledge

Each receiver, when addressed, must generate an acknowledge after the reception of each byte. The master must generate an extra clock pulse which is associated with this acknowledge bit.

Note: the AT69170E does not generate any acknowledge bit if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the DATA line during the acknowledge clock pulse in such a way that the DATA line is stable low during the high period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out by the slave. In this case, the slave must leave the data line high to enable the master to generate the STOP condition.

Figure 8-4. Acknowledge response from the receiver



8.3.5 Device Addressing

The first byte sent by the master after the START condition is the control byte. It enables the master to select a unique slave on the bus and indicate if the access is a read or a write operation.

The control byte is composed of three fields :

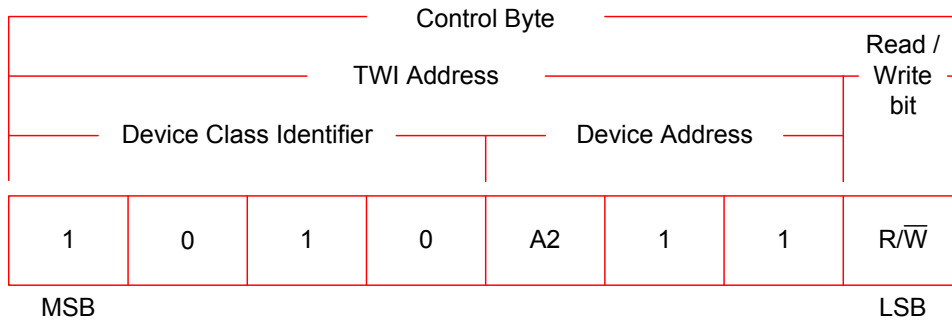
Device Class Identifier : the TWI bus is designed to support a variety of devices such as RAMs, EPROMs etc along with EEPROMs. Hence to properly identify various devices on the TWI bus, a 4-bit "Device Class" identifier string is used. For EEPROMs, the string is 1010.

Device Address : When multiple devices of the same type (e.g. multiple EEPROMs) are present on the TWI bus, the Device Address is used to properly identify the device in the Class.

The device Address of the AT69170E is "A2 1 1". A2 is the value of A2 pin. This address allows as many as two AT69170E on the same bus.

Read/Write bit : the last bit of the control byte indicates if the access is Read or Write. If the bit is "1", then the access is Read, whereas if the bit is "0", then the access is Write.

Figure 8-5. Control Byte Format



The most significant bit (MSB) of the control byte is transmitted first on the TWI bus.

The TWI addresses of the memory device are supplied in the table below.

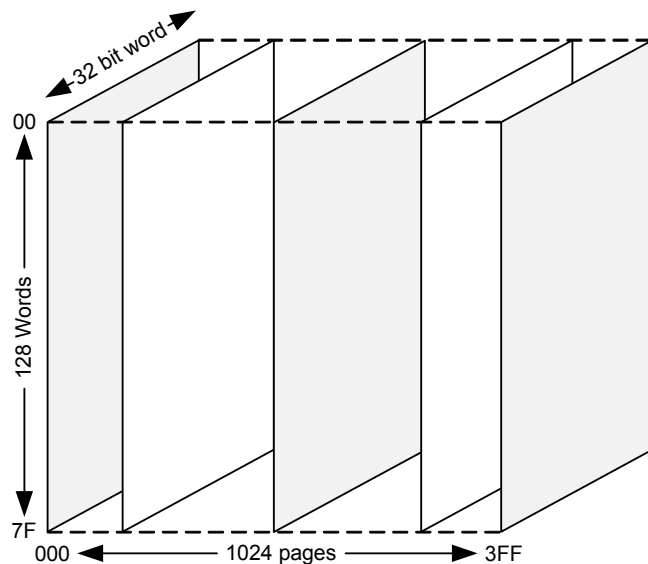
Table 8-1. TWI Device Address

| A2 pin | TWI Device Address |
|--------|--------------------|
| GND | 53h |
| VCC | 57h |

8.3.6 Internal Memory Addressing

The internal memory of the AT69170E is based on a 32-bit architecture interface and is accessed by pages of 128 words. A word is 32 bit wide. The AT69170E has a size of 1024 pages.

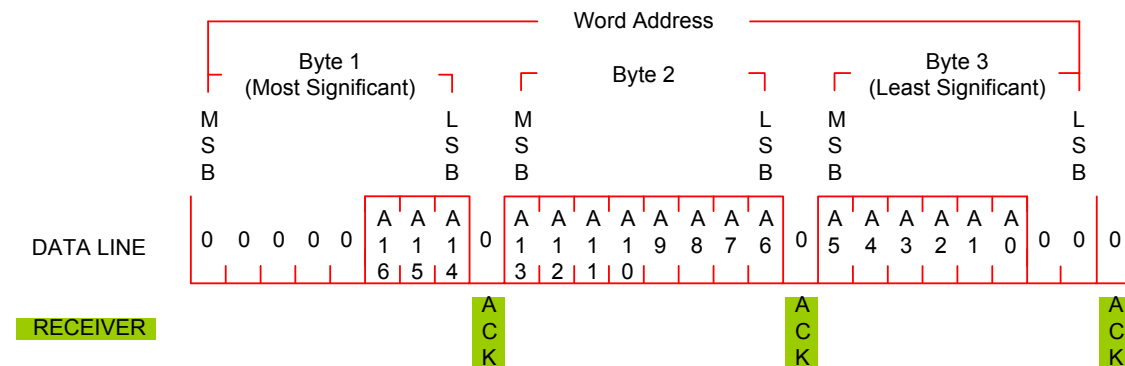
Figure 8-6. Internal Memory Access



Therefore a word address is composed of 17 bits which means that 3 bytes are necessary to define a word address.

The word address is encoded in a TWI frame as described hereafter :

Figure 8-7. TWI Word Address Format



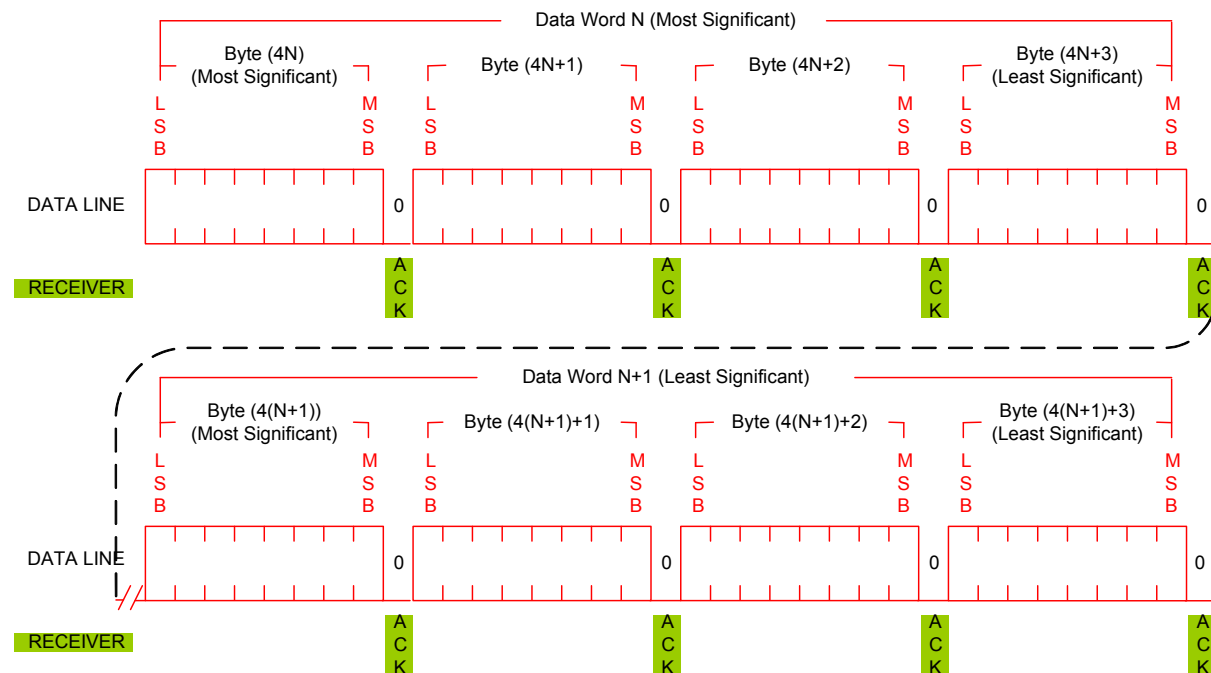
The word address must be shift left by two bits when encoded in a TWI frame. The unused bits must be cleared.

The most significant byte of the word address is transmitted first and the most significant bit of a byte is transmitted first. Each byte of a word address must be acknowledged by the receiver device.

8.3.7 Data Packets

The data packets are composed of an integer number of words and are encoded in a TWI frame in the following manner :

Figure 8-8. TWI Data Packets format



The data packets encoded in TWI frames must be multiples of a data word.

The most significant word of a data packet and the most significant byte of a data word are transmitted first while **the least significant bit of a byte is transmitted first**.

8.4 TWI Operations

8.4.1 Write Operations

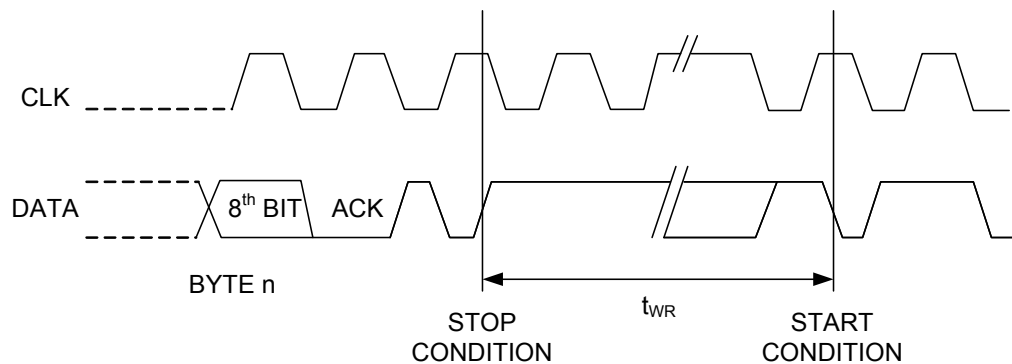
8.4.1.1 Page Write Sequence

In programming mode, the internal memory of AT69170E is organized as 1024 pages of 128 words. This organization involves that it's not possible to program an amount of data lower than a page during a write operation. A page is written through an internal FIFO buffer of 128 words. The buffer is filled by a unique TWI sequence called Page Write sequence.

The Stop Condition of a Page Write sequence generates an internal write cycle whose maximum duration is T_{WR} (see [Table 10-2 on page 31](#)). During this time, the AT69170E ignores the DATA and CLK signals and does not acknowledge any bytes that a transmitter could send.

A power loss during the reception of a page write sequence does not damage the memory contents while a STOP condition is not received. However, the data packet is lost and must be resent by the master.

Figure 8-9. Write Cycle Timing

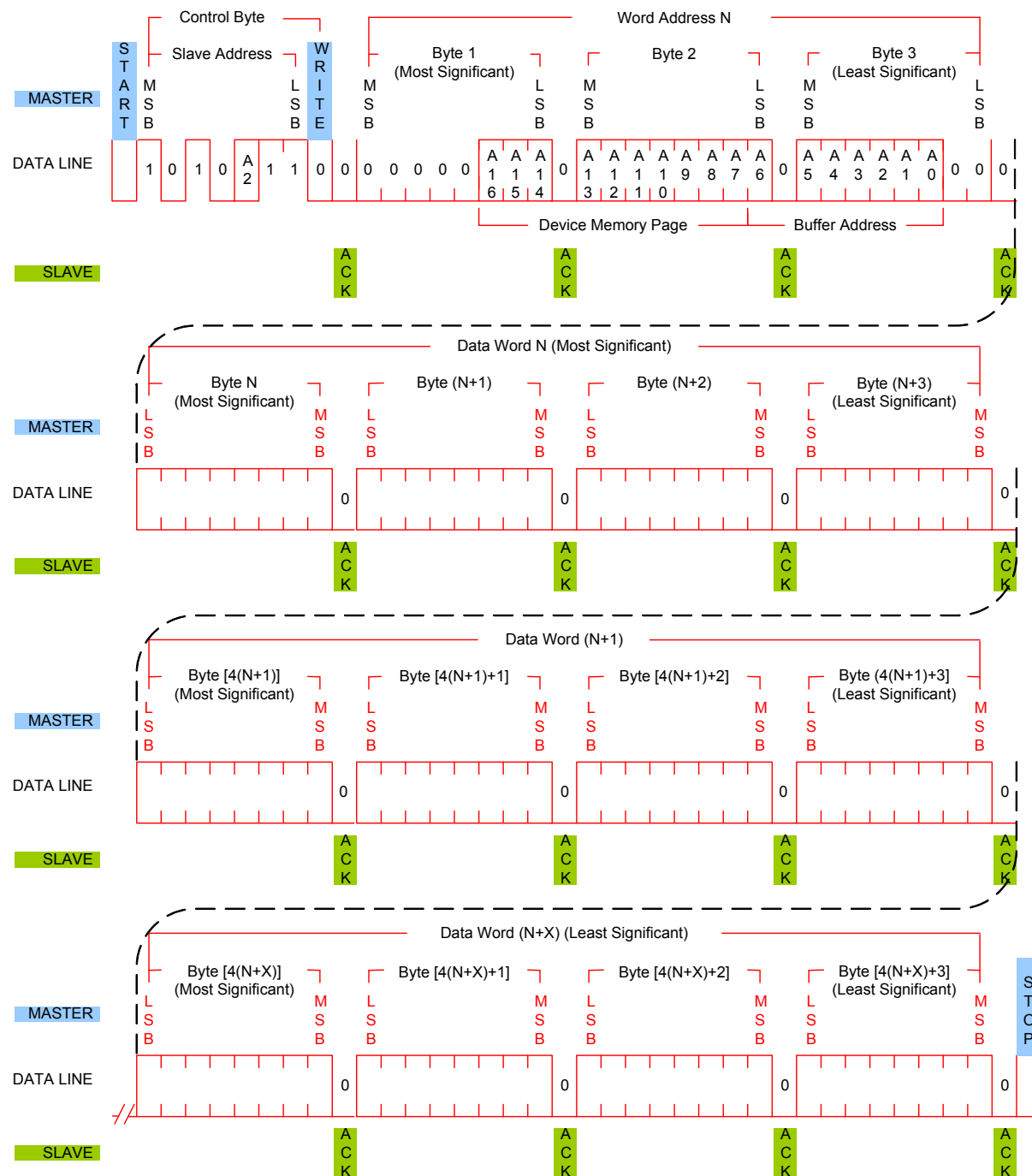


A Page Write frame is composed of the following fields :

- Control Byte
- Word Address
- Data Packet

The figure below describes a full page write sequence.

Figure 8-10. Page Write Sequence



The Data Packet field contains all the words that will be written to the buffer during a Page Write Sequence. Only an integer number of words is allowed.

The Word Address field contains only the address of the first word of the Data Packet field. This address is shifted left by two bits and the two least significant bits of the Word Address field are cleared. The Data Word Address is copied by the device into an internal Address Counter. The rest of data word addresses are internally generated by an automatic incrementation of the Address Counter. This involves that the buffer must be written by a packet of contiguous data words locations. The number of data words can range from 1 to 128. In case, the buffer is not entirely filled, the unwritten words are set to "FF FF FF FF" by default.

The Word Address field is composed of two sections :

- the Device Memory Page
- the Buffer Address

The Device Memory Page ranges from 0 to 1023 while the Buffer Address ranges from 0 to 127.

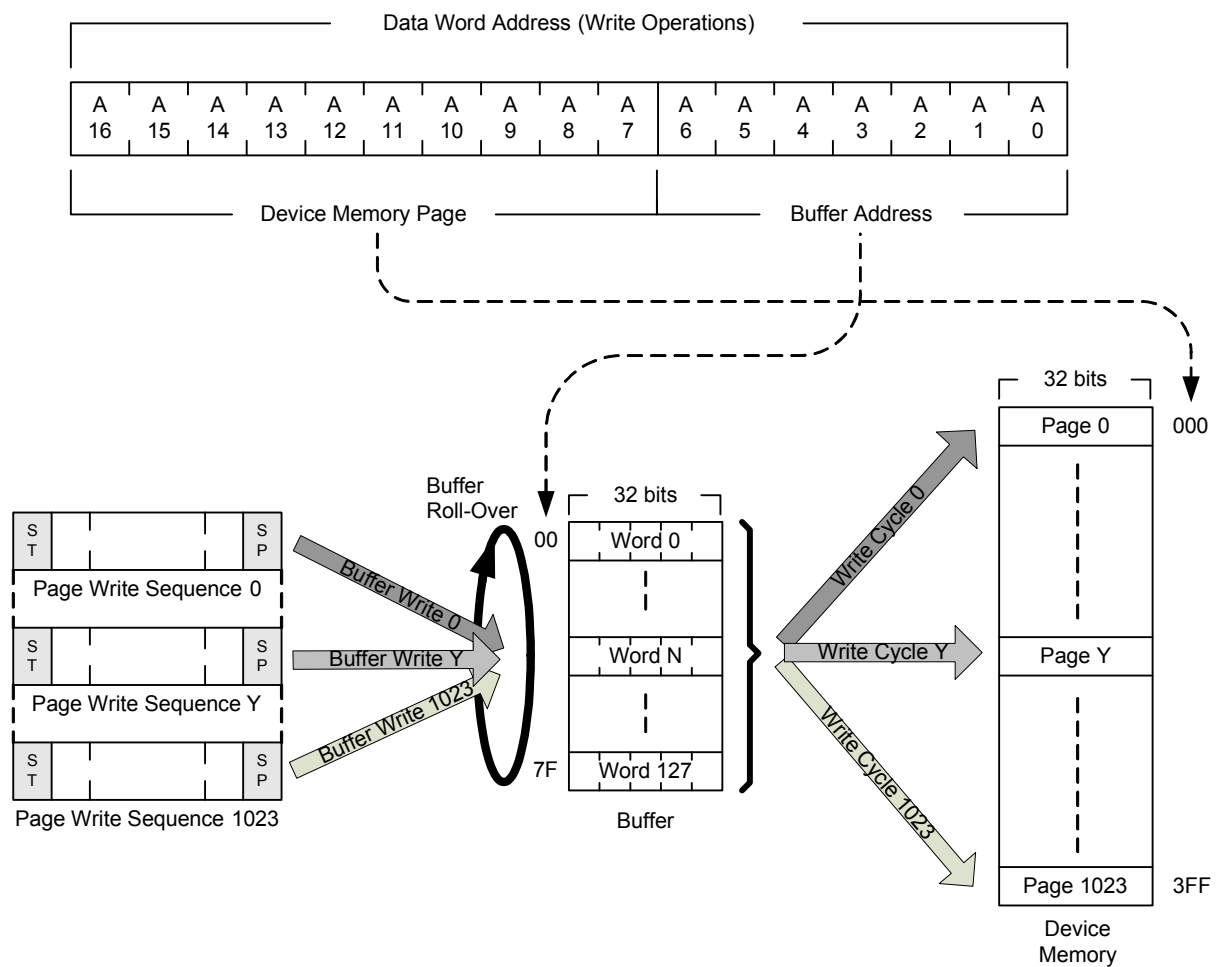
A Page Write operation can be initiated to begin at any location within the buffer, but then the entire buffer only is written to the memory page during a Write Cycle.

To modify a byte within a memory page, it is therefore necessary to read the entire page, modify the byte within the page and perform a Page Write operation.

When the Buffer Address reaches the buffer boundary and additional locations are continued to be accessed, the address “rolls over” from the last word to the first word of the buffer and previous data words are overwritten.

See figure below for a description of the complete writing process of the device memory.

Figure 8-11. Writing process of the device memory

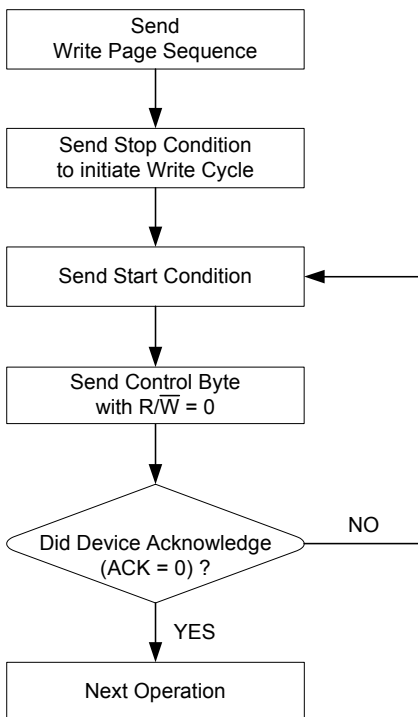


8.4.1.2 Acknowledge Polling

Since the AT69170E does not acknowledge during a write cycle, this can be used to determine when the cycle is complete. This feature can be used to maximize bus throughput. Once the stop condition for a Page Write sequence has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command ($R/\overline{W}=0$). If the AT69170E is still busy with the write cycle, then no ACK is returned. If the write cycle is complete, then the AT69170E returns the ACK and the master can then proceed with the next write or read operation. See figure below for the flow chart.

An alternative way to the acknowledge polling would be to wait for a t_{WR} time before initiating the next write or read operation.

Figure 8-12. Acknowledge Polling Flow



8.4.2 Read Operations

For read operations, the internal memory of AT69170E is directly accessed by the TWI bus in 32-bit mode.

Internally the AT69170E contains an address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or a write) is done to address N, the next read operation will access data word from address N+1.

When address N reaches the device memory boundary, the address counter is incremented by one and the word address “rolls-over” from the last to the first location of the memory.

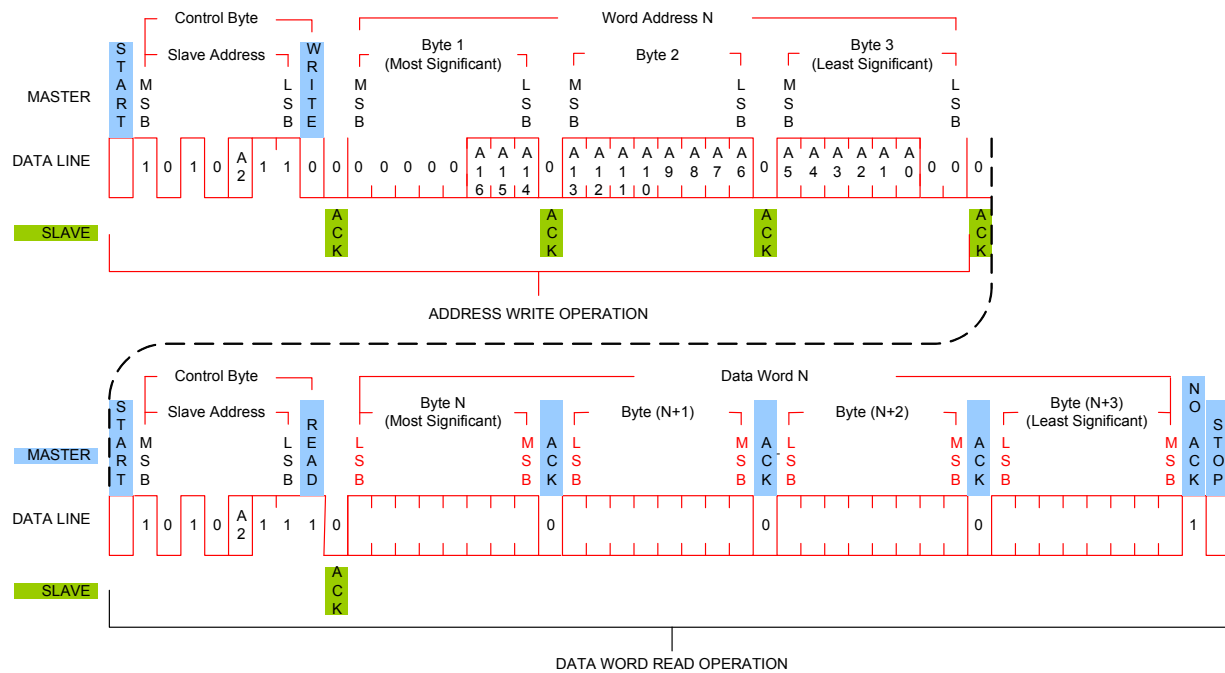
Read operations are initiated in the same manner as write operations. There are two basic read operations :

- random read
- sequential read

8.4.2.1 Random Read

A random read requires a word address write sequence to load in the address counter. Once the control byte and the word address are clocked in and acknowledged by the AT69170E, the master must generate another start condition. Then, the master initiates a read sequence by sending a control byte with the R/\overline{W} bit set to “1”. The AT69170E acknowledges the control byte and serially clocks out the data word. The master acknowledges all the bytes except the last one and then generates a stop condition to discontinue the transmission.

Figure 8-13. Random Read

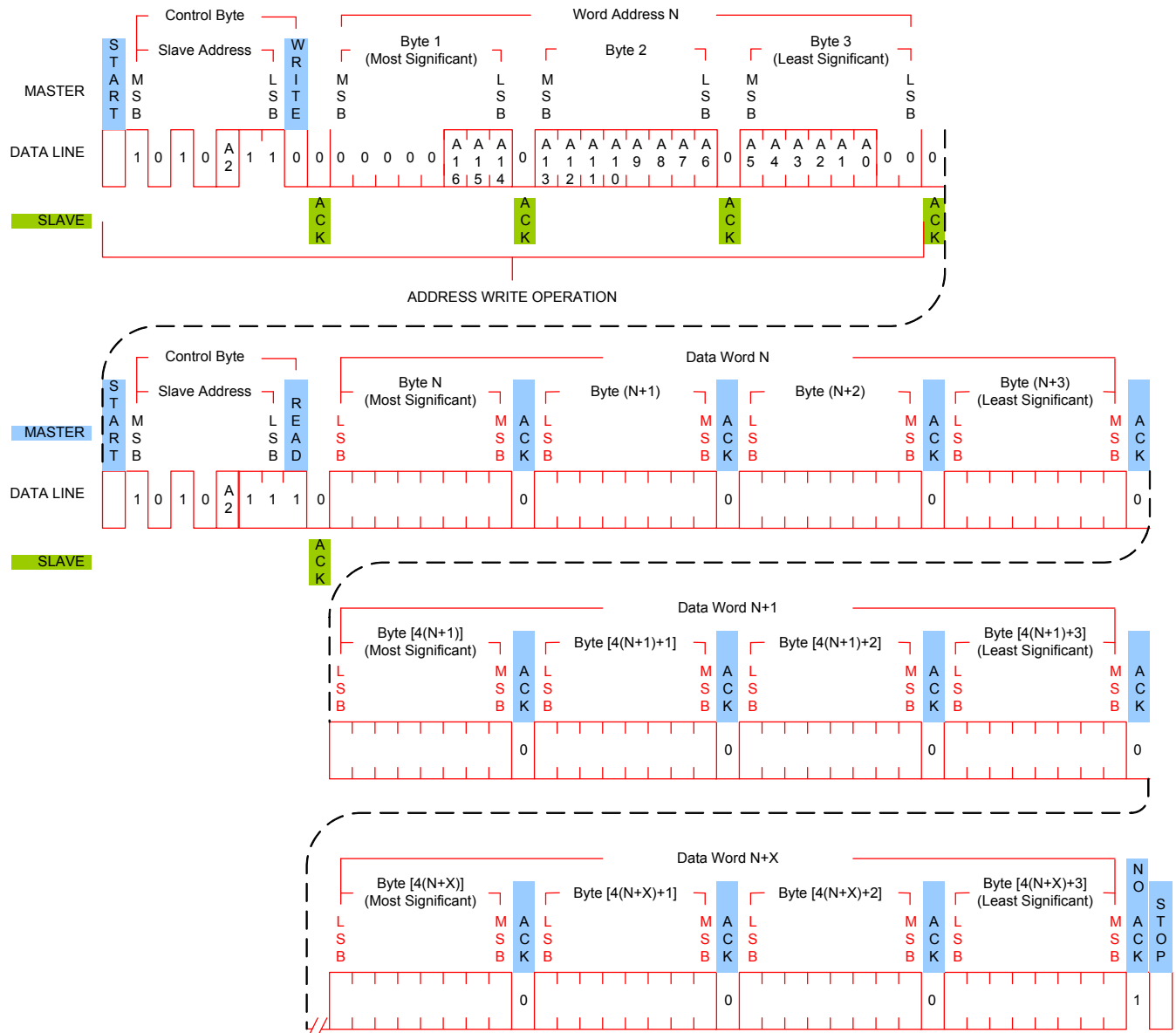


8.4.2.2 Sequential Read

Sequential reads must be initiated as random read access. The first word is clocked out by AT69170E in the same manner as the random read mode. However, the master now responds with an acknowledge indicating it requires additional data. As long as the AT69170E receives an acknowledge, it continues to increment the word address and serially clock out sequential data words. The read operation is terminated by the master which does not acknowledge the reception of the last byte but does generate the stop condition.

The data output is sequential, with the word from address N followed by the word from address N+1. The address counter for read operations increments all the byte addresses of a data word, allowing the entire memory contents to be serially read during one operation. When the memory address limit is reached, the word address will “roll-over” from the last to the first location of the memory and the AT69170E continues to output data for each acknowledge received.

Figure 8-14. Sequential Read



8.5 Special Functions

The AT69170E supports special functions that are accessible by commands sent through the TWI bus.

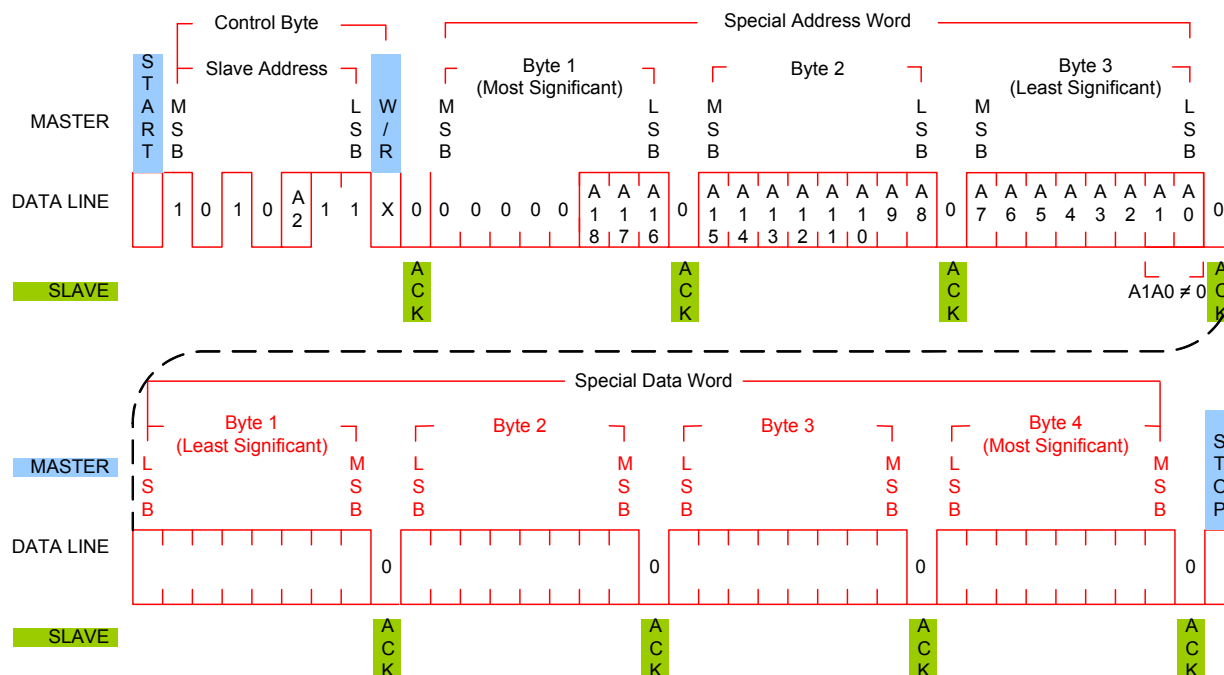
A Special Function command is obtained by the concatenation of special basic commands.

A special basic command frame is composed of the following fields :

- Control Byte
- Special Word Address
- Special Word Data

See figure below for a complete description of a special basic command frame.

Figure 8-15. Special basic command



A special basic command is differentiated from a normal read/write operation by means of the address field. The address word of read/write operations is shift left by two bits while the address word for special basic commands is not. The two least significant bits of the word address field are always cleared for read/write operations while they cannot be simultaneously equal to zero ($A1A0 \neq 0$) for special basic commands.

The least significant byte of a data word and the least significant bit of a byte are transmitted first.

Special Functions commands allow to read or write configurations which are saved by means of internal fuse bits.

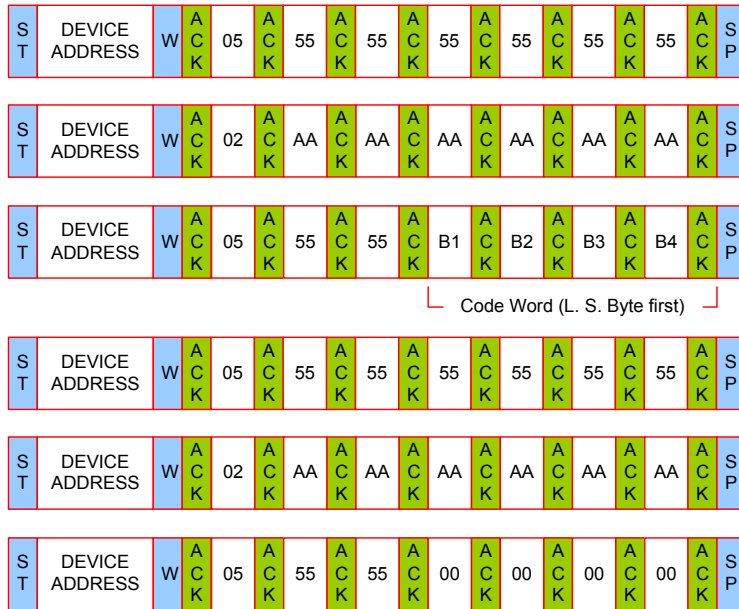
8.5.1 Configuration Write Function

The Configuration Write Function is built by the concatenation of the following special basic commands :

- write “AA AA AA AA” at address “05 55 55”
- write “55 55 55 55” at address “02 AA AA”
- write “Word Code” at address “05 55 55”
- write “AA AA AA AA” at address “05 55 55”
- write “55 55 55 55” at address “02 AA AA”
- write “00 00 00 00” at address “05 55 55”

See figure below for a complete description of the Configuration Write Function

Figure 8-16. Configuration Write Function



8.5.2 Configuration Read Function

The Configuration Read Function is built by the concatenation of the following special basic commands :

- write “AA AA AA AA” at address “05 55 55”
- write “55 55 55 55” at address “02 AA AA”
- write “Code Word” at address “05 55 55”
- read “Data Word” from address “00 00 01”
- write “AA AA AA AA” at address “05 55 55”
- write “55 55 55 55” at address “02 AA AA”
- write “00 00 00 00” at address “05 55 55”

See figure below for a complete description of the Configuration Read Function.

Figure 8-17. Configuration Read Function



The Special Functions are listed hereafter :

- Data Protection
- Chip Reset Polarity
- Full Chip Erase

8.5.3 Special Functions List

8.5.3.1 Data Protection

The AT69170E has a “Write Protection” feature that disables data write capability to the memory. When the lock is activated, the data uploaded into the buffer is not written to the memory which preserves its content.

The write protection is managed by an internal fuse bit only as the AT69170E does not provide any write protect pin.

Table 8-2. Data protection commands

| Special Function Name | Description | Operation | Code Word | Data Word |
|-------------------------|---|-----------|-------------|--|
| Enable Data Protection | Memory data protection is activated | Write | 00 00 00 A0 | |
| Disable Data Protection | Memory data protection is deactivated | Write | 00 00 00 20 | |
| Data Protection Status | Returns the state of the Data Protection fuse bit | Read | 00 00 00 F2 | 00 XX XX XX : Memory is not write protected FF XX XX XX : Memory is write protected |

The “Enable Data Protection” command must be received by the memory device before the last Page Write sequence when a bitstream is programmed into the memory. If this condition is not fulfilled, the memory will not be correctly protected against write operations.

When the memory is write protected the only way to deactivate the memory protection is to apply the “Disable Data Protection” command.

The Full Chip Erase function does not operate when the memory is write protected.

The device is supplied with memory data protection deactivated.

8.5.3.2 Chip Reset Polarity

The AT69170E allows the user to configure the polarity of the $\overline{\text{RESET}}$ pin as either active low or active high. This feature allows the memory device to work with various FPGA families. The device is supplied with the $\overline{\text{RESET}}$ pin active low.

The $\overline{\text{RESET}}$ polarity change is effective immediately. The written value can be verified by reading the Reset Polarity fuse bit.

Table 8-3. Chip reset polarity commands

| Special Function Name | Description | Operation | Code Word | Data Word |
|-----------------------|--|-----------|-------------|--|
| Reset Active Low | Chip Reset is active low | Write | 00 00 00 FF | |
| Reset Active High | Chip Reset is active high | Write | 00 00 FF FF | |
| Chip Reset Status | Returns the state of the Reset Polarity fuse bit | Read | 00 00 00 F2 | XX [B2] XX XX B2 = 0XXX XXXX : $\overline{\text{RESET}}$ Active Low B2 = 1XXX XXXX : $\overline{\text{RESET}}$ Active High |

8.5.3.3 Full Chip Erase

This command enables to erase the entire memory with a simple command. This command does not operate when the memory is write protected. The AT69170E does not acknowledge the TWI protocol during the memory erase cycle.

Table 8-4. Full chip erase

| Special Function Name | Description | Operation | Code Word | Data Word |
|-----------------------|-------------------------|-----------|-------------|-----------|
| Full Chip Erase | Erase the entire memory | Write | 00 00 00 B0 | |

9. FPGA Dump Mode

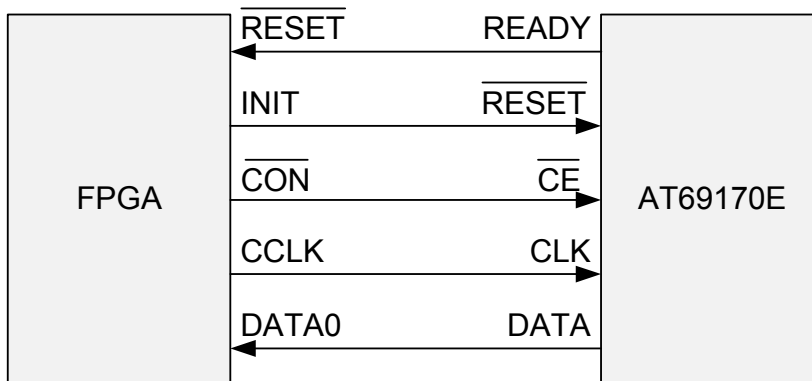
9.1 Operating Mode overview

The I/O and logic functions of any SRAM-based FPGA device are configured with a bitstream supplied by an external memory device. The FPGA's mode pins enable the way the bitstream is loaded into the FPGA. The bitstream can be supplied by a remote device or downloaded by the FPGA itself at power-on. In Master Serial Mode (Mode 0), the ATMEL's AT40K FPGA serie automatically downloads the bitstream from an external memory device without the need of an external smart controller. The AT69170E has been designed to support the Master Serial Mode of AT40K FPGA serie.

9.2 Single Device Configuration

The interface between FPGA and AT69170E device is composed of signals $\overline{\text{RESET}}$, $\overline{\text{CE}}$, CLK and DATA.

Figure 9-1. Interface between FPGA and AT69170E for single device configuration



When the power is up, the AT69170E's internal address counter is reset and the READY pin is driven high, enabling the FPGA to leave its reset state and start the download process.

The $\overline{\text{RESET}}$ and $\overline{\text{CE}}$ pins of the AT69170E device control the tri-state buffer of the DATA output pin and the internal address counter. When the $\overline{\text{RESET}}$ pin is driven low, regardless to the level of the $\overline{\text{CE}}$ pin, the AT69170E resets its address counter and the DATA pin is set in tri-state mode.

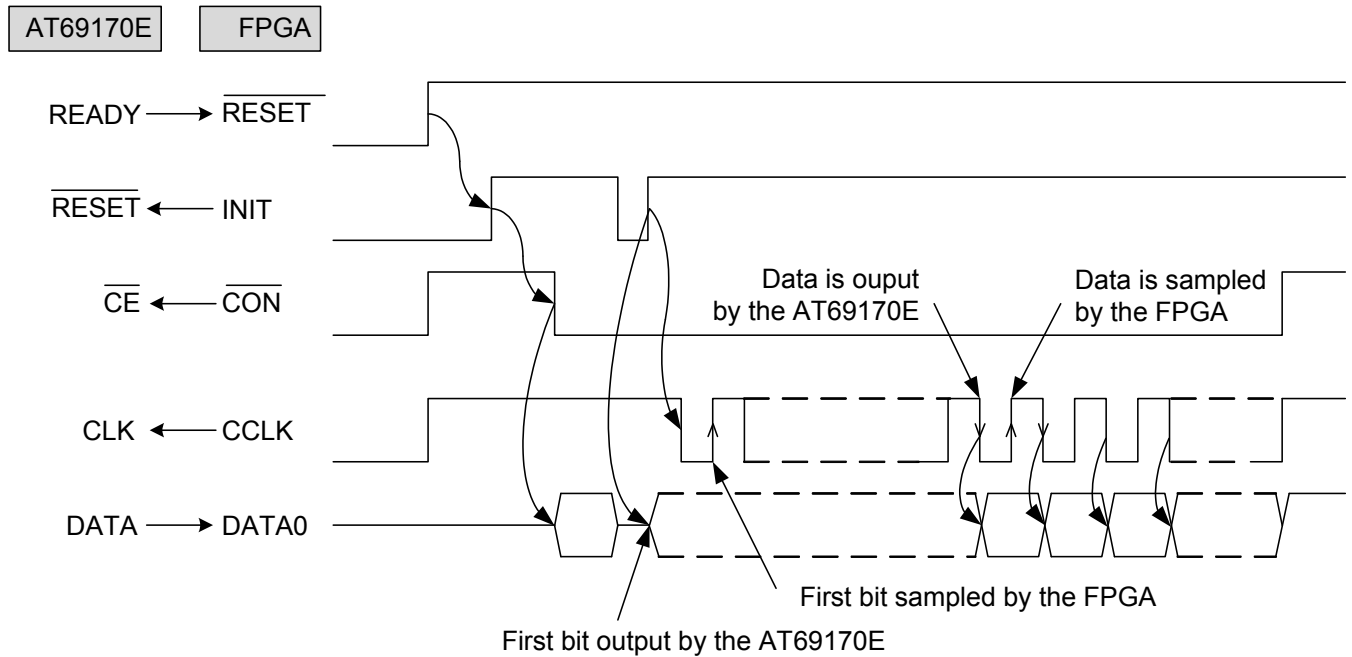
If the $\overline{\text{CE}}$ pin is hold high when $\overline{\text{RESET}}$ pin is released (driven high), the address counter is disabled and the DATA output pin is set in tri-state mode.

if the $\overline{\text{CE}}$ pin is hold low when the $\overline{\text{RESET}}$ pin is released, the address counter and the DATA pin outputs the first data bit which is sampled by the FPGA on the first rising edge of the clock.

The AT69170E is clocked by the FPGA. The internal address counter is incremented on each clock's period. The data bits are output by the AT69170E on the falling edges of the clock so that they can be sampled by the FPGA on the rising edges of the clock.

Once the bitstream's download is complete, the $\overline{\text{CON}}$ pin is released by the FPGA.

Figure 9-2. Dump Mode (Single Device Configuration)

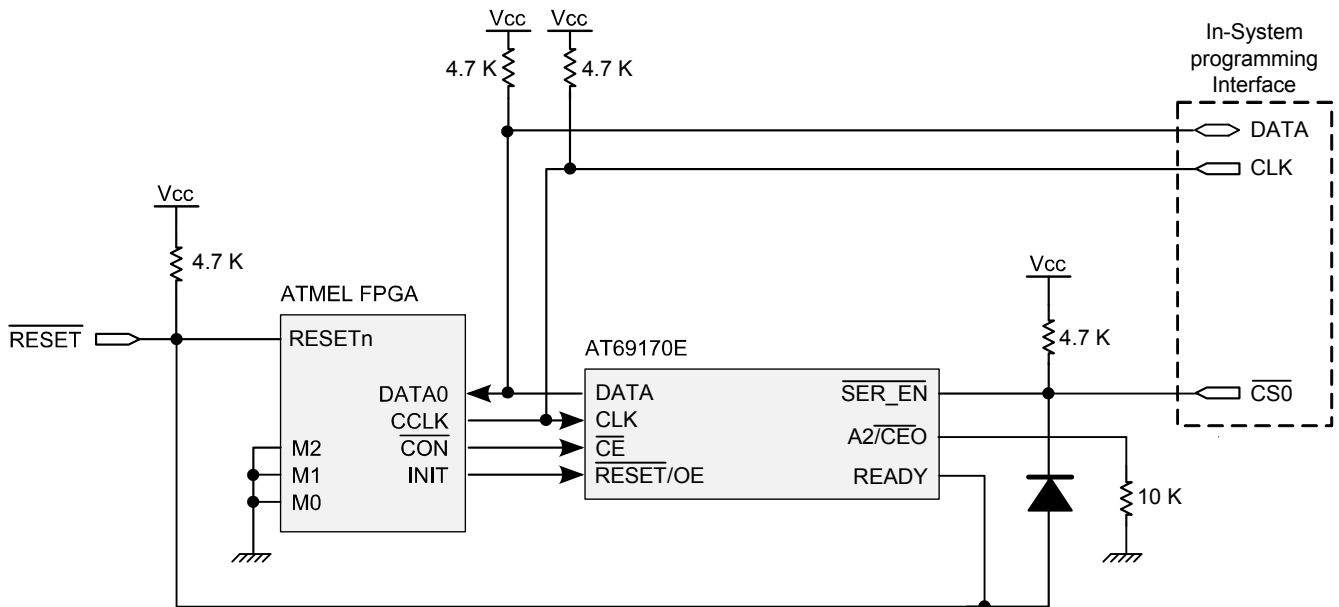


An example of application schematic is provided on [Figure 9.3 on page 25](#).

The **SER_EN** pin enables to configure the AT69170E in TWI or DUMP mode. This pin is pulled up to **Vcc** to select the dump mode by default. A diode between **READY** and **SER_EN** enables to set automatically the FPGA in the reset state when the TWI mode is selected in order to avoid signal contentions

Pull-up resistors are mandatory on **DATA** and **CLK** pins in TWI mode and on **READY** signal in DUMP mode.

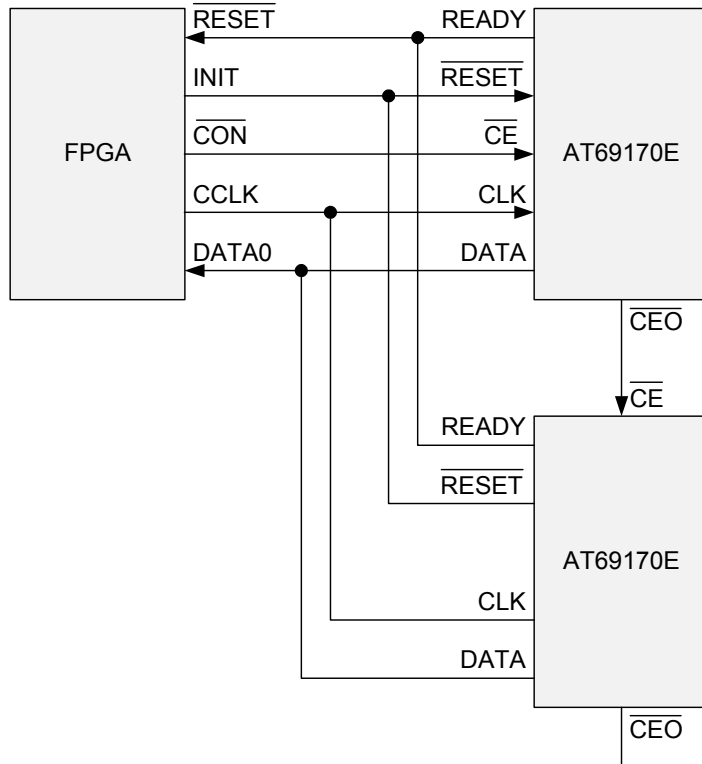
Figure 9-3. Single Device Configuration Schematic



9.3 Daisy Chain Configuration

The interface between FPGA and AT69170E devices is composed of signals $\overline{\text{READY}}$, $\overline{\text{RESET}}$, $\overline{\text{CE}}$, CLK, DATA and $\overline{\text{CEO}}$.

Figure 9-4. Interface between FPGA and AT69170E for Daisy Chain Configuration

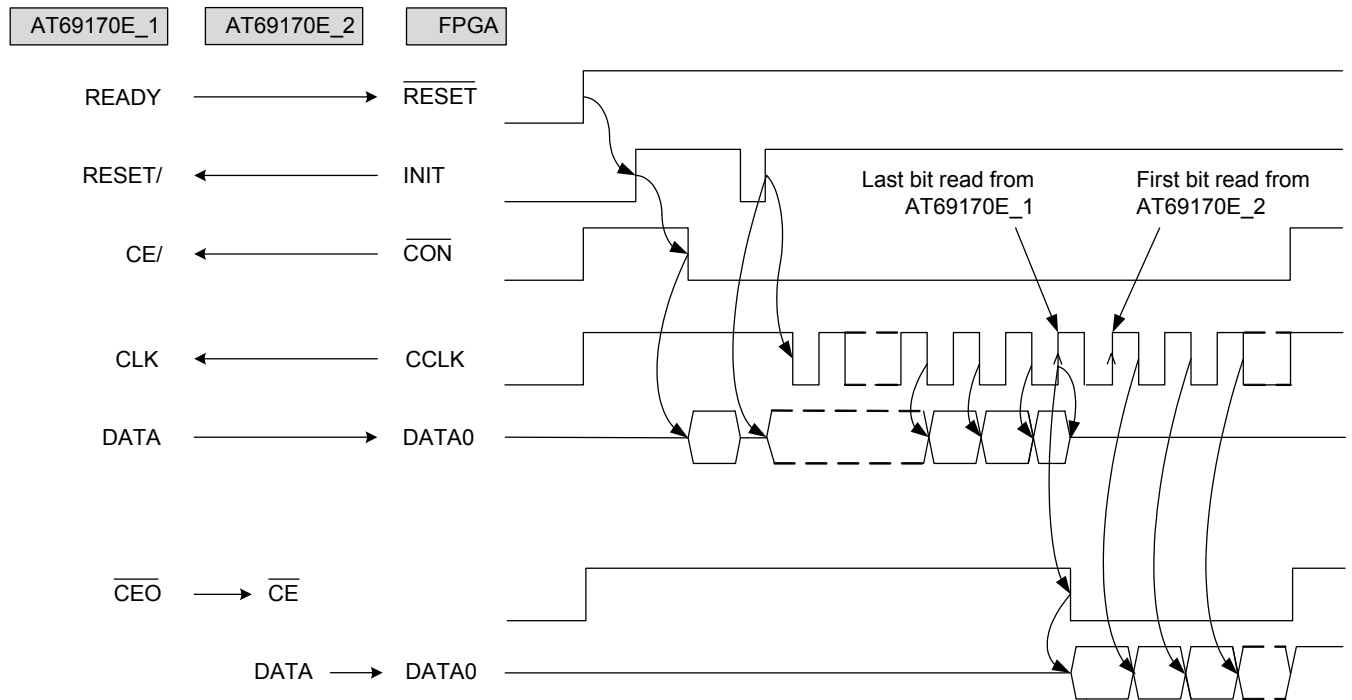


For multiple FPGAs configured as a daisy-chain, or for FPGAs requiring larger configuration memory, it is possible to cascade several AT69170E devices.

Once the last bit from the first AT69170E is read, the device drives its $\overline{\text{CEO}}$ pin low and disables its DATA pin to avoid signal contention with another AT69170E. The second AT69170E recognizes the Low level on its $\overline{\text{CE}}$ pin and enables its DATA pin. The same scenario repeats for the following AT69170E devices.

It is possible to daisy chain up to 4 AT69170E devices.

Figure 9-5. Dump Mode (Daisy Chain Configuration)

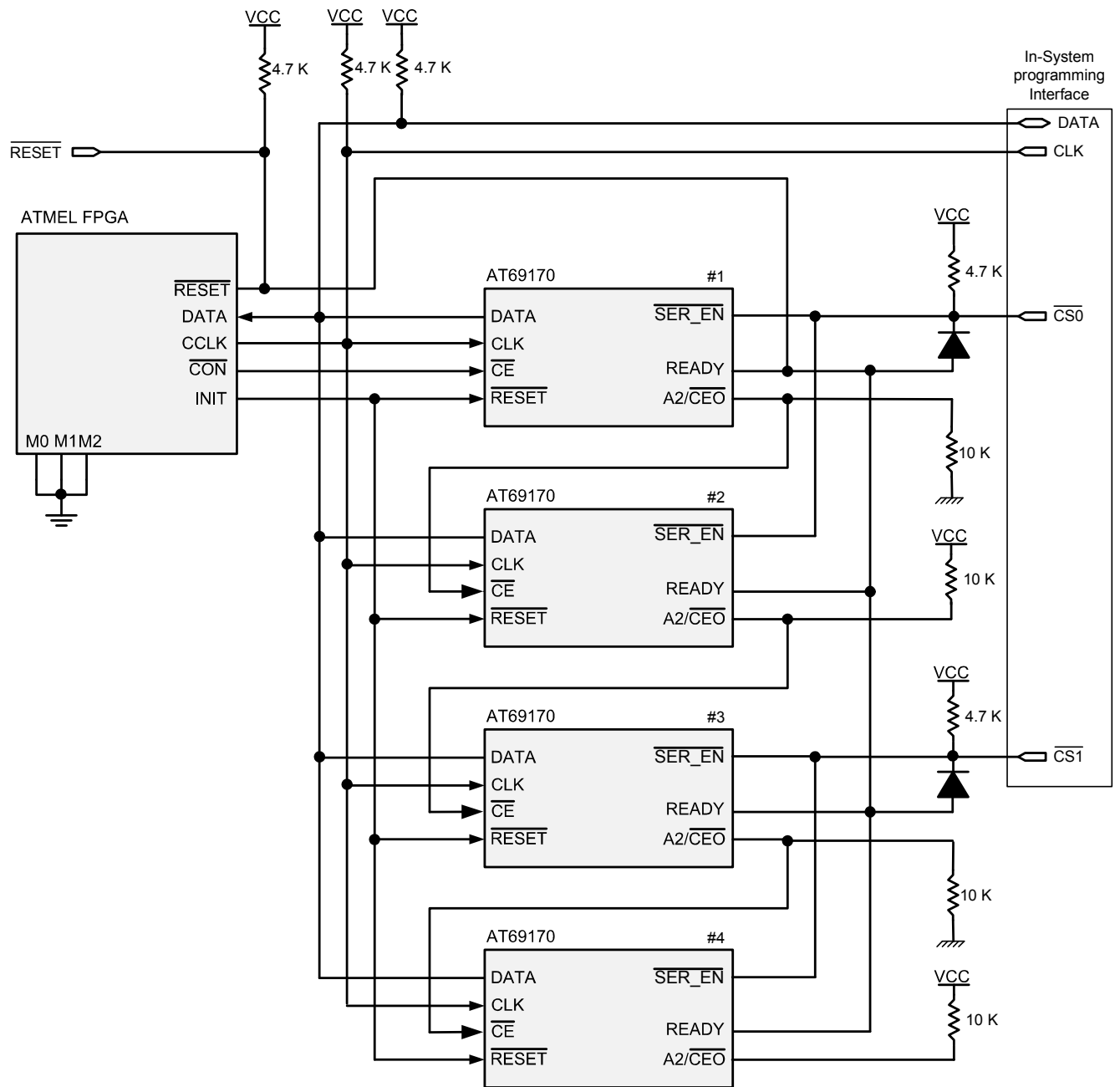


An example of application schematic is provided on [Figure 10. on page 28.](#)

In TWI mode, it is not possible to select more than two AT69170E devices at a time. Therefore, two chip selects CS1 and CS2 must be defined, each one selecting two devices, in order to program the all the devices two by two.

Pull-up resistors are mandatory on DATA and CLK pins in TWI mode and on READY signal in DUMP mode.

Figure 9-6. Daisy Chain Configuration Schematic



10. Electrical Specifications

10.1 Absolute Maximum Ratings*

| | |
|---|--------------------|
| Supply voltage to ground. | -0.5V to 4.6V |
| All input voltages (including NC pins) with respect to ground | -0.5V to +4.6V |
| All output voltages with respect to ground | -0.5V to VCC+ 0.5V |
| Storage temperature | 65°C to +150°C |
| ESD Voltage (MIL STD 883D Method 3015.3) | > 4000V |

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied.

Exposure between recommended DC operating and absolute maximum rating conditions for extended periods may affect device reliability.

10.2 Recommended DC Operating Conditions

| Symbol | Parameter | Min | Typ | Max | Unit |
|-----------------|------------------------------|-----|-----|-----|------|
| V _{CC} | Supply Voltage | 3.0 | 3.3 | 3.6 | V |
| Temp | Operating Temperature (Case) | -55 | 25 | 125 | °C |

10.3 Capacitance (F=1MHz, 25°C)

| Symbol | Description | Min | Typ | Max | Unit | Condition |
|---------------------------------|--------------------|-----|-----|-----|------|-----------------------|
| C _{IN} ⁽¹⁾ | Input Capacitance | | 7 | 10 | pF | V _{IN} = 0V |
| C _{OUT} ⁽¹⁾ | Output Capacitance | | 7 | 10 | pF | V _{OUT} = 0V |

Note: 1. Guaranteed but not tested

10.4 DC Characteristics

| Symbol | Parameter | Condition | Min | Max | Unit |
|-------------------------------------|--------------------------------|---|-----------|-----|------|
| I _{IL} , I _{IH} | Low Level Input Current | V _{IN} = 0 to 3.6V V _{CC} =3.6V | -1 | 1 | μA |
| I _{CSL} , I _{CSH} | Cold Sparing Leakage Current | V _{IN} = 0 to 3.6V V _{CC} = 0V | -1 | 1 | μA |
| I _{CCSB} | Static consumption in TWI mode | $\overline{\text{SER_EN}} = 0\text{V}$ $\overline{\text{CE}} \geq V_{CC}-0.3\text{V}$ f _{CLK} = 0 MHz V _{CC} = 3.6V | | 15 | mA |
| I _{CCOP} | Operating Current | I _{OUT} = 0 mA | | 20 | mA |
| V _{IL} | Input Low Voltage | V _{CC} = 3.0V | GND - 0.3 | 0.8 | V |

| Symbol | Parameter | Condition | Min | Max | Unit |
|----------|---------------------|--|----------------|--------------|------|
| V_{IH} | Input High Voltage | $V_{CC} = 3.6V$ | 2.2 | $V_{CC}+0.3$ | V |
| V_{OL} | Output Low Voltage | $I_{OL} = 8\text{ mA}$ $V_{CC} = 3.0\text{ to }3.6V$ | | 0.4 | V |
| V_{OH} | Output High Voltage | $I_{OH} = -8\text{ mA}$ $V_{CC} = 3.0\text{ to }3.6V$ | $V_{CC} - 0.4$ | | V |

10.5 AC Characteristics

Temperature Range: -55 +125°C

Supply Voltage: 3.3 ±0.3V

Input and Output Timing Reference Levels: 1.5V

10.5.1 Test Loads and Waveforms

Figure 10-1. Output Test Load

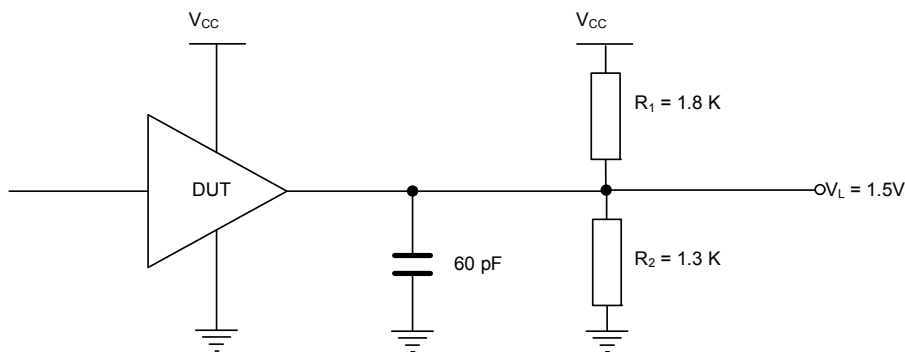
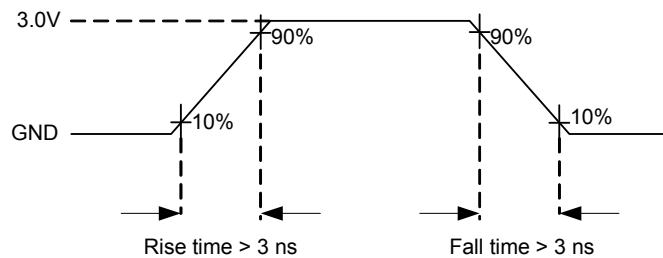


Figure 10-2. Waveform



10.5.2 TWI Mode Characteristics

Figure 10-3. TWI Data Transfer Waveforms

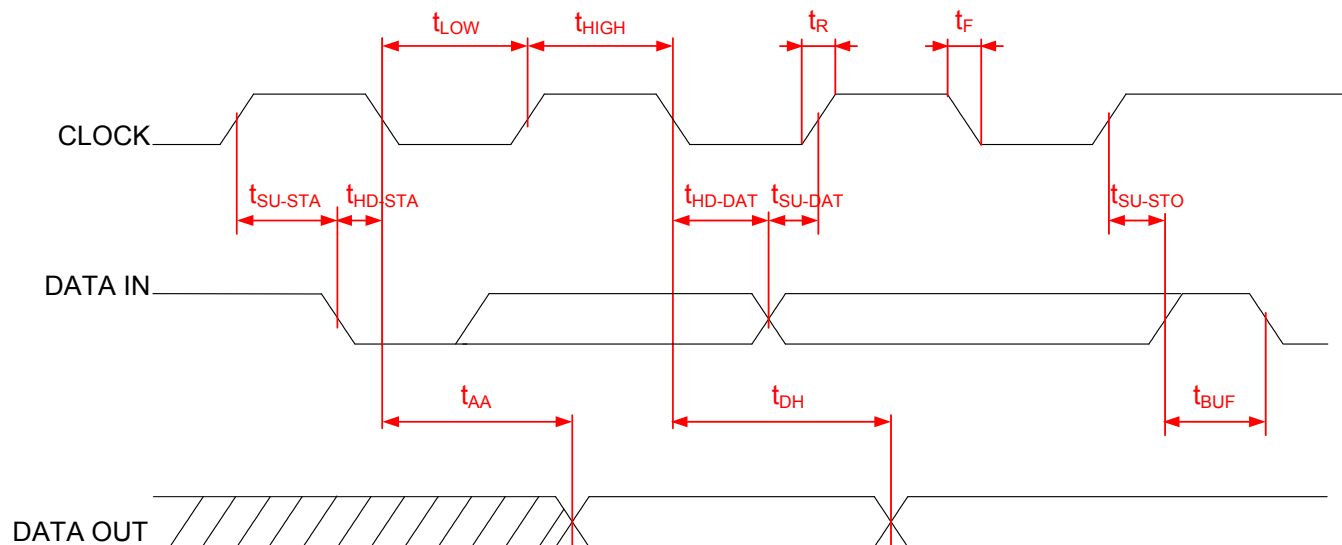


Table 10-1. TWI Data Transfer Timings

| Symbol | Description | Min | Max | Unit |
|--------------|---|-----|-----|---------|
| F_{CLOCK} | Clock Frequency | | 400 | KHz |
| T_{LOW} | Clock Low Pulse Width | 1.2 | | μs |
| T_{HIGH} | Clock High Pulse Width | 1.2 | | μs |
| T_{AA} | Clock Low to Data Out Valid | | 0.9 | μs |
| T_{BUF} | Time the bus must be free before a new transmission can start | 1.2 | | μs |
| T_{HD-STA} | Start Hold Time from CLOCK | 0.6 | | μs |
| T_{SU-STA} | Start Setup Time from CLOCK | 0.6 | | μs |
| T_{HD-DAT} | Data In Hold Time | 0.1 | | μs |
| T_{SU-DAT} | Data In Setup Time | 0.1 | | μs |
| T_{R} | Inputs Rise Time | | 0.3 | μs |
| T_{F} | Inputs Fall Time | | 0.3 | μs |
| T_{SU-STO} | Stop Setup Time | 0.6 | | μs |
| T_{DH} | Data Out Hold Time | 0 | | μs |

Figure 10-4. Write Cycle Waveform

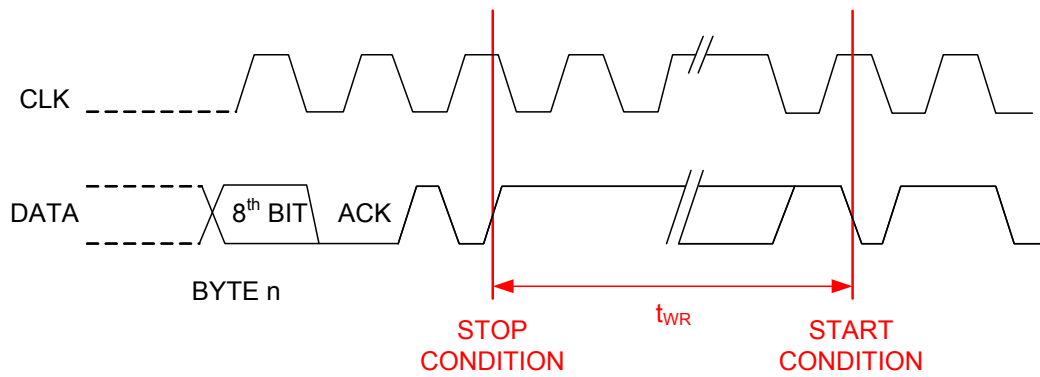


Table 10-2. Write Cycle Time

| Symbol | Description | Min | Max | Unit |
|----------|------------------|-----|-----|------|
| t_{WR} | Write Cycle Time | 34 | 68 | ms |

10.5.3 Dump Mode Characteristics

Figure 10-5. Dump Mode Waveforms

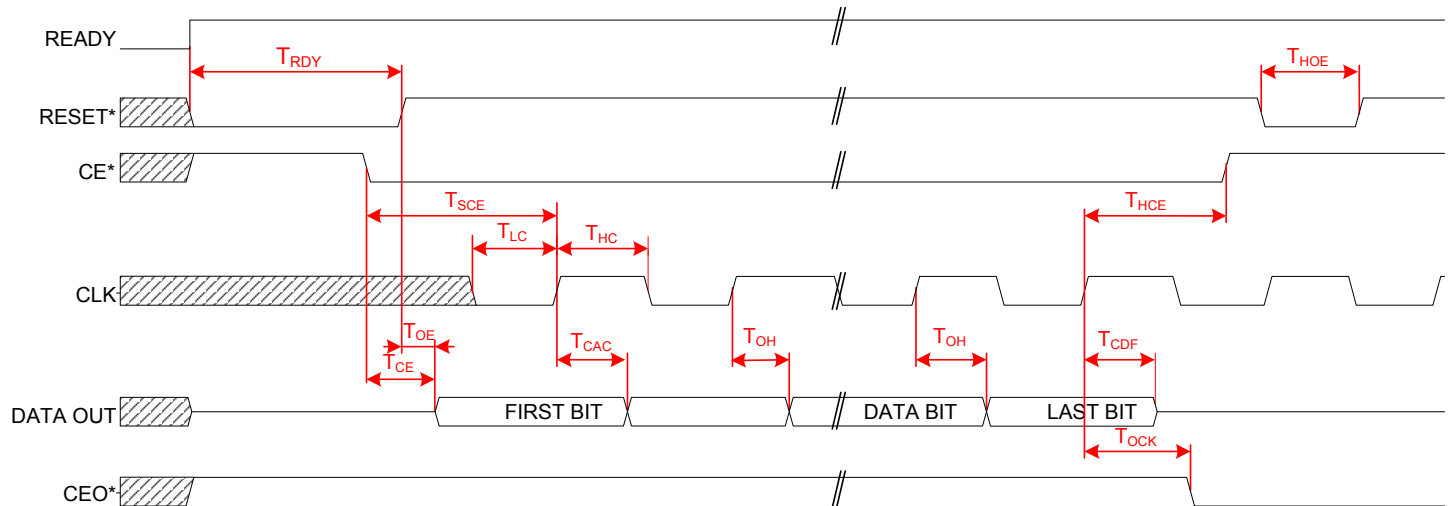


Figure 10-6. Cascade Mode Waveforms

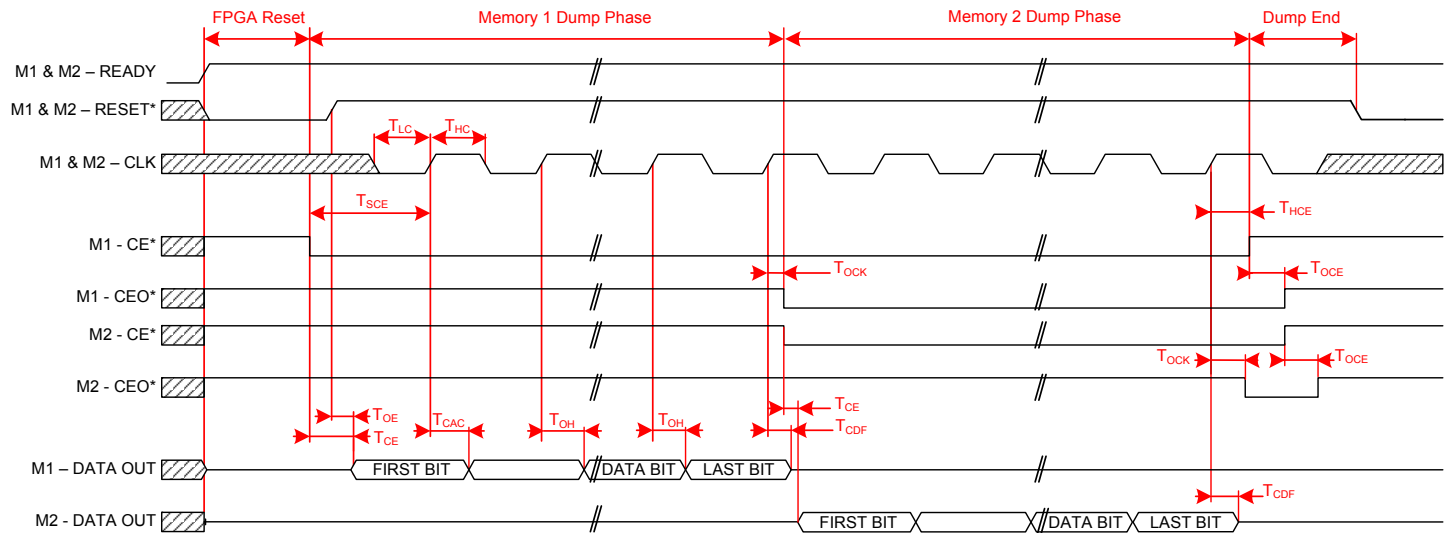


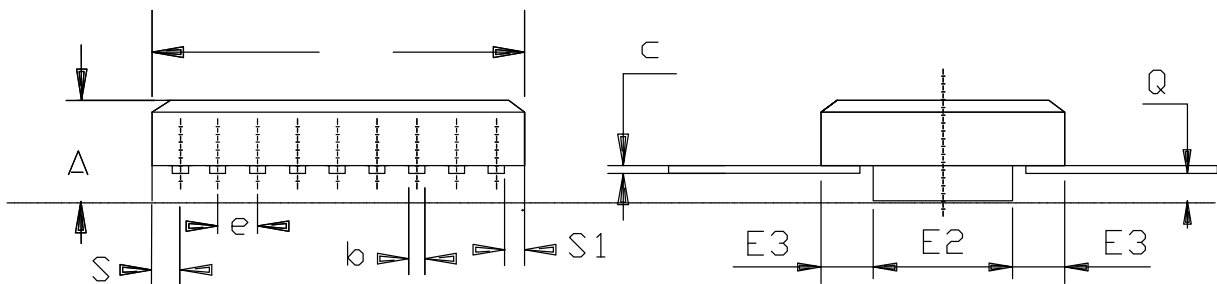
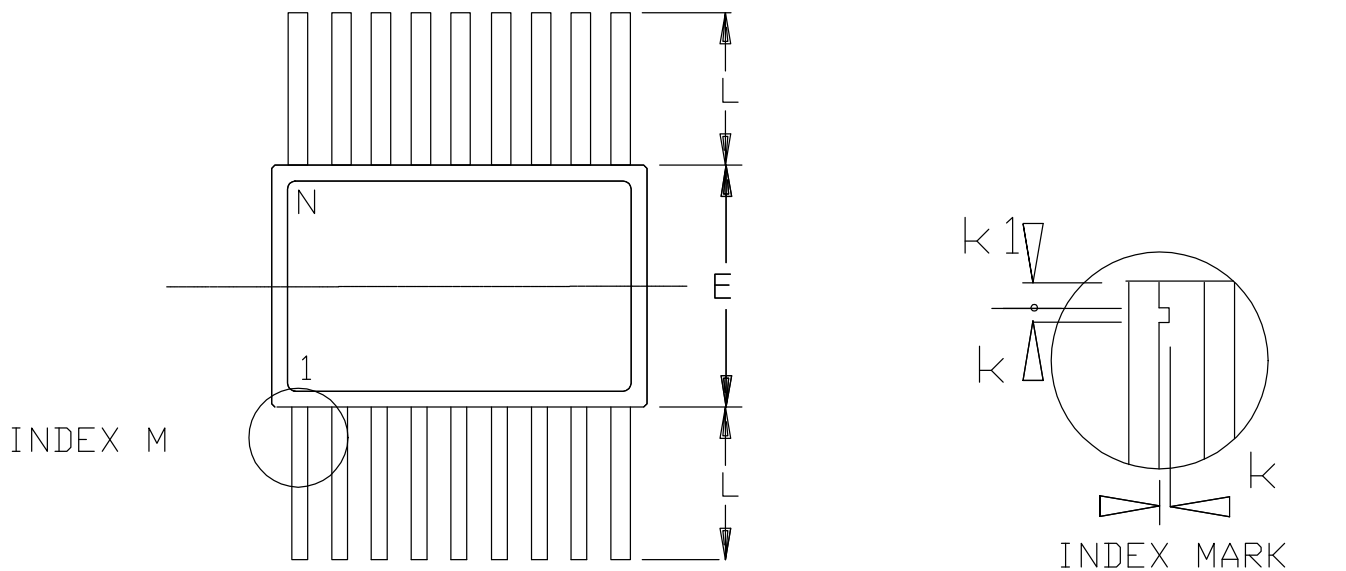
Table 10-3. Dump Mode Timings

| Symbol | Description | Min | Max | Unit |
|-----------|--|-----|-----|------|
| T_{OE} | Data Output Delay from \overline{RESET} | | 35 | ns |
| T_{CE} | Data Output Delay from \overline{CE} | | 40 | ns |
| T_{CAC} | Data Output Delay from CLK | | 40 | ns |
| T_{OH} | Data Hold from \overline{CE} , \overline{RESET} , or CLK | 0 | | ns |
| T_{DF} | Data Float Output Delay from \overline{CE} or \overline{RESET} | | 30 | ns |
| T_{CDF} | Data Float Output Delay from CLK | | 30 | ns |
| T_{OCK} | \overline{CEO} Output Delay from CLK | | 35 | ns |
| T_{OCE} | \overline{CEO} Output Delay from \overline{CE} | | 25 | ns |
| T_{OOE} | \overline{CEO} Output Delay from \overline{RESET} | | 25 | ns |
| T_{LC} | CLK Low Time | 20 | | ns |
| T_{HC} | CLK High Time | 20 | | ns |
| T_{SCE} | \overline{CE} Setup Time to CLK (to guarantee proper counting) | 20 | | ns |
| T_{HCE} | \overline{CE} Hold Time from CLK (to guarantee proper counting) | 5 | | ns |
| T_{HOE} | \overline{RESET} pulse width that guarantees the counter is reset | 60 | | ns |
| F_{MAX} | Maximum Clock Frequency | | 15 | MHz |
| T_{RDY} | \overline{RESET} hold Delay after READY | 0 | | ns |

11. Ordering Information

| Ordering Code | Package | Flow |
|----------------|---------|---------------------|
| AT69170E-DT-E | FP18 | Engineering Samples |
| AT69170E-DT-MQ | | QMLQ |
| AT69170E-DT-SV | | QMLV |

12. Packaging Information



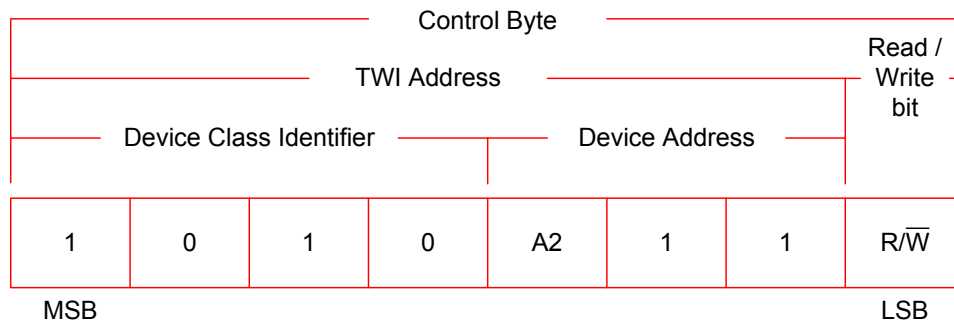
| | MM | | INCH | |
|----|----------|-------|----------|------|
| | Min | Max | Min | Max |
| A | 1.14 | 2.92 | .045 | .115 |
| b | 0.38 | 0.48 | .015 | .019 |
| c | 0.08 | 0.15 | .003 | .006 |
| D | --- | 12.45 | | .490 |
| E | 6.22 | 8.00 | .245 | .315 |
| E2 | 3.30 | | .130 | |
| E3 | 0.76 | --- | .030 | |
| k | 0.20 | 0.39 | .008 | .015 |
| k1 | 0.63 BSC | | .025 BSC | |
| e | 1.27 BSC | | .050 BSC | |
| L | 6.35 | 9.40 | .250 | .370 |
| Q | 0.66 | 1.14 | .026 | .045 |
| S | --- | 1.14 | --- | .045 |
| S1 | 0.13 | --- | .005 | |
| N | 18 | | | |

Note: The package lid is connected to GND

13. Active Errata

13.1 A2 pin input not properly processed

Issue: It's not possible to map the device with two TWI addresses by means of the A2 pin.

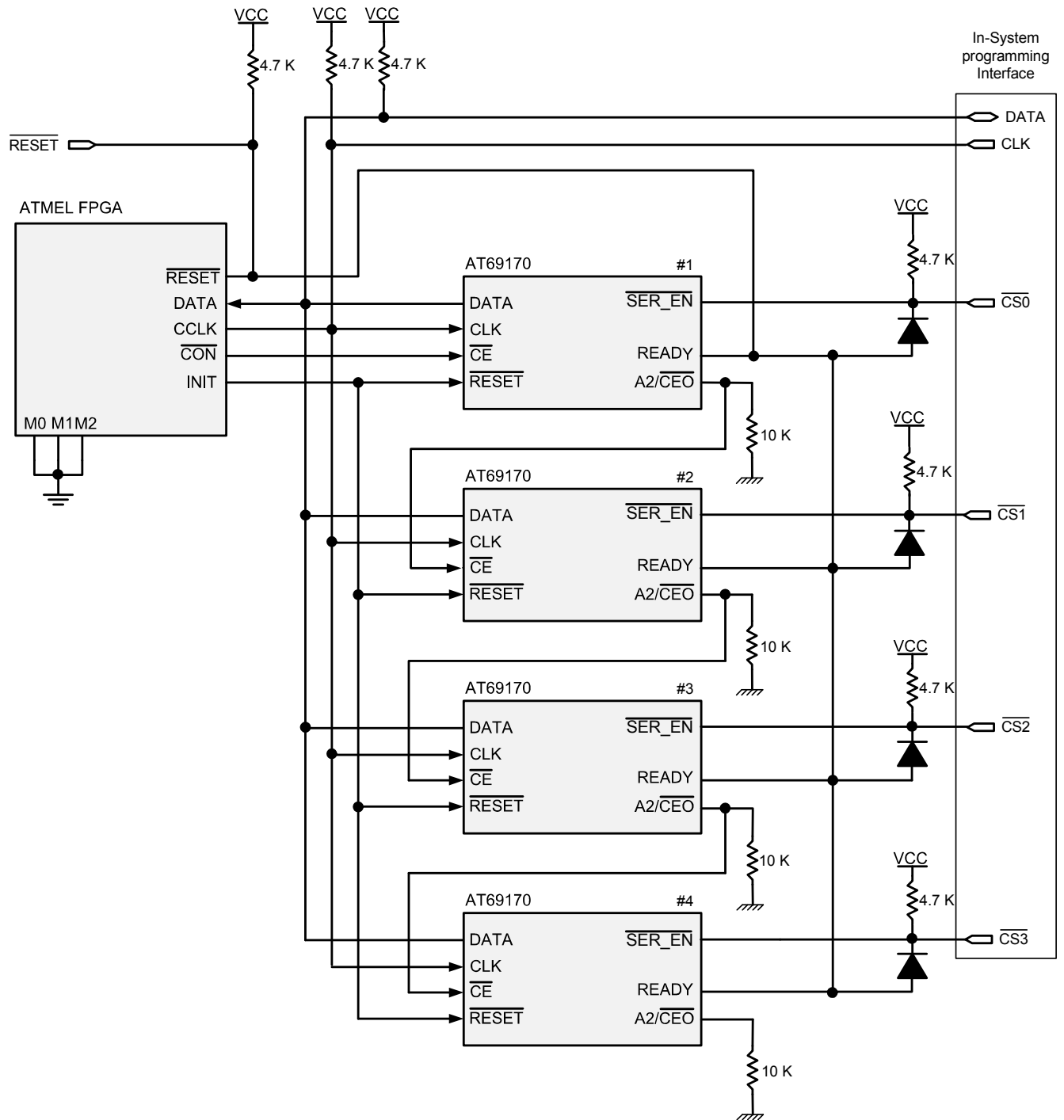


Workaround: There are two ways to work around this issue :

- implement only one AT69170E device on the same TWI bus,
- select only one AT69170E at a time by means of the $\overline{\text{SER_EN}}$ pin if two AT69170E are implemented on the same bus.

If several memory devices need to be cascaded, the following schematic may be used.

Figure 13-1. Cascade mode workaround



13.2 TWI address acknowledgement

Issue: The device acknowledges all TWI addresses whatever the value of R/W bit in the control byte, from 00h to 7Fh except for addresses 04h, 05h, 06h, 07h, 78h, 79h, 7Ah, 7Bh while it should only acknowledge its own TWI addresses given in the table below.

| A2 pin | TWI Device Address |
|--------|--------------------|
| GND | 53 h |
| VCC | 57 h |

However, no TWI write operations are processed by the memory device when the TWI device address supplied by the master does not match its own addresses but this issue may generate address conflicts with devices sharing the same TWI bus.

Workaround: Do not share the TWI bus with devices whose address is in the range of addresses acknowledged by the AT69170E.

13.3 TWI page write corruption

Issue: The very first page written just after the power on is always corrupted whatever the written page. All pages to follow are then correctly written.

Workaround: There are at least three ways to work around this issue.

a) Send a dummy page write sequence before the first valid page write. The dummy page write is corrupted but the first valid page write is correctly processed. The dummy page and the first valid page writes must be done of course at the same page number. A dummy page write may consist for instance to write only the first word of the page.

b) Send the very first page write twice so that the first is corrupted but not the second one.

c) Send a Full Chip Erase command before writing the first valid page write.

13.4 TWI write frequency limitation

Issue: The TWI write does not work at a frequency greater than 200 Khz

Workaround: The TWI write frequency must be limited to 200 Khz inclusive.

13.5 READY signal may not rise

Issue: Depending on the mode the device is powered on, the READY signal may not rise. In this case the device is inoperative in both TWI and DUMP modes.

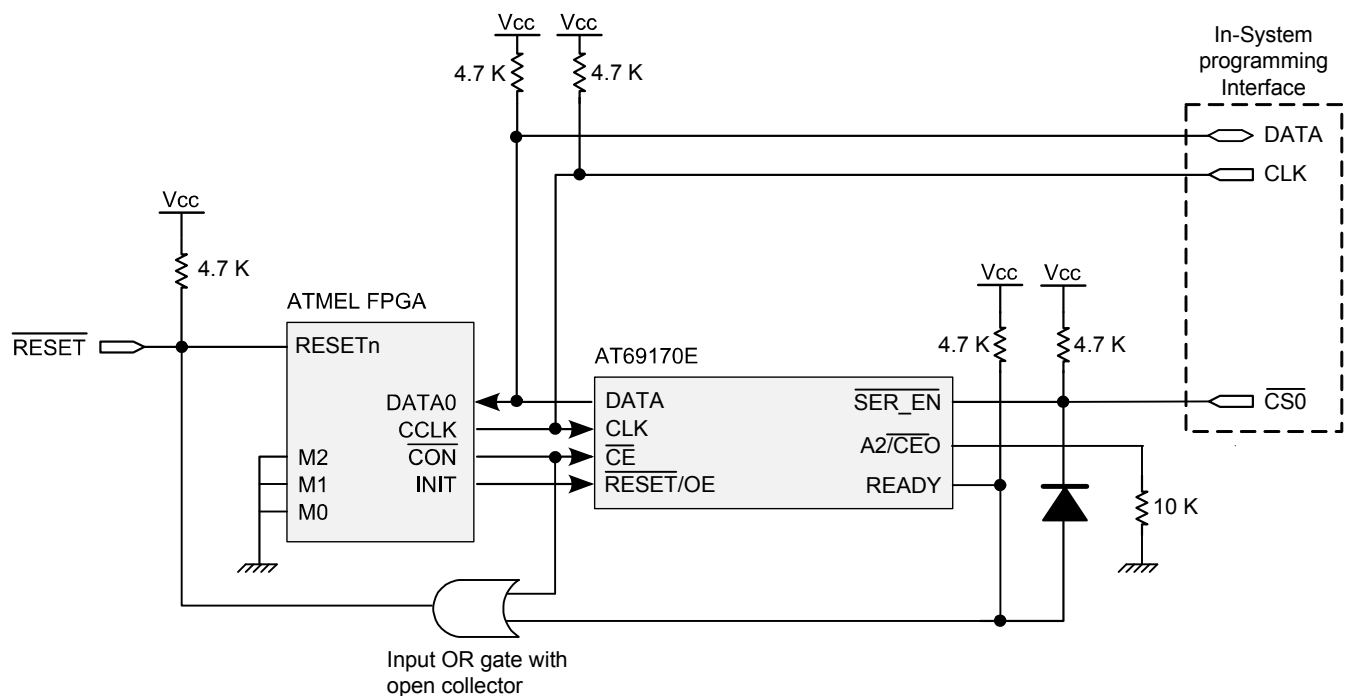
Workaround: To guarantee the rise of the READY signal, the following hardware condition must be applied when the device is powered on : $\overline{\text{RESET}} = 0$ and $\text{SER_EN} = 1$. Whatever the $\overline{\text{RESET}}$ polarity configuration, this hardware condition is true. Once the READY signal has risen, the TWI mode can be selected by setting the SER_EN pin to ground.

13.6 READY signal drops briefly at power off

Issue: Some applications need to switch the memory device off while keeping the FPGA device running. There is then an incompatibility between the memory device and those applications as the FPGA is reset at the time the device memory is switched off and unable to re-load its configuration.

Workaround: The implementation of an input OR gate with open collector between the $\overline{\text{READY}}$ and $\overline{\text{RESETn}}$ signals as described in the schematic below enables to solve the problem. At power up, the FPGA sets the $\overline{\text{CON}}$ and INIT signals to ground. As soon as the memory device releases the $\overline{\text{READY}}$ signal, the FPGA device exits from reset state and downloads its configuration. At the end of the download, the FPGA device sets the $\overline{\text{CON}}$ signal to VCC enabling the memory device to be switched off without resetting the FPGA.

Figure 13-2. Single Device Configuration (Workaround Schematic)



14. Revision History

| Doc. Rev. | Date | Comments |
|-----------|---------|---|
| F | 11/2013 | Update : Status changed from PRELIMINARY to DATASHEET (Complete) on first page Update : Total Dose parameter in "Features" section Update : Figure 8-6 on page 11 Update : Figure 8-11 on page 15 Update : Figure 9-3 on page 24 Update : Figure 9-5 on page 26 Update : Figure 9-6 on page 27 Update : Figure 13-1 on page 36 Update : Figure 13-2 on page 38 Add-on : "Test Loads and Waveforms" on page 29 Add-on : "READY signal drops briefly at power off" on page 38 |
| E | 02/2013 | Initial Document Release |



Enabling Unlimited Possibilities®

Atmel Corporation

1600 Technology Drive
San Jose, CA 95110
USA

Tel: (+1) (408) 441-0311

Fax: (+1) (408) 487-2600

www.atmel.com

Atmel Asia Limited

Unit 01-5 & 16, 19F
BEA Tower, Millennium City 5
418 Kwun Tong Roa
Kwun Tong, Kowloon
HONG KONG

Tel: (+852) 2245-6100

Fax: (+852) 2722-1369

Atmel Munich GmbH

Business Campus
Parkring 4
D-85748 Garching b. Munich
GERMANY

Tel: (+49) 89-31970-0

Fax: (+49) 89-3194621

Atmel Japan G.K.

16F Shin-Osaki Kangyo Bldg
1-6-4 Osaki, Shinagawa-ku
Tokyo 141-0032
JAPAN

Tel: (+81) (3) 6417-0300

Fax: (+81) (3) 6417-0370

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