mosaic

Mosaic Semiconductor Inc.

PUMA 2U4001

PUMA 2U4001-12/15/17/20

Issue 1.0 : November 1990

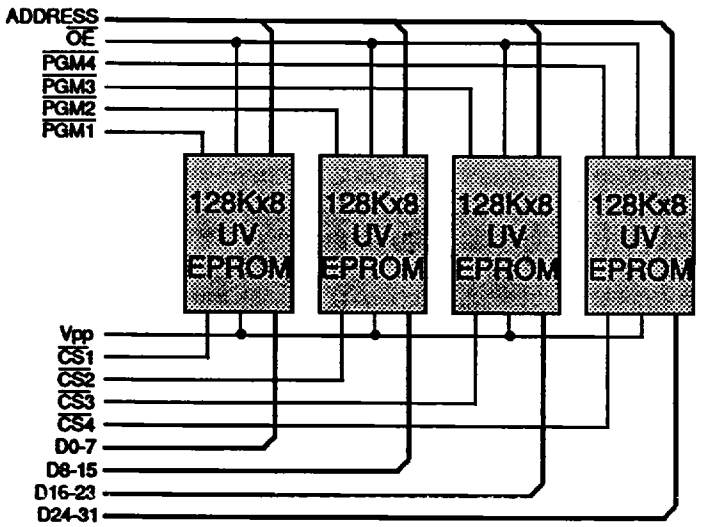
ADVANCE PRODUCT INFORMATION

4,194,304 bit CMOS High Speed Static RAM

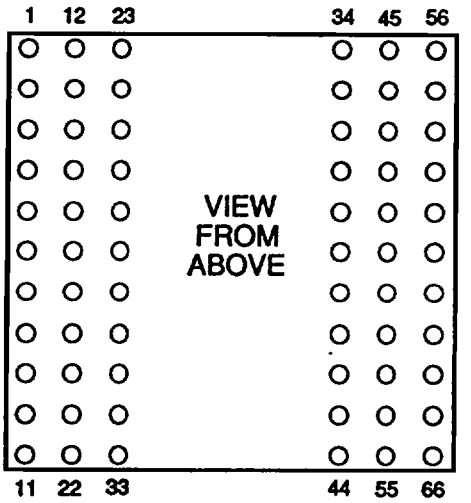
Features

Fast Access times of 120/150/170/200 ns
Pin grid array gives 2:1 improvement over DIL.
Package Suitable for Thermal Ladder Applications.
On board decoupling capacitors.
Configurable as 8 / 16 / 32 bit wide.
Operating Power 40 / 80 / 160 mW (typ)
Standby Power 400 µW (typ)
V_{PP} Voltage of 13.0V±0.25V.
Complete Device Programming in 13 seconds (typ)
May be screened in accordance with MIL-STD-883C.

Block Diagram



Pin Definition

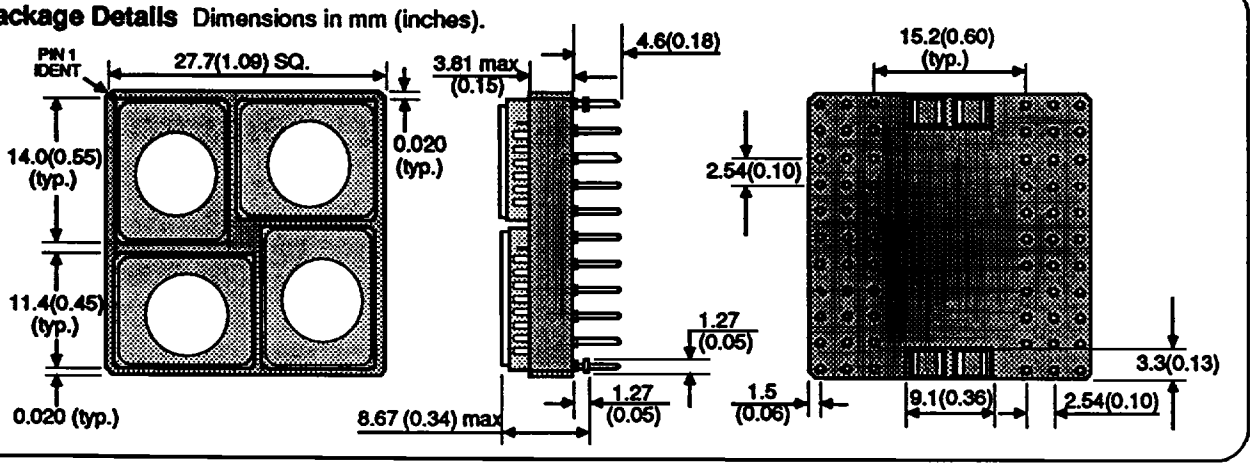


See page 7 for pinout

Pin Functions

A0 - A16	Address Inputs
D0 - D31	Data Inputs/Outputs
$\overline{CS1\text{-}4}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{PGM1\text{-}4}$	Program Enable
NC	No Connect
V_{PP}	Programming Voltage
V_{CC}	Power (+5V)
GND	Ground

Package Details Dimensions in mm (inches).



Absolute Maximum Ratings (1)

Voltage on pins V_{PP} and A_9 (2)	V_{TPP}	-0.6V to +14.0	V
Voltage on pin V_{CC}	V_{TCC}	-0.6V to + 7.0	V
Voltage on any other pins (2)	V_T	-0.6V to $+V_{CC}$+0.5	V
Power Dissipation	P_T	2	W
Storage Temperature	T_{STG}	-65 to +150	°C

Notes : (1) Stresses above those listed may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) Minimum DC input voltage is -0.6V. During transitions inputs may undershoot to -2.0V for periods less than 20 ns. Maximum DC voltage on output pins is V_{CC}+0.75V, which may overshoot to +7.0V for periods less than 20 ns.

Recommended Operating Conditions

		min	*typ*	*max*	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0	-	V_{CC}+1	V
Input Low Voltage	V_{IL}	-0.6	-	0.8	V
Operating Temperature	T_A	0	-	70	°C (2U4001)
	T_{AI}	-40	-	85	°C (2U4001I)
	T_{AM}	-55	-	125	°C (2U4001M, MB)

Capacitance (V_{CC}=5V±10%, T_A=25°C)

Parameter		*Symbol*	*Test Condition*	*typ*	*max*	*Unit*
Input Capacitance	Address, $\overline{OE}$	C_{IN1}	V_{IN} =0V	16	32	pF
	PGM1-4, $\overline{CS1-4}$	C_{IN2}	V_{IN} =0V	4	8	pF
I/O Capacitance	32 Bit Mode	$C_{I/O}$	$V_{I/O}$=0V	8	12	pF

Note: These parameters are calculated and not measured.

AC Test Conditions

*Input pulse levels: GND to 3.0V
*Input rise and fall times: 5 ns
*Input and Output timing reference levels: 1.5V
*Output load: 1 TTL gate + 100pF
*V_{cc}=5V±10%

Operating Modes

This table shows the inputs required to control the operating modes of the EPROMs on the PUMA 2U4001.

MODE		$\overline{CS}$	$\overline{OE}$	$\overline{PGM}$	A_0	A_9	V_{PP}	*OUTPUTS*
Read		V_{IL}	V_{IL}	X	X	X	X	D_{OUT}
Output Disable		X	V_{IH}	X	X	X	X	High Z
Standby		V_{IH}	X	X	X	X	X	High Z
Program		V_{IL}	V_{IH}	V_{IL}	X	X	V_{PP}	D_{IN}
Program Verify		V_{IL}	V_{IL}	V_{IH}	X	X	V_{PP}	D_{OUT}
Program Inhibit		V_{IH}	X	X	X	X	V_{PP}	High Z
Identifier (NOTE 1)	Manufacturer	V_{IL}	V_{IL}	X	V_{IL}	V_H	X	$1E_H$
	Device Code	V_{IL}	V_{IL}	X	V_{IH}	V_H	X	05_H

V_H=12.0V±0.5V
X=V_{IH} or V_{IL}

Notes (1) A1 - A8 = A10 - A16 = V_{IL}
(2) $\overline{CS}$ is accessed through $\overline{CS1-4}$, and $\overline{PGM}$ is accessed through $\overline{PGM1-4}$. For correct operation, $\overline{CS1-4}$ must operate simultaneously for 32 bit operation, in pairs for 16 bit operation, or singly for 8 bit operation. $\overline{PGM1-4}$ must also be operated in the same manner.
(3) The PUMA 2U4001 module is based on ATMEL AT27C010/L devices.

DC Electrical Characteristics (T_A=-55°C to +125°C, V_{CC}=5V ± 10%)

Parameter	Symbol	Test Condition	standard min	standard max	low power min	low power max	Unit
Input Leakage Current Address, $\overline{OE}$	I_{LI1}	V_{IN}=0V or V_{CC}, V_{PP}=V_{PPL}	-	20	-	20	µA
Other Pins	I_{LI2}	V_{IN}=0V or V_{CC}	-	5	-	5	µA
Output Leakage Current	I_{LO}	V_{OUT}=0V or V_{CC}, 8 bit	-	40	-	40	µA
V_{PP} Read Current	I_{PP1}	V_{PP}=V_{PPH}	-	40	-	40	µA
V_{CC} Operating Supply Current 32 bit	I_{CC32}	$\overline{CS}$=V_{IL}(1), I_{OUT}=0mA, f=5MHz(2)	-	200	-	120	mA
16 bit	I_{CC16}	As above	-	102	-	62	mA
8 bit	I_{CC8}	As above	-	53	-	33	mA
Standby Supply Current TTL levels	I_{SB1}	$\overline{CS}$=V_{IH}(1)	-	4	-	4	mA
CMOS levels	I_{SB2}	$\overline{CS}$=V_{CC}±0.3V(1)	-	400	-	400	µA
V_{PP} Voltage During Read Only	V_{PPL}		0	V_{CC}+1	0	V_{CC}+1	V
Output Low Voltage	V_{OL}	I_{OL}=2.1mA.	-	0.45	-	0.45	V
Output High Voltage	V_{OH}	I_{OH}=-400µA.	2.4	-	2.4	-	V

Notes (1) $\overline{CS}$ above are accessed through $\overline{CS1}$-4. These inputs must be operated simultaneoulsy for 32 bit operation, in pairs in 16 bit mode and singly for 8 bit mode.

(2) Maximum active current is the sum of I_{CC} and I_{PP}.

(3) **CAUTION**: the PUMA 2U4001 must not be removed from or inserted into a socket when V_{CC} or V_{PP} is applied.

Electrical Characteristics & Recommended AC Operating Conditions

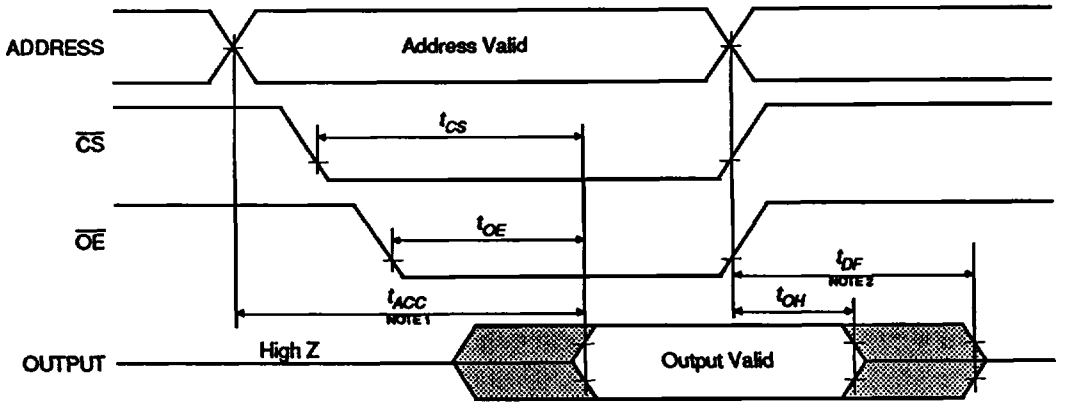
Read Cycle (1,3)

Parameter	Symbol	-12 min	-12 max	-15 min	-15 max	-17 min	-17 max	-20 min	-20 max	Unit
Address to Output Delay	t_{ACC}	-	120	-	150	-	170	-	200	ns
Chip Select Access Time	t_{CE}	-	120	-	150	-	170	-	200	ns
Output Enable to Output Valid	t_{OE}	-	35	-	40	-	65	-	75	ns
Chip Deselect to O/P high Z (2)	t_{DF}	-	30	-	40	-	50	-	55	ns
Output Hold from Address Change	t_{OH}	-	0	-	0	-	0	-	0	ns

Notes (1) V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

(2) This parameter is sampled, not 100% tested.

Read Cycle Timing Waveform



Notes: (1) $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the falling edge of $\overline{CS}$ without impact on t_{ACC}.

(2) t_{DF} is specified from $\overline{OE}$ or $\overline{CS}$ whichever occurs first.

PROGRAMMING OPERATION

The following information is provided for design purposes only.

DC Electrical Characteristics (V_{CC}=6.5V±0.25V,V_{PP}=13.0V±0.25V,T_A=25°C±5°C)

Parameter		*Symbol*	*Test Condition*	*min*	*max*	*Unit*
Input Leakage Current	Address, $\overline{OE}$	I_{LI1}	$V_{CC}=V_{CC}$ max, V_{IN}=0V or V_{CC},$V_{PP}=V_{PPH}$	-	40	µA
	Other Pins	I_{LI2}	$V_{CC}=V_{CC}$ max, V_{IN}=0V or V_{CC},$V_{PP}=V_{PPH}$	-	10	µA
V_{PP} Program Current	32 bit	I_{PP32}	Program, $\overline{CS}=V_{IL}$, $\overline{OE}=V_{IH}$	-	80	mA
	16 bit	I_{PP16}	As above	-	40	mA
	8 bit	I_{PP8}	As above	-	20	mA
V_{CC} Operating Supply Current	32 bit	I_{CC32}	Program and Verify	-	160	mA
	16 bit	I_{CC16}	As above	-	82	mA
	8 bit	I_{CC8}	As above	-	43	mA
V_{CC} Supply Voltage During Program		V_{CC1}		6.25	6.75	V
V_{PP} Voltage During Program		V_{PPH}		12.75	13.25	V
Identifier Select Voltage		V_H		11.5	12.5	V
Output Low Voltage		V_{OL}	I_{OL}=2.1mA.	-	0.45	V
Output High Voltage		V_{OH}	I_{OH}=-400µA.	2.4	-	V

Notes (1) $\overline{CS}$ above are accessed through $\overline{CS1-4}$. These inputs must be operated simultaneoulsy for 32 bit operation, in pairs in 16 bit mode and singly for 8 bit mode.

(2) V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.

(3) A 0.1µF or greater capacitor is required between V_{PP} and GND to suppress voltage transients.

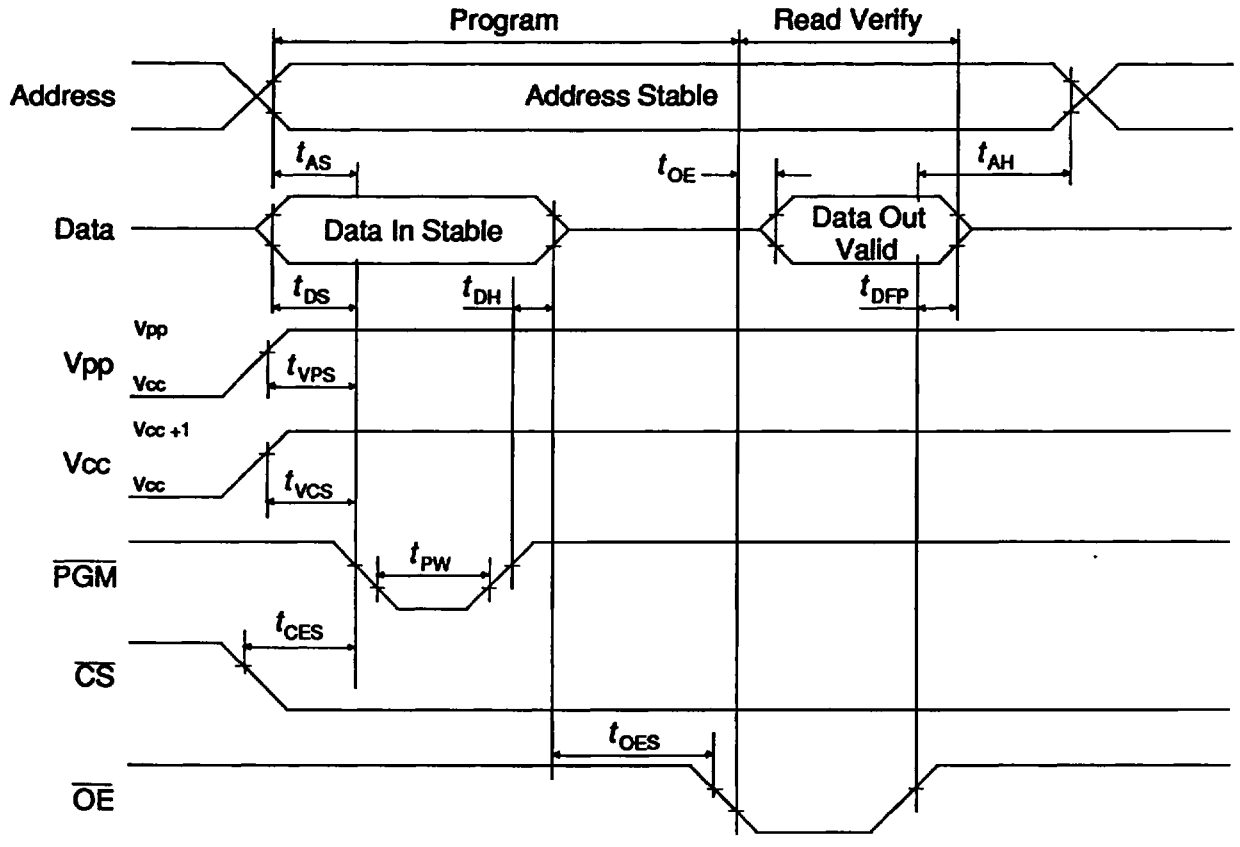
(4) **CAUTION**: the PUMA 2U4001 must not be removed from or inserted into a socket when V_{CC} or V_{PP} is applied.

(3) Programming characteristics are sampled but not 100% tested at worst case conditions.

AC Characteristics

Parameter	*Symbol*	*min*	*typ*	*max*	*Unit*
Address Setup Time	t_{AS}	2	-	-	µs
Output Enable Setup Time	t_{OES}	2	-	-	µs
Data Setup Time	t_{DS}	2	-	-	µs
Address Hold Time	t_{AH}	0	-	-	µs
Data Hold Time	t_{DH}	2	-	-	µs
Output Enable High to Output Float Delay	t_{DFP}	0	-	130	ns
V_{PP} Setup Time	t_{VPS}	2	-	-	µs
Initial Program Pulse Width	t_{PW}	95	-	105	µs
V_{CC} Setup Time	t_{VCS}	2	-	-	µs
Chip Select Setup Time	t_{CES}	2	-	-	µs
Data Valid from Output Enable	t_{OE}	-	-	150	ns

Programming Cycle Timing Waveform



High Performance Programming Algorithm

The PUMA2U4001 can be programmed using the alogorithm shown here. This allows faster programming times without stressing the device or causing deterioration in Data Retention Time. Each of the four devices used on this module is an ATMEL AT27C010; this information, together with the device identifier code, should allow the correct programming alogorithm to be selected automatically.

Although the flow chart specifically refers to a single EPROM, all four devices on the PUMA tile can be programmed simultaneously in 32 bit mode, in pairs in 16 bit mode or singly in 8 bit mode. Obviously 32 bit mode is potentially the fastest programming time, but this makes greater demands on the V_{PP} Supply Current as shown on the Programming Operation DC Characteristics on page 4.

Programming

Upon delivery, or after each erasure, the PUMA 2U4001 has all 4,194,304 bits in the ONE or HIGH state. ZEROs are loaded into the devices through the procedure of programming.

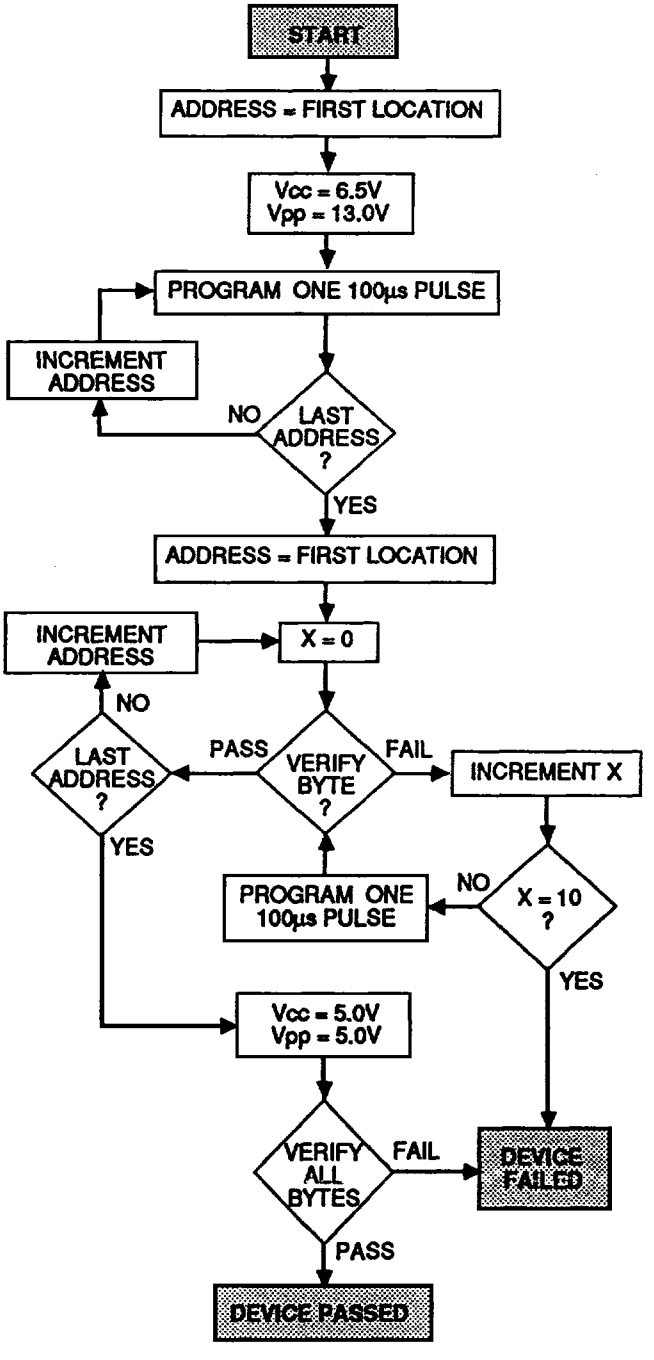
This mode is entered when 13.0V is applied to the V_{PP} pin, V_{CC} is raised to 6.5V, $\overline{CS}$ and $\overline{PGM}$ are at V_{IL} and $\overline{OE}$ is at V_{IH}, as shown on the Table on page 2. Data may be applied in 8, 16 or 32 bits in parallel depending on how $\overline{CS1\text{-}4}$ and $\overline{PGM1\text{-}4}$ are controlled.

The algorithm reduces programming time by initially programming all locations with 100µs pulses without verification. Subsequently a verification/reprogramming loop is excecuted for each address. If the data does not verify, up to 10 such loops can be used, after which, if verification fails, programming stops. This proccess is repeated for each memory location within the PUMA 2U4001.

This algorithm programs at V_{CC}=6.5V in order to ensure that each EPROM bit is programmed to a sufficiently high threshold voltage. After programming is complete, all bytes are compared with the original data with V_{CC}=5.0V±10%.

In order to overcome the voltage drop caused by the inductive effects of the printed circuit board on which the PUMA 2U4001 module is used, it is recommended that a 4.7µF electrolytic capacitor is used between V_{CC} and GND for every two PUMA modules. This capacitor should be placed close to the point where the power supply is routed to the UV EPROM array.

PROGRAMMING ALGORITHM



NOTE: THE ALGORITHM SHOWN HERE MUST BE USED TO ENSURE CORRECT PROGRAMMING OF THE PUMA 2U4001. THIS MAXIMIZES THE DATA RETENTION TIME OF THE UV EPROMS AND DOES NOT STRESS THE MEMORY CELL.

DEVICE IDENTIFIER MODE

The device identifier mode allows the reading out of a binary code from an EPROM which identify its manufacturer and specific type. It is intended to be used to automatically match the device to be programmed with the correct algorithm. This mode operates over the 25°C±5°C temperature range.

In order to activate this mode 12.0V±0.5V must be placed onto address line A9, after which two identifier bytes may be read by toggling A0 from V_{IL} to V_{IH}. All other address lines are held at V_{IL} during this sequence.

The manufacturer code is accessed with A0=V_{IL} and the device code with A0=V_{IH}; the values for these codes are given in the Operating Mode Table on page 2. Note that all identifiers for manufacturer and device codes will possess odd parity, with D7 defined as the parity bit.

ERASE

Complete erasure of the devices used on the PUMA 2U4001 is performed by exposure to an ultraviolet light source giving a dosage of 15WS/cm². This dosage can be obtained by using an ultraviolet lamp with a wavelength of 2537 Å at a minimum intensity of 12,000µW/cm², for approximately 15 - 20 minutes. The PUMA 2U4001 should be directly under and about 1 inch from the light source.

Note that sunlight and fluorescent light may contain sufficient ultraviolet light to erase the programmed information. Although erasure times will be much longer at these levels, the transparent lids on this module should be covered with an opaque label to realise maximum system reliability.

Connection Table

PGA Pin No.	*Signal Name*	*PGA Pin No.*	*Signal Name*	*PGA Pin No.*	*Signal Name*	*PGA Pin No.*	*Signal Name*	*PGA Pin No.*	*Signal Name*
1	D8	2	D9	3	D10	4	A14	5	A16
6	A11	7	A0	8	NC	9	D0	10	D1
11	D2	12	$\overline{PGM2}$	13	$\overline{CS2}$	14	GND	15	D11
16	A10	17	A9	18	A15	19	V_{CC}	20	$\overline{CS1}$
21	NC	22	D3	23	D15	24	D14	25	D13
26	D12	27	$\overline{OE}$	28	NC	29	$\overline{PGM1}$	30	D7
31	D6	32	D5	33	D4	34	D24	35	D25
36	D26	37	A7	38	A12	39	V_{PP}	40	A13
41	A8	42	D16	43	D17	44	D18	45	V_{CC}
46	$\overline{CS4}$	47	$\overline{PGM4}$	48	D27	49	A4	50	A5
51	A6	52	$\overline{PGM3}$	53	$\overline{CS3}$	54	GND	55	D19
56	D31	57	D30	58	D29	59	D28	60	A1
61	A2	62	A3	63	D23	64	D22	65	D21
66	D20								

Military Screening Procedure

Module Screening Flow for high reliability product is in accordance with MIL-STD-883C method 5004 Level B.

MB MODULE SCREENING FLOW		
SCREEN	*TEST METHOD*	*LEVEL*
Visual and Mechanical		
External visual	2017 Condition B (or manufacturers equivalent)	100%
Temperature cycle	1010 Condition C (10 Cycles,-65°C to +150°C)	100%
Burn-In		
Pre Burn-in Electrical	Per Applicable device Specifications at T_A = +25°C (optional)	100%
Burn-In	Method 1015, Condition D, T_A = +125°C	100%
Final Electrical Tests	Per applicable Device Specification	
Static (dc)	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Functional	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Switching (ac)	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Percent Defective Allowable (PDA)	Calculated at Post Burn-in at T_A=+25°C	10%
Quality Conformance	Per applicable Device Specification	Sample
External Visual	2009 Per vendor or customer specification	

Ordering Information

PUMA 2U4001LMB-15

- Speed
  - 12 = 100 ns
  - 15 = 120 ns
  - 17 = 170 ns
  - 20 = 200 ns
- Temp. range/screening
  - Blank = Commercial Temp.
  - I = Industrial Temp.
  - M = Military Temp.
  - MB = Screened in accordance with MIL-STD 883C
- Power Consumption
  - Blank = Standard Part
  - L = Low Power Part
- Memory Type
  - U4001 = 128K x 32 UV EPROM (user configurable as 256K x 8 or 512 K x 16)

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