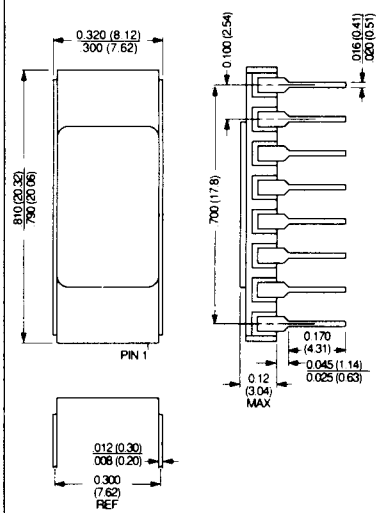
MICRO NETWORKS

MN5903

6-Bit, 75MHz
FLASH A/D CONVERTER

FEATURES

- **6-Bit Resolution**
- **75MHz Conversion Rate**
- **140MHz Input Bandwidth**
- **36dB SNR at 35MHz**
- **Low Harmonic Distortion**
  -44dB at 10MHz
  -36dB at 35MHz
- **Overflow Output (7th bit)**
- **Low Input Capacitance, 25pF**
- **ECL 10K Compatible Output Data**
- **Operating Temperature Range –55°C to +125°C, case (S and T Grades)**
- **Improved Pin-for-Pin Compatibility with AD9000 (MN5903 Model)**



Dimensions in Inches (millimeters)

DESCRIPTION

The MN5903 is an ultra-high speed 6-bit monolithic Analog to Digital converter with a guaranteed conversion speed (strobe frequency) of up to 75MHz. The MN5903 utilizes the "Flash" or parallel principle whereby a field of 64 comparators simultaneously determine the precise analog input. The comparators' outputs are converted to ECL compatible outputs through two encoding stages which are activated by the Encode signal.

The MN5903 is offered in two logic configurations. The MN5903A is designed to be used as a stand-alone 6-bit A/D converter or as a terminating device for a 7 or 8-bit A/D. The MN5903 is designed to be used as a cascading device with the MN5903A for 7 or 8-bit applications. The MN5903 also offers improved performance and pin-for-pin compatibility to the AD9000.

The MN5903 has a low input capacitance of 25pF and a 13kOhm input impedance which allows the input to be easily driven by interfacing circuitry.

The MN5903's broad input bandwidth of 140MHz and low aperture uncertainty of 25psec eliminate the user's need for an additional track and hold amplifier. The MN5903 also provides an overflow signal which indicates when the analog input signal exceeds the $+V_{REF}$ voltage. A hysteresis control function is provided that allows the user to modify the comparator's sensitivity.

Packaged in a small, 16-pin, hermetically sealed package, the MN5903 offers an outstanding Signal-to-Noise-Ratio (SNR) of 36dB at 35MHz and low Total Harmonic Distortion (THD) of –44dB at 10MHz.

Micro Networks offers premium "K" and "T" grades of the MN5903 and MN5903A devices. Their superior performance includes the following specifications which are guaranteed over their full operating temperature range: ±1/2LSB max. differential linearity, ±0.75LSB max. full scale error, 33dB min. SNR at 10MHz analog input and -35dB max. THD at 10MHz analog input.

MN5903 Devices are specified for 0°C to +70°C (case, J and K models) operation, and 55°C to +125°C (case, S and T models) operation. For applications in harsh-environment industrial or military/aerospace systems, S/B and T/B models are available with Environmental Stress Screening.

APPLICATIONS

Radar Systems
Digital Oscilloscopes
Automatic Test Equipment
ECM Equipment
Analytical Systems

July1990

MICRO NETWORKS
324 Clark St., Worcester, MA 01606 (508) 852-5400

MN5903 6 Bit 75MHz FLASH A/D CONVERTER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range (case)	-55°C to +125°C
Specified Temperature Range (case)	
MN5903J,MN5903K	0°C to +70°C
MN5903S, MN5903T	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Positive Supply Voltage ($+V_S$)	-0.3 to +6 Volts
Negative Supply Voltage ($-V_S$)	+0.3 to -6 Volts
Analog Input Voltages (V_{IN}, $+V_{REF}$, $-V_{REF}$)	-3.5 to +2.5 Volts
Encode Input Voltage	$-V_S$ to 0 Volts
Hysteresis Control Voltage (V_H)	0 to 3.0 Volts
Digital Input Voltages	-3.5 to +0.0 Volts
Digital Output Current	20 mA
Analog Ground to Digital Ground Voltage Differential	±0.5 Volts

ORDERING INFORMATION

PART NUMBER — **MN5903XX/B**

Select MN5903 or MN5903A Model.

Select suffix J, K, S, or T for desired performance and specified temperature range.

Add "/B" to "S" or "T" models for Environmental Stress Screening.

ELECTRICAL SPECIFICATIONS (T_A=+25°C, $+V_{REF}$=+1.0V, $-V_{REF}$=-1.0V, $+V_S$=+5.0V, $-V_S$=-5.2V unless otherwise indicated. Specifications apply to all grades unless specific grades are referenced).

PARAMETER	Min	Typ	Max	Units
RESOLUTION		6		Bits
ANALOG INPUTS				
Input Voltage Range over Temperature		±2		Volts
Input Bias Current (Sampling)			700	µA
over Temperature (Note 1)				
Input Bias Current (Latched)			700	µA
over Temperature (Note 1)				
Input Resistance		13		kOhms
Input Capacitance (Note 2)		25	50	pF
Full Power Bandwidth (Note 3)		140		MHz
REFERENCE INPUTS (Note 4)				
Reference Ladder Resistance	80		200	Ohms
Reference Ladder Tempco		0.275		Ohms/°C
Reference Input Bandwidth		20		MHz
TRANSFER CHARACTERISTICS				
Differential Linearity: Initial (+25°C): J, S Grades		0.25	0.5	LSB
over Temperature: J, S Grades			1.0	LSB
Differential Linearity: Initial (+25°C): K, T Grades		0.25	0.35	LSB
over Temperature: K, T Grades			0.5	LSB
Integral Linearity: Initial (+25°C): J, S Grades		0.25	0.5	LSB
over Temperature: J, S Grades			1.0	LSB
Integral Linearity: Initial (+25°C): K, T Grades		0.25	0.35	LSB
over Temperature: K, T Grades			0.5	LSB
No Missing Codes		Guaranteed Over Temperature		
+Full Scale Input Error: Initial (+25°C): J, S Grades		0.3	7/8	LSB
over Temperature: J, S Grades			1.5	LSB
+Full Scale Input Error: Initial (+25°C): K, T Grades		0.15	0.5	LSB
over Temperature: K, T Grades			0.75	LSB
-Full Scale Input Error: Initial (+25°C): J, S Grades		0.25	7/8	LSB
over Temperature: J, S Grades			1.5	LSB
-Full Scale Input Error: Initial (+25°C): K, T Grades		0.15	0.5	LSB
over Temperature: K, T Grades			0.75	LSB
DYNAMIC PERFORMANCE				
Conversion Rate: J Grade	50	70		MHz
Conversion Rate: K, S, and T Grades	75	80		MHz
Conversion Time: J Grade			20	nsec
Conversion Time: K, S, and T Grades			13.3	nsec
Aperture Delay (t_D)		2		nsec
Aperture Uncertainty (Jitter)		25		psec
Output Propagation Delay (t_{PD}) **(Note 2, 5)**	7		12	nsec
Output Hold Time (t_{OH}) **(Note 2, 6)**	8		14	nsec

ELECTRICAL SPECIFICATIONS (Continued)

PARAMETER	Min	Typ	Max	Units
DYNAMIC PERFORMANCE (Continued)				
Transient Response Time (Note 7)		13		nsec
Overvoltage Recovery Time (Note 8)		11		nsec
Output Rise or Fall Time: J Grade (Note 9)			5	nsec
Output Rise or Fall Time: K, S, and T Grades (Note 9)			4.5	nsec
ENCODE INPUT				
Logic "1" Voltage over Temperature	-1.1			Volts
Logic "0" Voltage over Temperature			-1.5	Volts
Logic "1" Current over Temperature			100	µA
Logic "1" Current over Temperature			100	µA
Encode Pulse Width High (t_{PWH})	6.6			nsec
Encode Pulse Width Low (t_{PWL})	6.6			nsec
AC LINEARITY (Note 10)				
Dynamic Linearity (Note 11)		0.5		LSB
In-Band Harmonics				
(DC to 1MHz)		48		dBc
(1MHz to 5MHz)		48		dBc
(5MHz to 8MHz)		46		dBc
Signal to Noise Ratio (Note 12)				
(540kHz Analog Input): J and S Grades	31	38		dB
(540kHz Analog Input): K and T Grades	35	38		dB
(10MHz Analog Input): J and S Grades		37		dB
(10MHz Analog Input): K and T Grades	35	37		dB
(10MHz Analog Input): K and T Grades over Temperature	33			dB
(20MHz Analog Input)		37		dB
(35MHz Analog Input): J and S Grades		36		dB
(35MHz Analog Input): K and T Grades	31	36		dB
Total Harmonic Distortion (THD)				
(2MHz Analog Input)		-47		dB
(10MHz Analog Input): J and S Grades		-44		dB
(10MHz Analog Input): K and T Grades		-44	-38	dB
over Temperature			-35	dB
(20MHz Analog Input)		-43		dB
(35MHz Analog Input): J and S Grades		-34		dB
(35MHz Analog Input): K and T Grades		-34	-30	dB
DIGITAL OUTPUTS (Note 13)				
Logic "1" Voltage over Temperature	-1.1			Volts
Logic "0" Voltage over Temperature			-1.5	Volts
POWER SUPPLIES				
Positive Supply Current (+5.0V)		71	85	mA
over Temperature			90	mA
Negative Supply Current (-5.2V)		65	75	mA
over Temperature			80	mA
Nominal Power Dissipation		693		mW
Reference Ladder Dissipation		20		mW

SPECIFICATION NOTES

1. Measured with $A_{IN}=+V_{REF}$.
2. Listed specification is for reference only and is not tested.
3. Full Power Bandwidth is the input frequency at a 75MHz sampling rate at which the reconstructed output amplitude drops 3dB with respect to the output.
4. The differential reference voltages may be varied under normal operating conditions from ±0.5 Volts to ±2.0 Volts. $+V_{REF}$ must always be greater than $-V_{REF}$.
5. Measured from leading edge of ENCODE to data out on Bit 1 (MSB).
6. Measured from trailing edge of ENCODE to data out on Bit 1 (MSB).
7. For a full-scale step input, 6 bit accuracy is obtained in the specified time.
8. Time to recover to 6 bit accuracy after an overvoltage whose input is equal to 150% of the full-scale input voltage.
9. Measured on the MSB (Bit 1) only.
10. Measured at 50MSPS encode rate.
11. Analog Input frequency =15MHz.
12. RMS signal to RMS noise.
13. Measured with outputs terminated with 100 Ohm resistors to -2.0 volts.

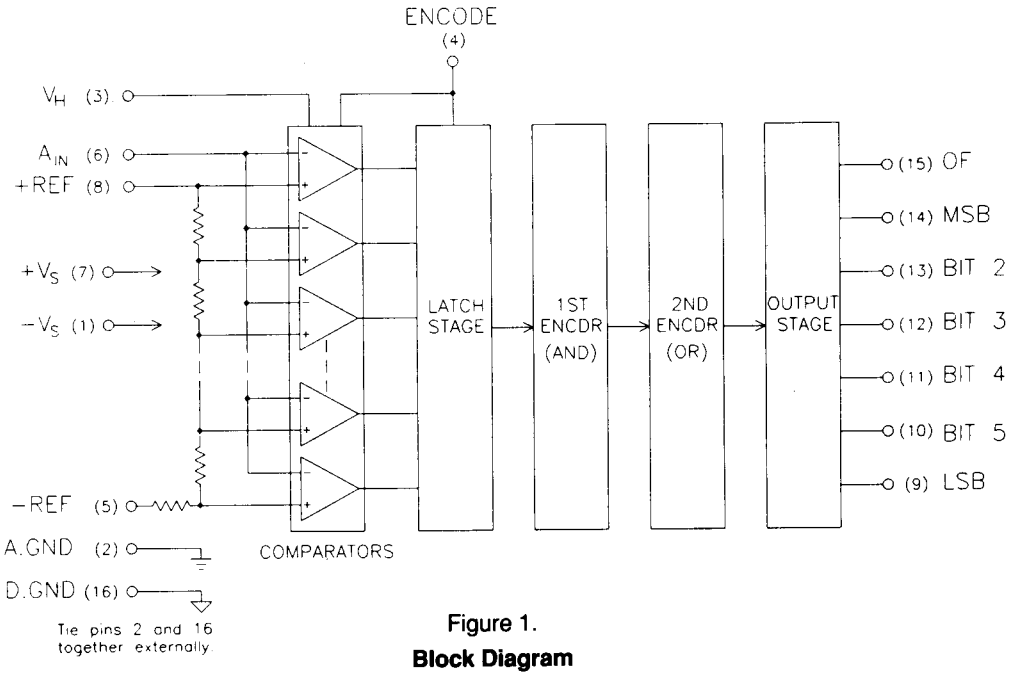


Figure 1.

Block Diagram

APPLICATION INFORMATION

The MN5903A has a nonreturn-to-zero output logic coding when $A_{IN} \geq +V_{REF}$. This coding is desirable for applications that require stand-alone 6-bit A/D converters. The MN5903 has a return-to-zero logic coding when $A_{IN} \geq +V_{REF}$. (See Digital Output Coding.) This facilitates the cascading of the MN5903 with the MN5903A for applications requiring 7 or 8-bits. The MN5903's coding is usually not desired for stand-alone 6-bit applications as additional external circuitry is required to convert the output logic to nonreturn-to-zero coding. The MN5903 is recommended for those applications that can benefit from superior performance and pin-for-pin compatibility with the AD9000.

The MN5903 and MN5903A have open emitter outputs which allow the output of several devices to be WIRE-OR'D when cascaded for increased resolution. Figure 3 shows how the MN5903 and MN5903A may be stacked together for usage as a 7-bit A/D converter.

HYSTERESIS CONTROL FUNCTION

The MN5903 has a Hysteresis Control Voltage Input, V_H, which allows the user to affect the comparators' sensitivity. An input voltage of 0V to +3V applied to V_H (Pin 3) causes the comparator hysteresis to vary from approximately 15mV to 50mV. Increasing the comparator hysteresis reduces the error rate (number of false full-scale output codes in a given period). The MN5903 is tested with the V_H input open and produces a very low error rate. Use of the hysteresis control function may be considered for error sensitive applications, especially those employing a high (greater than 50MHz) encode rate. The V_H input, when used, should be decoupled to ground through a 0.1µF ceramic capacitor.

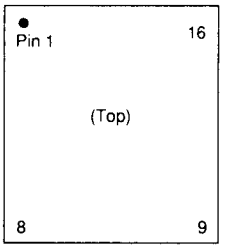
LAYOUT SUGGESTIONS

It is strongly recommended that a substantial ground plane be placed under and around the MN5903. It is recommended that the MN5903's Analog Ground and Digital Ground be connected together at the MN5903 and also connected to the ground plane.

The power supplies and reference inputs should be decoupled to ground directly at the MN5903 with 0.1µF ceramic capacitors in order to reduce the effects of system noise on converter accuracy. Chip capacitors will produce the best results because they do not have the lead inductance inherent to discrete devices. The reference inputs should be driven from a low source impedance. This will help to minimize errors caused by noise on the reference source and also minimize errors otherwise caused by the reference's source impedance. Test Figure 4 includes circuitry that has been proven to be a simple and effective means of driving the reference inputs.

PIN DESIGNATIONS

Pin	Symbol	Function	Pin	Symbol	Function
1	$-V_S$	Negative Supply Voltage.	16	Dig Gnd	Digital Ground
2	Ana Gnd	Analog Ground	15	OF	Overflow Signal
3	V_H	Hysteresis Control Voltage	14	Bit 1	Bit 1 (MSB)
4	Encode	Signal	13	Bit 2	Bit 2
5	$-V_{REF}$	Negative Reference Voltage	12	Bit 3	Bit 3
6	A_{IN}	Analog Input	11	Bit 4	Bit 4
7	$+V_S$	Positive Supply Voltage	10	Bit 5	Bit 5
8	$+V_{REF}$	Positive Reference Voltage	9	Bit 6	Bit 6 (LSB)



DIGITAL OUTPUT CODING

MN5903 Analog Input	Digital Output						
	OF	MSB (Bit 1)				LSB (Bit 6)	
$+V_{REF}$	1	0	0	0	0	0	0
$+V_{REF}$ -1/2LSB	*	*	*	*	*	*	*
$+V_{REF}$ -3/2LSB	0	1	1	1	1	1	*
+1/2LSB	0	1	0	0	0	0	*
0	0	1	0	0	0	0	0
-1/2LSB	0	*	*	*	*	*	*
$-V_{REF}$ +1/2LSB	0	0	0	0	0	0	*
$-V_{REF}$	0	0	0	0	0	0	0

MN5903A Analog Input	Digital Output						
	OF	MSB (Bit 1)				LSB (Bit 6)	
$+V_{REF}$	1	1	1	1	1	1	1
$+V_{REF}$ -1/2LSB	*	1	1	1	1	1	1
$+V_{REF}$ -3/2LSB	0	1	1	1	1	1	*
+1/2LSB	0	1	0	0	0	0	*
0	0	0	1	0	0	0	0
-1/2LSB	0	*	*	*	*	*	*
$-V_{REF}$ + 1/2LSB	0	0	0	0	0	0	*
$-V_{REF}$	0	0	0	0	0	0	0

Note: * indicates a bit transition whereby the output bit(s) is(are) changing from "1" to "0" or vice versa.
The analog input voltages shown above are the theoretical voltages for the corresponding digital output.
Example: With an analog input of $-V_{REF}$ + 1/2LSB, the output code will be at the transition of the codes 0 000000 and 0 000001.

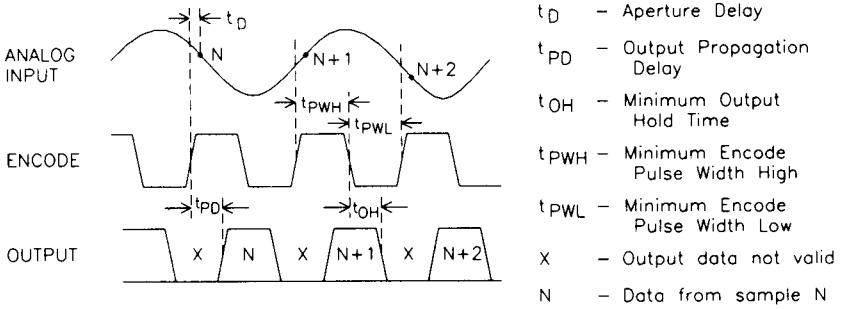


Figure 2.
Timing Diagram

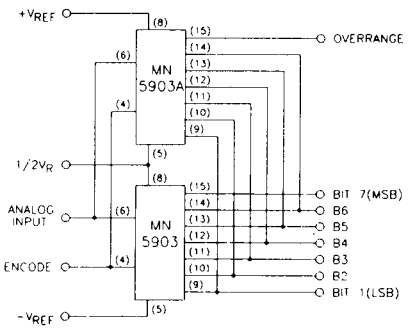


Figure 3.
Cascading 7-Bit Operation

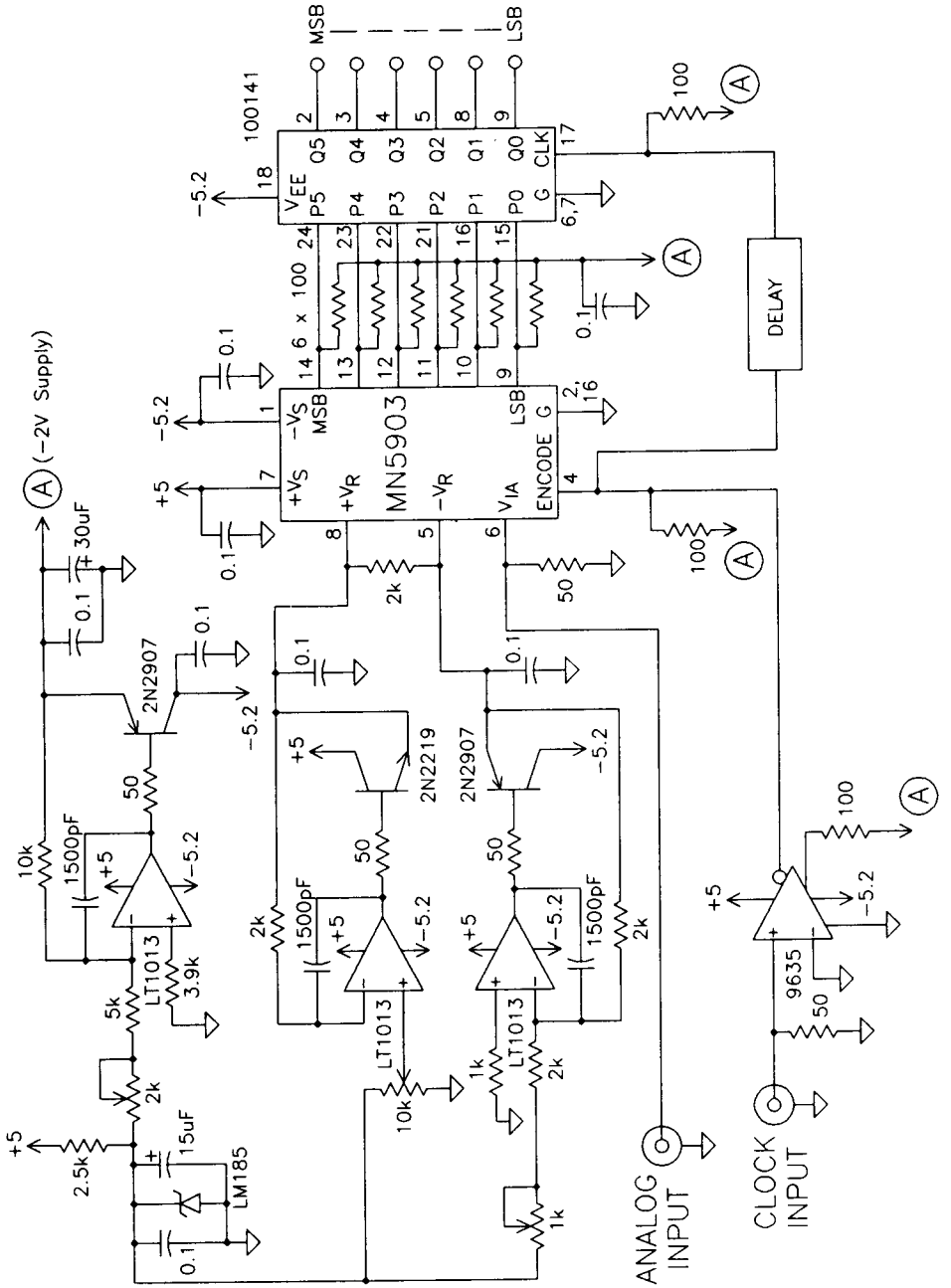


Figure 4.
Test Circuit