PW-8X075P6

MAGNUM MOTOR DRIVE SERIES™
75A, 600V MAGNUM MOTOR DRIVES

Make sure the next Card you purchase has...

DDC on Board™

FEATURES

- 600 Vdc Drive for 270 Vdc Motors
- 75 Amps @25°C, 50 Amps @85°C
- Operates with Brushless, Brush,and Induction Motors
- Input to Output Ground Isolation with Floating Output Stage
- Short Circuit Protection
- Trapezoidal or Sinusoidal Compatible
- DSP/Microprocessor Compatible
- PW-83075P6 - Half-Bridge Drive
- PW-84075P6 - Half-Bridge Drive with Current Sense
- PW-85075P6 - Half-Bridge Drive with Regenerative Clamp

DESCRIPTION

The PW-83075P6, PW-84075P6 and PW-85075P6 are half-bridge IGBT drive modules containing isolated switch drivers, a pair of solid-state switches, and an isolated power supply. In addition, the PW-84075P6 contains current sensing feedback and the PW-85075P6 contains a regenerative clamp protection circuit. The three modules can be used in any combination to create drives for brush, brushless DC, or AC induction motors. The current sense signal and logic inputs are compatible with DSP/microprocessors and/or FPGA/ASIC circuits used to control the motor drives. These modular drives are capable of operating from either a ±135Vdc or 270Vdc power source that is electrically isolated from the logic input signals. The modules are fault tolerant from output shorts, loss of any or all power supplies, and power supply sequencing.

APPLICATIONS

The high reliability and flexibility of these drives make them suitable for Military and Aerospace applications. Among the many applications are: actuator systems for primary and secondary flight controls on aircraft, fan and compressor motor drives for environment conditioning, pump motors for fuel and hydraulic fluid, antenna and radar positioning, and thrust vector position control of missiles, drones, and RPV's.

FOR MORE INFORMATION CONTACT:

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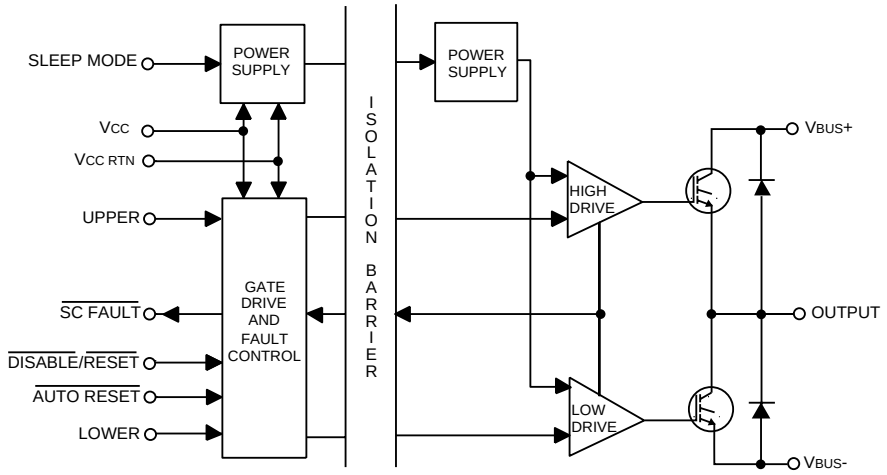


FIGURE 1A. PW-83075P6 BLOCK DIAGRAM

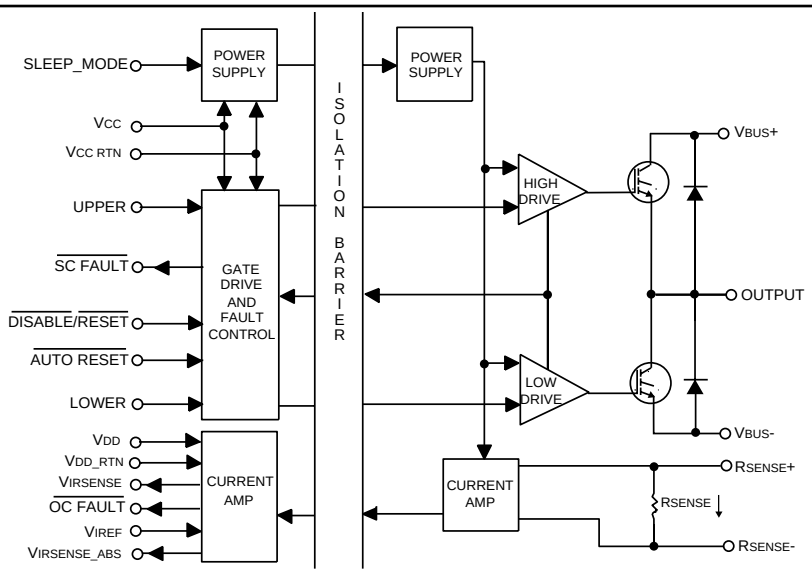


FIGURE 1B. PW-84075P6 BLOCK DIAGRAM

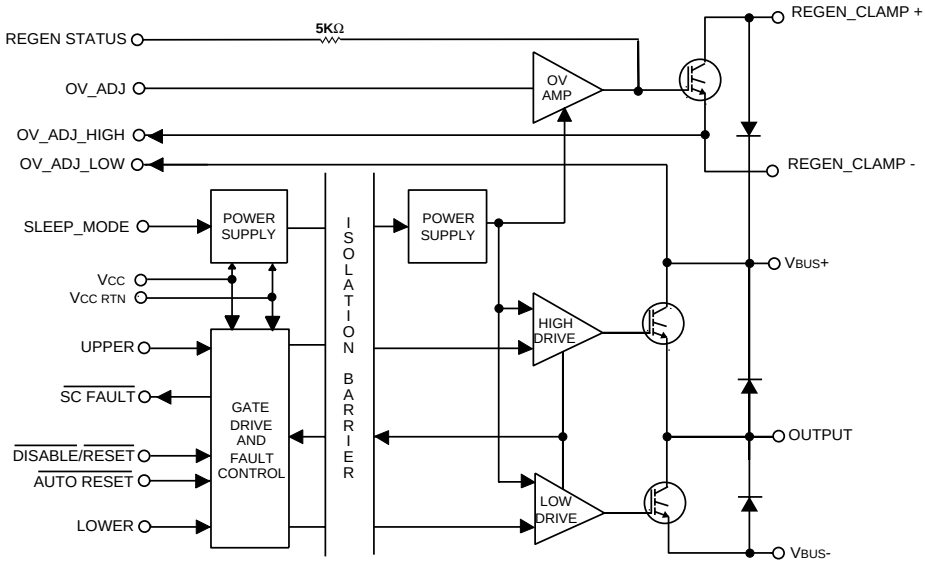


FIGURE 1C. PW-85075P6 BLOCK DIAGRAM

TABLE 1. PW-8X075P6 ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNITS
Drive Supply Voltage	V_{BUS}+ to V_{BUS}-	600	Vdc
Logic Power-In Supply Voltage	V_{CC}, V_{DD}	5.5	Vdc
Input Logic Voltage	UPPER, LOWER, $\overline{\text{DISABLE}}$/$\overline{\text{RESET}}$, SLEEPMODE, $\overline{\text{AUTO RESET}}$	5.5	Vdc
Reference Input Voltage	V_{IREF}	V_{DD} + 0.5	Vdc
Continuous Output Current	I_O	75	A
Peak Output Current (1 ms, Tc = 25°C)	I_{PEAK}	200	A
Storage Temperature Range	Tcs	-65 to +150	°C
Intermittent Case Operating Temperature	T_{CI}	-55 to +125	°C
Continuous Case Operating Temperature	Tc	-55 to +100	°C
Junction Temperature, Power Devices	Tj	+150	°C
Junction Temperature, Other Components	T_J	+125	°C
Ground Isolation Voltage (Note 1)	V_{ISO}	2500	Vdc

Note 1: From V_{CC-RTN} to V_{BUS}+, V_{BUS}-, OUTPUT, REGEN_CLAMP+, R_{SENSE}+, R_{SENSE}-.

TABLE 2. PW-8X075P6 SPECIFICATIONS
(V_{CC} = V_{DD} = 5V UNLESS OTHERWISE SPECIFIED, T_C = -55°C TO +100°C FOR MIN, MAX VALUES, T_C = +25°C FOR TYPICAL VALUES.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT STAGE						
Drive Supply Voltage (motor)	V_{BUS}+ to V_{BUS}-	Unipolar/Bipolar		270	600	Vdc
Output Switch Transistors (each)						
Continuous Current Drive	I_O	+25°C case			75	A
		+85°C case			50	A
Turn-on energy per pulse	E_{ON}	V_{CE} = 270V, I = 50A T_j = +125° C		0.68		mJ
Turn-off energy per pulse	E_{OFF}	V_{CE} = 270V, I = 50A T_j = +125° C		4.5		mJ
Peak Current	I_{PEAK}	+85°C case,≤10 ms			150	A
Short Circuit Trip Current (Note 1)	I_{SC}	≤5 µs	200	350	400	A
Output Voltage Drop (IGBT)	$V_{CE(SAT)}$	I_O = 50A		2.2	2.6	Vdc
FLYBACK DIODE						
Forward Voltage	V_F	I_O = 50A		1.7	1.9	Vdc
Reverse Recovery Time @ Tj = +125° C	trr (FIGURE 2B)	I_O = 50A		175		ns
Reverse recovery Peak Current	Irr (FIGURE 2B)	di/dt = 480A/µs I_F = 50A (90 °C)		19	33	A
Reverse Leakage Current @ Tj = +25° C	Ir	V_{BUS} = 480Vdc		30	325	µA
Reverse Leakage Current @Tj = +125° C	Ir	V_{BUS} = 480Vdc			17	mA
OUTPUT SWITCHING CHARACTERISTICS (SEE FIGURE 3)						
Turn-on Propagation Delay	t_d(on) (FIGURE 2H)		150	430	650	ns
Turn-off Propagation Delay	t_d(off) (FIGURE 2H)		740	790	1800	ns
$\overline{\text{DISABLE}}$ / $\overline{\text{RESET}}$ Propagation Delay	t_{sd} (FIGURE 2C)		25	33	45	µs
Turn-on Rise Time	t_r (FIGURE 2H)		100		200	ns
Turn-off Fall Time	t_f (FIGURE 2H)		140		200	ns
Sleep_Mode off Delay	td (sleep_off) (FIGURE 2D)			3.7		ms
Output Switching Frequency	f_{PWM} (FIGURE 2A)		0		35	KHz

TABLE 2. PW-8X075P6 SPECIFICATIONS (CONT.)
(V_{CC} = V_{DD} = 5V UNLESS OTHERWISE SPECIFIED, T_C = -55°C TO +100°C FOR MIN, MAX VALUES, T_C = +25°C FOR TYPICAL VALUES.)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
CONTROL INPUTS						
UPPER, LOWER, DISABLE/RESET						
AUTO RESET		V_{CC} = 4.5V				
High Level Input Voltage	VIH		1.55	2.5	3.15	Vdc
Low Level Input Voltage	VIL		0.9	1.6	2.45	Vdc
Hysteresis Voltage	V_{HYST}		0.4	0.9	2.1	Vdc
UPPER, LOWER						
High Level Input Current	I_{IH}	Vin = VCC	22	23	24	µA
Low Level Input Current	I_{IL}	Vin = 0V	0	0.1	100	nA
DISABLE/RESET						
High Level Input Current	I_{IH}	Vin = VCC		0		µA
Low Level Input Current	I_{IL}	Vin = 0V	22	23	24	µA
AUTO RESET						
High Level Input Current	I_{IH}	Vin = VCC		0		µA
Low Level Input Current	I_{IL}	Vin = 0V	1.3	1.4	1.5	mA
SLEEP_MODE						
High Level Input Voltage	V_{IH}	V_{CC} = 4.5V	2.4			Vdc
Low Level Input Voltage	V_{IL}	V_{CC} = 4.5V			0.8	Vdc
High Level Input Current	I_{IH}	Vin = VCC		0.1		µA
Low Level Input Current	I_{IL}	Vin = 0V	0.4		0.5	mA
OUTPUT SWITCHING						
UPPER-LOWER DEADTIME	tdead (FIGURE 2A)		1.0			µs
AUTO RESET Delay to SC FAULT off	tdoff.auto			202		ms
AUTO RESET Delay to output enabled	tdon.auto (FIGURE 2F)			3.0		ms
DISABLE/RESET pulsewidth to clear SC FAULT	tpw.reset (FIGURE 2G)		200			ns
Cycle time between AUTO RESET retries	tcycle.auto (FIGURE 2E)	(See Note 2)	40	100		ms
CONTROL OUTPUTS						
SC FAULT						
High Level Output Current	ISCFLTH	Vo = V_{CC}	22	23	24	µA
Low Level Output Current	ISCFLTL	Vo = 0.4V	5	10		mA
THERMAL						
Maximum Thermal Resistance - IGBT	θjc	Each Output Switch		0.5	0.55	°C/W
- Diode	θjc			0.8	0.87	°C/W
Junction Temperature Range	Tj		-55		+150	°C
Case Operating Temperature	Tc		-55		+100	°C
Case Storage Temperature	Tcs		-65		+150	°C
MECHANICAL						
Maximum Lead Soldering Temp	Ts				+250	°C
Mounting Torque			3		6.5	in-lbs
Weight					3.1 (88)	oz (gr)

Note 1: V_{BUS}+ to V_{BUS}- must be ≥ 10V (during short circuit) for short circuit protection to operate.
Note 2: AUTO RESET tied to SC FAULT

TABLE 3. PW-83075P6 SPECIFICATIONS
(T_C= +25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
POWER AND LOGIC SUPPLY						
Voltage	V_{CC}, V_{DD}		4.5	5	5.5	V
Logic Supply Current (see Note 1)	I_{CC}	SLEEP MODE		11		mA
		f_{PWM} = 25KHz		110	200	mA

Note 1: During initial power-on @ Vcc ~3.5 Vdc, a transient current pulse of up to 100mA above Icc may be observed.

TABLE 2 TIMING DIAGRAMS

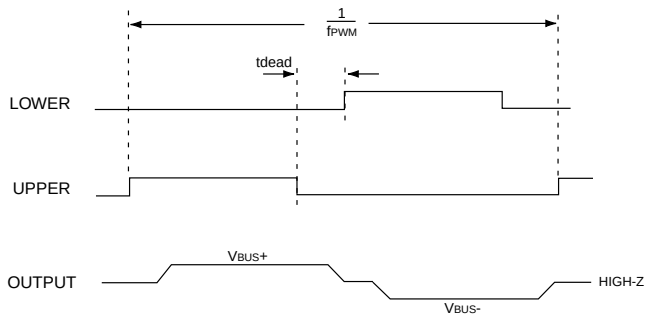


FIGURE 2A. STANDARD TIMING OPERATION

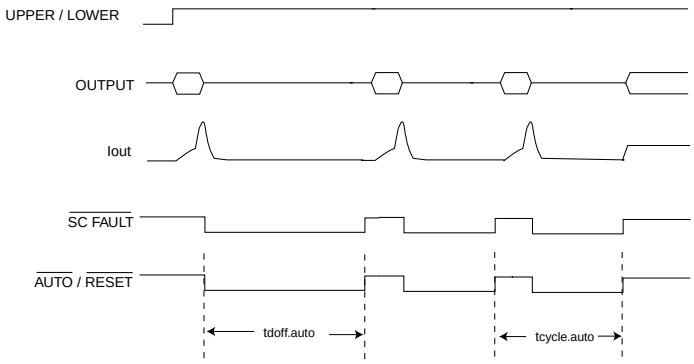


FIGURE 2E. AUTO RESET OPERATION WITH SHORT AT TURN ON THAT CLEARS

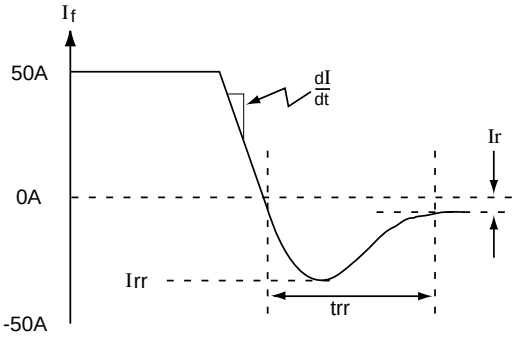


FIGURE 2B. DIODE REVERSE RECOVERY

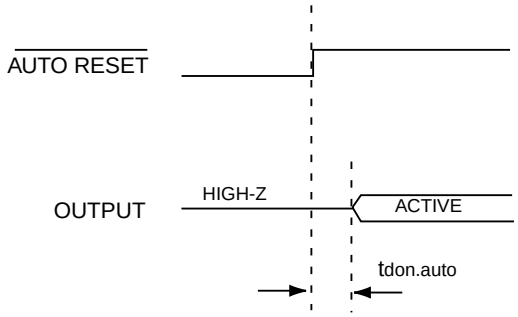


FIGURE 2F. tdon.auto TIMING

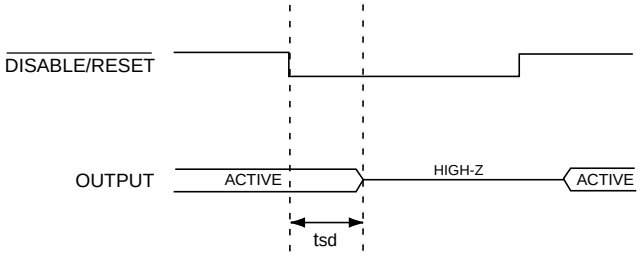


FIGURE 2C. DISABLE / RESET PROPAGATION DELAY

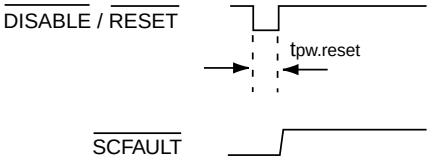


FIGURE 2G. DISABLE / RESET PULSE WIDTH

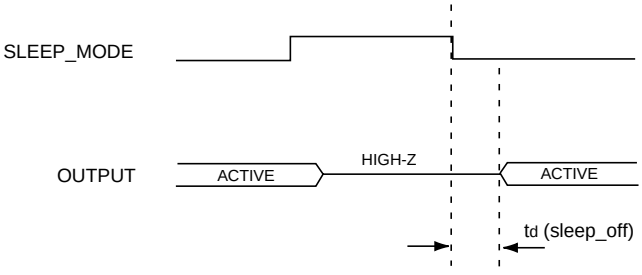


FIGURE 2D. SLEEP MODE OFF DELAY

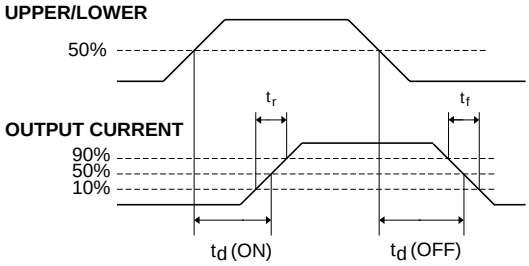


FIGURE 2H. OUTPUT TIMING

TABLE 4. PW-84075P6 SPECIFICATIONS
(T_C = +25°C, V_{CC} = V_{DD} = 5V UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
POWER & LOGIC SUPPLY (-55 TO 100 °C)						
Voltage	V_{CC}, V_{DD}		4.5	5	5.5	V
Logic Supply Current (see Note 1)	I_{CC}	SLEEP MODE		11		mA
		f_{PWM} = 25KHz		136	200	mA
Current Amplifier Supply Current	I_{DD}		8	10	20	mA
CURRENT AMPLIFIER						
$V_{IRSENSE}$ Gain	Gvout	V_{IREF} = 5.0V		29.76		mV/A
$V_{IRSENSE}$ Gain Error	Evout		-4		4	%
$V_{IRSENSE}$ Gain Drift	Gdrift			±330		ppm/°C
$V_{IRSENSE}$ Offset	Vos	V_{IREF} = 5.0V	-30		30	mV
$V_{IRSENSE}$ Offset Drift	TCVos	V_{IREF} = 5.0V	-90		110	µV/°C
$V_{IRSENSE}$ Gain %	Gvout%			0.595		%V_{IREF}/A
$V_{IRSENSE}$ Offset %	Vos%VIREF		-0.6		0.6	%V_{IREF}
$V_{IRSENSE}$ Offset % Drift	TCVos%		-18		22	ppm of V_{IREF}/°C
$V_{IRSENSE}$ Output Resistance	Rout			0.2		Ω
$I_{VIRSENSE}$ Output Current	$I_{VIRSENSE}$				20	mA
$V_{IRSENSE\_ABS}$ Output Resistance	Rabs			0.3		Ω
$I_{VIRSENSE\_ABS}$ Output Current	$I_{VIRSENSE\_ABS}$				20	mA
$V_{IRSENSE\_ABS}$ Gain	Gvabs	V_{IREF} = 5.0V		59.52		mV/A
$V_{IRSENSE\_ABS}$ Gain Error	Evabs		-6		6	%
$V_{IRSENSE\_ABS}$ Gain Drift	ABSGdrift			±330		ppm/°C
$V_{IRSENSE\_ABS}$ Offset	Vosabs	V_{IREF} = 5.0V	-131		131	mV
$V_{IRSENSE\_ABS}$ Offset Drift	TCVosabs	V_{IREF} = 5.0V	-90		110	µV/°C
$V_{IRSENSE\_ABS}$ Gain %	Gvout%			1.19		%V_{IREF}/A
$V_{IRSENSE\_ABS}$ Offset %	Vosabs% V_{IREF}		-2.6		2.6	%V_{IREF}
$V_{IRSENSE\_ABS}$ Offset % Drift	TCVosabs%		-18		22	ppm of V_{IREF}/°C
Delay Time	tdelay (FIGURE 3A)	-55 to 100 °C		9	20	µs
Bandwidth	fBW (FIGURE 3B)	-55 to 100 °C	20	30		kHz
Linear Range	Irange	-55 to 100 °C		±67		A
$\overline{OC\_FAULT}$ Trip Level	I_{OC}	-55 to 100 °C	±75	±85	±95	A
Trip Delay Time	T_{IOC} (FIGURE 3C)	-55 to 100 °C, 10k pull up to Vdd		3	6	µs
Reference Voltage Current Input	Iviref	-55 to 100 °C		0.26	1	mA
Reference Voltage Input	V_{IREF}	-55 to 100 °C	4.0		V_{DD}	Vdc
Reference Voltage Input Capacitance	Cin			0.1		µF
$\overline{OC\_FAULT}$ (-55 TO 100 °C)						
High Level Output Current	IOCFLTH	Vo = V_{DD}		0.2	15	µA
Low Level Output Current	IOCFLTL	Vo = 0.8V	4			mA

Note 1: During initial power-on @ Vcc ~3.5 Vdc, a transient current pulse of up to 100mA above Icc may be observed.

TABLE 4 REFERENCE DIAGRAMS

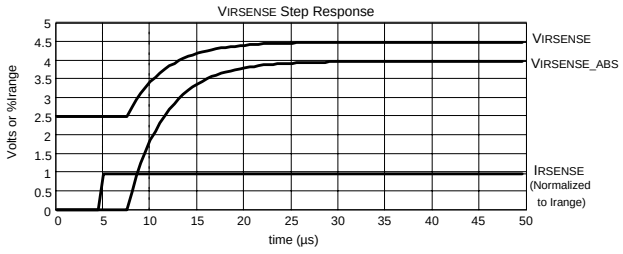


FIGURE 3A. VIRSENSE STEP RESPONSE

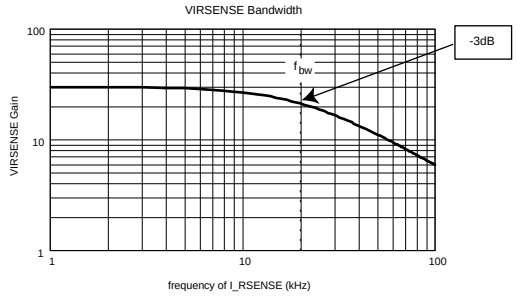


FIGURE 3B. VIRSENSE BANDWIDTH

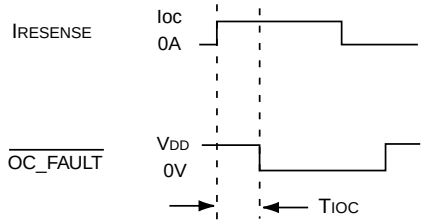


FIGURE 3C. OC FAULT TRIP RESPONSE TIME

TABLE 5. PW-85075P6 SPECIFICATIONS
(V_{CC} = V_{DD} = 5V UNLESS OTHERWISE SPECIFIED, T_C = -55°C TO +100°C FOR MIN, MAX VALUES, T_C = +25°C FOR TYPICAL VALUES.)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
OVERVOLTAGE TRANSISTOR						
Continuous Current Drive	Io	+25°C Case			35	A
		+85°C Case			30	A
Peak Current	I_{PEAK}	+85°C Case, 15 ms			60	A
Output Voltage Drop (IGBT)	$V_{CE(SAT)}$			2.0	3.0	Vdc
Reverse Leakage @ TJ = +25°C	Ir	600 Vdc			250	µA
Reverse Leakage @ TJ = +125°C	Ir	600 Vdc			1.0	mA
THERMAL						
Maximum Thermal Resistance	θjc			0.8	1.2	°C/W
OVERVOLTAGE FLYBACK DIODE						
Reverse Leakage @ Tc = +25°C	Ir	480 Vdc		20	50	µA
Reverse Leakage @ Tc = +125°C	Ir	480 Vdc		1	7	mA
Overvoltage Trip	Vtrip	no external adjustments	358	400	440	Vdc
Trip Level Hysteresis	Vhyst		34	40	45	Vdc
POWER AND LOGIC SUPPLY						
Voltage	V_{CC}		4.5	5	5.5	V
Current (see Note 1)	I_{CC}	Sleep Mode		11		mA
		f_{PWM} = 25KHz		137	250	mA
REGEN STATUS (ref. to REGEN CLAMP-)						
High Level Output Voltage	VOHstatus	No Load	13.8	15	15.6	Vdc
Low Level Output Voltage	VOLstatus	No Load		0.2	0.4	Vdc
Output resistance	Rstatus		4.2	4.75	4.8	KΩ
Vtrip rise to status ON Delay	tdon.status			36		µs
Vtrip fall status OFF Delay	tdoff.status			48		µs

Note 1: During initial power-on @ Vcc ~3.5 Vdc, a transient current pulse of up to 100mA above Icc may be observed.

INTRODUCTION

The PW-8X075P6 Magnum family is a series of universal modular half-bridge motor drives intended for use with brush, brushless DC and AC induction motors in aerospace applications.

The PW-8X075P6 contains an isolation barrier between the power and control stages, which attenuates ground noise generated from the high speed, high power switching. All signals from the control to the power sections are isolated from power and ground of the other section. This eliminates false triggering of the input signals and any need for creative grounding schemes. The isolation barrier also allows the user to operate the output stage from either unipolar or bipolar power supplies without level shifting the input signals. A built in power supply located in the control stage provides power to all electronics in the power stage. This eliminates the need for refresh cycles or external power supplies for the gate drive circuitry and allows switching duty cycles from 0 - 100%. (Reference FIGURES 1A, 1B, 1C)

The output power transistors on all modules are protected from a short circuit applied to the output pin. When a short circuit condition is detected, the output transistors are shut down and a flag $\overline{\text{SC FAULT}}$ is made active (logic low (L)) indicating a short has occurred. The PW-84075P6 contains additional current sensing circuitry that can monitor either motor current or DC bus current. The output voltage of the current sensing circuit can be used as a feedback signal in a servo drive to create a torque loop (Reference FIGURE 1B).

All output power transistors can be protected from regenerative bus over-voltage when utilizing dynamic braking with the addition of one PW-85075P6 module. This module contains an over-voltage switch that is enabled when an over-voltage condition is detected. This switch is normally wired to an external (user supplied, application specific) load dump resistor to provide a load across the high voltage bus when over-voltage is detected. During an over-voltage condition, the status flag REGEN_STATUS is active (logic high (H)) indicating an over-voltage condition is occurring. (Reference FIGURE 1C)

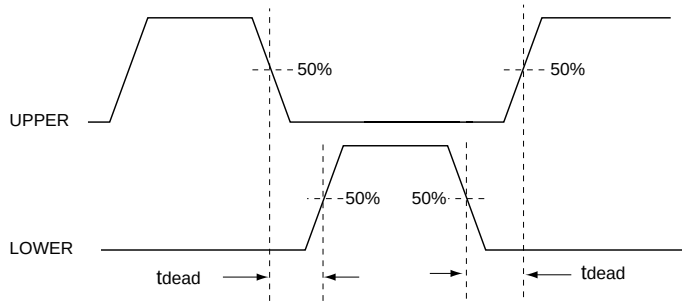


FIGURE 4. PW-8X075P6 DEAD BAND REQUIREMENT

PW-8X075 I/O AND OPERATION

UPPER, LOWER (INPUTS)

UPPER and LOWER are active high CMOS Schmitt-trigger inputs that control the gate drives of the output transistors (TTL compatibility requires external 10K pull-up resistors). Each input is electrically isolated from the output. A dead band, as shown in FIGURE 4, between turn off and turn on of UPPER and LOWER inputs is necessary to prevent output shoot through conduction.

$\overline{\text{SC FAULT}}$ (OUTPUT)

$\overline{\text{SC FAULT}}$ is an active low open collector output signal that indicates when the output of the module has experienced a short circuit condition. $\overline{\text{SC FAULT}}$ will remain active until $\overline{\text{DISABLE/RESET}}$ is made active (L). The signal is inactive (high impedance) during normal operation. See SHORT CIRCUIT PROTECTION for more detail.

$\overline{\text{DISABLE}}$ / $\overline{\text{RESET}}$ (INPUT)

$\overline{\text{DISABLE}}$ / $\overline{\text{RESET}}$ is an active low CMOS Schmitt-trigger input. When $\overline{\text{DISABLE}}$ / $\overline{\text{RESET}}$ is held active it does two things: 1.) Resets the $\overline{\text{SC FAULT}}$ (if it was active), and 2.) Disables the output (makes the output high impedance). If this line is used solely to clear $\overline{\text{SC FAULT}}$ then it only needs to be pulsed active. The duration of the $\overline{\text{DISABLE}}$ / $\overline{\text{RESET}}$ active pulse must be at least tpw.reset to ensure that $\overline{\text{SC FAULT}}$ is cleared properly. When this line is inactive, the OUTPUT is allowed to respond to the other control lines of the module (UPPER, LOWER, SLEEP_MODE).

Note: TTL compatibility requires an external pull-up resistor.

$\overline{\text{AUTO RESET}}$ (INPUT)

$\overline{\text{AUTO RESET}}$ is an active low (L) input. When $\overline{\text{AUTO RESET}}$ is tied to $\overline{\text{SC FAULT}}$ the protection circuit will reset automatically after the short circuit fault has occurred, and a delay period, tcycle.auto, has expired. This automatic reset enables the output to respond to the input commands. See SHORT CIRCUIT PROTECTION for more detail.

SLEEP_MODE (INPUT)

SLEEP_MODE is an active high input that turns the internal power supply off. A logic low (L) enables the power supply and allows the motor drive to operate normally.

A logic high (H) on the SLEEP_MODE input disables the internal power supply, disabling the motor drive output. No damage will occur to the motor drive during turn on or turn off of the power supply. Additionally, no special power up sequence is required.

The UPPER and LOWER logic gate driver inputs should not be active while transitioning in and out of sleep mode. If the UPPER

and LOWER logic inputs must be active while entering sleep mode then DISABLE / RESET must be held active while coming out of sleep mode.

Note: SLEEP_MODE has an internal pull-up resistor. If the input is not connected, it will default to logic high, turning the power supply and the motor drive off.

VCC,VCC-RTN (INPUTS)
The VCC and VCC-RTN are power connections that supply input power to the internal power supply, the gate drive and fault control circuits.

VBUS+, VBUS- (INPUTS)
VBUS+ and VBUS- are the high voltage power connections to the output stage. The high voltage can be either unipolar (+V and ground) or bipolar (+/- V). Care must be taken to ensure that the transient bus voltage VBUS at the module terminals never exceeds the absolute maximum supply ratings during switching excursions. External capacitor filtering will be required (See DDC's Applications Note AN/H-7).

OUTPUT (OUTPUT)
Output is the power switch output that is connected to one input of the motor and applies VBUS+, VBUS-, or high impedance to the motor based on the state of the control inputs. It is capable of sourcing or sinking up to the rated output current, and can withstand a short circuit to VBUS+ or VBUS- without any damage by automatically turning itself off (high impedance state).

SHORT CIRCUIT PROTECTION

The PW-8X075P6 modules have provisions for complete short circuit protection from either a hard or soft short to the VBUS+ or VBUS- lines. Each output transistor on all PW-8X075P6 modules is protected from a hard (direct, low impedance) short to the VBUS+ or VBUS- lines by circuitry that detects the de-saturation voltage for that transistor during a short condition. Once a hard short circuit condition is detected, the affected output transistor is shut down and SC FAULT output is set active (logic low (L)). The SC FAULT signal can be used by a controller as a signal to initiate a fault routine to reset or shut down the system. The DISABLE / RESET input can be used to shut down the gate drivers if a short persists. If the AUTO RESET is tied to SC FAULT, the circuit will automatically reset when a fault occurs. This inactivates SC FAULT and reactivates the output transistor within the tcycle.auto time period. If the short is still present, the circuit will repeat the shut down and automatically reset until the short is clear.

Protecting against a soft-short requires the addition of current sensing PW-84075P6 modules and external circuitry. When a soft short occurs, the external circuit can set DISABLE / RESET low (L) to shut down the gate drivers.

PW-84075 I/O AND OPERATION

PW-84075P6 modules can be added to a motor drive to provide current monitoring and overcurrent protection capability. The following section describes the PW-84075P6 module and its features.

VDD, VDD-RTN
VDD and VDD-RTN supplies input power to the current amplifier.

VIRSENSE (OUTPUT)
VIRSENSE is an output that provides a voltage proportional to the current passing through RSENSE. The voltage is scaled by a reference voltage VREF and is equal to VREF/2 to represent zero current. A voltage greater than VIREF/2 indicates a positive current flow (positive voltage from RSENSE + to RSENSE -) through RSENSE. See FIGURE 1B.

This VIRSENSE voltage is scaled by the input voltage at VIREF, where:

VIRSENSE = (VIREF/2) + (VIREF/168) * (IRSENSE)

Note: IRSENSE is current flowing through RSENSE. Zero amps in RSENSE is indicated when VIRSENSE = VIREF/2. A voltage greater (less) than VIREF/2 indicates a positive (negative) current flow through RSENSE with a value defined by the VIRSENSE equation. VIRSENSE is electrically isolated from the output stage. A positive (negative) current flow from RSENSE + to RSENSE - produces a positive (negative) voltage measurement (See FIGURE 1B). When the power supply is shut down (SLEEP_MODE input high), the voltage at VIRSENSE will indicate 0V.

Note: During normal operation 0 Volts at VIRSENSE represents maximum negative current.

VIREF (INPUT)
A precision voltage reference from an external source is connected to the VIREF pin to set the output voltage scale for VIRSENSE and VIRSENSE_ABS. Note: The accuracy of the VIRSENSE and VIRSENSE_ABS outputs are subject to the accuracy and temperature coefficient of VIREF. These must be taken into account in calculating the overall accuracy of VIRSENSE.

RSENSE+, RSENSE- (INPUTS)
The RSENSE+ and RSENSE- pins are connected to an internal shunt resistor and monitoring circuitry. These pins can be connected anywhere within the isolation restrictions on the pins (600V to power pins, 2500V to logic pins). These pins are typically connected in series with the OUTPUT, VBUS+ or VBUS-, to measure motor drive current.

VIRSENSE_ABS (OUTPUT)
VIRSENSE_ABS output voltage is the absolute value of the VIRSENSE voltage signal. VIRSENSE_ABS is zero volts when there is no current flowing through the RSENSE resistor. It will increase towards the value of VIREF as the current in RSENSE approaches

either ± full-scale current (measurement limits of VIRSENSE). VIRSENSE_ABS is an open source output and is "wire-OR-able". When two or more VIRSENSE_ABS outputs are "wire-OR-ed", the highest voltage will appear on the common signal. A typical use for combining these outputs is for determining when an overload condition has occurred. The VIRSENSE_ABS voltage is scaled by the input voltage VIRSENSE where:

$$V_{IRSENSE\_ABS} = 2 \times |V_{IRSENSE} - V_{IREF}/2|$$

$\overline{\text{OC FAULT}}$ OUTPUT

$\overline{\text{OC FAULT}}$ is an active low open drain output that goes active when the current flowing through RSENSE has exceeded the $\overline{\text{OC FAULT}}$ trip level. This signal is not latched like $\overline{\text{SC FAULT}}$, and goes inactive as soon as the over current condition stops.

PW-85075 I/O AND OPERATION

PW-85075P6 modules can be added to a motor drive to provide overvoltage protection capability. The following section describes the PW-85075P6 module and its features.

REGEN_STATUS (OUTPUT)

The REGEN_STATUS pin is referenced to VBUS-, and indicates the state of the regen clamp switch (H = on, L = off). An external opto-isolator input can be connected between REGEN_STATUS and VBUS- to translate this status to logic circuits if desired. The REGEN_STATUS output is connected to the overvoltage amp through a 5KΩ resistor. When the regen clamp switch is active (inactive), the overvoltage amp sources +15V (0V) through the 5KΩ resistor. (see FIGURE. 1C).

REGEN_CLAMP (OUTPUT) (REF. R20 ON FIGURES 14 AND 15)

An external load dump resistor is connected between REGEN_CLAMP and VBUS+. When VBUS+ reaches the over-voltage trip level set by the OV_ADJ, the internal clamp circuit will apply the load dump resistor from VBUS+ to the VBUS-, thereby dissipating the regenerative energy of the bus into the external resistor.

OV_ADJ (INPUT)

The PW-85075P6 is internally set for a trip voltage of 400V. The trip point can be adjusted to a higher or lower voltage by connecting an external over-voltage adjust resistor ROV_ADJ (Ref. R21 on FIGURES 14 and 15)

To set the overvoltage trip point to a voltage above 400 volts connect ROV_ADJ between the OV_ADJ and OV_ADJ_HIGH pins. To set the OV trip point to a voltage below 400 volts connect ROV_ADJ between the OV_ADJ and OV_ADJ_LOW pins. The value of ROV_ADJ for voltages above (below) 400 volts should be selected based upon FIGURE 5A (5B).

PW-8X075P6 TYPICAL OVERVOLTAGE TRIP VS. OV ADJUST SETTINGS

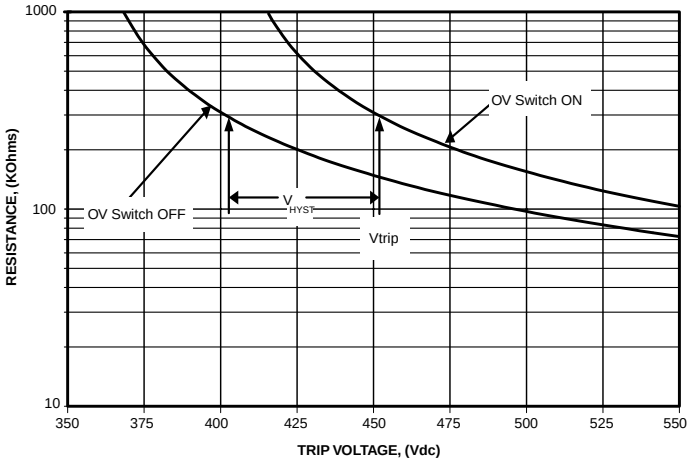


FIGURE 5A. EXTERNAL OV ADJUST RESISTOR CONNECTED TO OV_ADJ_HIGH

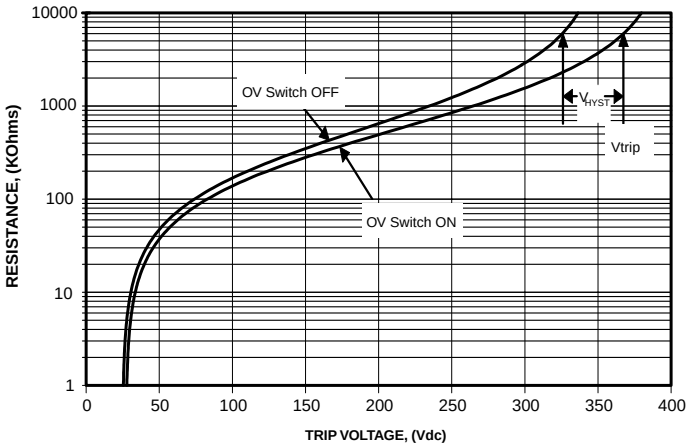


FIGURE 5B. EXTERNAL OV ADJUST RESISTOR CONNECTED TO OV_ADJ_LOW

POWER DISSIPATION

There are three major contributors to power dissipation in the motor driver: conduction losses, switching losses, and flyback diode losses. Consider the following operating conditions:

VBUS = +270V
f_{PWM} = 10kHz
duty cycle = 50% (ton = 50µs; toff = 50µs)
I_O = 40A, Module Output Current
during ton, Ic = I_O; during toff, If = I_O

The power dissipation of the circuit shown in FIGURE 6 can now be calculated using information from the data sheet as follows:

Transistor data

$T_{J\ MAX}$ = 150 °C (TABLE 2)
$\theta_{JC.IGBT}$ = 0.55°C/W (TABLE 2)
$V_{CE(SAT)}$ = 1.56V
(FIGURE 9a, 2.2V x 0.71 = 1.56, tj = 150°C, Ic = 40A)
E_{ON} (50A, 270V) = 0.675 mJ (TABLE 2)
E_{OFF} (50A, 270V) = 4.5 mJ (TABLE 2)

Flyback diode data

$T_{VJ\ MAX}$ = 150 °C
θ_{JC}.diode = 0.87°C/W (TABLE 2)
V_F(avg) = 1.23V (FIGURE 9c, Tvj = 150°C, If = 40A)

1. Transistor Conduction Losses (P_C)

$P_C = I_C \times V_{CE(SAT)}$ x duty cycle
P_C = 40A x 1.56V x 50%
P_C = 40A x 1.56V x 0.5
P_C = 31.2W

2. Transistor Switching Losses (P_S)

$P_S = [E\text{-}_{ON}\text{ (scaled)} + E\text{-}_{OFF}\text{ (scaled)}] \times f_{PWM}$

E_{ON} (scaled) = E_{ON} (50A, 270V) x (V_{BUS} / 270V) x (I_O/50A)]
$E\text{-}_{ON}$ (scaled) = [0.675mJ x (270V / 270V) x (40A / 50A)]
$E\text{-}_{ON}$ (scaled) = 0.54 mJ

$E\text{-}_{OFF}$(scaled) = [E_{OFF} (50A, 270V) x (V_{BUS}/270V) x (I_O/50A)]
$E\text{-}_{OFF}$(scaled) = [4.5 mJ x (270V/270V) x (40A/50A)]
$E\text{-}_{OFF}$(scaled) = 3.6 mJ

P_S = (0.54 mJ + 3.6 mJ) x 10kHz
P_S = 41.4W

3. Flyback diode Losses (Pd)

Pd = I_O x V_F(avg) x [1 - duty cycle]
Pd = 40A x 1.23V x [1 - 50%]
Pd = 40A x 1.23V x [1 - 0.5]
Pd = 40A x 1.23V x 0.5
Pd = 24.6W

4. Transistor Power Dissipation (P_T)

$P_T = P_C + P_S$
P_T = 31.2W + 41.4W
P_T = 72.6W

5. Maximum Allowed Module Case Temperature

$T_{CASE.ALLOWED.IGBT} = T_{jmax} - \theta_{jc.IGBT} \times P_T$
$T_{CASE.ALLOWED.IGBT}$ = 150°C - [(0.55°C/W) x (72.6W)]
$T_{CASE.ALLOWED.IGBT}$ = 110°C

$T_{CASE.ALLOWED.diode} = T_{vjmax} - \theta_{jc.diode} \times P_d$
$T_{CASE.ALLOWED.diode}$ = 150°C - [(0.87°C/W) x (24.6W)]
$T_{CASE.ALLOWED.diode}$ = 129°C

Maximum allowed case temperature for the module will be the lesser of the allowed diode and allowed IGBT case temperatures:

$T_{CASE.ALLOWED}$
= smaller of $T_{CASE.ALLOWED.diode}$ or $T_{CASE.ALLOWED.IGBT}$

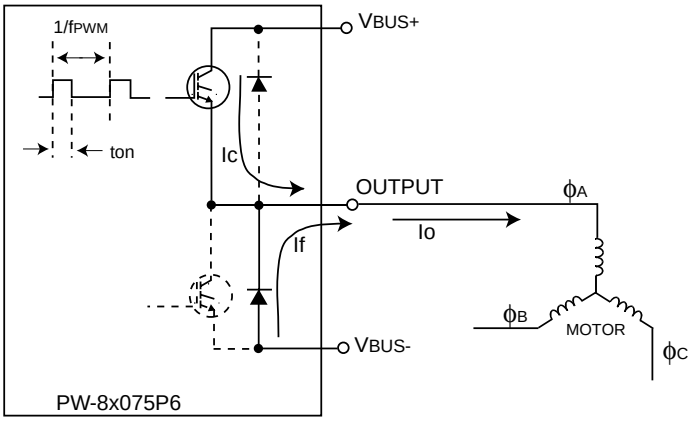


FIGURE 6. POWER DISSIPATION CIRCUIT

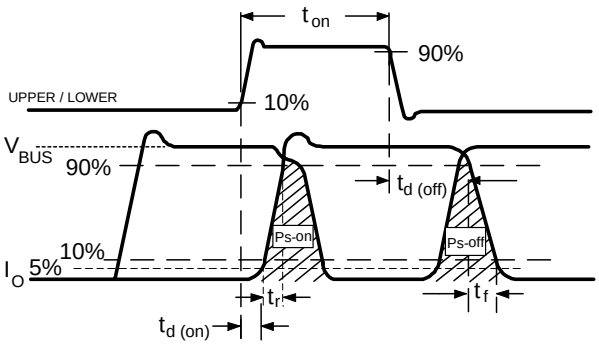


FIGURE 7. OUTPUT CHARACTERISTICS

MAXIMUM ALLOWED CASE TEMPERATURES

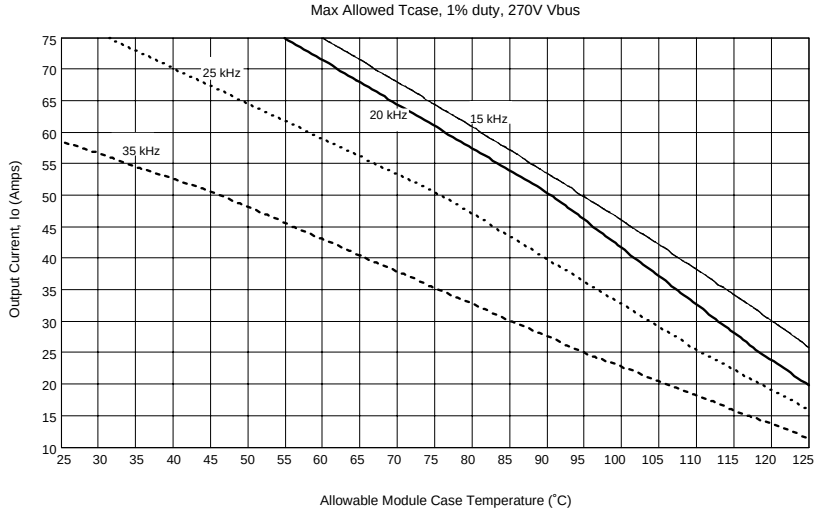


FIGURE 8A. MAXIMUM ALLOWED CASE TEMPERATURES 1% DUTY CYCLE

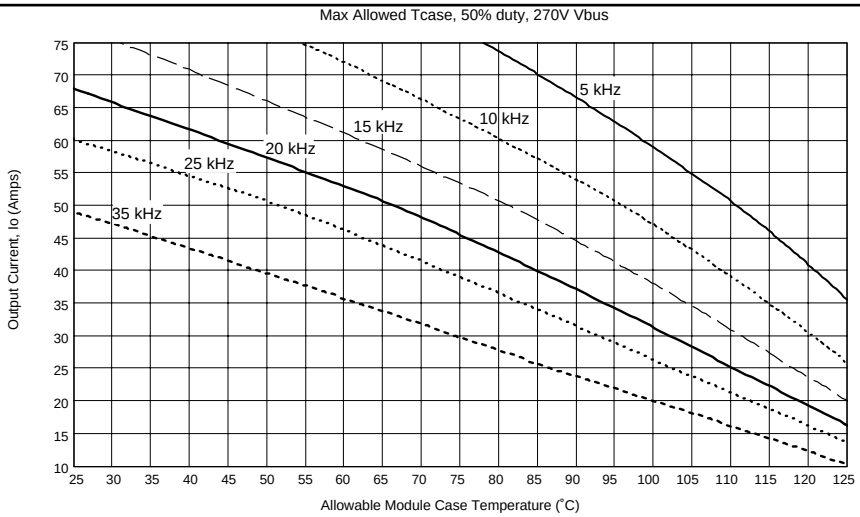


FIGURE 8B. MAXIMUM ALLOWED CASE TEMPERATURES 50% DUTY CYCLE

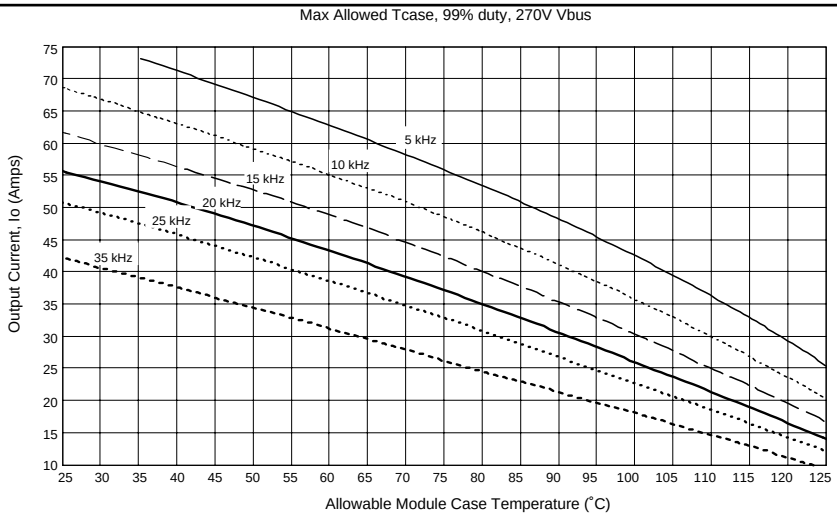
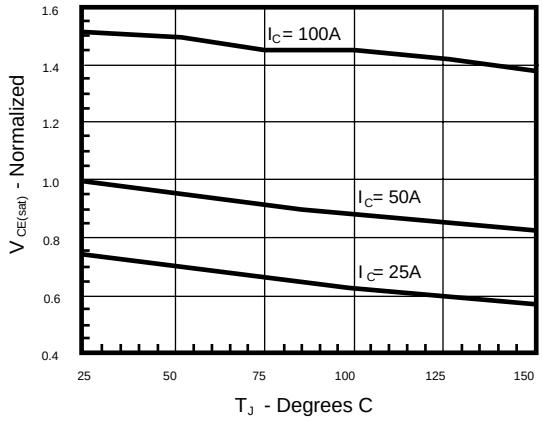


FIGURE 8C. MAXIMUM ALLOWED CASE TEMPERATURES 99% DUTY CYCLE

CHARACTERISTIC CURVES FOR OUTPUT POWER TRANSISTORS ON PW-8X075P6



Note: $V_{CE(sat)}$ typical = 2.2V @ 50A, 25˚C

FIGURE 9A. TEMPERATURE DEPENDENCE OF $V_{CE(SAT)}$;

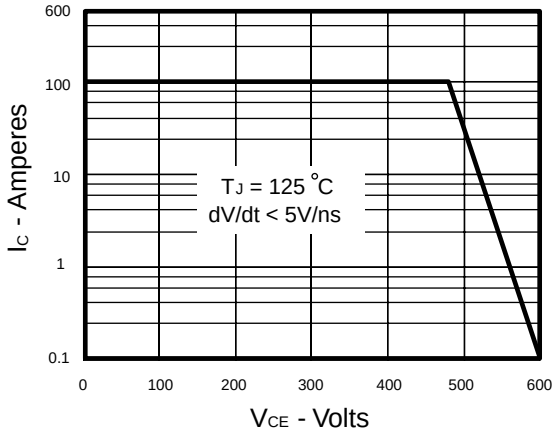


FIGURE 9B. OUTPUT SAFE OPERATING AREA

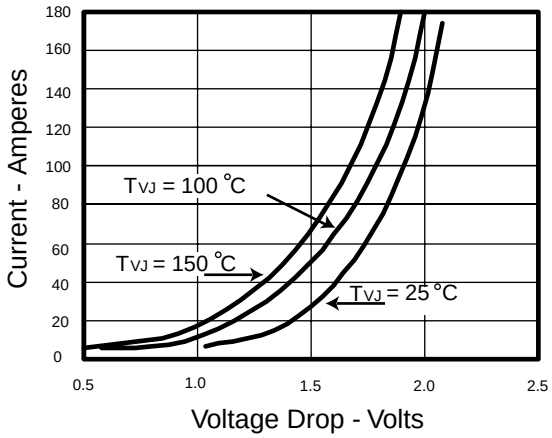


FIGURE 9C. FORWARD VOLTAGE DROP (FLYBACK DIODE)

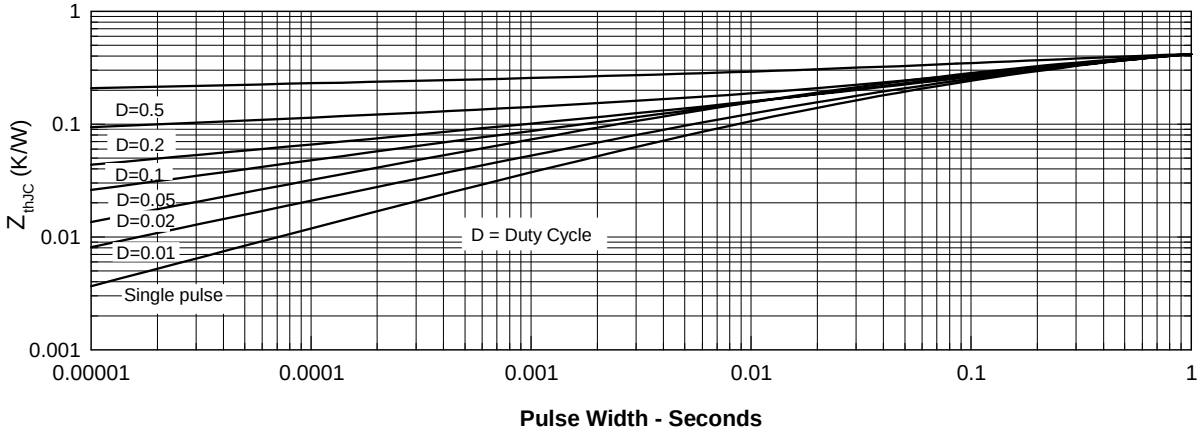


FIGURE 9D. TRANSIENT THERMAL IMPEDANCE

CHARACTERISTIC CURVES USED FOR OVERVOLTAGE SWITCH TRANSISTOR USED ON PW-85075P6

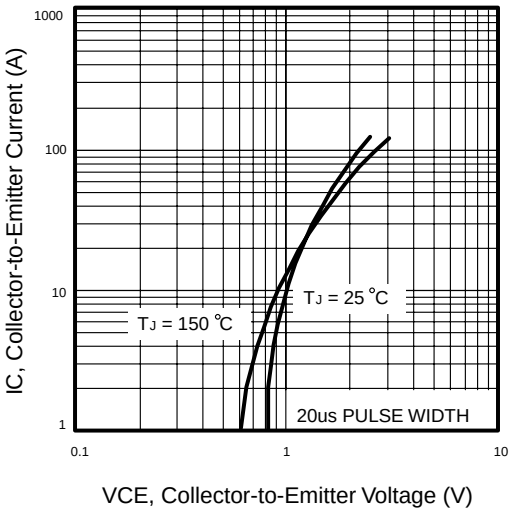


FIGURE 10A. TYPICAL OUTPUT CHARACTERISTICS

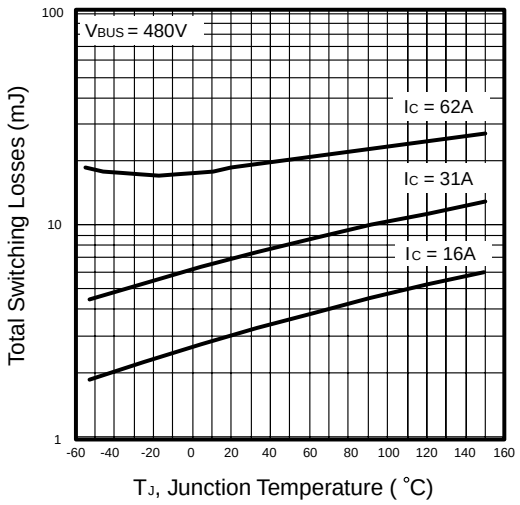


FIGURE 10C. TYPICAL SWITCHING LOSSES VS. JUNCTION TEMPERATURE

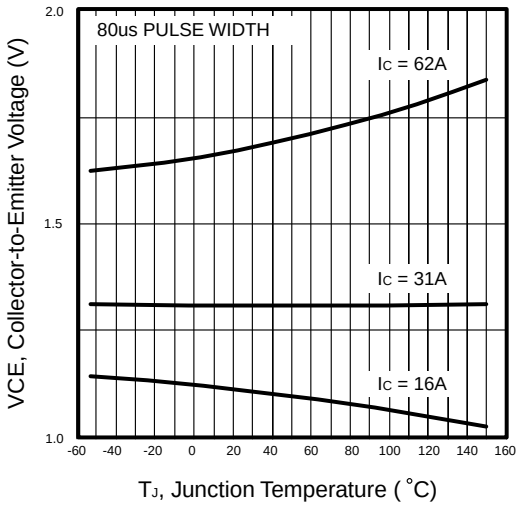


FIGURE 10B. COLLECTOR-TO-EMITTER VOLTAGE VS. JUNCTION TEMPERATURE

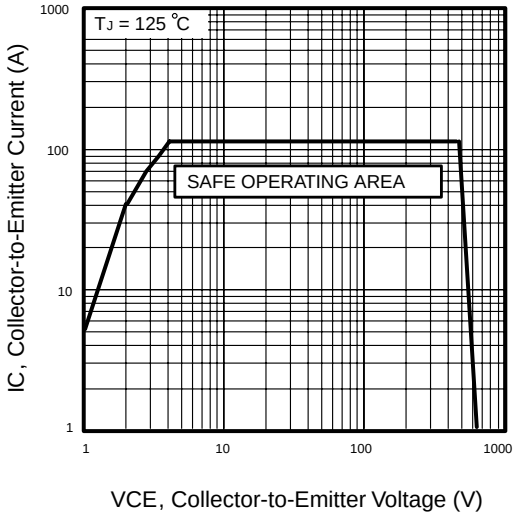


FIGURE 10D. TURN-OFF SAFE OPERATING AREA

TABLE 6. PW-8X075P6 TRUTH TABLE					
UPPER	**LOWER**	**$\overline{\text{DISABLE}}$/ RESET**	**SLEEP-MODE**	**$\overline{\text{SC-FAULT}}$**	**OUT**
0	0	X	X	X	Z
1	0	1	0	1	VBUS+
0	1	1	0	1	VBUS-
1	1	X	X	X	Z
1	0	1	0	0	*
0	1	1	0	0	*
X	X	0	X	X	Z
X	X	X	1	X	Z

X = Indicates that this input is irrelevant.
Z = High Impedance (off).
*= Fault will disable the transistor that caused the fault. The output state could be Z or ON.

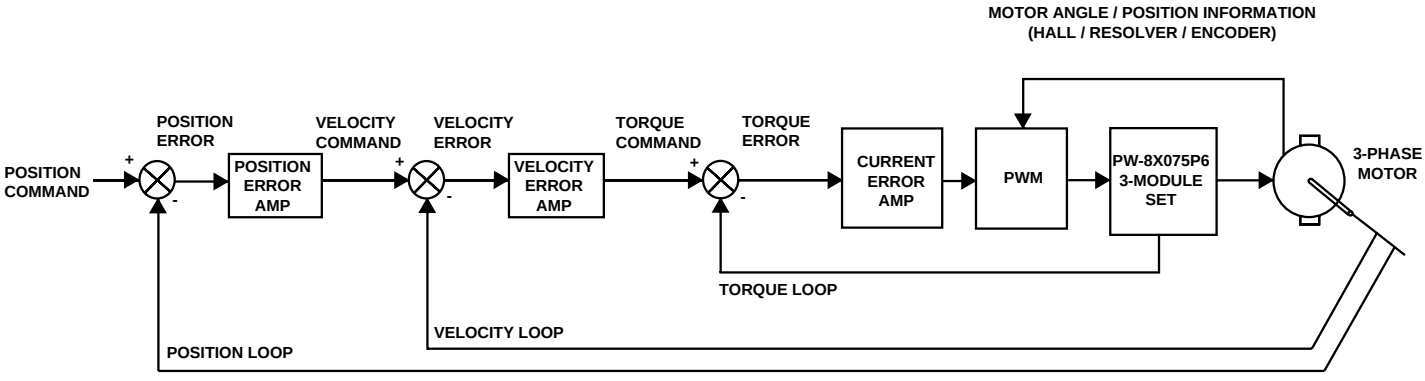


FIGURE 11. TYPICAL POSITION, VELOCITY AND TORQUE CONTROL LOOP

APPLICATIONS

POSITION OR VELOCITY CONTROL USING DSP

FIGURE 14 shows an example of position and/or velocity control hook-up with inner torque loop using the Digital Signal Processor (DSP) for motor control. Using software, the DSP can be implemented with one of several motor control algorithms such as FOC (Field Oriented Control) with SVM (Space Vector Modulation).

TORQUE CONTROL USING UC-2625 MOTOR CONTROLLER

FIGURE 15 shows an example of torque control loop with regenerative clamp protection using a UC2625, two PW-84075P6, and one PW-85075P6. The two PW-84075P6 modules (½ bridge with current sense) sense the current in motor phase B and C. VIRSENSE _ABS pins on each of the PW-84075P6 are tied together to generate a single composite analog output which is compared to the torque commanded input to produce an error signal. The UC2625 uses this error signal to regulate the output current (or torque) by controlling the duty cycle of the output transistors.

For the case when a resolver is available instead of Hall-effect devices, the circuit shown in FIGURE 16 converts the resolver (sin and cos) signals to Hall signals which can be used to commutate the output transistors.

HALL SIGNAL COMMUTATION

The hall signals HAB, HBC, HCA are logic signals from the motor Hall-effect sensors. The UC2625 uses a phasing convention referred to as 120 degree spacing; that is, the output of HAB is in phase with motor back EMF voltage VAB, the output of HBC is in phase with motor back EMF voltage VBC, and the output of HCA is in phase with motor back EMF voltage VCA. Logic "1" (or HIGH) is defined by an input greater than 2.4Vdc or an open circuit to the controller; Logic "0"(or LOW) is defined as any Hall voltage input less than 0.8Vdc.

The UC2625 will operate with Hall phasing of 60° or 120° electrical spacing. If 60° commutation is used, then the output of HCA must be inverted as shown in FIGURES 12 and 13. In FIGURE 12 the Hall sensor outputs are shown with the corresponding back EMF voltage they are in phase with.

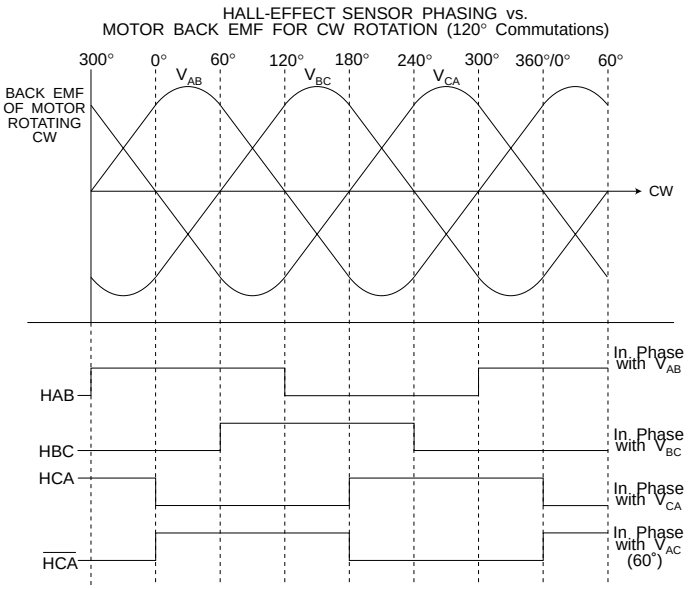


FIGURE 12. HALL PHASING

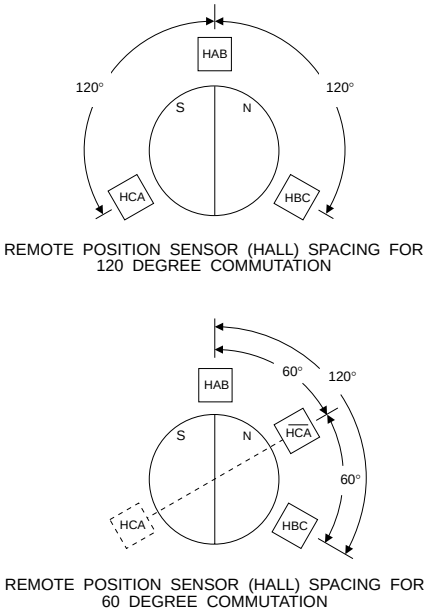
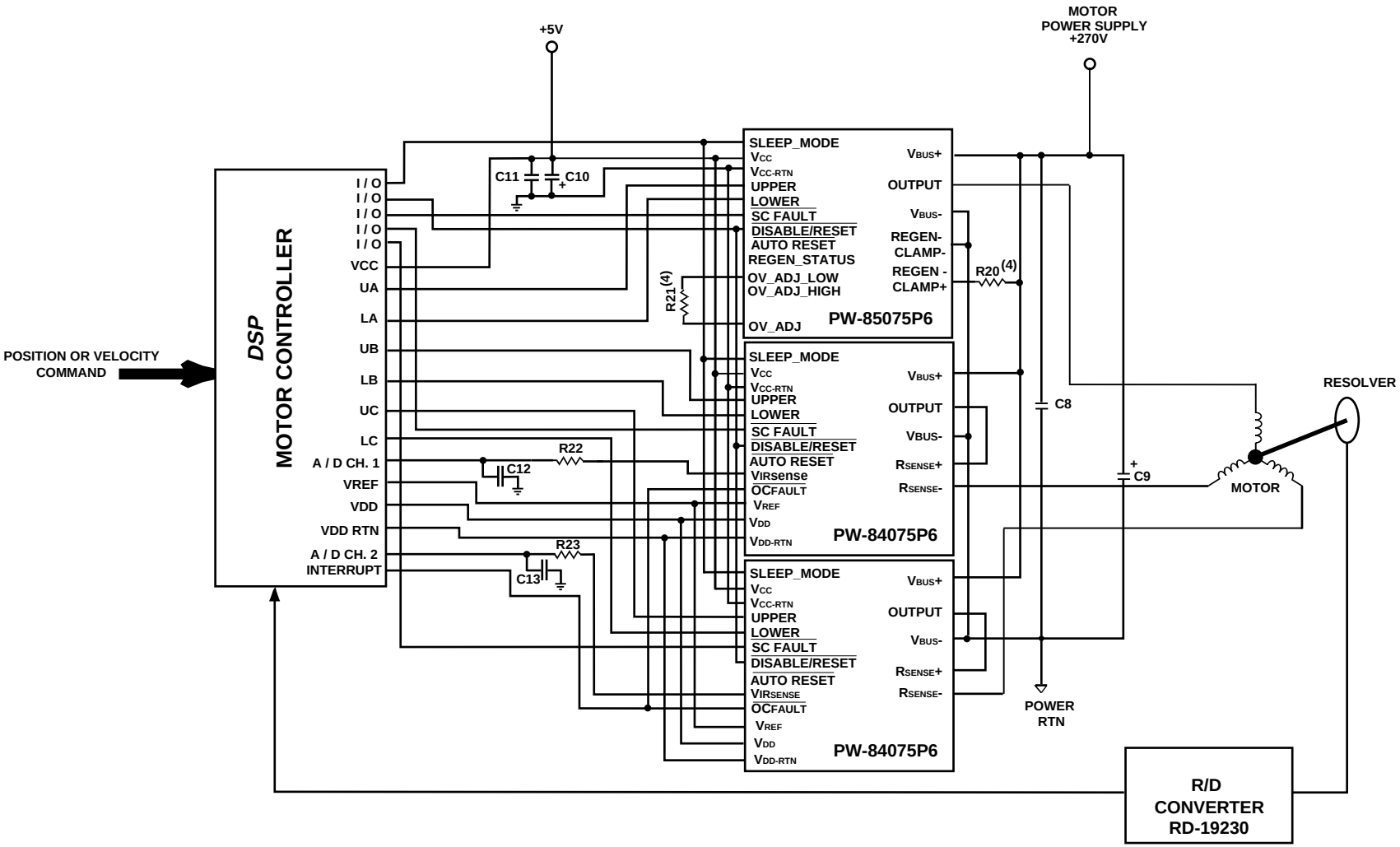


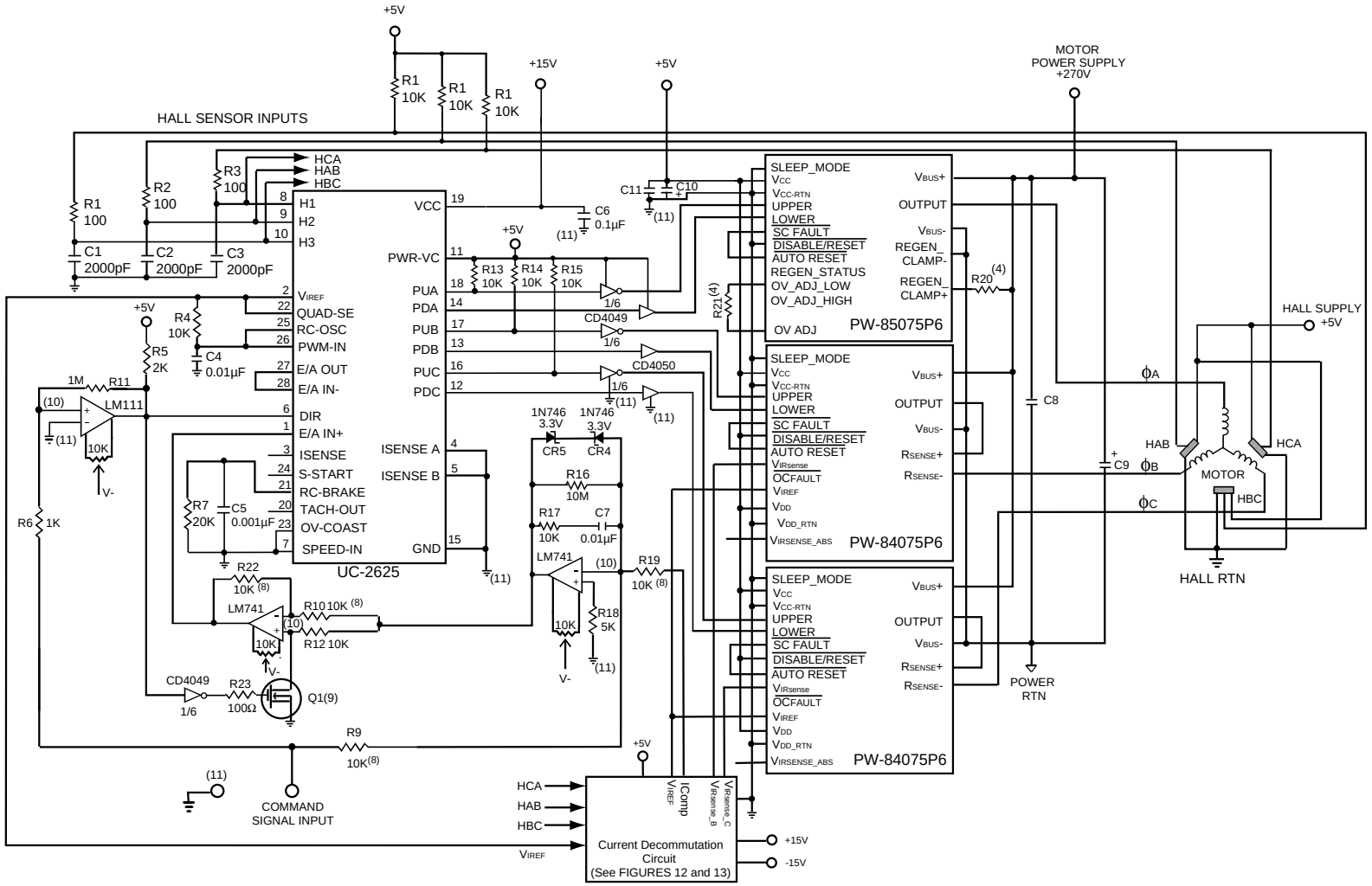
FIGURE 13. HALL SENSOR SPACING



NOTES:

1. C8 is a ceramic capacitor and should be selected per DDC Application Note AN/H-7, PW-82351 Motor Drive Power Supply, equation 1.
2. C9 is an electrolytic capacitor and should be selected per DDC Application Note AN/H-7, PW-82351 Motor Drive Power Supply, equation 1.
3. C10 is 22 µF, 15 V electrolytic capacitor. C11 is 0.1 µF, 50 V ceramic capacitor.
4. Resistance and power of R20 (Load dump resistor), and R21 (OV Adjust resistor) is application specific. (See OV Adjust and Regen description for details)

FIGURE 14. PW-8X075P6 POSITION OR VELOCITY HOOK-UP USING DSP MOTOR CONTROLLER



NOTES:

1. C8 is a ceramic capacitor and should be selected per DDC Application Note AN/H-7, Magnum Motor Drive Power Supply Capacitor Selection.
2. C9 is an electrolytic capacitor and should be selected per DDC Application Note AN/H-7, Magnum Motor Drive Power Supply Capacitor Selection.
3. C10 is 22 µF, 15 V electrolytic capacitor. C11 is 0.1 µF, 50 V ceramic capacitor.
4. Resistance and power of R20 (Load dump resistor), and R21 (OV Adjust resistor) is application specific. (See OV Adjust and Regen description for details)5. All resistors have a tolerance of ±10%, unless otherwise specified.
6. The CD4050 converts the +15V logic output of the UC-2625 to +5V logic signals.
7. The CD4049 inverts the +15V logic signal from the UC-2625, and converts it to a +5V logic signal.
8. 1% or better, depending on required accuracy.
9. Q1 can be either IRML2402 or IRMU014 or IRLD014.
10. These high impedance inputs and summing junctions of the operational amplifiers are highly sensitive to noise.
11. These grounds should be closely tied together to reduce ground noise effect.
12. Connect Hall sensor inputs to motor shaft position sensors that are 120 electrical degrees apart. Motors with 60 electrical degree position sensor coding can be used if one of the position sensor signals are inverted (See FIGURES 12 and 13).

FIGURE 15. PW-8X075P6 TORQUE HOOK-UP USING UC-2625 MOTOR CONTROLLER

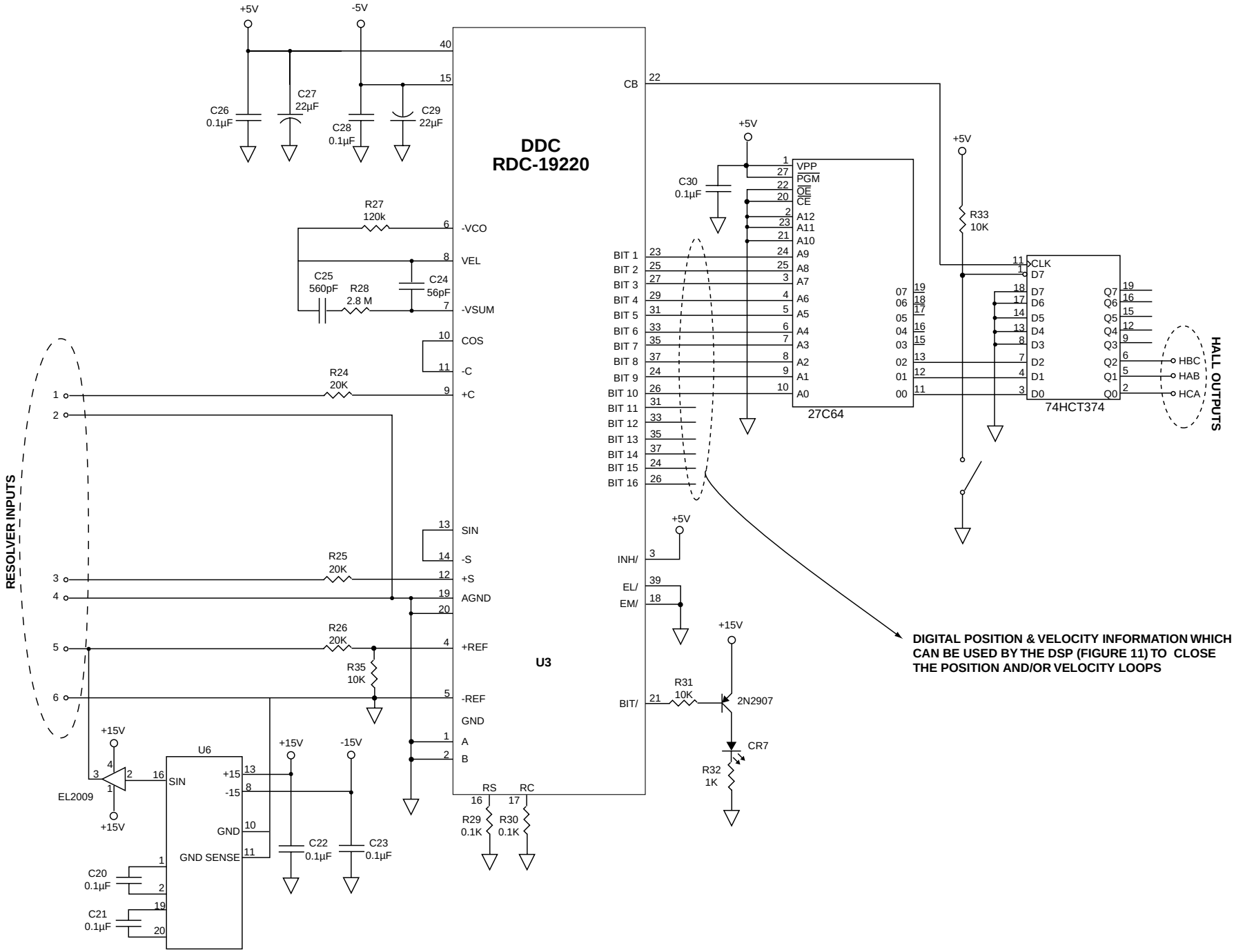
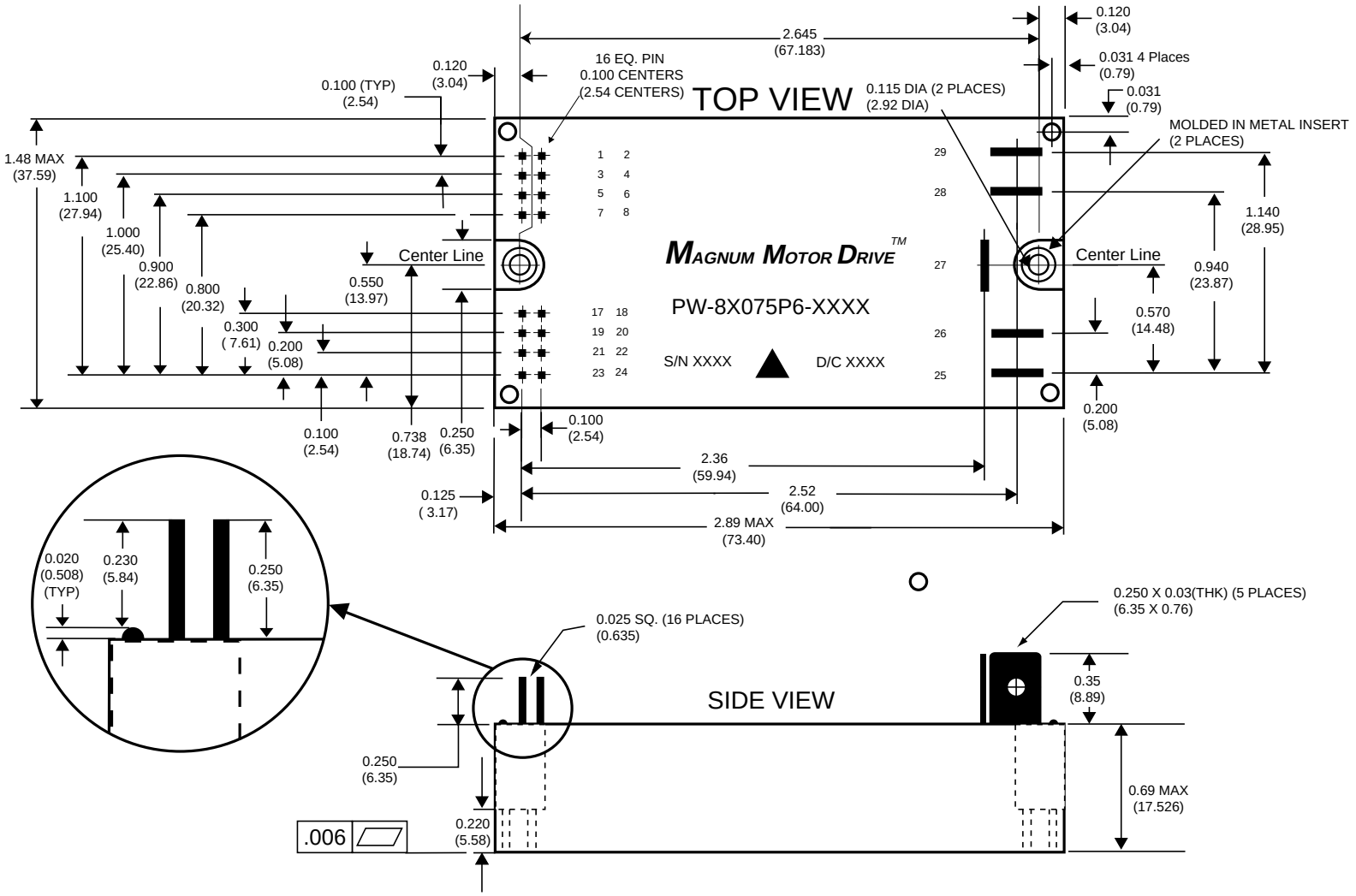


FIGURE 16. RESOLVER TO HALL SIGNAL CONVERSION CIRCUIT



NOTES:
1. Dimensions are in inches (mm).

MOUNTING CONSIDERATIONS:
For 2 or more modules, minimum spacing center line to center line - 1.5 inches (38.1 mm)

FIGURE 17. PW-8X075P6 OUTLINE

TABLE 7: PIN ASSIGNMENTS			
PIN #	FUNCTIONS DESCRIPTION		
	PW-83075P6	PW-84075P6	PW-85075P6
CONTROL PINS			
1	$\overline{\text{DISABLE}}$ / $\overline{\text{RESET}}$	$\overline{\text{DISABLE}}$ / $\overline{\text{RESET}}$	$\overline{\text{DISABLE}}$ / $\overline{\text{RESET}}$
2	V_{CC}	V_{CC}	V_{CC}
3	UPPER	UPPER	UPPER
4	$V_{CC\text{-}RTN}$	$V_{CC\text{-}RTN}$	$V_{CC\text{-}RTN}$
5	LOWER	LOWER	LOWER
6	SLEEP_MODE	SLEEP_MODE	SLEEP_MODE
7	$\overline{\text{SC FAULT}}$	$\overline{\text{SC FAULT}}$	$\overline{\text{SC FAULT}}$
8	$\overline{\text{AUTO RESET}}$	$\overline{\text{AUTO RESET}}$	$\overline{\text{AUTO RESET}}$
17	N/C	V_{IREF}	OV_ADJ_HIGH (1) (2)
18	N/C	$V_{IRSENSE}$	REGEN_STATUS
19	N/C	$V_{IRSENSE\_ABS}$	N/C
20	N/C	V_{DD}	OV_ADJ
21	N/C	$V_{DD\text{-}RTN}$	N/C
22	N/C	$\overline{\text{OC FAULT}}$	OV_ADJ_LOW (1) (3)
23	N/C	N/C	N/C
24	N/C	N/C	N/C
POWER PINS			
25	N/C	R_{SENSE} -	REGEN_CLAMP+
26	N/C	R_{SENSE}+	REGEN_CLAMP-
27	V_{BUS}+	V_{BUS}+	V_{BUS}+
28	OUTPUT	OUTPUT	OUTPUT
29	V_{BUS}-	V_{BUS}-	V_{BUS}-

NOTES:
(1) Connection for external OV adjust resistor only.
(2) Caution: V_{BUS}- voltage present on this pin.
(3) Caution: V_{BUS}+ voltage present on this pin.

NOTES:

NOTES:

ORDERING INFORMATION

PW-8X 075 PX- X X 0

Process Requirements:
- 0 = Standard DDC Procedures no Burn-In
- 2 = High Reliability Processing with Burn-In

Temperature Grade/Data Requirements:
- 1 = -55°C to +100°C
- 3 = -0°C to +70°C
- 4 = -55°C to +100°C with Variables Test Data
- 8 = 0°C to +70°C with Variables Test Data
- 9 = -55°C to 85°C

Voltage Rating
- 6 = 600V

Current Rating
- 075 = 75A

Features
- 3 = Standard ½ Bridge
- 4 = Standard ½ Bridge w/ current sense
- 5 = Standard ½ Bridge w/ regenerative voltage clamp

DDC™
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