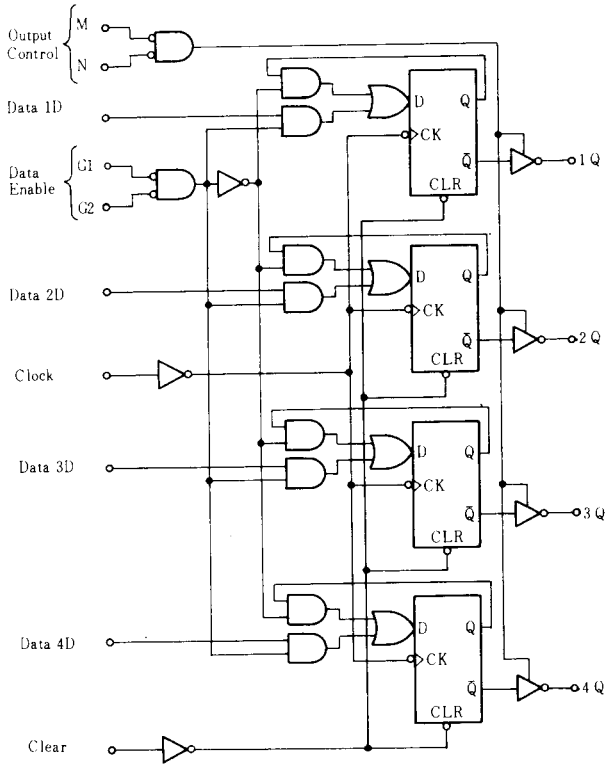
HD74LS173 ●4-Bit D-Type Registers (with three-state outputs)

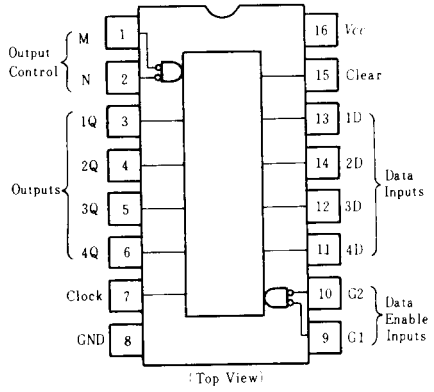
The HD74LS173 four-bit register includes D-type flip-flops featuring totempole three-state outputs capable of driving highly capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these flip-flops with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. Gated enable inputs are provided on the HD74LS173 for controlling the entry of data into the flip-flops. When both data-enable inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the buffered clock input. Gate output control inputs are also provided.

When both are low, the normal logic states (high or low levels) of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a high logic level at either output control input. The outputs then present a high impedance and neither load nor drive the bus line. Detailed operation is given in the function table.

■BLOCK DIAGRAM



■PIN ARRANGEMENT



■FUNCTION TABLE

Inputs					Output
Clear	Clock	Data Enable		Data	
		G_1	G_2	D	Q
H	X	X	X	X	L
L	L	X	X	X	Q_0
L	↑	H	X	X	Q_0
L	↑	X	H	X	Q_0
L	↑	L	L	L	L
L	↑	L	L	H	H

H; high level, L; low level X; irrelevant

When either M or N (or both) is (are) high the output is disabled to the high-impedance state; however sequential operation of the flip-flops is not afected.

■RECOMMENDED OPERATING CONDITIONS

Item		Symbol	min	typ	max	Unit
High level output current		I_{OH}	—	—	−2.6	mA
Low level output current		I_{OL}	—	—	24	mA
Clock frequency		f_{clock}	0	—	30	MHz
Clock and clear pulse width		t_w	20	—	—	ns
Setup time	Data enable	t_{su}	17	—	—	ns
	Data		17	—	—	
	Clear inactive state		10	—	—	
Hold time	Data enable	t_h	0	—	—	ns
	Data		0	—	—	

■ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75°C$)

Item	Symbol	Test Conditions		min	typ*	max	Unit
Input voltage	V_{IH}			2.0	—	—	V
	V_{IL}			—	—	0.8	
Output voltage	V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-2.6mA$		2.4	—	—	V
	V_{OL}	$V_{CC}=4.75V$, $V_{IL}=0.8V$	$I_{OL}=12mA$	—	—	0.4	
			$I_{OL}=24mA$	—	—	0.5	
Off-state output current	$I_{O(off)}$	$V_{CC}=5.25V$, $V_{IH}=2V$	$V_O=2.7V$	—	—	20	μA
			$V_O=0.4V$	—	—	−20	
Input current	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$		—	—	20	μA
	I_{IL}	$V_{CC}=5.25V$, $V_I=0.4V$		—	—	−0.4	mA
	I_I	$V_{CC}=5.25V$, $V_I=7V$		—	—	0.1	mA
Short-circuit output current	I_{OS}	$V_{CC}=5.25V$		−30	—	−130	mA
Supply current	I_{CC}**	$V_{CC}=5.25V$,		—	17	30	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$, $I_{IN}=-18mA$		—	—	−1.5	V

* V_{CC}=5V, Ta=25°C

** I_{CC} is measured with all outputs open; clear grounded following momentary connection to 4.5V; N, G1, G2, and all data inputs grounded; and the clock input and M at 4.5V.

■SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $Ta=25°C$)

Item	Symbol	Test Conditions		min	typ	max	Unit
Maximum clock frequency	f_{max}	$C_L=45pF$, $R_L=667\Omega$		30	50	—	MHz
Propagation delay time	t_{PHL}	Clear→Q	$C_L=45pF$ $R_L=667\Omega$	—	20	30	ns
	t_{PLH}	Clock→Q		—	16	29	
	t_{PHL}			—	20	30	
Output enable time	t_{ZH}	$C_L=45pF$, $R_L=667\Omega$		—	13	21	ns
	t_{ZL}			—	24	36	
Output disable time	t_{HZ}	$C_L=5pF$, $R_L=667\Omega$		—	11	17	ns
	t_{LZ}			—	15	23	