GEC PLESSEY
SEMICONDUCTORS

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PRELIMINARY INFORMATION
DS3984 - 2.8

MV6640

POCSAG DECODER

The MV6640 POCSAG decoder is capable of operating at 512 or 1200 baud. This device together with a suitable receiver, provides the major components for a POCSAG pager.

POCSAG is the acronym for Post Office Code Standardisation Advisory Group. The POCSAG code is the most accepted radio paging standard, (CCIR RPC No.1) and provides for over 2 million pager IDs, four of which may be held in this device. The POCSAG code format is shown in figure 3.

The design is optimised for very low power, low voltage use. Advanced features allow the decoder to be used in a wide range of applications.

The pinout and architecture are shown in figures 1 and 2.

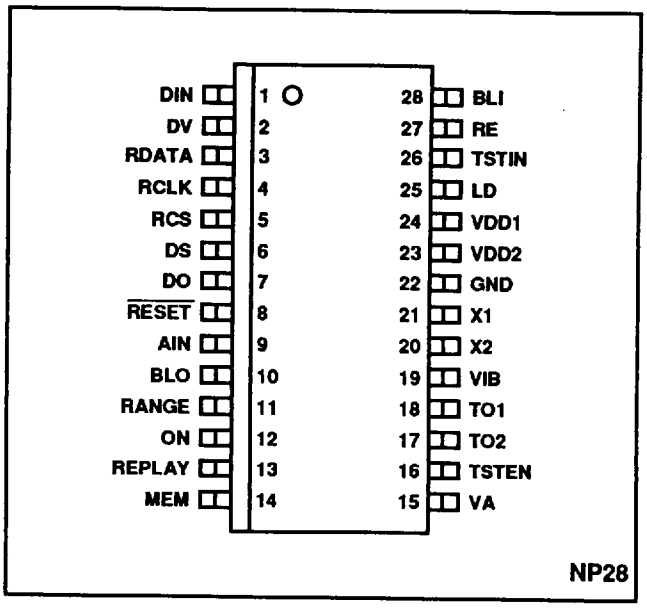


Fig. 1 Pin Connection
(top view - not to scale)

FEATURES

- Low voltage supply (1V min, 3.5V max)
- Low current consumption (Typically 15µA)
- Voltage doubler for radio receiver or µP and Display
- True 2 bit CRC error correction with error status indication
- Tone only and/or messaging pager at 512 or 1200 baud using a single 32768Hz crystal
- Silent call storage
- Directly drives tone transducer
- Programmable tone generator output frequency (2048 or 2731 Hz)
- Interface to SL6609 radio receiver chip
- Low battery alert
- Interface to Standard 3 wire EEPROM
- True or Inverted data

APPLICATIONS

- Wrist watch pager
- Message display pager
- Tone only pager
- Data receivers

ABSOLUTE MAXIMUM RATINGS

Supply voltage (VDD2 - GND)	-0.5V to 5V
Voltage on any pin	-0.3V to VDD2 + 0.3V
Operating temperature	-20°C to + 70°C
Storage temperature	-55°C to +125°C

ORDERING INFORMATION

MV6640/KG/NPDS - devices in anti-static sticks
MV6640/KG/NPDE - devices in tape & reel

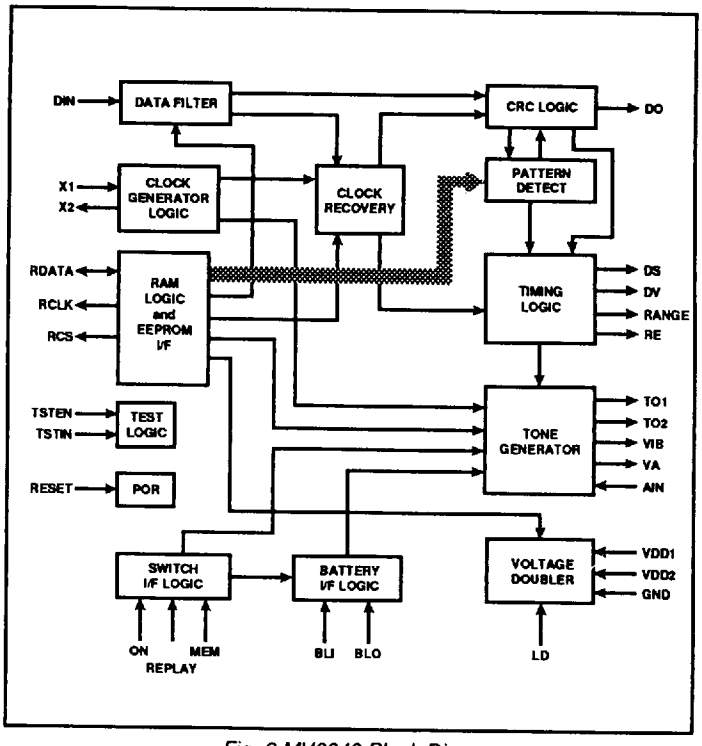


Fig. 2 MV6640 Block Diagram

Pin Description.

Pin No	Pin Name	Pin Description
1	DIN	Serial data input to the device. Inverted or non-inverted POCSAG code at 512 or 1200 baud. Polarity and data rate programmable.
2	DV	Data Valid output high indicates that a valid message is being received. It can be used as a 'wake up' signal for a micro controller.
3	RDATA	Bi-directional data port for reading in the EEPROM data to internal memory. High Impedance when not in use.
4	RCLK	Data Clock output for the EEPROM interface. High impedance when not in use.
5	RCS	Chip select for external EEPROM. High impedance when not in use. Active High.
6	DS	Data Strobe. This output goes active high prior to each bit of valid message data being transmitted on DO.
7	DO	Data Output. Valid address and message data is output on this pin.
8	$\overline{\text{RESET}}$	This pin is used to activate the power on reset circuit. A capacitor between this pin and GND sets the reset time when powered up. The device may also be externally reset from this input.
9	AIN	Alert in. One of two inputs to the tone generator circuit. This input when high produces a continuous tone at the two tone outputs.
10	BLO	Battery level output. This goes high if battery level input (BLI) is high for 8ms.
11	RANGE	If no preamble or sync word is detected for 60 batches, the range output goes high.
12	ON	Decoder is switched 'ON' by holding this pin high.
13	REPLAY	Pulsed high to cancel tones or replay calls.
14	MEM	Decoder is switched to 'MEM' (memory or 'silent' mode) by holding this pin high.
15	VA	Visual alert. Pulses high to indicate incoming call when in silent mode. Can be used to drive an LED.
16	TSTEN	Test input active high. Hold low during normal operation.
17	TO2	The beep codes and alerts are output on this pin. The output configuration and tone output frequencies are programmable.
18	TO1	The beep codes and alerts are output on this pin. The output configuration and tone output frequencies are programmable.
19	VIB	Output to external bipolar vibrator driver when in silent mode.
20	X2	Crystal oscillator output.
21	X1	Crystal oscillator input.
22	GND	Negative supply input.
23	VDD2	Positive supply, doubled if voltage doubler active, otherwise connected to VDD1.
24	VDD1	Positive supply input (1V min).
25	LD	Connect external inductor and diode for voltage doubler if required.
26	TSTIN	Test input. Held low for normal operation.
27	RE	Receiver Enable. This output when low powers down or disables the receiver to save power.
28	BLI	Battery level input from receiver. Normally tied low. The high level indicates battery flat and triggers a tone if high for 8ms.

DECODER APPLICATIONS

The MV6640 can be used in either a "Tone Only" or a "Tone and Message" pager. When used in tone only applications, the only additional IC requirements are a receiver (such as the SL6609) and a small EEPROM (primarily for holding the pager identification). A full tone and message pager can be implemented with the addition of a simple microprocessor/LCD driver.

OPERATION

On power up the MV6640 reads four addresses and other set-up information from the EEPROM. It then enables the receiver and searches the incoming data for a sync code word. Once sync. has been achieved the MV6640 will power down the receiver except for those periods when valid data is expected. When the receiver is enabled, the incoming data is searched for the expected addresses.

When a valid address is detected the MV6640 activates external indicators to alert the user. Data Valid goes high and the Data Output DO shows which address has been received, the function bits and the error status. If the address is followed by a message this is also output on DO. When the message has finished the MV6640 returns to searching for a valid address.

THE POCSAG CODE

A transmission of POCSAG code consists of at least 576 bits of preamble, i.e. alternate 1010s, followed by batches of codewords, each batch starting with a synchronisation codeword (SC) followed by 8 frames of data. (see figure 3a).

Each frame consists of 2 codewords, where the pager ID's 3 least significant bits correspond to the frame number in the batch.

Each codeword consists of 32 bits as shown in figure 3b. There are two types of codeword, address and message. The SC and IC are special cases of address codewords. Bits 20-21 of the address codeword transmitted determine the tone cadence pattern to be output by the decoder.

Message codewords immediately follow their particular address and are only displaced by the SC. An idle codeword (IC) is transmitted in the absence of an address or message codeword. In a message sequence, the end of the message is denoted by another address or idle codeword.

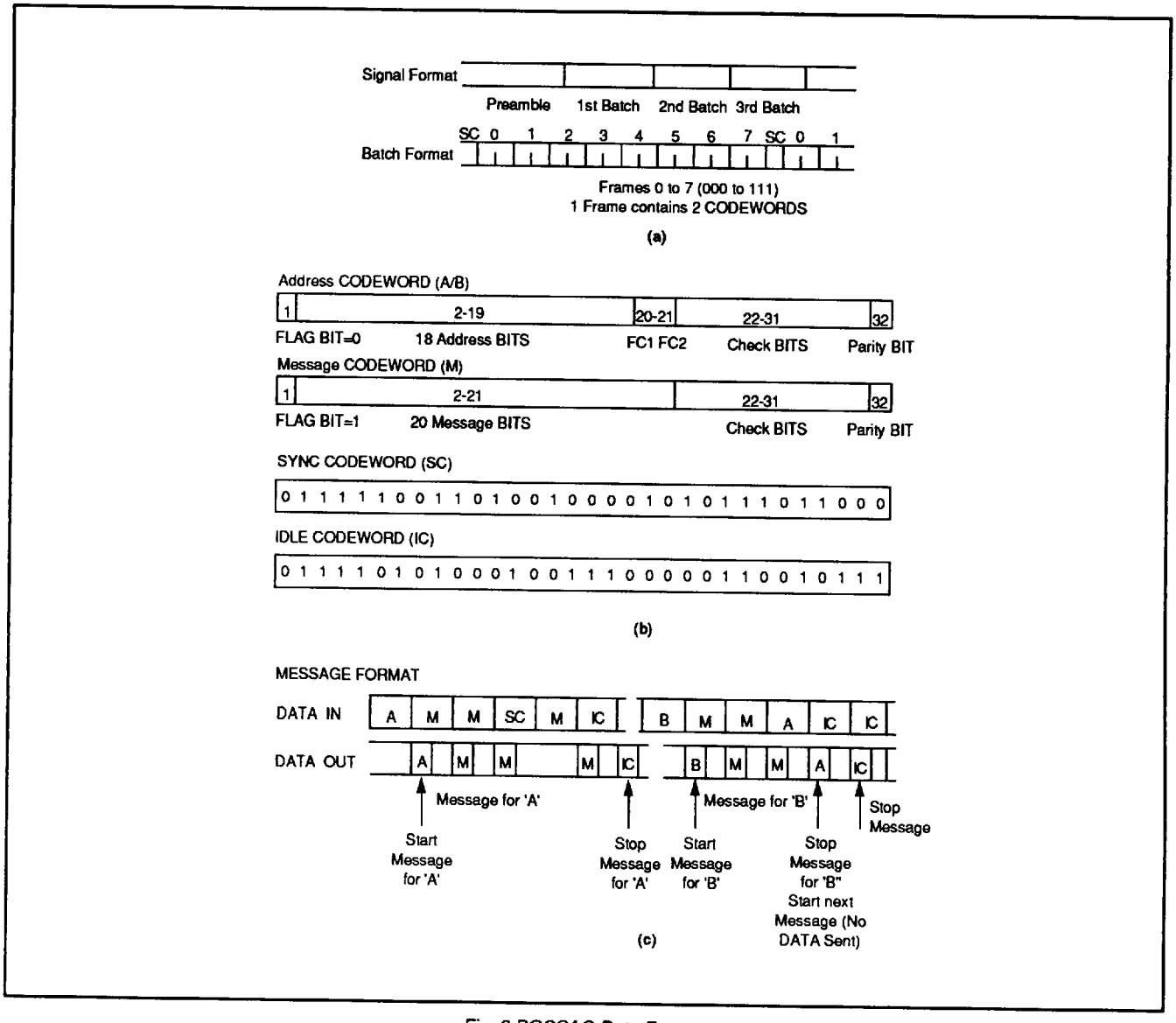


Fig. 3 POCSAG Data Format

ACCESSING THE EEPROM

The decoder initiates an EEPROM read by taking the chip select (RCS) high. The EEPROM clock (RCLK) and data (RDATA) outputs become active and a "Read starting at address 0" instruction is output. The instruction is clocked into the EEPROM on the positive edge of RCLK. Eighty five bits of data are then clocked out of the EEPROM on the positive edge of RCLK and sampled by the MV6640 on the negative edge.

Note that the EEPROM must be a 1k bit device with three wire interface that supports sequential read. Suitable EEPROMs include the Exel XL93C46, Microchip 93AA46 and the SII S-2913. The EEPROM should be configured as 16-bit organisation.

The first eighteen bits of data are address A1, in the same order as they are transmitted in the POCSAG code. The next eighteen bits are address A2 in the same order followed by three bits defining which frame of the POCSAG signal will be checked for addresses A1 and A2. The next thirty nine bits are addresses and frame B1 and B2 in the same order as above.

	Function Bit		Feature
FB1	Data rate select	0: 1:	1200 baud. 512 baud.
FB2	Voltage Doubler	0: 1:	Disabled. Enabled.
FB3	Silent Override A1	0: 1:	Enabled. Disabled.
FB4	Silent Override B1	0: 1:	Enabled. Disabled.
FB5	Tone Frequency	0: 1:	2048Hz. 2731Hz.
FB6	Tone Configuration	0: 1:	Two Tone Levels. Single Tone Level.
FB7	Input Data polarity	0: 1:	No Inversion. Inversion.

Fig. 4 Function Bit Allocation

The last seven bits are used to configure the decoder. The baud rate, voltage doubler, silent override, tone generation and data polarity, can be programmed as in figure 4.

The function of each bit loaded from the EEPROM is described in figure 17.

The EEPROM data is loaded 3 seconds after power up or an external reset. The delay allows the voltage doubler to attain its correct voltage. The data is reloaded when the decoder is switched from STANDBY to ON or MEM modes as above but without the 3 second delay as the voltage doubler will already have reached its correct output voltage.

The RCS, RCLK and RDATA pins default to high impedance state when the MV6640 is not accessing the EEPROM. This allows other devices to share the EEPROM (eg a microcontroller). To prevent the signals floating the pins have pull-down resistors (50kΩ nominal) which are disabled when the EEPROM chip select goes high.

If only one address is required all four addresses should be programmed with the same data; both sets of frame position bits should be identical and FB3 and FB4 the same. The address code output from DO will be B2.

If two addresses are required A1 and A2 should both contain copies of one of them and B1 and B2 the other. The address output code will be A2 or B2 respectively.

If three addresses are required then either A1 and A2 or B1 and B2 should contain duplicate copies of the same data. The address output will be A2 in the former case or B2 in the latter.

The address codes output on D0 are shown in figure 8.

The silent overide facility is only available for addresses A1 and B1. If A1 and A2 are the same the overide facility is available and similarly if B1 and B2 are the same.

POCSAG CODE SYNCHRONISATION

After the decoder has been powered up and the EEPROM read completed, synchronisation to the incoming POCSAG data is performed. Once bit synchronisation is achieved by the clock recovery circuit, the data stream is checked bitwise for the sync codeword (SC).

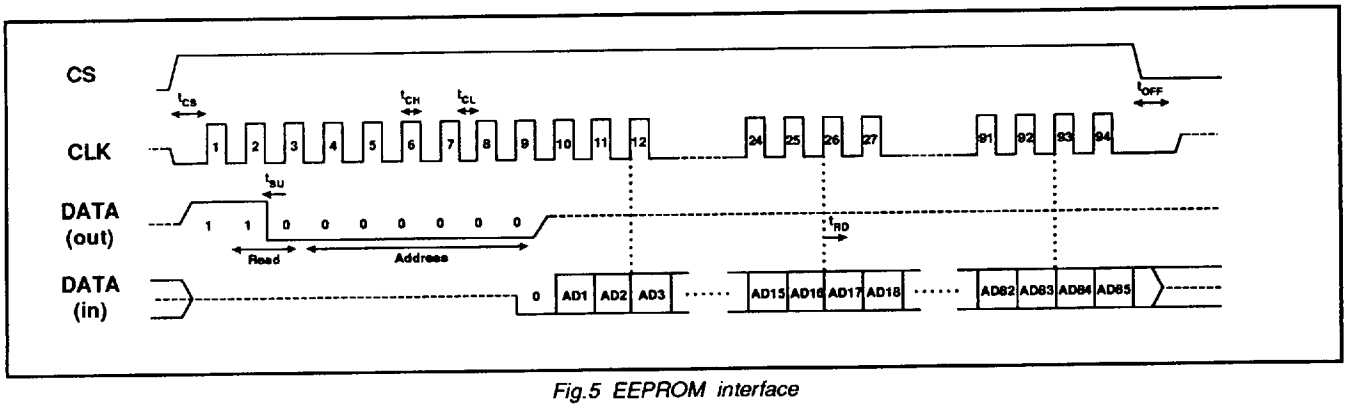


Fig.5 EEPROM interface

After the SC is found, the receiver is disabled. It is turned on for each of the programmed search frames and for each sync. If SC is not found, a search procedure is initiated. The receiver is enabled for one frame in 9 to search for either SC or preamble. If, after 60 such search cycles, SC or preamble have not been detected, the out of range (RANGE) signal goes active high. RANGE is reset if SC or preamble is detected or the decoder is switched to STANDBY.

DESCRIPTION OF DECODER CIRCUITS

CLOCK GENERATOR LOGIC

Most of the required clock signals for the chip are produced by the clock generator circuit, from the 32768Hz crystal controlled oscillator. These are as follows:-

32.768 kHz for clock recovery
2048/2731 Hz (programmble) for the tone generator
16 Hz to control tone cadencing

Clocks will be disabled as required depending on the mode of operation of the device.

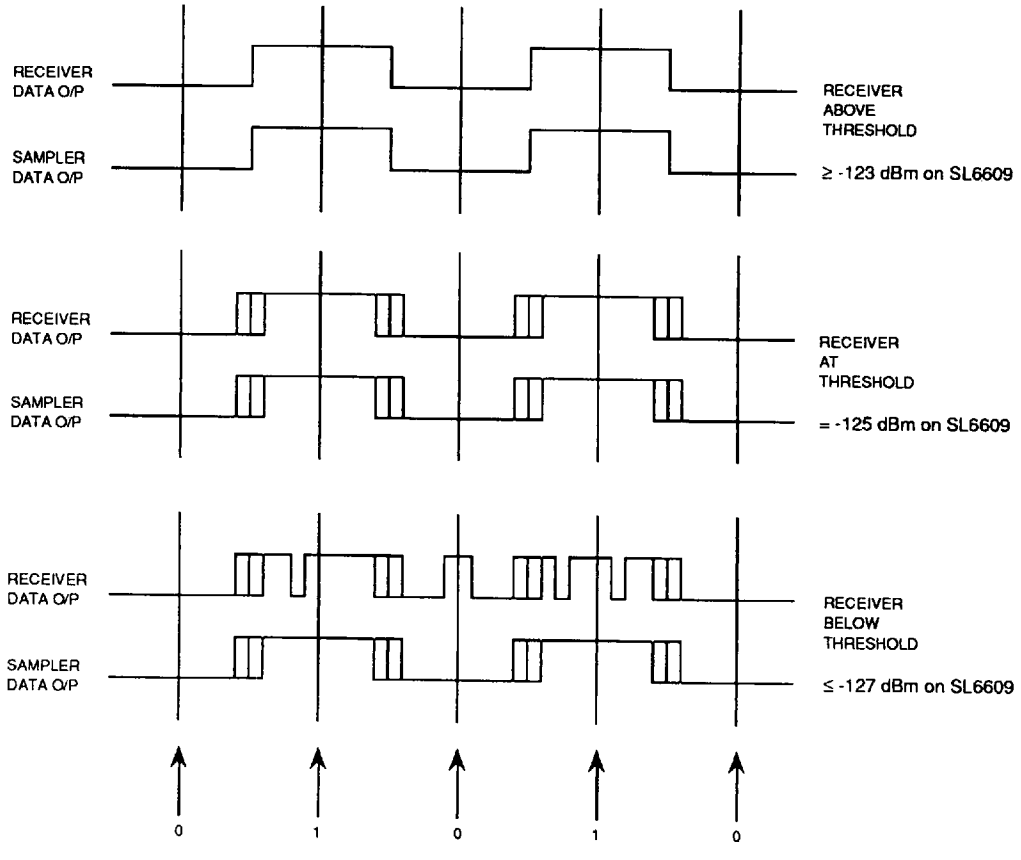
An external clock may be applied to X1 if X2 is left open circuit. Note that X1 has non-standard input thresholds.

CLOCK RECOVERY

The clock recovery circuit produces a clock signal correctly synchronised to the incoming data. The circuit is similar in operation to a digital phase locked loop. This circuit together with the timing logic monitors and maintains bit sync.

DATA FILTER

The data filter digitally cleans up the incoming data as shown in figure 6 and works with the clock recovery circuit to synchronise the internal clocks to the incoming data. The circuits minimise the effects of edge jitter and "drop-outs" in the data, which can occur at low signal levels.



DATA SAMPLING POINTS FOR CRC LOGIC.

AT 512 BAUD, GLITCHES ≤ 0.428 mS ARE FILTERED OUT
AT 1200 BAUD, GLITCHES ≤ 0.214 mS ARE FILTERED OUT

Fig. 6 Data Filter Operation

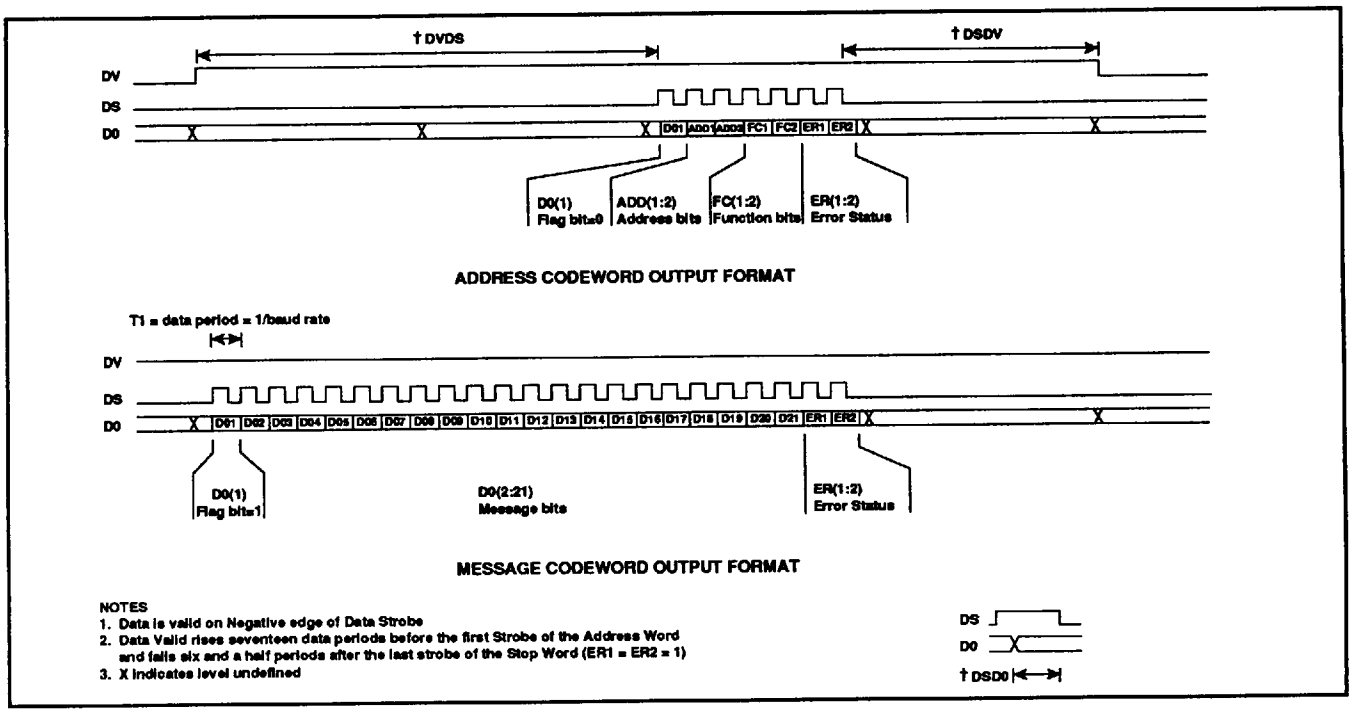


Fig. 7 Data Output Timing

CRC LOGIC

This circuit receives the incoming serial data and performs 2 bit CRC error correction according to the POCSAG standard on all incoming data. Together with the timing logic and pattern detector, this circuit maintains word sync.

PATTERN DETECTOR

This circuit operates on checked and corrected data. It receives data and checks for SC, IC and all of the four programmed pager addresses.

TIMING LOGIC

This logic provides the bit, word and batch frame sync in conjunction with the pattern detector, CRC logic and clock recovery circuit. The timing logic also generates the receiver enable (RE), data strobe (DS) and out-of-range (RANGE), output signals. RE goes active one word at 1200 baud, half word at 512 baud, before the address is expected to allow time for the receiver to power up.

DATA INTERFACE

When one of the four addresses is recognised the Data Valid pin (DV) goes high and a string is clocked out of the Data Output (DO) by the Data Strobe (DS). Data is valid on the falling edge of DS. The data string will start with an address word followed by a series of message words (if there is a message in the POCSAG code) then terminate with a special form of the address word indicating the end of message. After the stop codeword DV goes low.

An address codeword consists of seven bits, the first of which starts at least 17 data periods after DV goes high. The first bit is a zero indicating that this is an address word, the second and third show which of the four addresses was received (encoded as in figure 8), the next two are copies of the Function bits from the received data and the final two indicate the number of errors in the address word.

ADD2	ADD1	Address Received
0	0	Address A1
0	1	Address A2
1	0	Address B1
1	1	Address B2
0	1	Address A1 = Address A2
1	1	Address B1 = Address B2
1	1	A1 = A2 = B1 = B2

Fig. 8 Address Codes

ER2	ER1	Description
0	0	No errors found or one detected and corrected
0	1	Two errors detected and corrected
1	0	More than two errors detected, none corrected
1	1	Address Codeword: STOP word Data Codeword: NOT USED

Fig. 9 Error Status Bits

A message codeword consists of twenty three bits. The first is a one followed by twenty message bits in the order received but error corrected where necessary and possible and finally two error status bits as in the address word.

The final codeword will be an address codeword as above, but with both error status bits set to one this indicates that the message is ending. The address codes and function bits will be zero. DV returns low 6.5 data periods after the last DS edge.

BATTERY INTERFACE LOGIC

The decoder will accept a 'battery low' flag from a radio receiver on the BLI pin. The decoder samples the state of this pin at 256 Hz when the receiver is enabled, as shown in figure 10. The tone generator will output a 16 second continuous signal if BLI input is high (battery fail condition) for 3 or more consecutive samples. In addition, a battery low flag is output on the BLO pin. Note that any active tone generator and BLO output can be cancelled by pulsing the REPLAY/CANCEL input pin. The low battery detection circuit will be re-armed whenever decoder status is changed from STANDBY to ON or MEM.

TEST LOGIC

Test logic is included as required to supplement the inherent testability and fault coverage of the device during manufacture.

POWER ON/OFF AND SWITCH INTERFACE LOGIC

There are three operating modes for the decoder, STANDBY, ON and MEM (memory). When the decoder is required to be OFF it is preferable to disconnect the battery supply to the decoder, as shown in figure 16, to conserve battery power. If STANDBY mode is used all of the chip apart from the crystal oscillator and voltage doubler (if programmed ON) is disabled.

MEM or 'Silent' mode is selected if the user wishes to store incoming calls rather than producing alert tones immediately when the pager recognises a valid address. MEM mode is activated with a logic '1' on the MEM pin. The tone outputs TO1, TO2 are inhibited and the vibrator (VIB) and Visual Alert (VA) outputs enabled. In the MEM mode up to four incoming calls can be memorised. MEM mode does not affect the operation of the DO pin which continues to output calls when received. The silent mode can be overridden on either address A1 or B1 by setting the appropriate silent override function bit (see figure 4).

When a message is received with silent override active the decoder operates as in ON mode for that message.

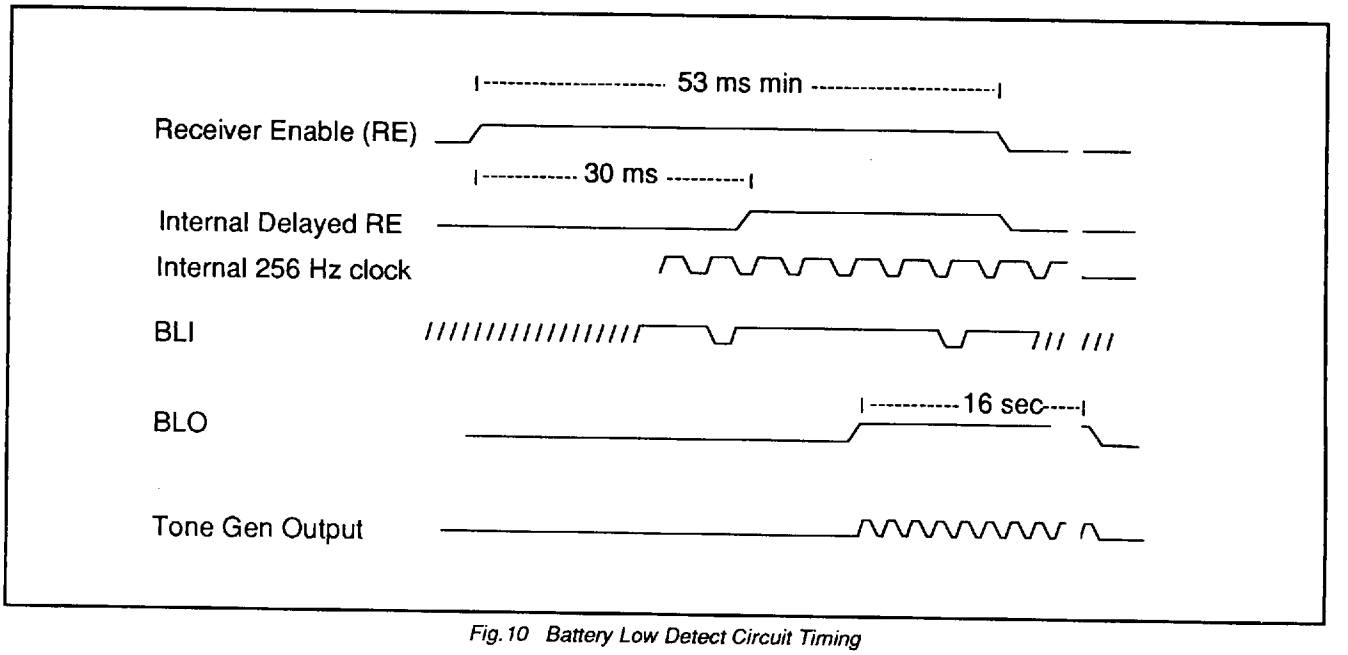


Fig. 10 Battery Low Detect Circuit Timing

The Switch Interface logic truth table is shown in figure 11 below:

ON	MEM	REPLAY	Decoder Status
0	0	0	Decoder off. No messages received. (STANDBY mode)
1	0	0	Decoder active. Messages received and decoded. (ON mode)
X	1	0	Decoder active and in silent / store call mode. (MEM mode)
1	0	⎍	Replay stored calls / cancel current tones.
X	1	⎍	Cancel current tones or Vibrator and Visual Alert outputs.

Fig. 11 Decoder Status Truth Table

In ON mode pulsing REPLAY to a logic '1' replays stored calls. Pulsing the REPLAY input will also cancel any current tone, vibrator or visual alert outputs.

Different tone patterns are generated when changing the status of the pager (eg from 'ON' to 'MEM'). These are described in the tone generation section.

Contact debounce circuitry is included in all switch and push button interfaces.

TONE VIBRATOR AND VISIBLE ALERT SIGNAL GENERATION

The tone generator block produces audio or low frequency vibrator signals in response to the operating mode of the pager, to messages, or low battery level. Four paging tone cadence patterns are provided and also the ability to output a continuous alert tone. Two volume levels are available and the tone generator frequency and output drive configuration is programmable.

TONE AND VIBRATOR GENERATOR OUTPUT CONFIGURATION

The internal tone generator circuit feeds an external beeper via the TO1 and TO2 pins. Figures 12(a) and (b) show the two common methods of beeper interface. Fig 12 (a) shows a high efficiency resonant drive circuit with one fixed volume level. In this configuration the TO1 and TO2 outputs are push - pull, switching in anti - phase. Fig 12 (b) shows a more flexible drive network which delivers two different power levels to the transducer. This mode is selected by clearing bit 6 of the function register low (figure 4). When an alert tone is output, TO2 stays low for the first six seconds and TO1 switches in accordance with the cadence pattern, producing a low level tone. For the next ten seconds TO2 also switches, producing a high tone level.

The vibrator output VIB drives an external bipolar transistor with vibrator alerter as shown in figure 12(c).

The tone frequency can be customer specified at either 2048Hz or 2731Hz. The control bit FB5 determines which frequency is used (see figure 4).

Four different paging tone cadence patterns are available and these are shown in Figure 14. The particular cadence output is determined by the FC1 and FC2 bits which form part of the address codeword (figure 3).

ALERT OVERIDE TONE

Direct input of cadence patterns is possible via the AIN pin. A high input on this pin will gate the selected tone frequency to the TO1 and TO2 outputs. Both TO1 and TO2 outputs are active when AIN is high and function register bit 6 is set high, to deliver maximum power to the external beeper.

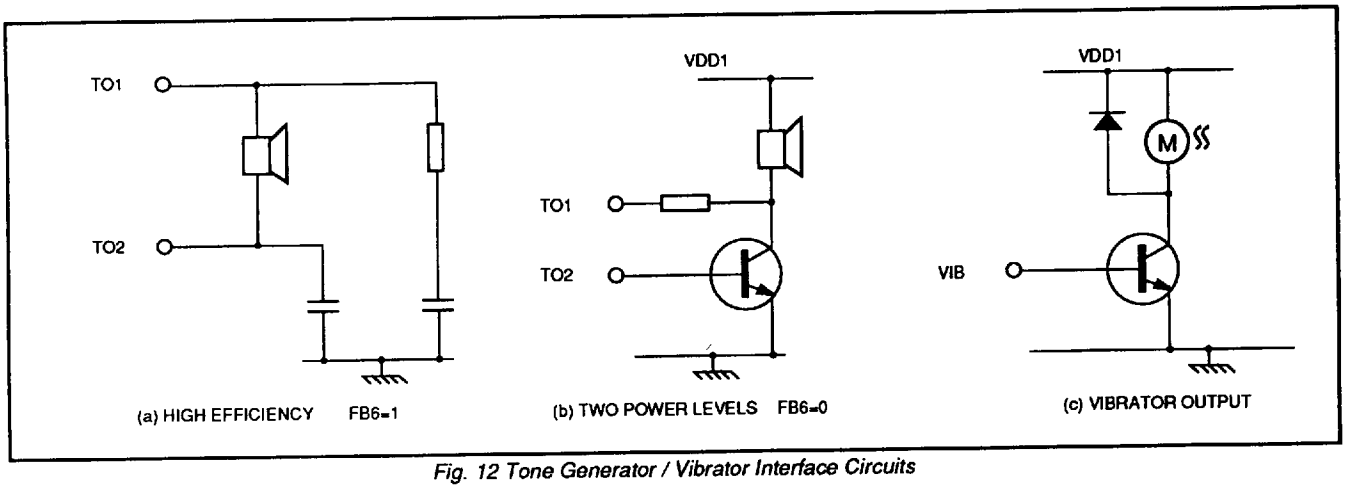


Fig. 12 Tone Generator / Vibrator Interface Circuits

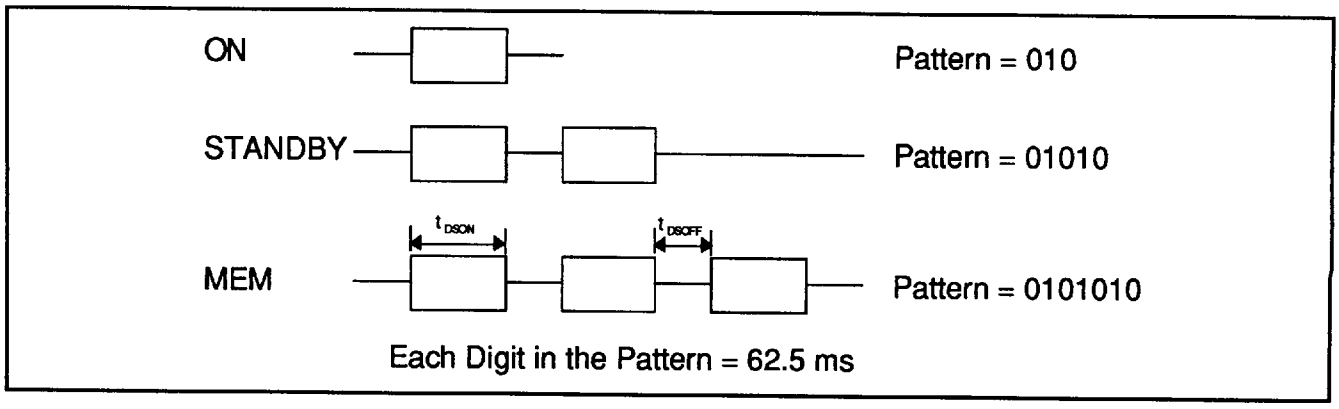


Fig. 13 Decoder Status Tones

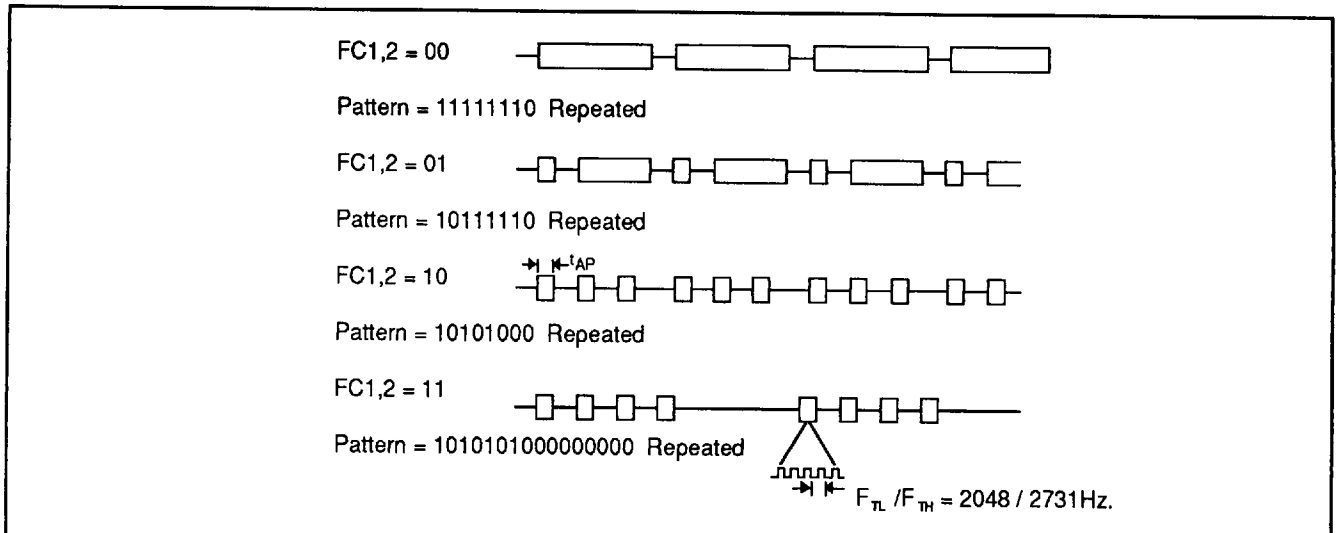
PAGER STATUS TONE GENERATION

The decoder produces tones to acknowledge a change in its status. When ON is selected the decoder will output a single short tone as shown in figure 13. In the ON, (or active) mode the decoder is able to receive and decode messages. Received calls are compared with the four user addresses assigned to the pager. These are programmed into the external E²PROM and read into the decoders internal memory.

Setting the decoder to the MEM (or Silent) state is indicated by three short tones. This operating mode is similar to the ON condition except that audio alert tones (cadences) are inhibited. Instead, the external vibrator alerter is activated by providing an 8Hz drive signal out of the VIB pin (see figure 15). A visible alert can be generated by feeding the VA output into the external buffer transistor and LED. VA is pulsed high as shown in figure 15. Up to four alert cadence calls can be stored in the decoder and these calls can be successively replayed by switching from MEM to ON and supplying pulses to the REPLAY input. When the vibrator output is active after receiving a message in the MEM mode, the device can be switched to ON mode to hear the remainder of the 16 second tone. The tone is also stored for REPLAY at a more convenient time. Pulsing REPLAY before the 16 second tone cadence has been completed will automatically cancel the current tone and replay the next tone as shown in figure 15. Whatever the pager status, a tone output, vibrator or visible alert can be cancelled by pulsing the REPLAY input.

Priority messages can be programmed to override the silent mode. Two of the seven 'Function bits' (figure 4) programmed into the external EEPROM, control the silent override for addresses A1 and B1.

Setting the decoder to the STANDBY state is indicated by two short tones.



NOTES:-
1. FC1,2 are bits 20,21 in an address codeword.
2. Each digit in the pattern = 125 ms.
3. When used as a "Tone and Message" pager, alert cadences are activated after decoder has output message.

Fig. 14 Alert Cadences

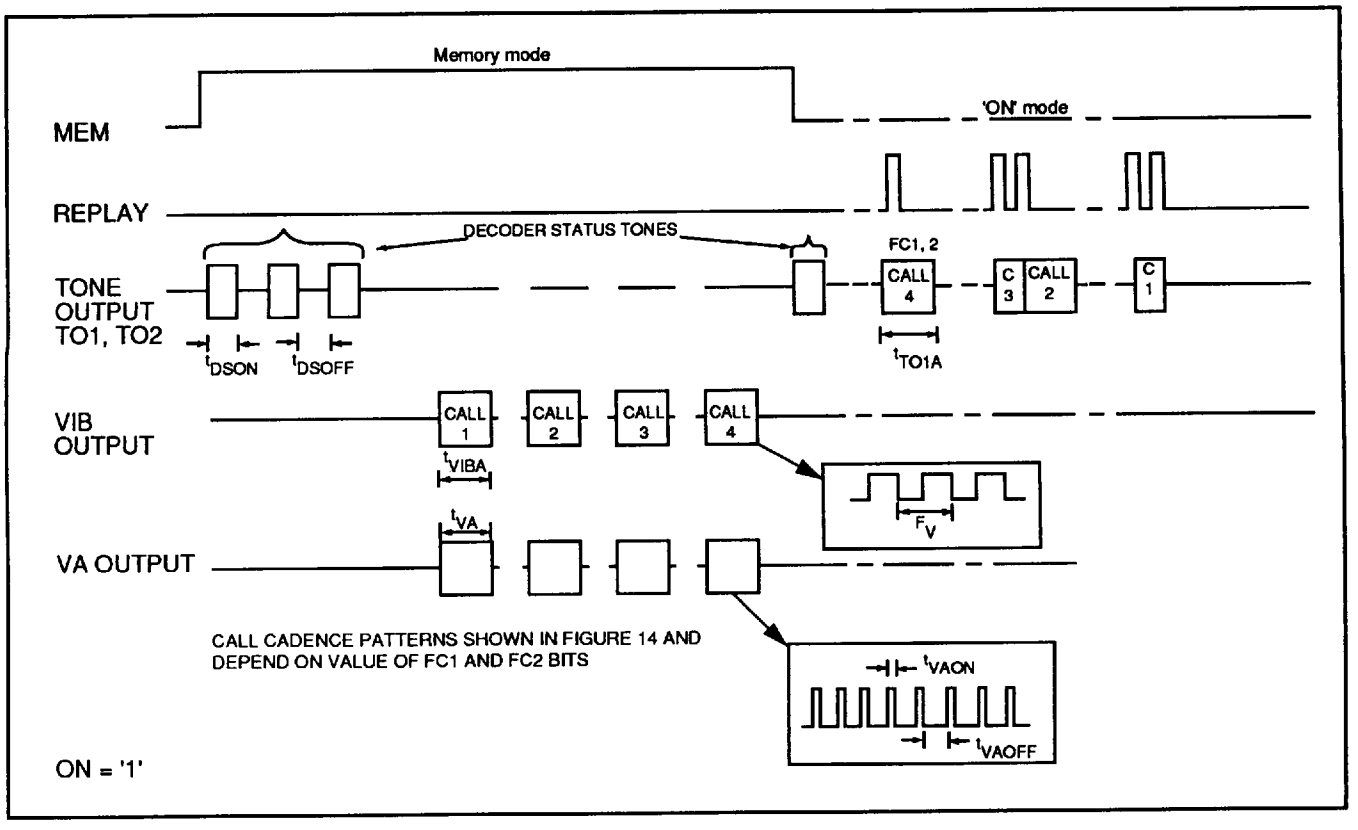


Fig. 15 Recall / Cancel of Stored Calls

VOLTAGE DOUBLER

The decoder is capable of operating with a supply between 1 and 3.5V. Other devices in the pager, for example the receiver, may require a higher voltage than 1V. The voltage doubler enables these devices to be used without additional circuitry.

The voltage conversion is performed by charging an inductor, then discharging it through a diode onto a reservoir capacitor on the output. To maximise the efficiency the resistance of the inductor and the forward voltage drop of the diode should be as low as possible. The diode should therefore be a schottky diode. The inductor used in the test and evaluation circuits has a DC resistance of less than 20 ohms.

The voltage on VDD2 should not exceed 3.5V, so VDD1 should be less than 1.75V if the doubler is enabled. If the doubler is not used VDD1 and VDD2 should be shorted together and the LD pin left open circuit.

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions unless otherwise stated:
VDD1 = 1V. Tamb = -20 to +70°C. All outputs open circuit. Voltage doubler disabled. VDD2 = VDD1

Parameters	Symbol	Min	Typ	Max	Units	Comments
SUPPLY CURRENT						
Decoder on	I_{VDD}		10	22	µA	
INPUT LOGIC HIGH						
RDATA, AIN, ON, REPLAY, MEM	V_{IH}	0.90			V	
BLI, DIN	V_{IH}	0.70			V	
NRESET	V_{IH}	0.90			V	
X1	V_{IH}	0.90			V	
INPUT LOGIC LOW						
RDATA, AIN, ON, REPLAY, MEM	V_{IL}			0.20	V	
BLI, DIN	V_{IL}			0.30	V	
NRESET	V_{IL}			0.30	V	
X1	V_{IL}			0.20	V	
LOGIC HIGH INPUT CURRENT						
ON, MEM, REPLAY	I_{IH}		0.01	1	µA	Note 1. $V_{IH} = V_{VDD1}$
AIN, NRESET	I_{IH}		0.13	1	µA	Note 1. $V_{IH} = V_{VDD1}$
BLI, DIN, RDATA, X1	I_{ILH}		0.01	1	µA	$V_{IH} = V_{VDD1}$
LOGIC LOW INPUT CURRENT						
All inputs except NRESET	I_{ILL}		-0.01	-1	µA	$V_{IL} = 0V$
NRESET	I_{IL}		-5.48	-10	µA	$V_{IL} = 0V$ internal pullup
OUTPUT LEVELS, HIGH						
All outputs except TO1, TO2, VIB	V_{OH}	0.90	0.99		V	$I_{LOAD} = 10µA$
TO1, TO2, VIB	V_{OH}	0.90	0.98		V	$I_{LOAD} = 10µA$
OUTPUT LEVELS LOW						
All outputs	V_{OL}		0.03	0.10	V	$I_{LOAD} = -10µA$
OUTPUT CURRENTS LOW						
TO1	I_{OL}	1.50			mA	$V_{OUT} = {}^{VDD1}/_{2}$
TO2, VIB, VA	I_{OL}	0.30			mA	$V_{OUT} = {}^{VDD1}/_{2}$
OUTPUT CURRENTS HIGH						
TO1, TO2, VIB	I_{OH}	0.30			mA	$V_{OUT} = {}^{VDD1}/_{2}$
VA	I_{OH}	0.20			mA	$V_{OUT} = {}^{VDD1}/_{2}$

NOTES
1. These inputs have internal pullup or pulldown resistors.

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions unless otherwise stated:
VDD1 = 1.5V. Tamb = -20 to +70°C. All outputs open circuit. Voltage doubler disabled. VDD2 = VDD1

Parameters	Symbol	Min	Typ	Max	Units	Comments
SUPPLY CURRENT						
Decoder on	I_{VDD}		12	26	µA	
INPUT LOGIC HIGH						
RDATA, AIN, ON, REPLAY, MEM	V_{IH}	1.2			V	
BLI, DIN	V_{IH}	1.0			V	
NRESET	V_{IH}	1.2			V	
X1	V_{IH}	0.9			V	
INPUT LOGIC LOW						
RDATA, AIN, ON, REPLAY, MEM	V_{IL}			0.3	V	
BLI, DIN	V_{IL}			0.5	V	
NRESET	V_{IL}			0.5	V	
X1	V_{IL}			0.2	V	
LOGIC HIGH INPUT CURRENT						
ON, MEM, REPLAY	I_{IH}		0.01	1	µA	Note 1. $V_{IH} = V_{VDD1}$
AIN, NRESET	I_{IH}		0.6	5	µA	Note 1. $V_{IH} = V_{VDD1}$
BLI, DIN, RDATA, X1	I_{ILH}		0.01	1	µA	$V_{IH} = V_{VDD1}$
LOGIC LOW INPUT CURRENT						
All inputs except NRESET	I_{ILL}		0.01	-1	µA	$V_{IL} = 0V$
NRESET	I_{IL}		-20	-40	µA	$V_{IL} = 0V$ internal pullup
OUTPUT LEVELS, HIGH						
All outputs except TO1, TO2, VIB	V_{OH}	1.3	1.5		V	$I_{LOAD} = 10µA$
TO1, TO2, VIB	V_{OH}	1.3	1.5		V	$I_{LOAD} = 10µA$
OUTPUT LEVELS LOW						
All outputs	V_{OL}		0.03	0.15	V	$I_{LOAD} = -10µA$
OUTPUT CURRENTS LOW						
TO1	I_{OL}	5			mA	$V_{OUT} = {}^{VDD1}/_{2}$
TO2, VIB, VA	I_{OL}	1			mA	$V_{OUT} = {}^{VDD1}/_{2}$
OUTPUT CURRENTS HIGH						
TO1, TO2, VIB	I_{OH}	1.5			mA	$V_{OUT} = {}^{VDD1}/_{2}$
VA	I_{OH}	1			mA	$V_{OUT} = {}^{VDD1}/_{2}$

NOTES
1. These inputs have internal pullup or pulldown resistors.

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions unless otherwise stated:
VDD1 = 3.5V. Tamb = -20 to +70°C. All outputs open circuit. Voltage doubler disabled. VDD2 = VDD1

Parameters	Symbol	Min	Typ	Max	Units	Comments
SUPPLY CURRENT						
Decoder on	I_{VDD}		31	50	µA	
INPUT LOGIC HIGH						
RDATA, AIN, ON, REPLAY, MEM	V_{IH}	2.8			V	
BLI, DIN	V_{IH}	2.0			V	
NRESET	V_{IH}	3.0			V	
X1	V_{IH}	0.9			V	
INPUT LOGIC LOW						
RDATA, AIN, ON, REPLAY, MEM	V_{IL}			0.8	V	
BLI, DIN	V_{IL}			1.2	V	
NRESET	V_{IL}			1.5	V	
X1	V_{IL}			0.2	V	
LOGIC HIGH INPUT CURRENT						
ON, MEM, REPLAY	I_{IH}		0.1	1	µA	Note 1. $V_{IH} = V_{VDD1}$
TSTIN, TSTEN, AIN, NRESET	I_{IH}		5.5	10	µA	Note 1. $V_{IH} = V_{VDD1}$
BLI, DIN, RDATA, X1	I_{ILH}		0.05	1	µA	$V_{IH} = V_{VDD1}$
LOGIC LOW INPUT CURRENT						
All inputs except NRESET	I_{ILL}		-0.05	-1	µA	$V_{IL} = 0V$
NRESET	I_{IL}		-180	-300	µA	$V_{IL} = 0V$ internal pullup
OUTPUT LEVELS, HIGH						
All outputs except TO1, TO2, VIB	V_{OH}	3.2	3.5		V	$I_{LOAD} = 10µA$
TO1, TO2, VIB	V_{OH}	3.2	3.4		V	$I_{LOAD} = 10µA$
OUTPUT LEVELS LOW						
All outputs	V_{OL}		0.05	0.3	V	$I_{LOAD} = -10µA$
OUTPUT CURRENTS LOW						
TO1	I_{OL}	10			mA	$V_{OUT} = {}^{VDD1}/_{2}$
TO2, VIB, VA	I_{OL}	2			mA	$V_{OUT} = {}^{VDD1}/_{2}$
OUTPUT CURRENTS HIGH						
TO1, TO2, VIB	I_{OH}	2			mA	$V_{OUT} = {}^{VDD1}/_{2}$
VA	I_{OH}	1			mA	$V_{OUT} = {}^{VDD1}/_{2}$

NOTES

1. These inputs have internal pullup or pulldown resistors.

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions unless otherwise stated:
VDD1 = 1V. Tamb = -20 to +70°C. All outputs open circuit. Voltage doubler ON.

Parameters	Symbol	Min	Typ	Max	Units	Comments
VOLTAGE DOUBLER						
VDD2 (Doubled Voltage) no ext. load	V_{VDD2}		1.95		V	
VDD2 (Doubled Voltage) 1.2mA ext. load	V_{VDD2}	1.80			V	
Max external load at VDD2 = 1.8 x VDD1	I_{VDD1}	1.20			mA	
SUPPLY CURRENT						
Decoder	I_{VDD1}			100	µA	
Decoder 1.2mA ext. doubler load	I_{VDD1}			4.1	mA	
Decoder Max ext. doubler load	I_{VDD1}			5.9	mA	
INPUT LOGIC HIGH						
RDATA, AIN, ON, REPLAY, MEM	V_{IH}	V_{VDD2}-0.4			V	
BLI, DIN	V_{IH}	V_{VDD2}-0.5			V	
NRESET	V_{IH}	V_{VDD2}-0.3			V	
X1	V_{IH}	1.0			V	
INPUT LOGIC LOW						
RDATA, AIN, ON, REPLAY, MEM	V_{IL}			0.4	V	
BLI, DIN	V_{IL}			0.6	V	
NRESET	V_{IL}			0.5	V	
X1	V_{IL}			0.2	V	
LOGIC HIGH INPUT CURRENT						
ON, MEM, REPLAY	I_{IH}			1	µA	Note 1. $V_{IH} = V_{VDD2}$
AIN, NRESET	I_{IH}			6	µA	Note 1. $V_{IH} = V_{VDD2}$
BLI, DIN, RDATA, X1	I_{ILH}			1	µA	$V_{IH} = V_{VDD2}$
LOGIC LOW INPUT CURRENT						
All inputs except NRESET	I_{ILL}			-1	µA	V_{IL} = 0V
NRESET	I_{IL}			-150	µA	V_{IL} = 0V, internal pullup
OUTPUT LEVELS, HIGH						
All outputs except TO1, TO2, VIB	V_{OH}	V_{VDD2}-0.2			V	I_{LOAD} = 10µA
TO1, TO2, VIB	V_{OH}	0.9			V	I_{LOAD} = 10µA
OUTPUT LEVELS LOW						
All outputs	V_{OL}			0.20	V	I_{LOAD} = -10µA
OUTPUT CURRENTS LOW						
TO1	I_{OL}	7.0			mA	$V_{OUT} = {}^{VDD1}/_{2}$
TO2, VIB, VA	I_{OL}	1.5			mA	$V_{OUT} = {}^{VDD1}/_{2}$
OUTPUT CURRENTS HIGH						
TO1, TO2, VIB (current source)	I_{OH}	1.2			mA	$V_{OUT} = {}^{VDD1}/_{2}$
VA (current source)	I_{OH}	1.0			mA	$V_{OUT} = {}^{VDD1}/_{2}$
VOLTAGE DOUBLER FREQUENCY						
	F_{VD}	8	11	15	kHz	Note 3 VD Load = 0
	F_{VD}	44	68	108	kHz	Note 3 VD Load = 550µA
	F_{VD}	96	140	196	kHz	Note 3 VD Load = 1.2mA
	F_{VD}	130	166	214	kHz	Note 2, 3 VD Load = Max

NOTES
1. These inputs have internal pullup or pulldown resistors.
2. VD Load = Max is load current such that VDD2 = 1.8 x VDD1.
3. Not production tested.

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions unless otherwise stated:
VDD1 = 1.5V. Tamb = -20 to +70°C. All outputs open circuit. Voltage doubler ON.

Parameters	Symbol	Min	Typ	Max	Units	Comments
VOLTAGE DOUBLER						
VDD2 (Doubled Voltage) no ext. load	V_{DD2}		2.90		V	
VDD2 (Doubled Voltage) 1.2mA ext. load	V_{DD2}	2.75			V	
Max external load at VDD2 = 1.8 x VDD1	I_{VDD1}	2.00			mA	
SUPPLY CURRENT						
Decoder	I_{VDD1}			120	µA	
Decoder 1.2mA ext. doubler load	I_{VDD1}			3.8	mA	
Decoder Max ext. doubler load	I_{VDD1}			8.6	mA	
INPUT LOGIC HIGH						
RDATA, AIN, ON, REPLAY, MEM	V_{IH}	V_{VDD2}-0.6			V	
BLI, DIN	V_{IH}	V_{VDD2}-0.8			V	
NRESET	V_{IH}	V_{VDD2}-0.4			V	
X1	V_{IH}	1.0			V	
INPUT LOGIC LOW						
RDATA, AIN, ON, REPLAY, MEM	V_{IL}			0.60	V	
BLI, DIN	V_{IL}			0.80	V	
NRESET	V_{IL}			1.50	V	
X1	V_{IL}			0.20	V	
LOGIC HIGH INPUT CURRENT						
ON, MEM, REPLAY	I_{IH}			1	µA	Note 1. $V_{IH} = V_{VDD2}$
AIN, NRESET	I_{IH}			8	µA	Note 1. $V_{IH} = V_{VDD2}$
BLI, DIN, RDATA, X1	I_{ILH}			1	µA	$V_{IH} = V_{VDD2}$
LOGIC LOW INPUT CURRENT						
All inputs except NRESET	I_{ILL}			-1	µA	V_{IL} = 0V
NRESET	I_{IL}			-250	µA	V_{IL} = 0V, internal pullup
OUTPUT LEVELS, HIGH						
All outputs except TO1, TO2, VIB	V_{OH}	V_{VDD2}-0.3			V	I_{LOAD} = 10µA
TO1, TO2, VIB	V_{OH}	1.35			V	I_{LOAD} = 10µA
OUTPUT LEVELS LOW						
All outputs	V_{OL}			0.30	V	I_{LOAD} = -10µA
OUTPUT CURRENTS LOW						
TO1	I_{OL}	10.0			mA	$V_{OUT} = {}^{VDD1}/_{2}$
TO2, VIB, VA	I_{OL}	2.0			mA	$V_{OUT} = {}^{VDD1}/_{2}$
OUTPUT CURRENTS HIGH						
TO1, TO2, VIB (current source)	I_{OH}	2.0			mA	$V_{OUT} = {}^{VDD1}/_{2}$
VA (current source)	I_{OH}	1.0			mA	$V_{OUT} = {}^{VDD1}/_{2}$
VOLTAGE DOUBLER FREQUENCY						
	F_{VD}	8	11	17	kHz	Note 3 VD Load = 0
	F_{VD}	27	38	54	kHz	Note 3 VD Load = 550µA
	F_{VD}	56	77	116	kHz	Note 3 VD Load = 1.2mA
	F_{VD}	119	154	206	kHz	Note 2, 3 VD Load = Max

NOTES

1. These inputs have internal pullup or pulldown resistors.
2. VD Load = Max is load current such that VDD2 = 1.8 x VDD1.
3. Not production tested.

AC ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions unless otherwise stated:
VDD1= 1 to 3.5V, VDD1 < = VDD2 < = 3.5V, Tamb = -20 to +70°C.

Parameters		Symbol	Min	Typ	Max	Units	Comments
Crystal Frequency		F_C		32768		Hz	
SYSTEM INPUTS TO DECODER						Hz	
Input Data Rate	(Low Speed)	F_D		512		baud	} Selectable
	(High Speed)			1200			} See Fig 4
Preamble Time	(512 baud)	t_{PA}	1.125			s	
	(1200 baud)		0.48			s	
Batch Time	(512 baud)	t_B		1.0625		s	
	(1200 baud)			0.4533		s	
TONE GENERATOR							
Output Frequency		F_{TL}		2048		Hz	} Selectable
		F_{TH}		2731		Hz	} See Fig 4
Vibrator Output Freq.		F_V		8		Hz	Fig 15
Vibrator Alert Period		t_{VIBA}		16		s	Fig 15
Visible Alert Period		t_{VA}		16		s	Fig 15
Visible Alert LED ON time		t_{VAON}		0.25		s	Fig 15
Visible Alert LED OFF time		t_{VAOFF}		1.75		s	Fig 15
TO1 Alert Period		t_{TO1A}		16		s	Fig 15
TO2 Alert Period		t_{TO2A}		10		s	} Selectable
TO2 Alert Period		t_{TO2B}		16		s	} See Fig 4
TO1, TO2 Alert Pulse Time		t_{AP}		125		ms	Fig 14
Decoder Status TO1, TO2 on		t_{DSON}		62.5		ms	Fig 13
Decoder Status TO1, TO2 off		t_{DSOFF}		62.5		ms	Fig 13
REPLAY pulse width		t_{REP}	80			ms	
Decoder RAM / E²PROM Timing							
Power up delay				3		s	Note 1
RCLK Frequency				16		kHz	Fig 5
RCS setup time		t_{CS}		31.25		µs	Fig 5
Clock High Level Time		t_{CH}		31.25		µs	Fig 5
Clock Low Level Time		t_{CL}		31.25		µs	Fig 5
RCLK to Data read		t_{RD}		31.25		µs	Fig 5
Data setup Time RDATA		t_{SU}				µs	Fig 5
RCS low to Output tristate		t_{OFF}		62.5		µs	Fig 5
Data Strobe frequency		F_{DS}		Baud rate		Hz	
Data Strobe to Data Output Delay		t_{DSDO}			50	µs	Fig 7
Data Valid to positive Strobe Edge		t_{DVDS}		$17/F_{DS}$		s	Fig 7
Data Strobe low to Data Valid low		t_{DSDV}		$6.5/F_{DS}$		s	Fig 7
Power On RESET capacitor		C_{RS}		10		nF	Fig 7
Voltage Doubler Output Ripple		V_D			1	mV p-p	Note 2

NOTES

1. A 3 second reset pulse is generated when power is applied to the MV6640. This allows time for the voltage doubler output (if enabled) to stabilise.

2. VDD2 decoupling capacitor 100µF. Output current 10µA - 1.2mA.

APPLICATION EXAMPLE: 1 VOLT PAGER SYSTEM

A typical 1 Volt pager system, suitable as a wrist watch application is shown in figure 16. Only 3 chips are required. GPS's SL6609 Direct Conversion Receiver, MV6640 POCSAG Decoder and an EEPROM.

A 32kHz watch crystal is used as the reference frequency to the decoder. The SL6609 receives and demodulates the data, and monitors the battery voltage. The interface between the decoder and receiver consists of only 3 connections excluding the supplies.

The decoder voltage doubler output V_{VDD2} is available to power not only the receiver and E²PROM but also a microprocessor / LCD driver for a full tone and message pager.

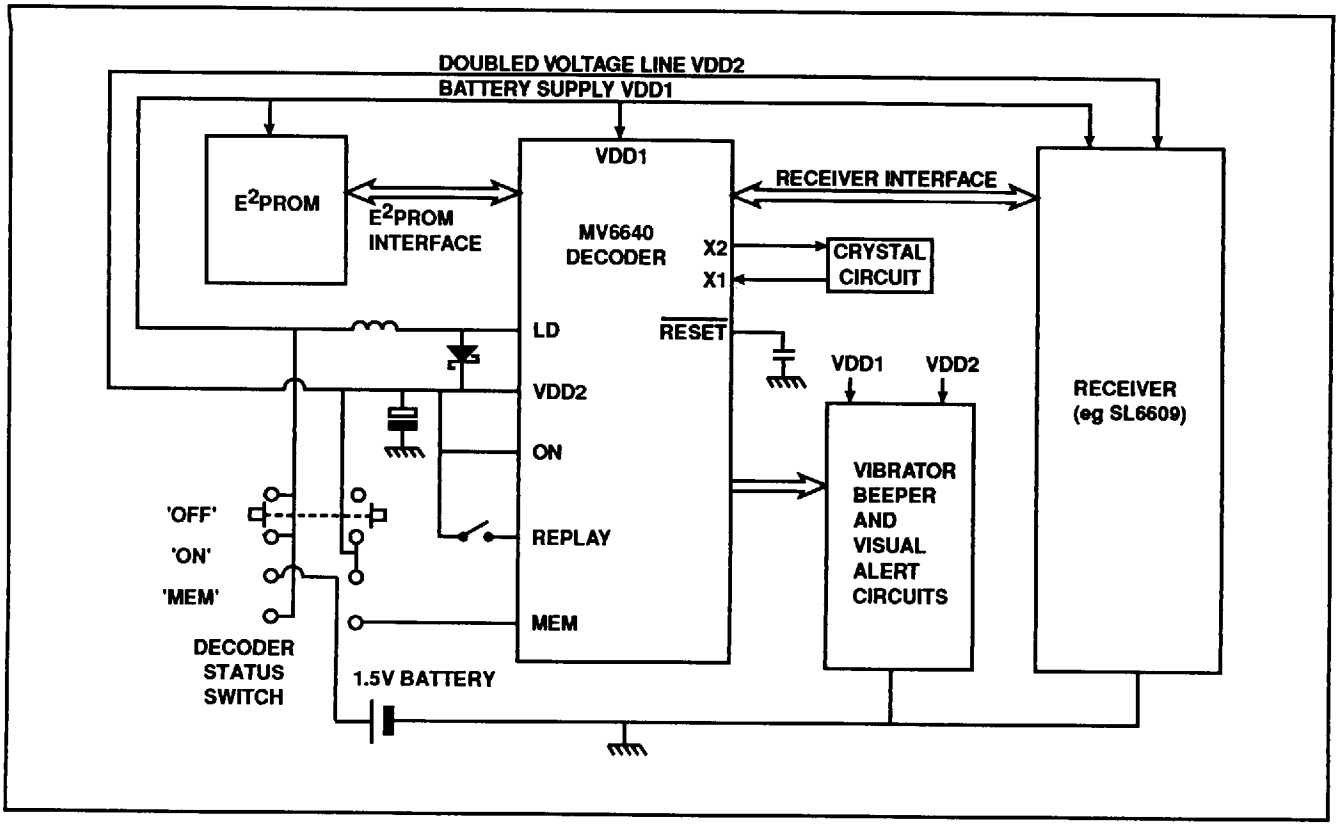


Fig.16 Tone Pager applications example showing interface with SL6609 receiver

Appendix A. The EEPROM

The MV6640 will work with any 1 k bit serial EEPROM with a three wire interface (Microwire™) that supports automatic address incrementing. If running from the voltage doubler the EEPROM's power requirements should be compatible. Suitable devices include the Exel XLS93C46, Microchip 93AA46 and the SII S-2913.

NB. 1. Not all manufacturer's 93xx46 support automatic address incrementing.

2. Most manufacturers provide two pinouts of the surface mount package. Make sure PCB and devices match when ordering.

The EEPROM output places bit 15 of each data word on the data line first, hence the programming looks at first glance disjointed and back to front. Figure 17 should make the order clear.

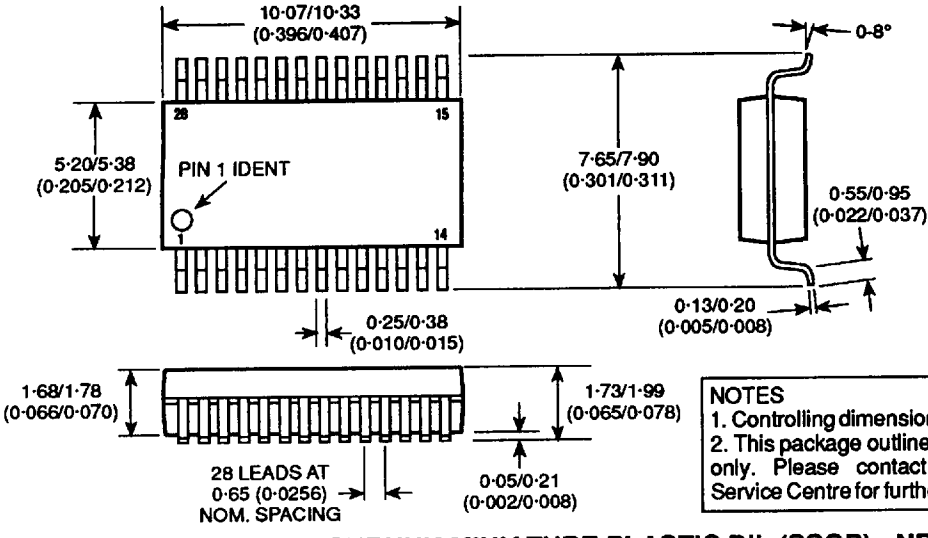
Thus Bit 15 of EEPROM address 0 is the first bit read and this corresponds to the first bit of POCSAG address A1. Bit 11 of EEPROM address 5 is the last bit read and this corresponds to Function Bit 7 which controls whether true or inverted data is read.

Note: Microwire is a trademark of the National Semiconductor Corporation.

EEPROM Word	Bit	Control Data		Name		POCSAG		EEPROM Word	Bit	Control Data		Name		POCSAG	
0	15	AD	1	A1	0	Bit	2	3	15	AD	49	B1	9	Bit	11
0	14	AD	2	A1	1	Bit	3	3	14	AD	50	B1	10	Bit	12
0	13	AD	3	A1	2	Bit	4	3	13	AD	51	B1	11	Bit	13
0	12	AD	4	A1	3	Bit	5	3	12	AD	52	B1	12	Bit	14
0	11	AD	5	A1	4	Bit	6	3	11	AD	53	B1	13	Bit	15
0	10	AD	6	A1	5	Bit	7	3	10	AD	54	B1	14	Bit	16
0	9	AD	7	A1	6	Bit	8	3	9	AD	55	B1	15	Bit	17
0	8	AD	8	A1	7	Bit	9	3	8	AD	56	B1	16	Bit	18
0	7	AD	9	A1	8	Bit	10	3	7	AD	57	B1	17	Bit	19
0	6	AD	10	A1	9	Bit	11	3	6	AD	58	B2	0	Bit	2
0	5	AD	11	A1	10	Bit	12	3	5	AD	59	B2	1	Bit	3
0	4	AD	12	A1	11	Bit	13	3	4	AD	60	B2	2	Bit	4
0	3	AD	13	A1	12	Bit	14	3	3	AD	61	B2	3	Bit	5
0	2	AD	14	A1	13	Bit	15	3	2	AD	62	B2	4	Bit	6
0	1	AD	15	A1	14	Bit	16	3	1	AD	63	B2	5	Bit	7
0	0	AD	16	A1	15	Bit	17	3	0	AD	64	B2	6	Bit	8
1	15	AD	17	A1	16	Bit	18	4	15	AD	65	B2	7	Bit	9
1	14	AD	18	A1	17	Bit	19	4	14	AD	66	B2	8	Bit	10
1	13	AD	19	A2	0	Bit	2	4	13	AD	67	B2	9	Bit	11
1	12	AD	20	A2	1	Bit	3	4	12	AD	68	B2	10	Bit	12
1	11	AD	21	A2	2	Bit	4	4	11	AD	69	B2	11	Bit	13
1	10	AD	22	A2	3	Bit	5	4	10	AD	70	B2	12	Bit	14
1	9	AD	23	A2	4	Bit	6	4	9	AD	71	B2	13	Bit	15
1	8	AD	24	A2	5	Bit	7	4	8	AD	72	B2	14	Bit	16
1	7	AD	25	A2	6	Bit	8	4	7	AD	73	B2	15	Bit	17
1	6	AD	26	A2	7	Bit	9	4	6	AD	74	B2	16	Bit	18
1	5	AD	27	A2	8	Bit	10	4	5	AD	75	B2	17	Bit	19
1	4	AD	28	A2	9	Bit	11	4	4	AD	76	BF	0	Frame	MSB
1	3	AD	29	A2	10	Bit	12	4	3	AD	77	BF	1	Frame	
1	2	AD	30	A2	11	Bit	13	4	2	AD	78	BF	2	Frame	LSB
1	1	AD	31	A2	12	Bit	14	4	1	AD	79	FB	1	N/A	
1	0	AD	32	A2	13	Bit	15	4	0	AD	80	FB	2	N/A	
2	15	AD	33	A2	14	Bit	16	5	15	AD	81	FB	3	N/A	
2	14	AD	34	A2	15	Bit	17	5	14	AD	82	FB	4	N/A	
2	13	AD	35	A2	16	Bit	18	5	13	AD	83	FB	5	N/A	
2	12	AD	36	A2	17	Bit	19	5	12	AD	84	FB	6	N/A	
2	11	AD	37	AF	0	Frame	MSB	5	11	AD	85	FB	7	N/A	
2	10	AD	38	AF	1	Frame		5	10	not used					
2	9	AD	39	AF	2	Frame	LSB	5	9	not used					
2	8	AD	40	B1	0	Bit	2	5	8	not used					
2	7	AD	41	B1	1	Bit	3	5	7	not used					
2	6	AD	42	B1	2	Bit	4	5	6	not used					
2	5	AD	43	B1	3	Bit	5	5	5	not used					
2	4	AD	44	B1	4	Bit	6	5	4	not used					
2	3	AD	45	B1	5	Bit	7	5	3	not used					
2	2	AD	46	B1	6	Bit	8	5	2	not used					
2	1	AD	47	B1	7	Bit	9	5	1	not used					
2	0	AD	48	B1	8	Bit	10	5	0	not used					

Fig.17 MV6640 EEPROM Bit Map

Dimensions are shown thus: mm (in).



NOTES
1. Controlling dimensions are inches.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

28-LEAD SHRUNK MINIATURE PLASTIC DIL (SSOP) - NP28

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