Synchronous Presettable 4-Bit Counter with Output Register (Multiplexed 3-State Outputs)

TC74HC697 Binary, Asynchronous clear

The TC74HC697A is a high speed CMOS UP/DOWN COUNTER fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The TC74HC697A is a 4-bit binary counter.

It counts on the rising edge of the Counter Clock (CCK) input when "counter mode" is selected. If the up/down (U/$\overline{D}$) input is held high, the internal counter counts up. Conversely, if U/$\overline{D}$ is held low, it counts down. The internal counters output is latched into the output registers on the rising edge of the Register Clock (RCK) input.

The outputs (QA ~ QD) are selected as either internal counter or registered outputs by the output select (R/$\overline{C}$) input. When high, the outputs are counter outputs and when low, they are registered outputs.

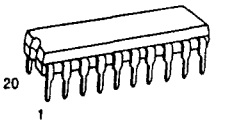
The TC74HC697A is cleared asynchronously.

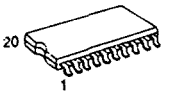
Two enable ($\overline{ENP}$, $\overline{ENT}$) inputs and carry ($\overline{RCO}$) outputs are provided to enable cascading of the counters. This facilitates easy implementation of n-bit counters without using external gates.

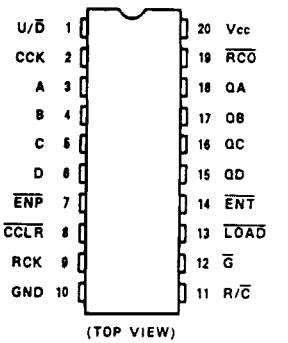
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

Features

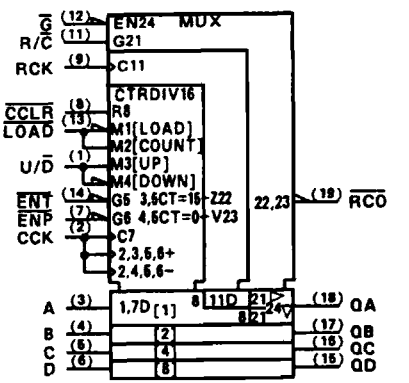
- High Speed: f_{MAX} = 38MHz(Typ.) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 4μA(Max.) at Ta = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min)
- Output Drive Capability: 15 LSTTL Loads For QA ~ QH
  10 LSTTL Loads For $\overline{RCO}$
- Symmetrical Output Impedance: $|I_{OH}| = I_{OL}$ = 6mA(Min.)
  For QA ~ QH
  $|I_{OH}| = I_{OL}$ = 4mA(Min.)
  For $\overline{RCO}$
- Balanced Propagation Delays: $t_{pLH} = t_{pHL}$
- Wide Operating Voltage Range: V_{CC}(opr) = 2V ~ 6V
- Pin and Function Compatible with 74LS697







Pin Assignment

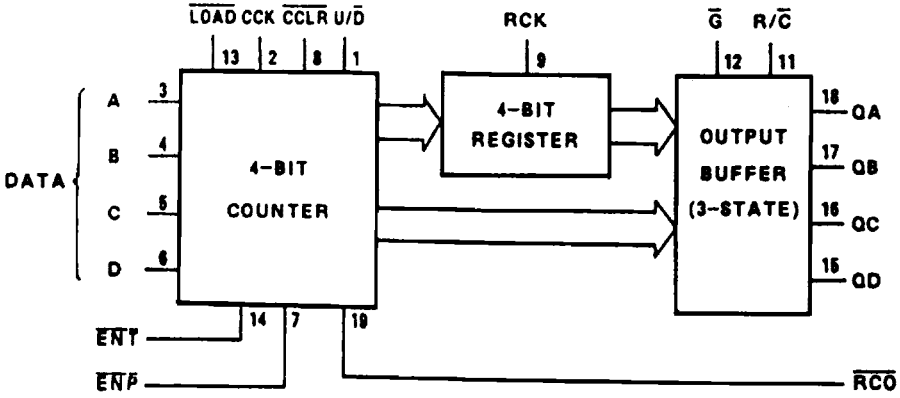


IEC Logic Symbol

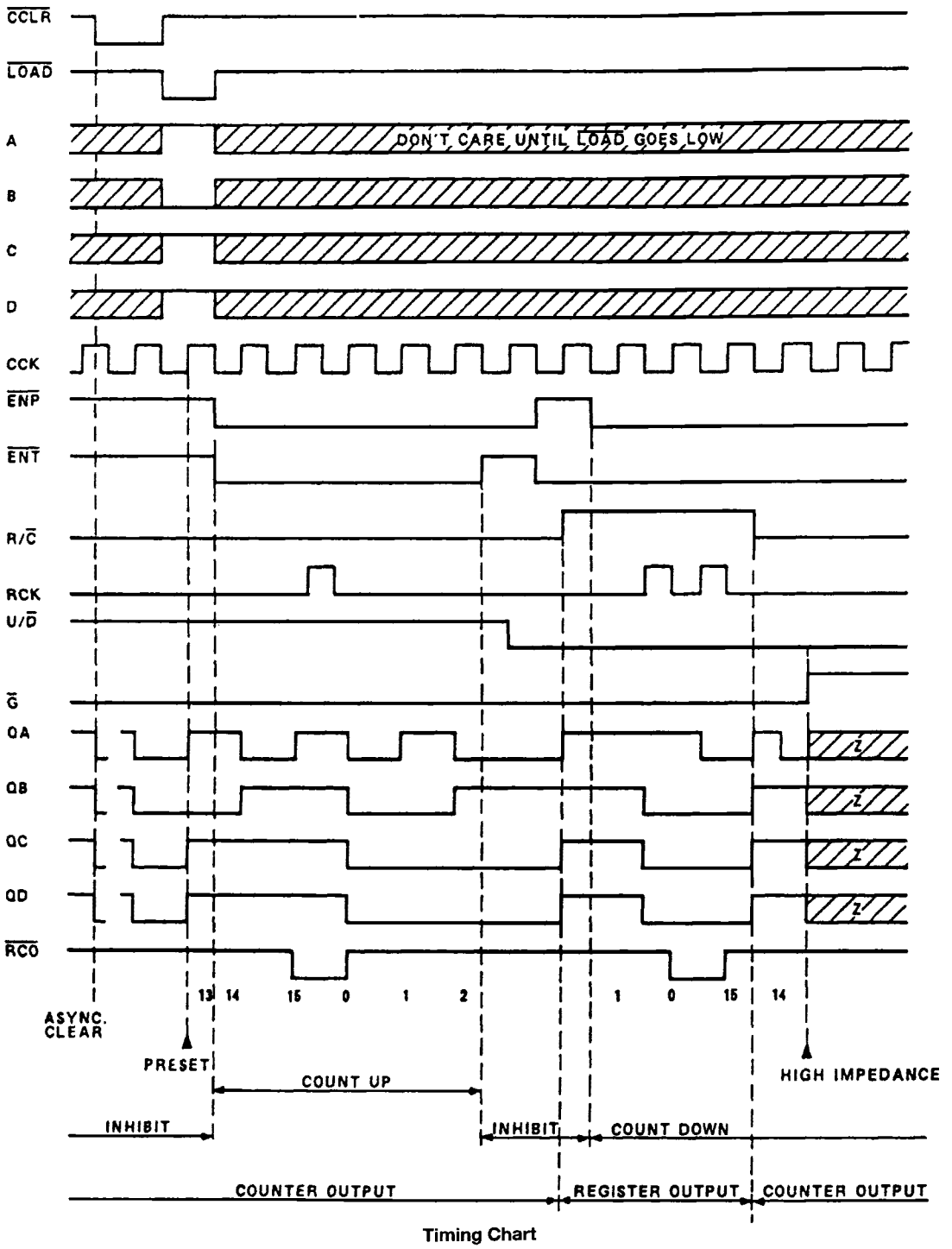
Truth Table

Inputs									Outputs				Function
$\overline{CCLR}$	$\overline{LOAD}$	$\overline{ENP}$	$\overline{ENT}$	CCK	U/$\overline{D}$	RCK	R/$\overline{C}$	$\overline{G}$	QA	QB	QC	CD	
X	X	X	X	X	X	X	X	H	Z	Z	Z	Z	High Impedance
L	X	X	X	X	X	X	L	L	L	L	L	L	Counter Clear
H	L	X	X	↑	X	X	L	L	a	b	c	d	Load Data
H	H	L	X	↑	X	X	L	L	No change				No count
H	H	X	H	↑	X	X	L	L					
H	H	L	L	↑	H	X	L	L	Count up				Count
H	H	L	L	↑	L	X	L	L	Count down				count
H	X	X	X	↓	X	↑	H	L	No change				No count
X	X	X	X	X	X	↑	H	L	a'	b'	c'	d'	Load register
X	X	X	X	X	X	↓	H	L	No change				No count

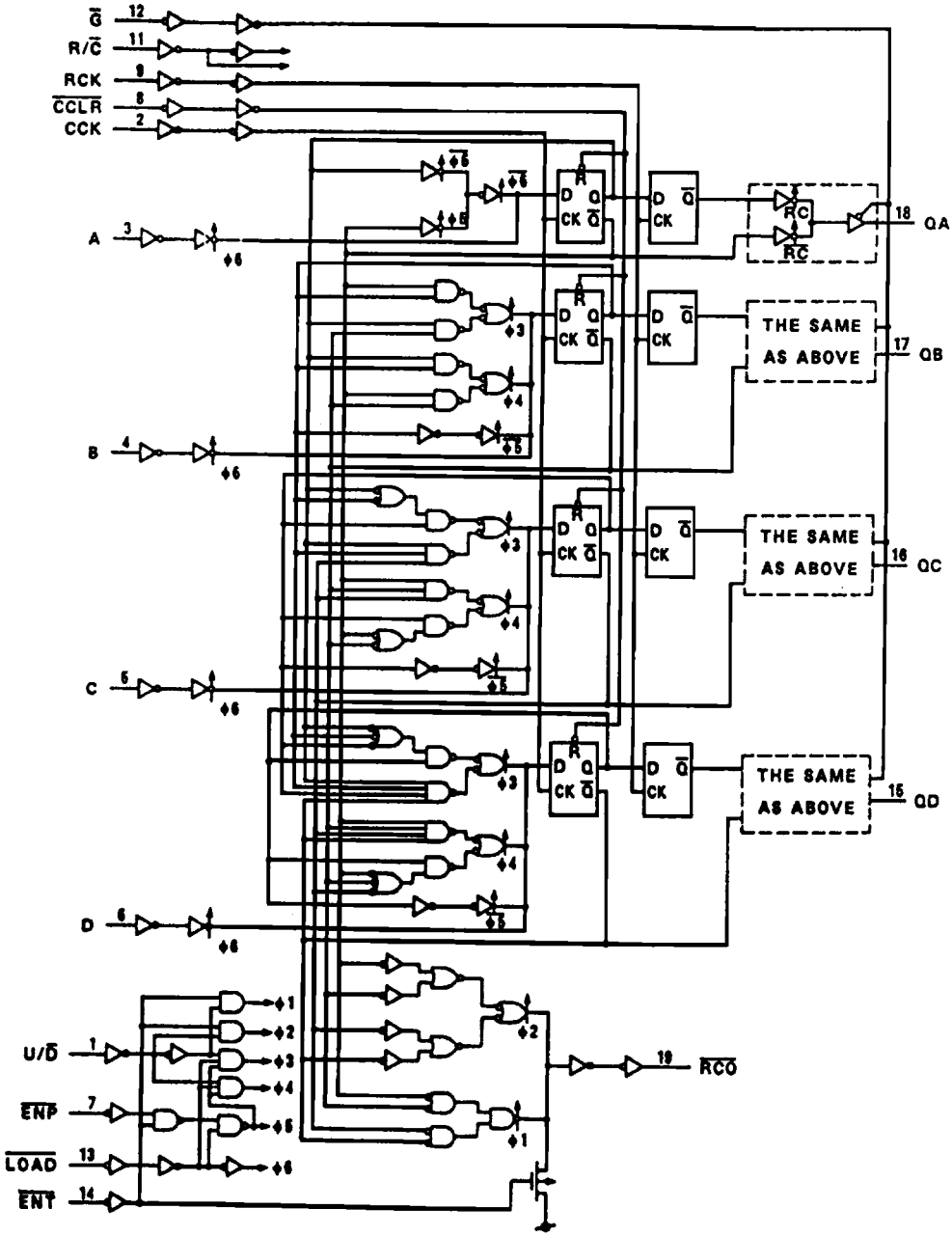
X : Don't Care
Z : High Impedance
a ~ d: The level of steady state input voltage at inputs A ~ D respectively.
a' ~ d': The level of steady state outputs at internal counter outputs QA' through QD' respectively.



Block Diagram



Timing Chart



Logic Diagram

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC} + 0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC} + 0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current ($\overline{RCO}$) (Q_A ~ Q_H)	I_{OUT}	±25 ±35	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

*500mW in the range of Ta = -40°C ~ 65°C. From Ta = 65°C to 85°C a derating factor of -10mW/°C shall be applied until 300mW.

Recommended Operating Conditions

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC} = 2.0V) 0 ~ 500(V_{CC} = 4.5V) 0 ~ 400(V_{CC} = 6.0V)	ns

DC Electrical Characteristics

Parameter	Symbol	Test Condition		Ta = 25°C				Ta = -40 ~ 85°C		Unit
				V_{CC}	Min.	Typ.	Max.	Min.	Max.	
High-Level Input Voltage	V_{IH}	–		2.0 4.5 6.0	1.5 3.15 4.2	– – –	– – –	1.5 3.15 4.2	– – –	V
Low-Level Input Voltage	V_{IL}	–		2.0 4.5 6.0	– – –	– – –	0.5 1.35 1.8	– – –	0.5 1.35 1.8	V
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	– – –	1.9 4.4 5.9	– – –	V
		$\overline{RCO}$	I_{OH} = -4 mA I_{OH} = -5.2mA	4.5 6.0	4.18 5.68	4.31 5.80	– –	4.13 5.63	– –	
		Q_A ~ Q_H	I_{OH} = -6 mA I_{OH} = -7.8mA	4.5 6.0	4.18 5.68	4.31 5.80	– –	4.13 5.63	– –	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20μA	2.0 4.5 6.0	– – –	0.0 0.0 0.0	0.1 0.1 0.1	– – –	0.1 0.1 0.1	V
		$\overline{RCO}$	I_{OH} = 4 mA I_{OH} = 5.2mA	4.5 6.0	– –	0.17 0.18	0.26 0.26	– –	0.33 0.33	
		Q_A ~ Q_H	I_{OL} = 6 mA I_{OL} = 7.8mA	4.5 6.0	– –	0.17 0.18	0.26 0.26	– –	0.33 0.33	
3-State Output Off-State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	–	–	±0.5	–	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	–	–	±0.1	–	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	–	–	4.0	–	40.0	

Timing Requirements (Input $t_r = t_f = 6ns$)

Parameter	Symbol	Test Condition		Ta = 25°C		Ta = -40 ~ 85°C	Unit
			V_{CC}	Typ.	Limit	Limit	
Minimum Pulse Width (CCK, RCK)	$t_{W(H)}$ $t_{W(L)}$	–	2.0	–	75	95	ns
			4.5	–	15	19	
			6.0	–	13	16	
Minimum Pulse Width ($\overline{CCLR}$)	$t_{W(L)}$	–	2.0	–	75	95	
			4.5	–	15	19	
			6.0	–	13	16	
Minimum Setup Time ($\overline{LOAD}$, ENT, $\overline{ENP}$)	t_s	–	2.0	–	150	190	
			4.5	–	30	38	
			6.0	–	13	25	
Minimum Setup Time (A, B, C, D)	t_s	–	2.0	–	50	65	
			4.5	–	10	13	
			6.0	–	9	11	
Minimum Setup Time (U/$\overline{D}$)	t_s	–	2.0	–	100	125	
			4.5	–	20	25	
			6.0	–	17	21	
Minimum Setup Time (CCK-RCK)	t_s	–	2.0	–	100	125	
			4.5	–	20	25	
			6.0	–	17	21	
Minimum Hold Time (A, B, C, D)	t_h	–	2.0	–	5	5	
			4.5	–	5	5	
			6.0	–	5	5	
Minimum Hold Time	t_h	–	2.0	–	0	0	
			4.5	–	0	0	
			6.0	–	0	0	
Minimum Removal Time	t_{rem}	–	2.0	–	5	5	
			4.5	–	5	5	
			6.0	–	5	5	
Clock Frequency	f	–	2.0	–	5	4	MHz
			4.5	–	25	20	
			6.0	–	29	24	

AC Electrical Characteristics ($C_L = 15pF$, $V_{CC} = 5V$, Ta = 25°C)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Output Transition Time ($\overline{RCO}$)	t_{TLH} t_{THL}	–	–	4	8	ns
Propagation Delay Time (CCK-$\overline{RCO}$)	t_{pLH} t_{pHL}	–	–	24	41	
Propagation Delay Time (ENT-RCO)	t_{pLH} t_{pHL}	–	–	13	23	
Propagation Delay Time ($\overline{CCLR}$-$\overline{RCO}$)	t_{pLH} t_{pHL}	–	–	23	38	
Maximum Clock Frequency	f_{MAX}	–	25	38	–	MHz

AC Electrical Characteristics (C_L = 50pF, Input $t_r = t_f$ = 6ns)

Parameter	Symbol	Test Condition			Ta = 25°C			Ta = -40 ~ 85°C		Unit
			CL	V_{CC}	Min.	Typ.	Max.	Min.	Max.	
Output Transition Time (Q)	t_{TLH} t_{THL}	–	50	2.0	–	25	60	–	75	ns
				4.5	–	7	12	–	15	
				6.0	–	6	10	–	13	
Output Transition Time ($\overline{RCO}$)	t_{TLH} t_{THL}	–	50	2.0	–	30	75	–	95	
				4.5	–	8	15	–	19	
				6.0	–	7	13	–	16	
Propagation Delay Time (CCK-Q)	t_{pLH} t_{pHL}	–	50	2.0	–	90	195	–	245	
				4.5	–	26	39	–	49	
				6.0	–	19	33	–	42	
			150	2.0	–	103	235	–	295	
				4.5	–	31	47	–	59	
				6.0	–	23	40	–	50	
Propagation Delay Time (RCK-Q)	t_{pLH} t_{pHL}	–	50	2.0	–	82	180	–	225	
				4.5	–	24	36	–	45	
				6.0	–	18	31	–	38	
			150	2.0	–	95	220	–	275	
				4.5	–	29	44	–	55	
				6.0	–	22	25	–	47	
Propagation Delay Time (R/$\overline{C}$-Q)	t_{pLH} t_{pHL}	–	50	2.0	–	60	145	–	180	
				4.5	–	19	29	–	36	
				6.0	–	14	25	–	31	
			150	2.0	–	73	185	–	230	
				4.5	–	24	37	–	46	
				6.0	–	18	31	–	39	
Propagation Delay Time ($\overline{CCLR}$-Q)	t_{pHL}	–	50	2.0	–	89	195	–	245	
				4.5	–	26	39	–	49	
				6.0	–	20	33	–	42	
			150	2.0	–	102	235	–	295	
				4.5	–	31	47	–	59	
				6.0	–	24	40	–	50	
Propagation Delay Time (CCK-$\overline{RCO}$)	t_{pLH} t_{pHL}	–	50	2.0	–	108	235	–	295	
				4.5	–	31	47	–	59	
				6.0	–	23	40	–	50	
Propagation Delay Time ($\overline{ENT}$-$\overline{RCO}$)	t_{pLH} t_{pHL}	–	50	2.0	–	63	135	–	170	
				4.5	–	18	27	–	34	
				6.0	–	14	23	–	29	
Propagation Delay Time ($\overline{CCLR}$-RCO)	t_{pHL}	–	50	2.0	–	98	220	–	275	
				4.5	–	29	44	–	55	
				6.0	–	23	37	–	47	
Output Enable Time ($\overline{G}$-Q)	t_{pZL} t_{pZH}	R_L = 1kΩ	50	2.0	–	45	115	–	145	
				4.5	–	15	23	–	29	
				6.0	–	12	20	–	25	
			150	2.0	–	58	155	–	195	
				4.5	–	20	31	–	39	
				6.0	–	16	26	–	33	
Output Disable Time ($\overline{G}$-Q)	t_{pLZ} t_{pHZ}	R_L = 1kΩ	50	2.0	–	32	115	–	145	
				4.5	–	17	23	–	29	
				6.0	–	14	20	–	25	
Maximum Clock Frequency	f_{MAX}	–	50	2.0	5	11	–	4	–	
				4.5	25	38	–	20	–	
				6.0	29	52	–	24	–	
Input Capacitance	C_{IN}	–			–	5	10	–	10	pF
Output Capacitance	C_{OUT}	–			–	13	–	–	–	
Power Dissipation Capacitance	C_{PD}(1)	–			–	72	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:

$I_{CC(opr)} = C_{PD} \bullet V_{CC} \bullet f_{IN} + I_{CC}$

Notes